FE-I4 chip for ATLAS

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on behalf of the ATLAS PIXEL Upgrade FE-I4 collaboration

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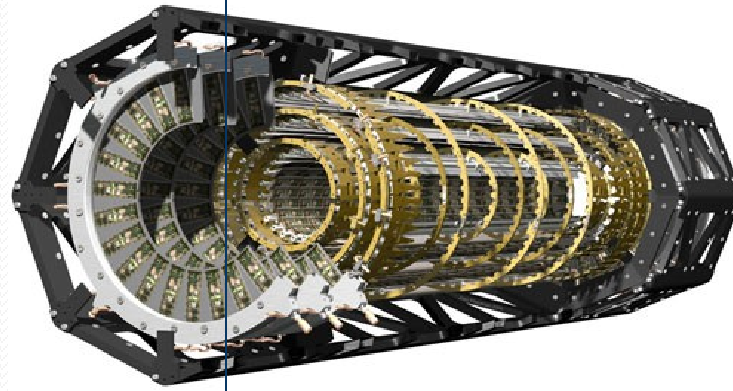
Outline

- Introduction
  - Motivations, Specifications and Description of the FEI4 chip
- The architecture
  - The chip overview
  - The Digital Readout Functionalities
  - The Analog Pixel
  - The Digital Pixel
- Test results
  - Measurements : Threshold, Noise, …
  - Wafers Testing
  - Module results
  - Irradiation
- Conclusion and Perspectives

Motivations

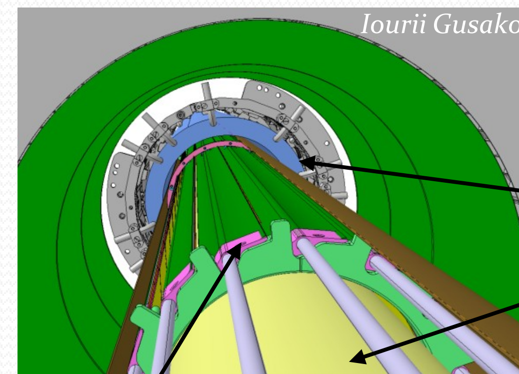
- Two applications are foreseen for FE-I4 :
- Insertion of the B-Layer (2013)
  - Small radius : 3.3 cm
  - Increase tracking performance
  - The FE-I4 designed to respect :
    - Higher hit occupancy per pixel
    - Higher level of radiations
- Phase 1 or Phase 2
  - New pixel detector planned
    - 2 removable internal layers at radii of about 3.3 – 10 cm
    - 2-3 fixed outer layers at radii of about 15 – 25 cm
  - FE-I4 fits requirements for outer layers in terms of hit occupancy and radiation hardness

ATLAS Pixel Detector



Present beam pipe & B-Layer

- 3 barrel layers / 3 end-caps
- end-cap: z± 49.5 / 58 / 65 cm
- barrel: r~ 5.0 / 8.8 / 12.2 cm

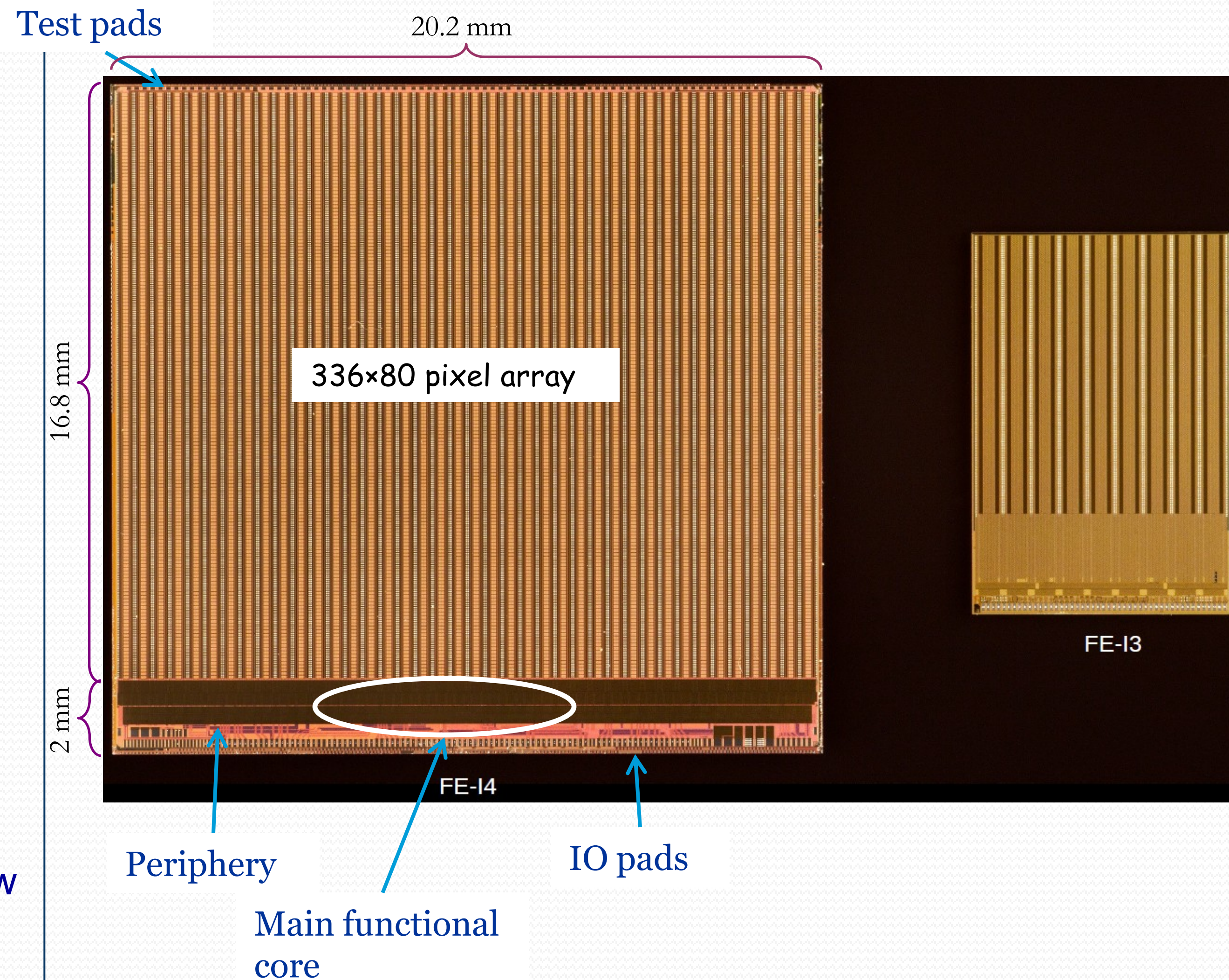


FE-I4 main specifications

Pixel size	50 x 250	μm^2
Pixel array size	80 x 336	Col x Row
Normal pixel input capacitance range	100-500	fF
Edge pixels input capacitance range	150-700	fF
In-time threshold with 20ns gate (400 fF)	4000	e-
Single channel ENC sigma (400 fF)	<300	e-
Tuned threshold dispersion	<100	e-
Charge resolution (ToT method)	4	bits
Operating temperature range	-40 to +60	°C
Radiation tolerance	300	MRad
DC leakage current tolerance	100	nA
Single serial command input (nominal)	40	Mb/s
Single serial data output (nominal)	160	Mb/s
Output data encoding	8b/10b	

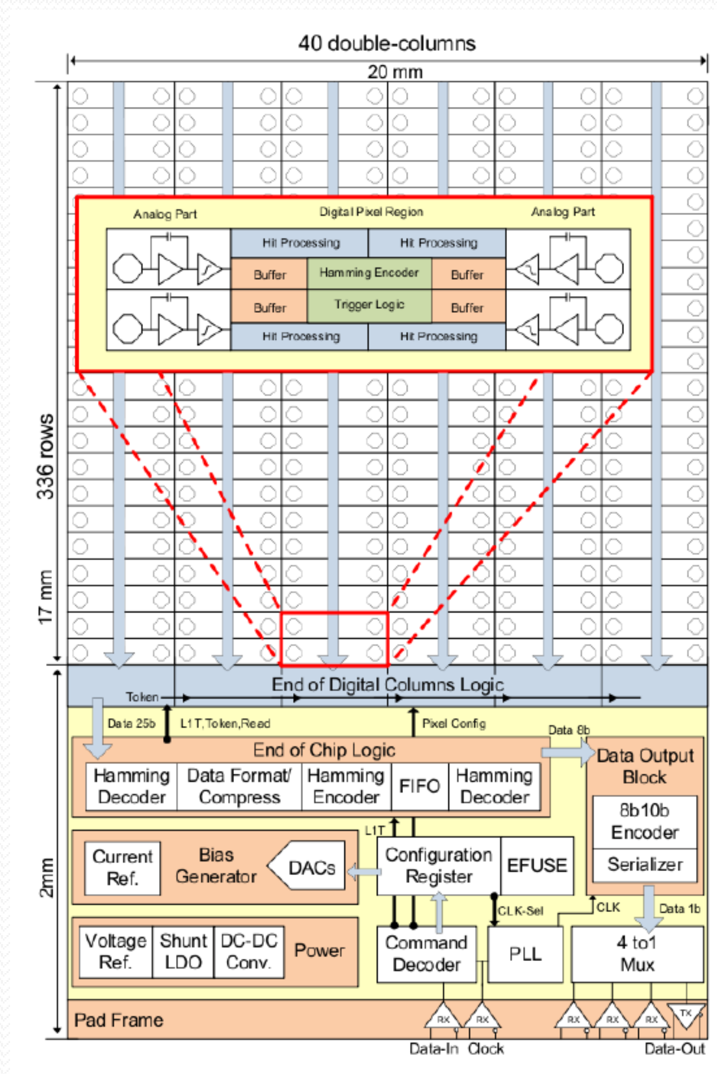
FE-I4A chip overview

- The FE-I4A chip is a full scale prototype and is designed in a 130 nm CMOS process
- All transistors are linear, but not all conventional :
  - Extra guard rings are used
- There are wire bonding pads along the bottom and the top of the chip
  - Pads at the top are just for characterization
- Submitted July 1, 2010
- Wafer ship date September 14th
- The chip and hybrid modules still now under test and characterization



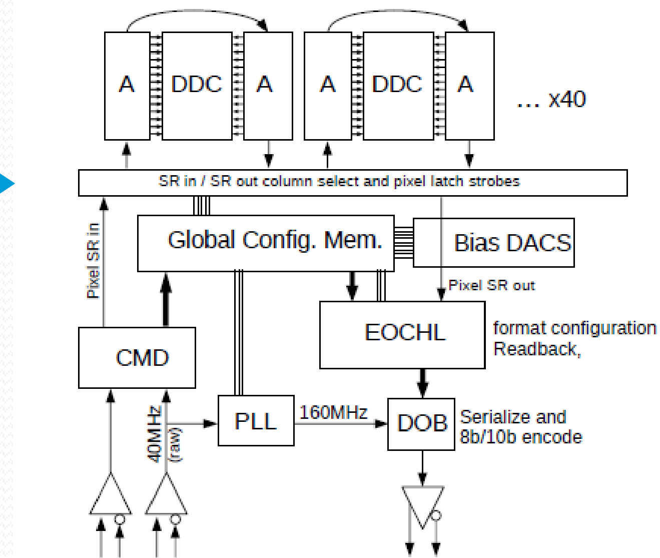
FE-I4 chip overview

- The FE-I4 pixel array is organized in Double Columns (DC) like the present detector's FE-I3
- Double Column is divided into 2 × 2 pixel regions
- The readout architecture is very different from the FE-I3:
  - Information data is stored locally in the pixel digital region and moved only if selected by trigger
- Each FE-I4 pixel contains :
  - An independent amplification stage with adjustable shaping
  - A discriminator with independently adjustable threshold
  - Pixel Digital Region (PDR) Shared by 4 pixels
- Sensors are DC coupled to FE-I4 with negative charge collection
- Like FE-I3 electronics, FE-I4 is divided into 2 different operating modes:
  - Data path for data acquisition
  - Command and Configuration

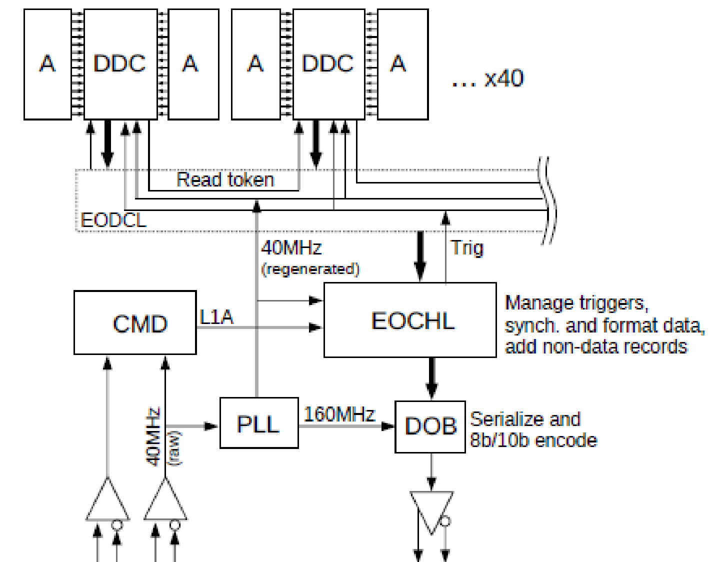


Digital Readout Functionalities

- Configuration Mode :
  - The FE is initialized to a low current mode
  - Global configuration memory is written
  - Pixels are configured/tuned using shift registers that address any of the 40 double columns

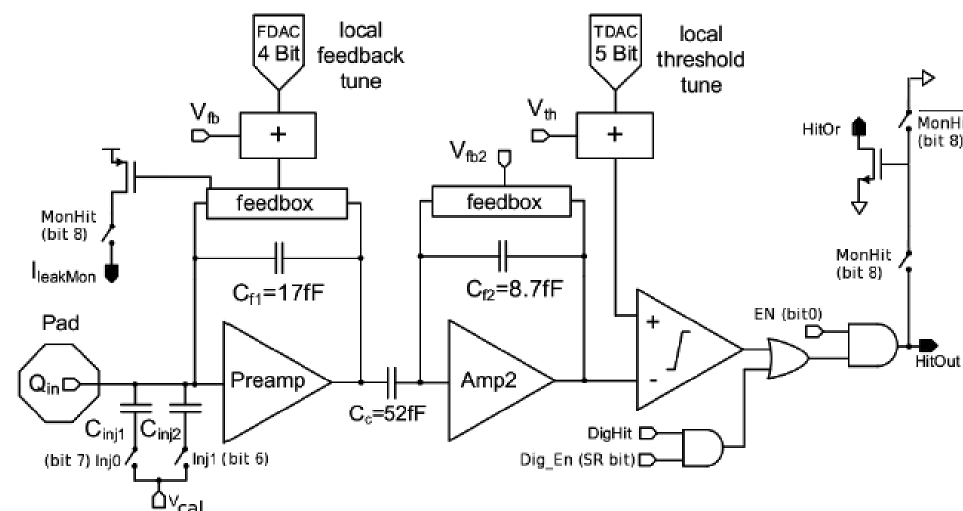


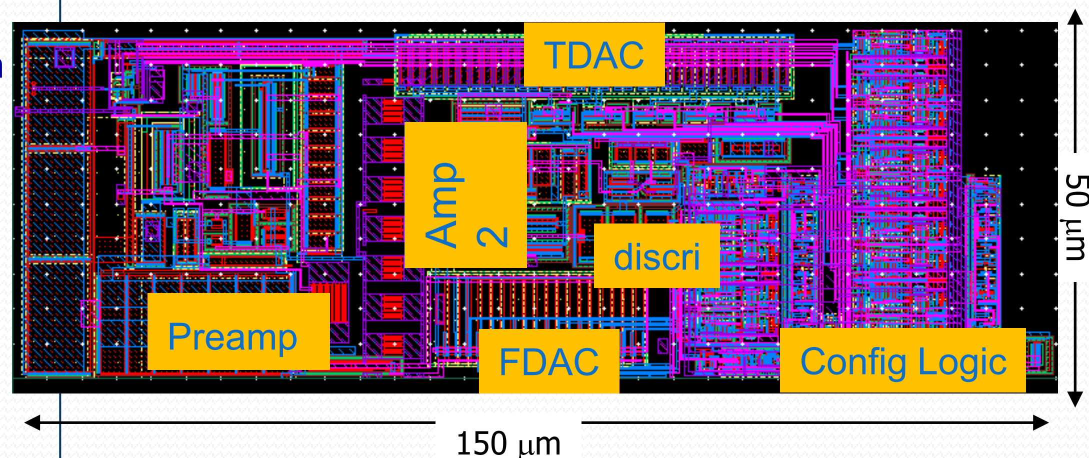
- Run Mode :
  - The FE responds to Trigger and Fast commands
  - Data is fetched from the double columns via a Read token
  - All hits matching the time stamp of the Trigger are read out
  - Data is sent to the Data Formatter, encoded and sent out on a 160 Mb/s data link
  - System messages and/or errors are encoded together with data



Analog Pixel

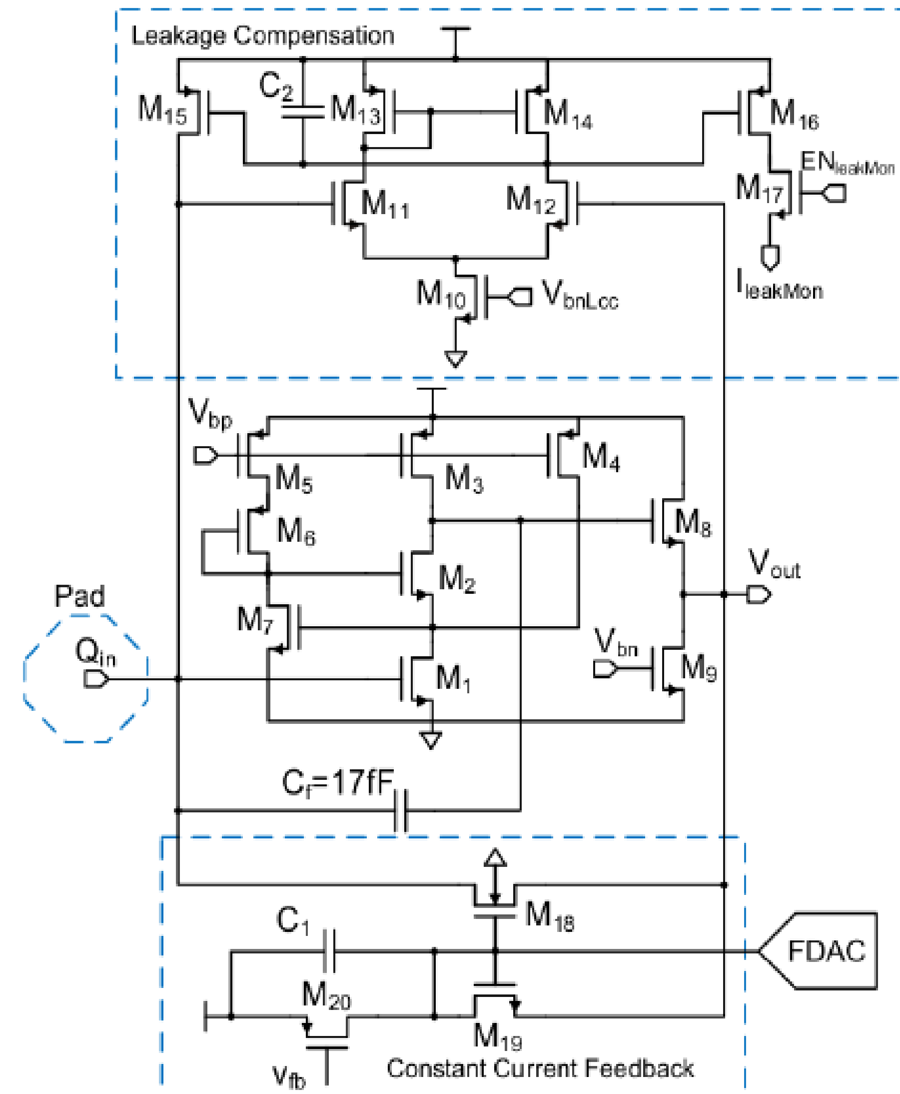
- Two-stage Amplifier configuration
  - Optimized for low power, low noise and fast rise time
- The second stage Amp2 is AC coupled to the preamplifier
  - Additional gain Cc/Cf2~ 6
  - decoupled from preamplifier DC potential shift caused by leakage
- The main motivation on the 2 stage structure is to provide a High gain
  - More flexibility on the choice of Cf1
  - The charge collection less dependent on the detector capacitor
- Local DACs for tuning feedback current and global threshold
- Charge injection circuitry for testing and characterization
- 13 bits for pixel configuration:
  - 4 FDAC: tuning feedback current
  - 5 TDAC: tuning of discriminator threshold
  - 2 Local charge injection circuitry
  - 1 Hit Enable
  - 1 HitBus / IleakMonitor





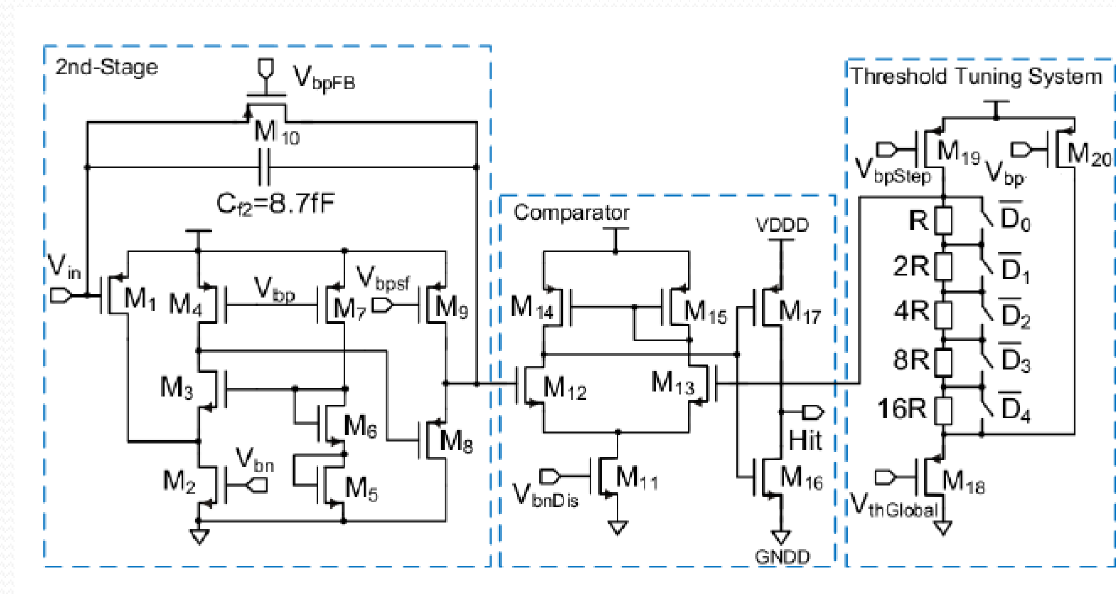
Preamplifier design

- Regulated telescopic cascode
  - The current flows into the input transistor and not through biasing structure : Low noise
  - nMOS as input transistor (M1)
  - High transconductance
  - High dynamic range for expected positive output signals
  - Triple Well structure avoid substrate noise
  - Source follower stage to drive the capacitance of the Amp2
- Continuous reset provided by M18 biased with a current mirror stage
  - The Feed back current is tuned by a local DAC
  - For high output signals, M18 becomes saturated
    - Linear return to the baseline
    - Time over Threshold : ToT
- Leakage compensation structure
  - Tracks the DC shift between input and output
  - Bandwidth of the M11-M12 pair is limited by C2
  - Insensitive to quick variations (Signal)
- The leakage current is monitored by M16-M17



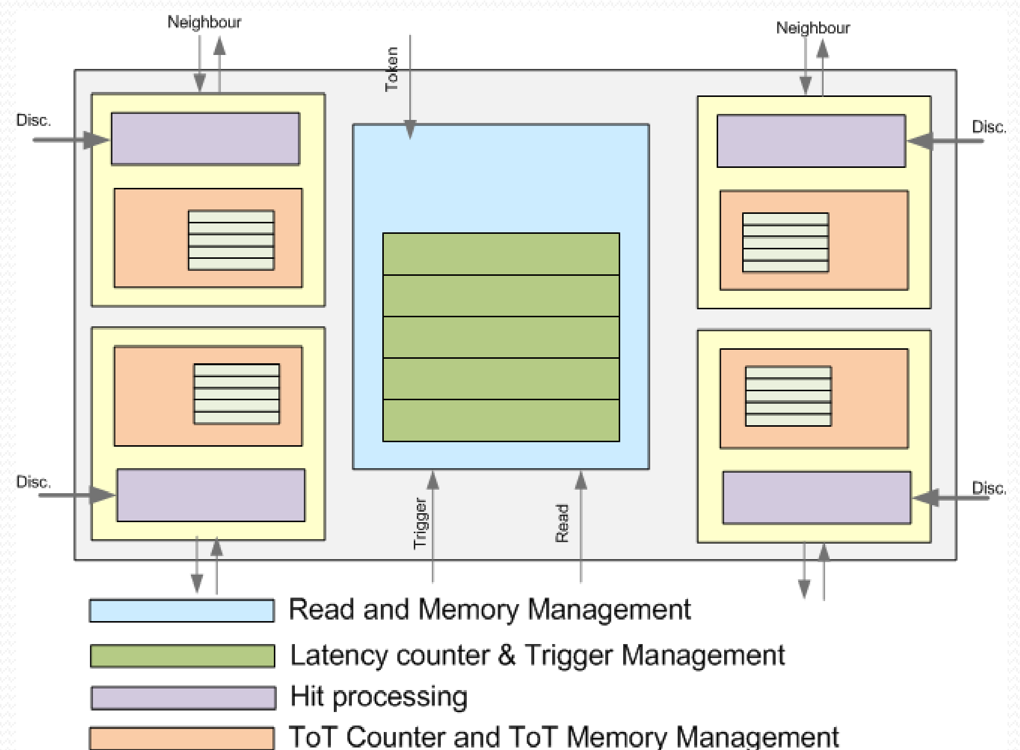
Amplifier and discriminator stages

- The second stage amplifier (Amp2) uses :
  - pMOS input transistor for large dynamic range
  - Feedback time constant of the amplifier is significantly larger than that of the preamplifier
  - M10 used mainly to set the DC operating point
- Classic 2-stage comparator design
  - The second comparator stage is powered by the digital supply voltage
- The global threshold VthGlobal is applied to the input of a source-follower (M18, M19 and M20)
- A local voltage offset is added by the threshold tuning DAC (TDAC) :
  - Resistor ladder and the current source M19
- M18 adds a Vgs to VthGlobal
  - The drawback is the Vgs variation with the temperature
  - Needs to introduce a compensation circuit

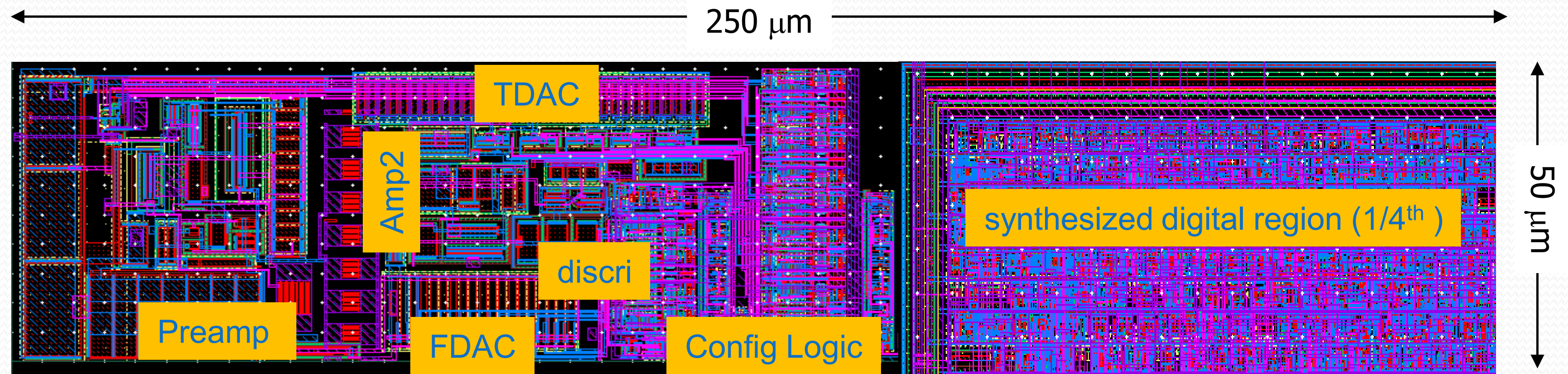


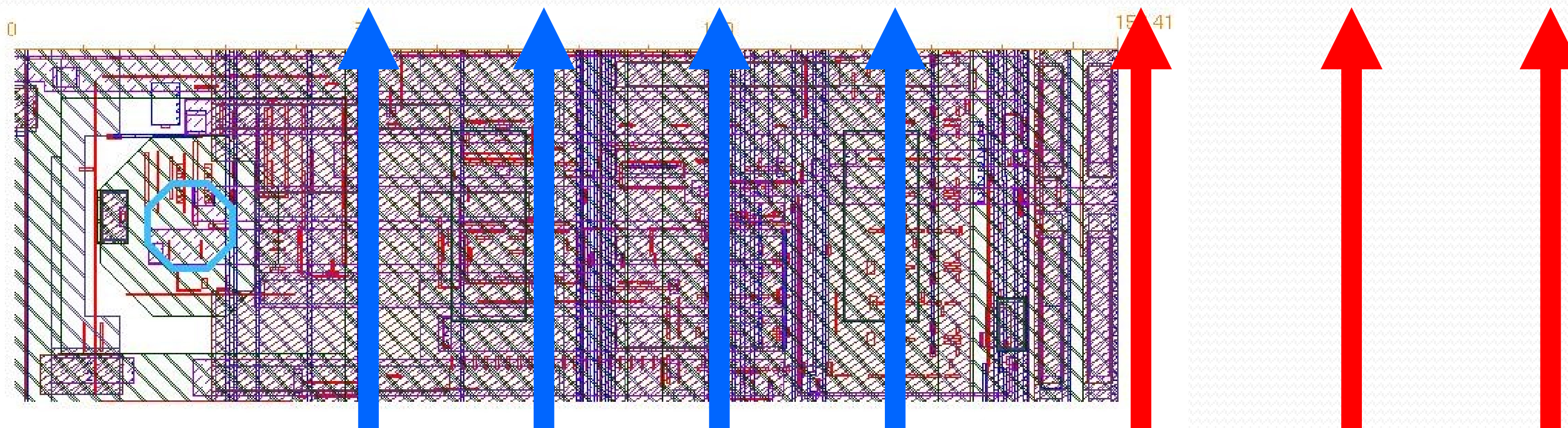
Pixel Digital Region

- In the present chip (FEI3) :
  - Each pixel is logically independent inside the DC
  - All hit pixels are shipped to End of Column buffer
  - A hit pixel need to transfer its data to EoC before accepting new hit : Congestion Problem for a high hit rate
- For the FEI4 chip
  - Basic idea is to store the hit locally until L1T
  - Implementation of local buffers is possible because of the smaller feature size (130 nm)
  - Organized on PDR : Pixel Digital Region
- A PDR processes the data from 4 pixel discriminator
  - Store locally up to 5 events/hits (different BC)
  - Small/big hit discrimination (3 programmable modes)
  - 2 BC association for small hit
  - 4 bit ToT (small hit, no hit, long hit, 13 x value)
  - Neighbor logic (1 bit)
  - Records up to 16 consecutive triggers (4 bit)
  - Programmable latency max. 257 BC
  - Token type readout



Pixel Layout

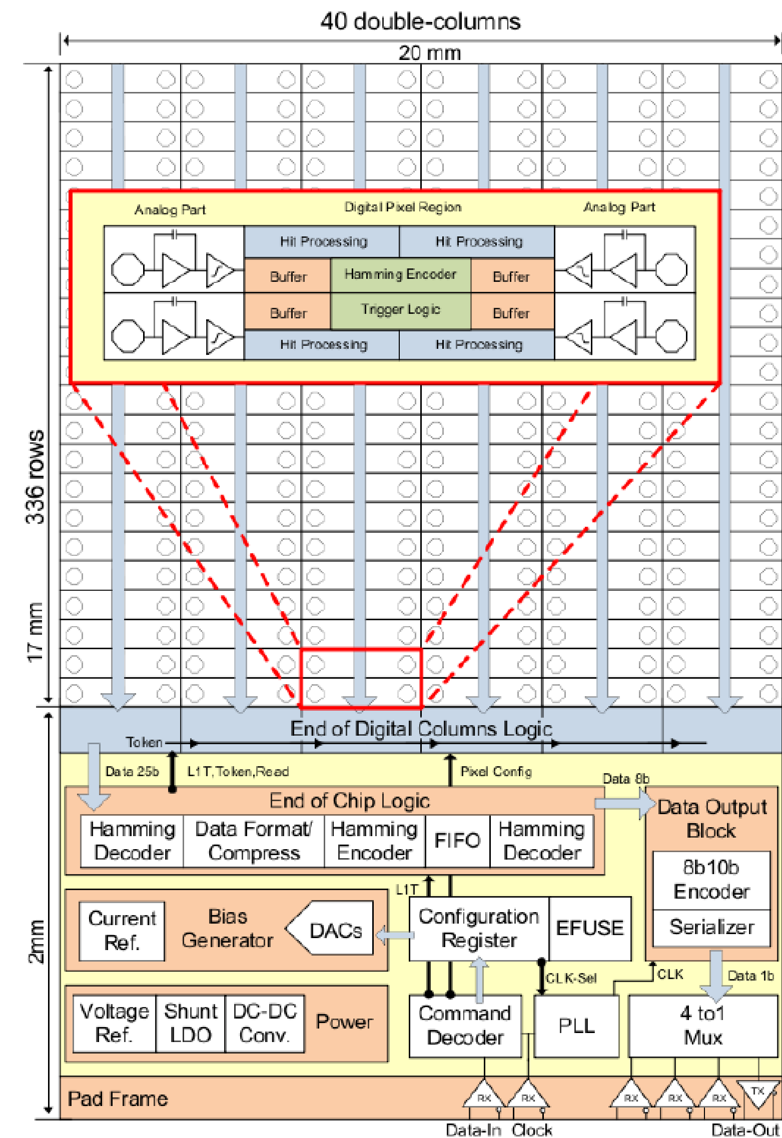




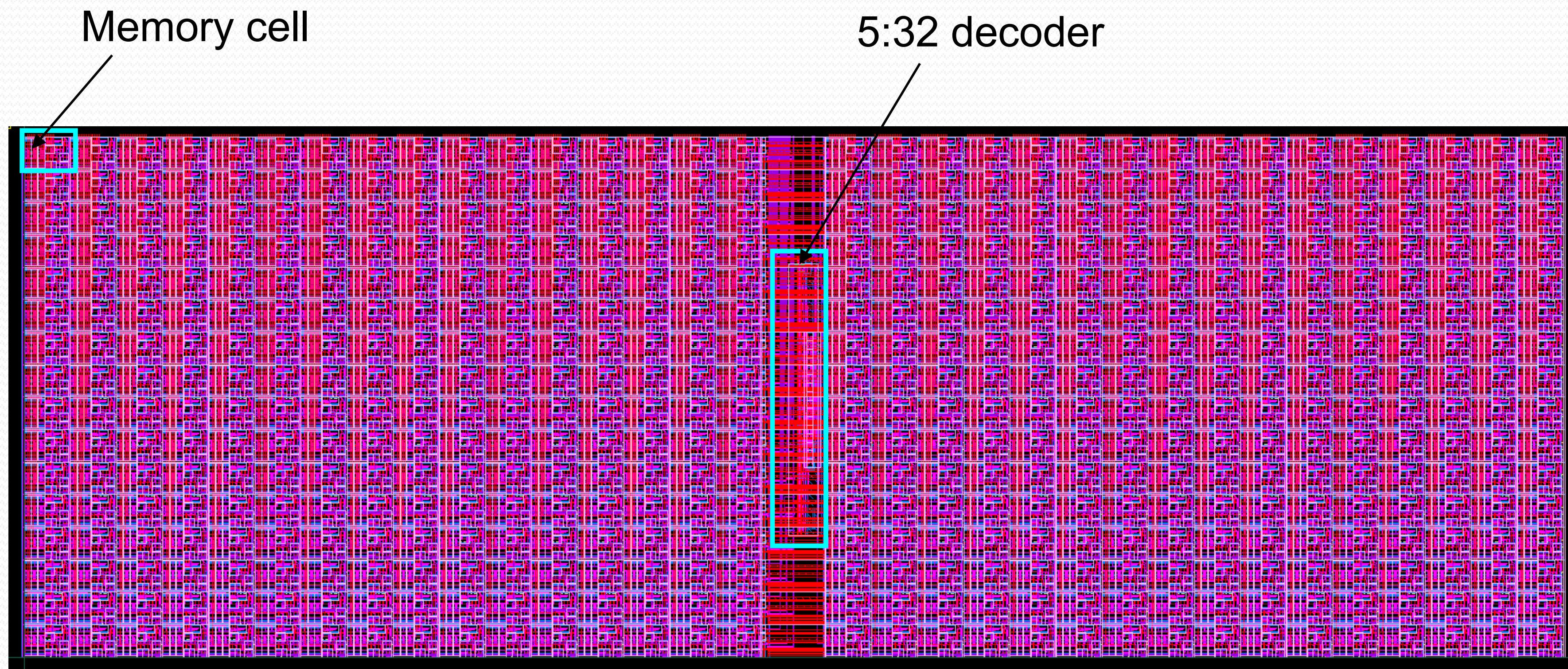
- Power distribution Only Vertical – No Analog/Digital crossing
- Shield on top Metals
- Digital ground tied to substrate, mixed signal environment BUT digital region placed in “T3” deep n-well

Other designed blocks

- Clock Generator
  - PLL generating 8×, 4×, 2×, and 1× clocks waveforms with 50% duty from the 40 MHz clock
- Command Decoder
  - The command decoder (CMD) is responsible for interpreting the serial commands to control the chip
  - The CMD state machine is triplicated, so that there are actually three distinct copies inside the FE-I4 and all CMD outputs are selected with a majority voting circuit.
- Global Configuration Memory
- Efuse Memory
- Pulse Generator for calibration



The Global Configuration Memory



- 16 rows by 32 columns
- All inputs and outputs pins are on the top side
- Block dimensions : 900 μm × 360 μm
- Each cell is a triplication of a DICE latch

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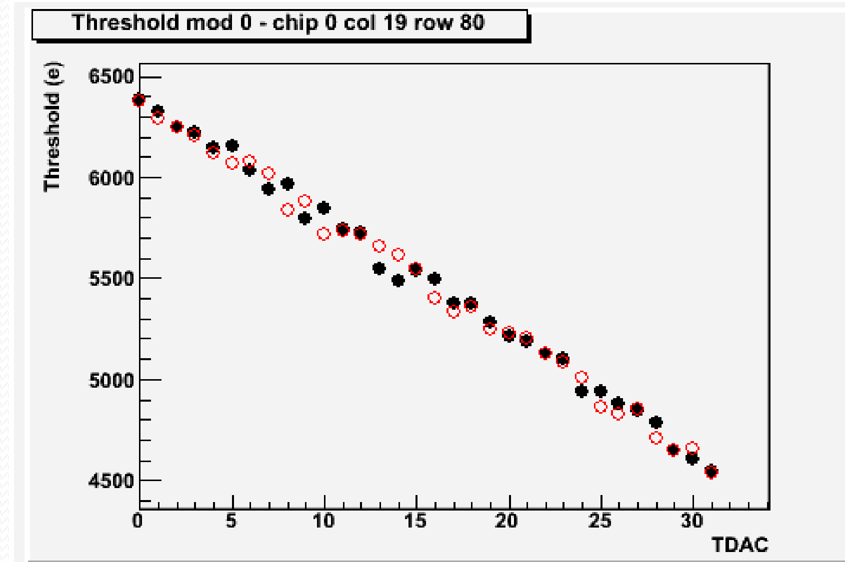
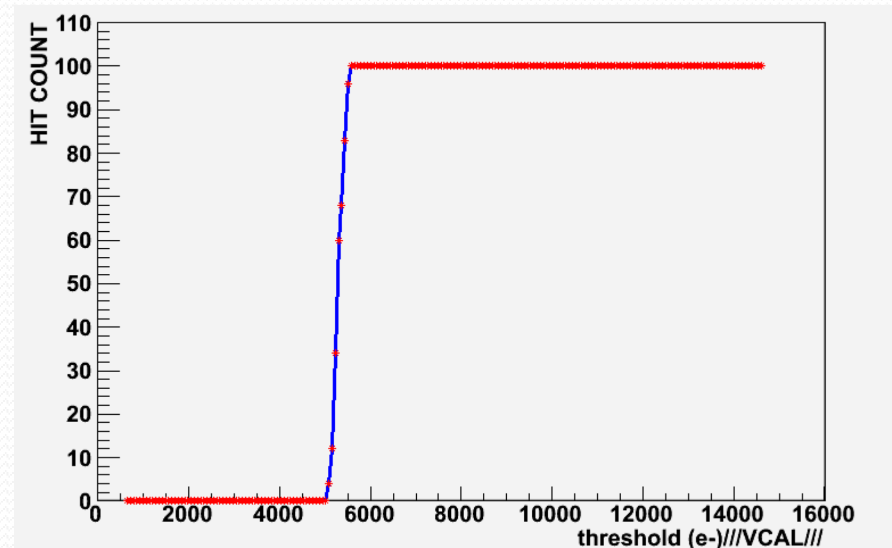
  - Module results
  - Irradiation and SEU
- Conclusion, Perspectives and Design changes for FE-I4

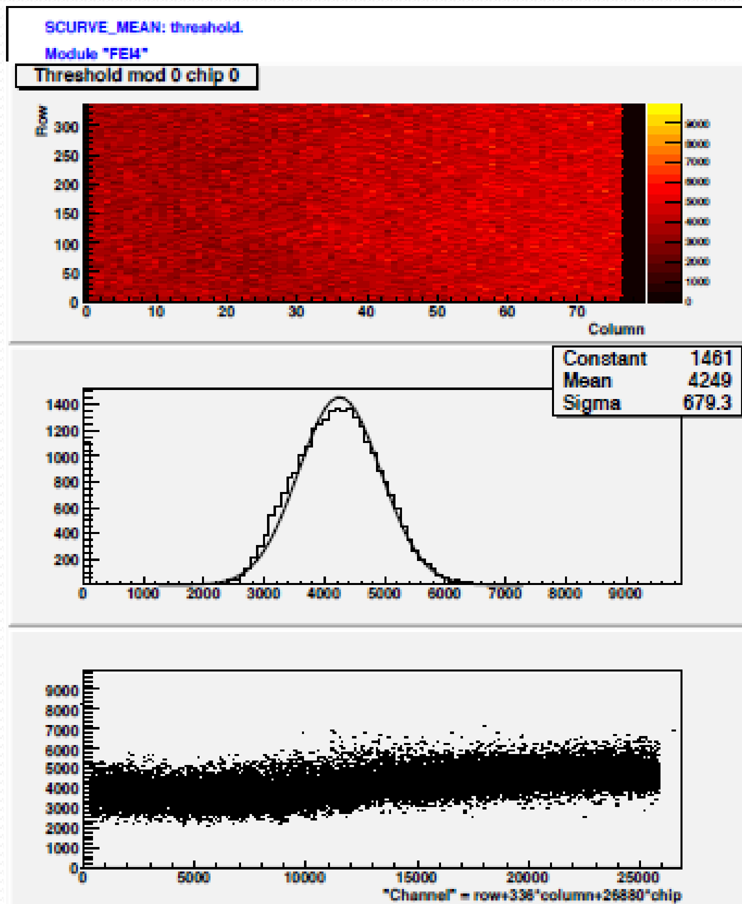
Threshold and Noise

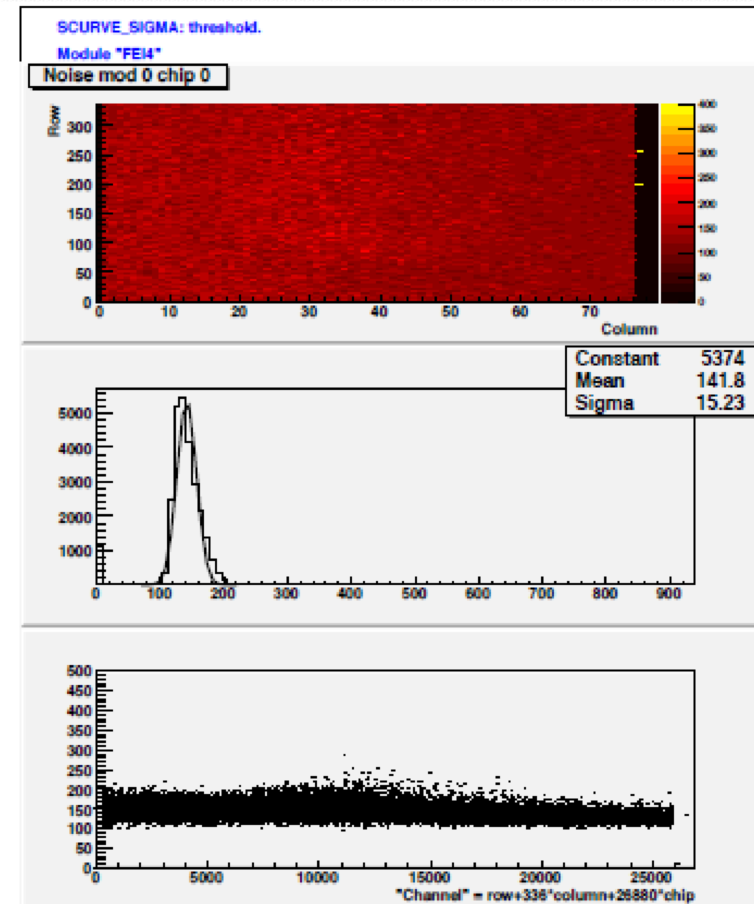
- In order to determine the threshold and noise values of the individual pixels, automated threshold scans were performed
- For a fixed threshold, N calibration pulses are applied to the amplifiers
- The count rate in the pixels is then recorded as a function of the applied calibration voltage
- This assumes a good DAC linearity
- From the resulting scan curve, the threshold and the RMS noise of each pixel are determined





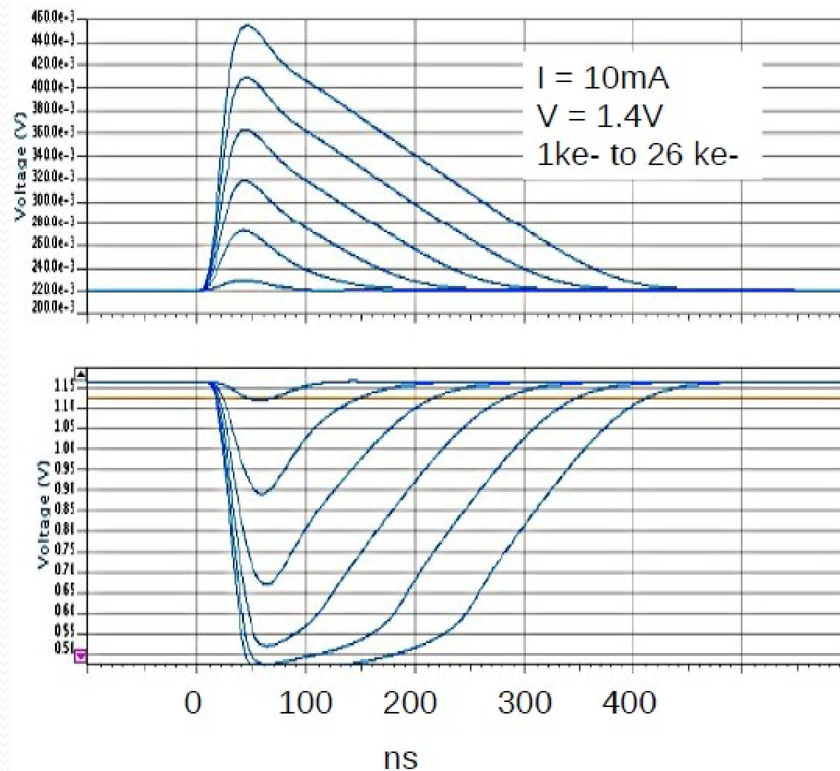
Threshold and Noise





- The threshold value for each pixel is shown for a setting of 4000e-
- The threshold dispersion before tuning is 680 e- RMS
- After Tuning the threshold dispersion reaches a value of 30 to 50 e- RMS
- The RMS noise value is 142 e-

Pulse shape and ToT



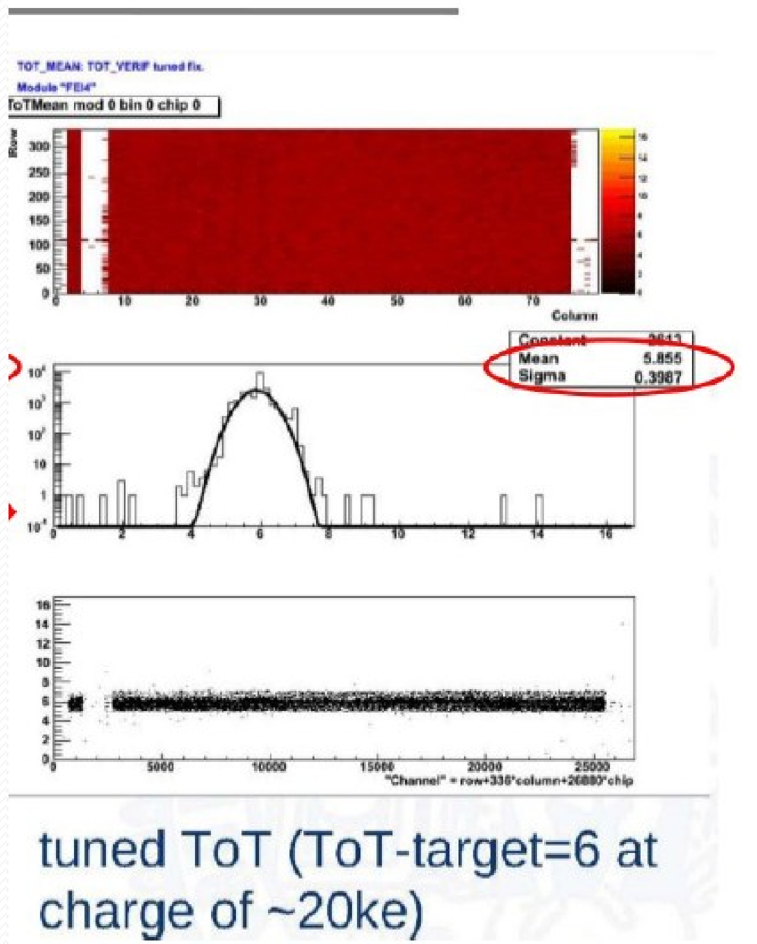
"True" ToT (clocks)	HitDiscCnfg 00	01	10	11
Below tresh	F	F	F	x
1	0	E	E	x
2	1	0	E	x
3	2	1	0	x
4	3	2	1	x
5	4	3	2	x
6	5	4	3	x
7	6	5	4	x
8	7	6	5	x
9	8	7	6	x
10	9	8	7	x
11	A	9	8	x
12	B	A	9	x
13	C	B	A	x
14	D	C	B	x
15	D	D	C	x
≥16	D	D	D	x

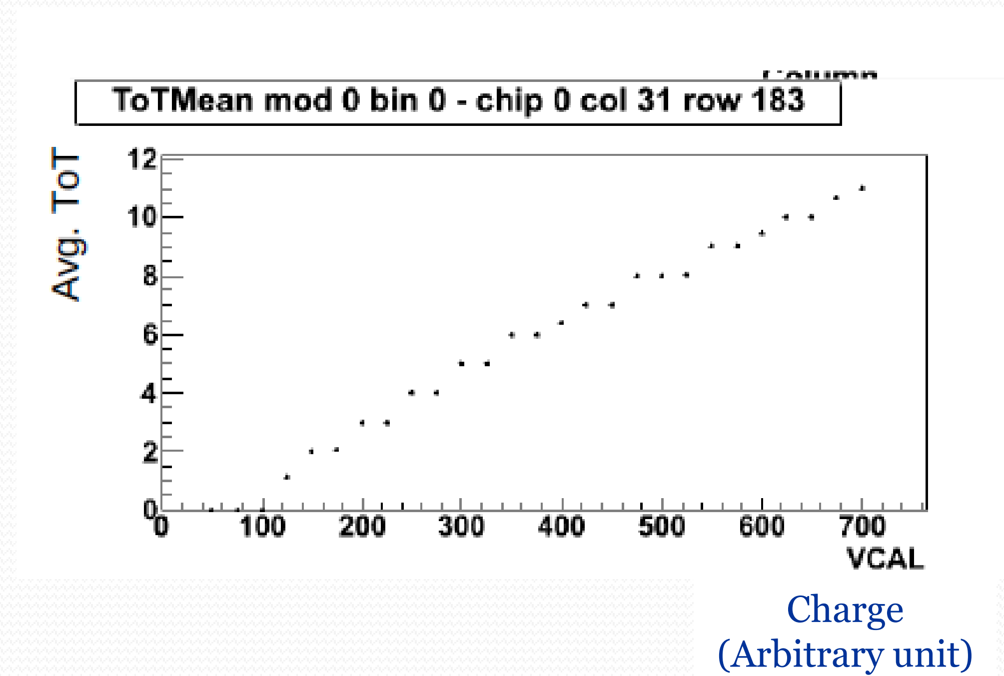
Corrected for timewalk

Not corrected for t-wlk

- Small hits might arrive in later BC than big hits due to time walk
- In order to reduce the time walk effect
  - A time window of 2 clock cycles is considered
  - Used to associate small hits to big hits
- Small/big hit discrimination is defined by HitDiscConfig bit

Charge measurement





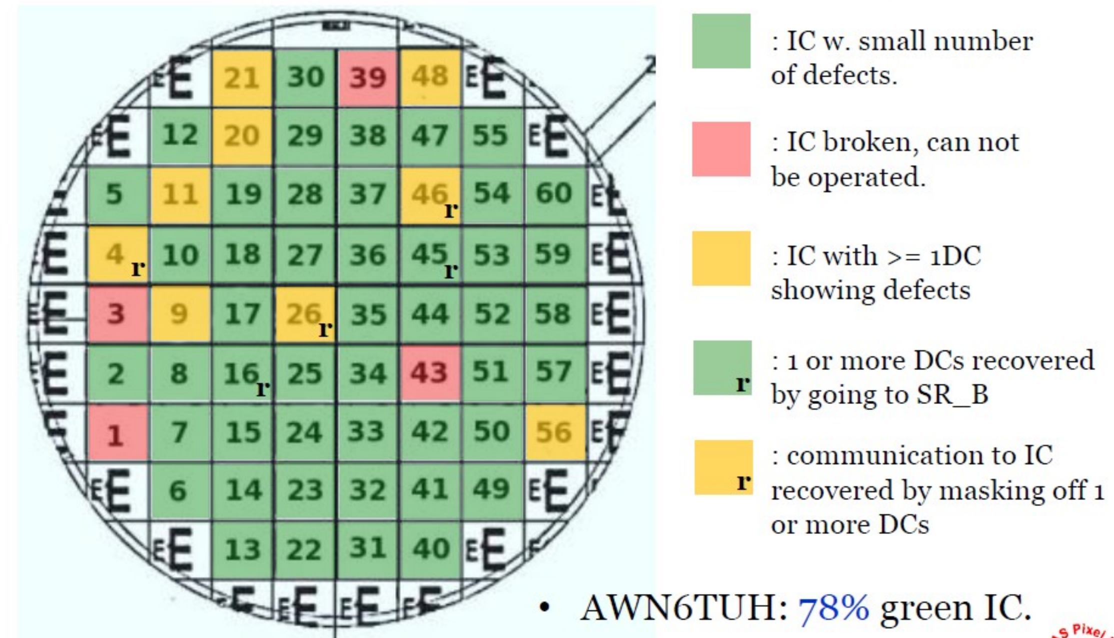
- ToT versusFDAC works:
- The tuning works too
- ToT versus the Charge scan works

Wafer testing

- 16 wafers received
  - Testing started in October 2010
- Wafers tested and "fully characterized" at Bonn
  - Testing done with USBpixTest / STctrl
  - Web-based inventory system: http://icwiki.physik.uni-bonn.de/twiki/bin/view/Systems/UsbPix#Inventory
  - Data available on server in Bonn
- Wafer Test Methodology :
  - Record Voltages / Currents (VDDA1, VDDA2, VDDD1, VDDD2)
    - At the power-up
    - With various global configuration + Global Configuration register tests
  - Pixel Latch tests (13 latches / pixel) : Defect mapping
  - Simple HitOR mapping (inject in fraction of pixels, 21/DC)
  - Digital injection : Digital hit map
  - Analog injection : Analog hit map
  - Threshold scan : Threshold and noise histogram

What is the Yield ?

- Based on 9 wafers
  - Focus on having "fast" some wafers available (sensors tests, thinning tests…)
  - Rather loose criteria so-far
- RED: IC can not be operated
  - High currents
  - Many DCs broken
  - Configuration failing
  - Injection failing, empty maps (analog / digital).
- Yellow: IC with some defects
  - Few DCs broken
  - Bad Pixel Register tests but works
  - High currents but works
  - "Regional" failures (e.g. corners)
  - Very high threshold / noise.
- Yield for the 9 wafers : 68%, 78%, 67%, 32%, 70%, 88%, 57%, 65%, 63%...
- Global yield : ~65%



Module testing

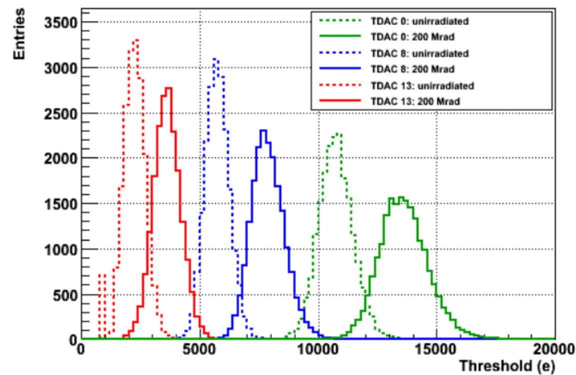
- 16 FE-I4 assembled, mostly with planar silicon and some with 3D sensors
  - IZM bump-bonding
  - 14 of them were tested
- 3 modules each irradiated at Karlsruhe (2...3.10^{15} n/cm2) and irradiated at Ljubljana (~5.10^{15} n/cm2)
- Several modules in test beam at DESY
- Lab tests:
  - Noise and threshold tuning are OK
  - First irradiated modules OK (some problems with tuning, under investigation)
- Source, cosmics and test beam measurements very successful
  - Data taking works
  - Hit efficiency is high
  - ToT spectrum is as expected
  - ToT code works
  - Timing ~OK

Irradiation

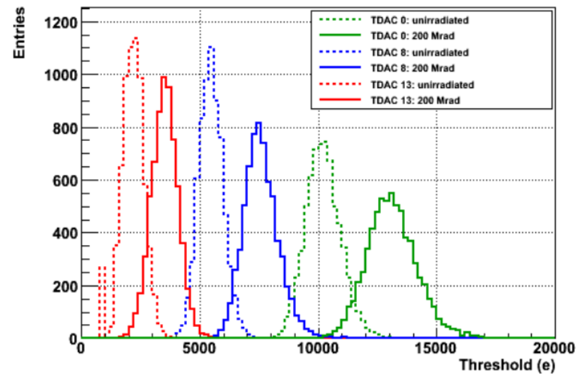
- Irradiated 3 chips on December 4-6, 2010 in Los Alamos
- 3 cm diameter beam spot of 800 MeV protons
- Target doses averaged over the whole chip :
  - ~6 Mrad
  - ~75 Mrad
  - ~200 Mrad
- FE-I4A powered, but not configured during irradiation
- All three chips survived irradiation
  - Digital and Analog part work well after irradiation
- Current reference changes by about 2-3%
  - Centering of trim range is done in the new design (FE-I4B)
- Increase in the leakage current
  - Maximum change at 6 Mrad (Compatible with CERN threshold shift study)
- Threshold dispersion still unchanged
- Noise increases by about 20%
- SEU measurements are done now at CERN PS

Effect on the threshold

Threshold Scans: Chip 46 (200 Mrad)



Nominal DCs



CfIsVncap DCs

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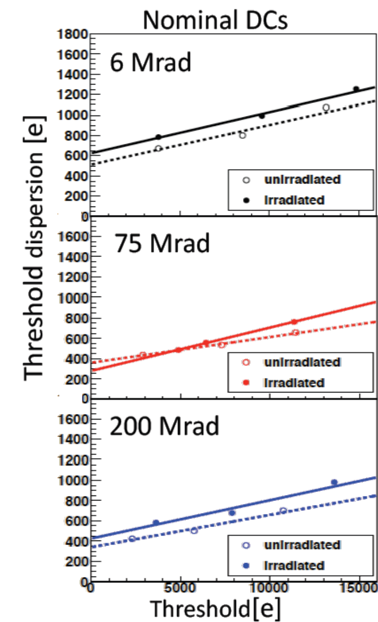
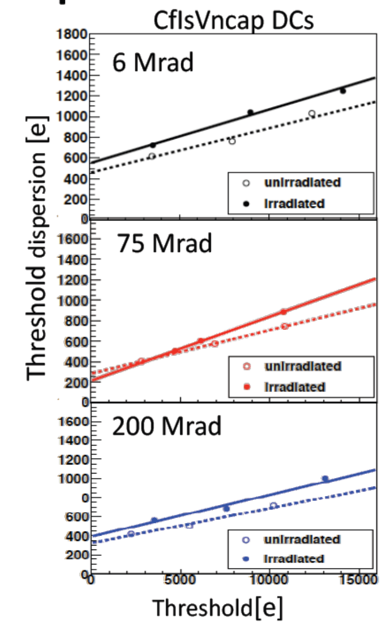
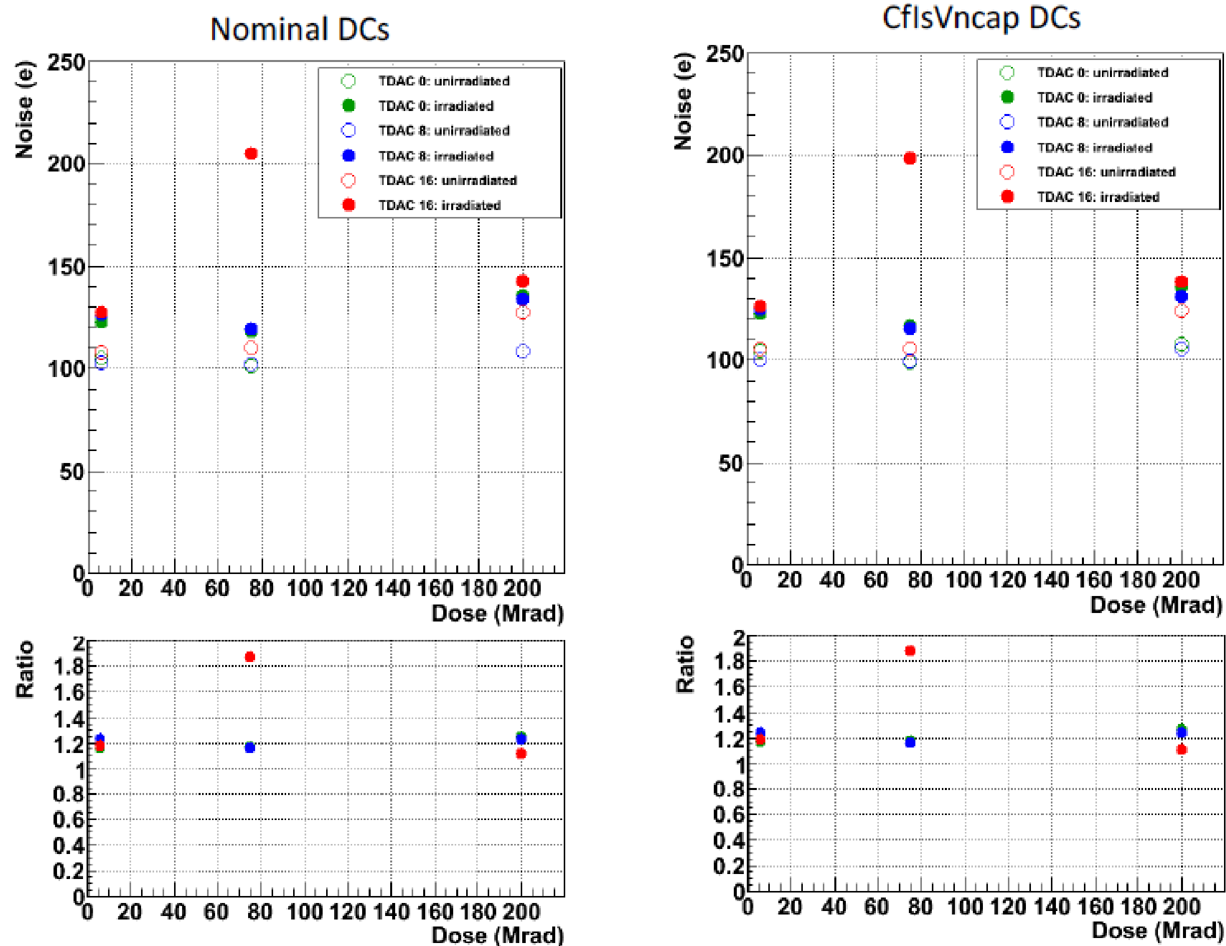
Threshold Dispersion





- Threshold dispersion still unchanged
- Comparable results for the 2 columns variants

Effect on the noise



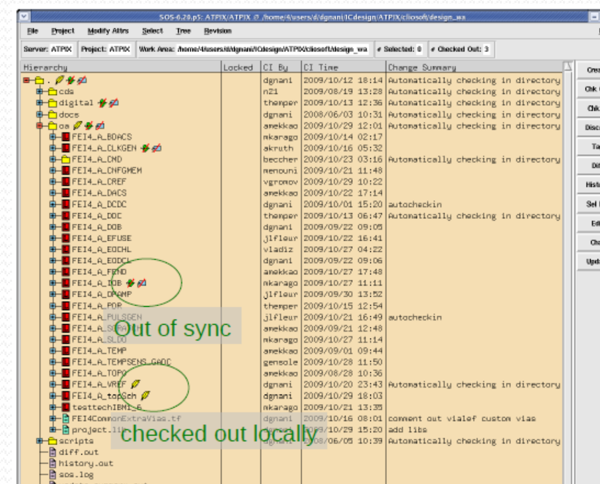
- Noise increases by about 20% after irradiation
- Similar noise distribution for nominal DCs and CFIsVncap variants DCs
- Noise increases by about 20% but no systematic effects observed

Conclusion

- Measurement with FE-I4A modules are very promising
  - Test Beam and Source testing OK
  - We only tested the main functionalities
    - Still to test many things
    - Irradiation tests started and have to finalize SEU tests
- The FE-I4A chip respects most specifications
  - Some minor changes have to be done
  - Starting FE-I4B design effort aiming to submit in June 2011: production version for IBL installation in 2013
- For the IBL :
  - Production of the FE-I4B version for this Summer
  - IBL is simple : 1 Module = 1 Chip
  - No power conversion
  - Chip has direct data link to DAQ crate
- For the upgrade phase2 (phase 1?)
  - FE-I4 size and other features aimed at covering large areas with pixels in future
  - Module = 4 × FE-I4 chips and no module controller
  - Power conversion (either serial or DC-DC)
  - Module data link have to go to high speed serializer such as GBT
  - FE-I4C Design for the internal layers

FE-I4A Collaboration

- Collaborate remotely using Cliosoft.com platform.
- Repository hosted at LBNL and mirrored at all other sites
- Participating institutes :
  - *Bonn* : David Arutinov, Malte Backhaus, Marlon Barbero, Tomasz Hemperek, Laura Gonella, Michael Karagounis, Hans Krueger, Andre Kruth
  - *Genova*: Roberto Beccherle, Giovanni Darbo
  - *LBNL*: Lea Caminada, Sourabh Dube, Julien Fleury (LAL), Dario Gnani, Maurice Garcia-Sciveres, Frank Jensen, Yunpeng Lu (IHEP), Abderrezak Mekkaoui
  - *CPPM*: Patrick Breugnon, Denis Fougeron, Fabrice Gensolen, Mohsine Menouni, Sasha Rozanov
  - *NiKHEF*: Vladimir Gromov, Ruud Kluit, Jan David Schipper, Vladimir Zivkovic
  - *Goettingen*: Joern Grosse-Knetter, Jens Weingarten



Seamless Integration	
Cadence IC Platform	Manage Cadence IC libraries directly from the Cadence IC Platform. Manage cell views without worrying about the physical files that make up these design units.
Synopsys Custom Designer	Manage Open Access libraries directly from Custom Designer.
Mentor HDL Designer	Manage Mentor's HDL Designer Series libraries directly from Mentor's Design Browser. Manage logical design units without worrying about the physical files.
SpringSoft Laker	Design Browser allows easy navigation of libraries and provides convenient access to DM features from Laker.
C API	A complete C programming interface to integrate any in-house tools with the SOS data collaboration platform. Readily available multi-site DM support in all tools.