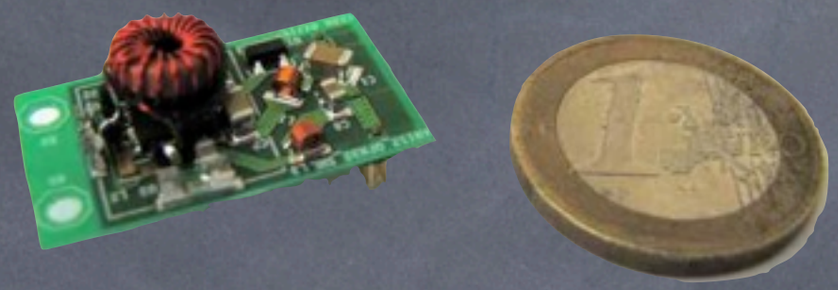


DCDC conversion ASIC developments

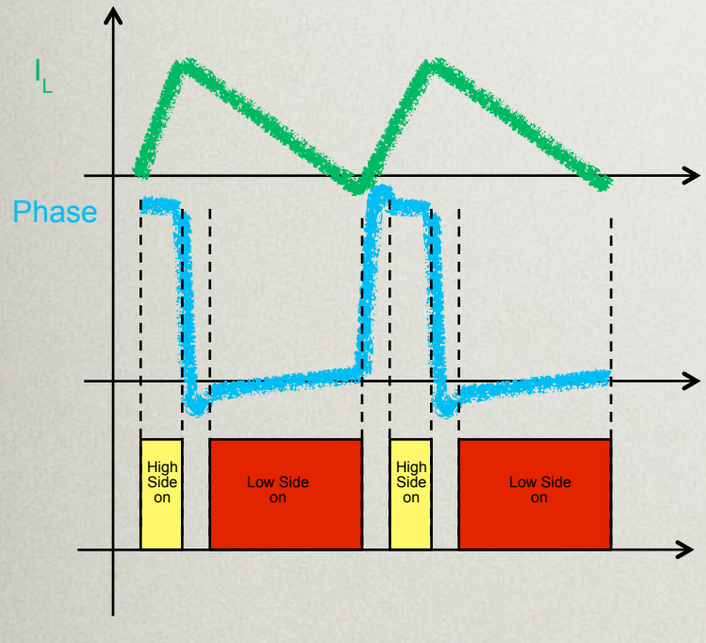
S.Michelis, F.Faccio, G.Blanchot, C.Fuentes, B.Allongue
CERN - PH/ESE

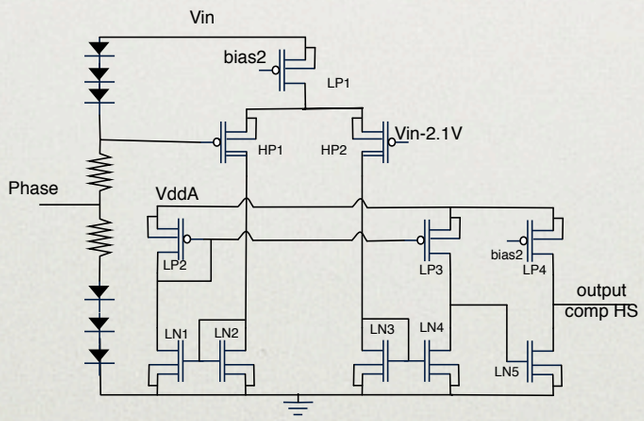
stefano.michelis@cern.ch

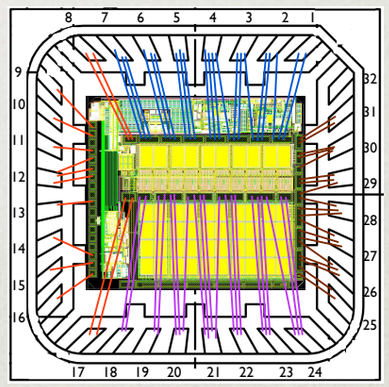
http://cern.ch/project-dcdc

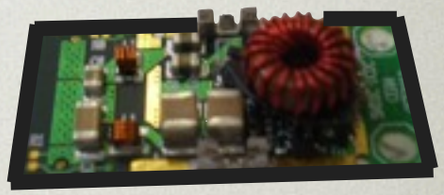
DCDC

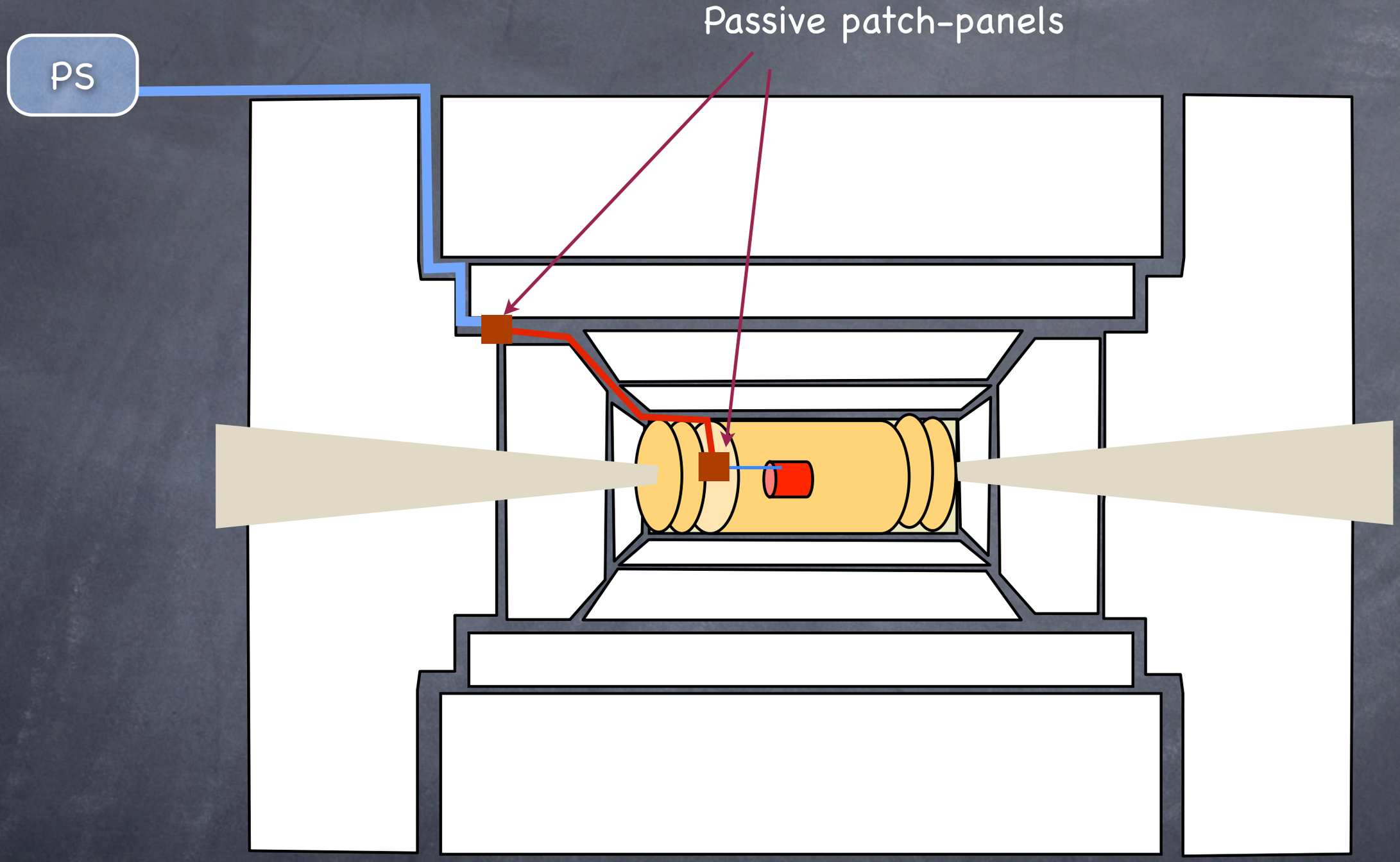
???


I_L
Phase
High Side on
Low Side on
High Side on
Low Side on


Vin
bias2
LP1
HP1
HP2
Vin-2.1V
Phase
VddA
LP2
LP3
bias2
LP4
output
comp HS
LN1
LN2
LN3
LN4
LN5


8 7 6 5 4 3 2 1
9 10 11 12 13 14 15 16
32 31 30 29 28 27 26 25
17 18 19 20 21 22 23 24





Conceptual representation of the power distribution system typically used in the LHC experiments

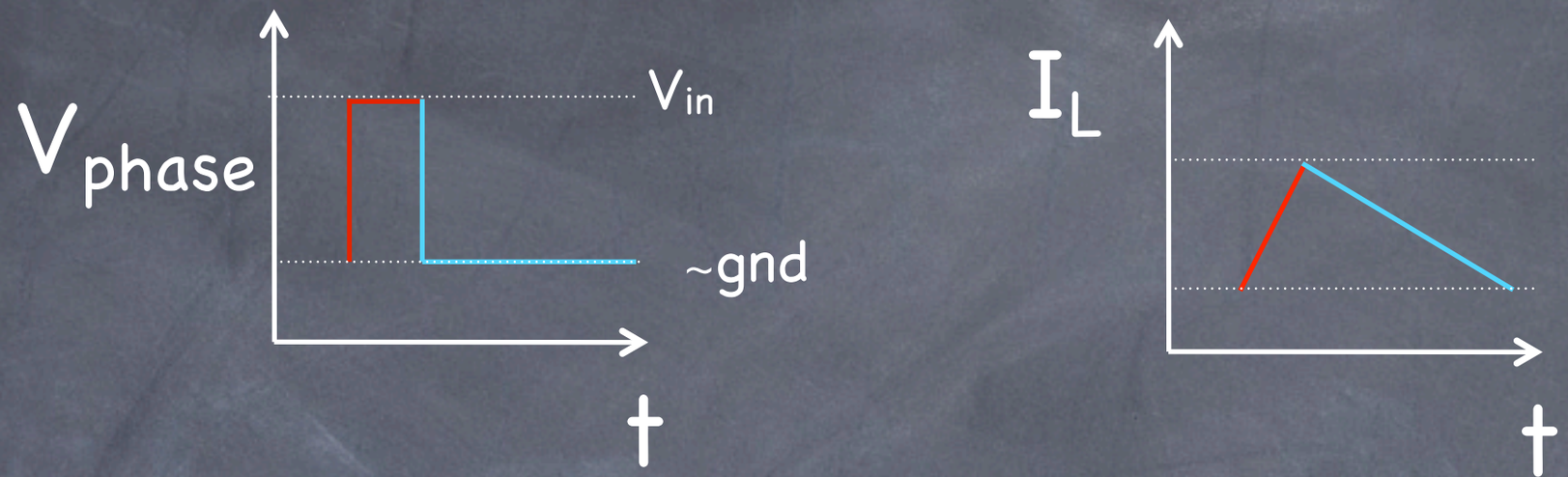
Power loss in cables: $P_{Loss}=R_{cable}I^2$

The electronics load (the FE boards) needs power at a precise voltage $P_{Load}=V_{Load}I_{Load}$

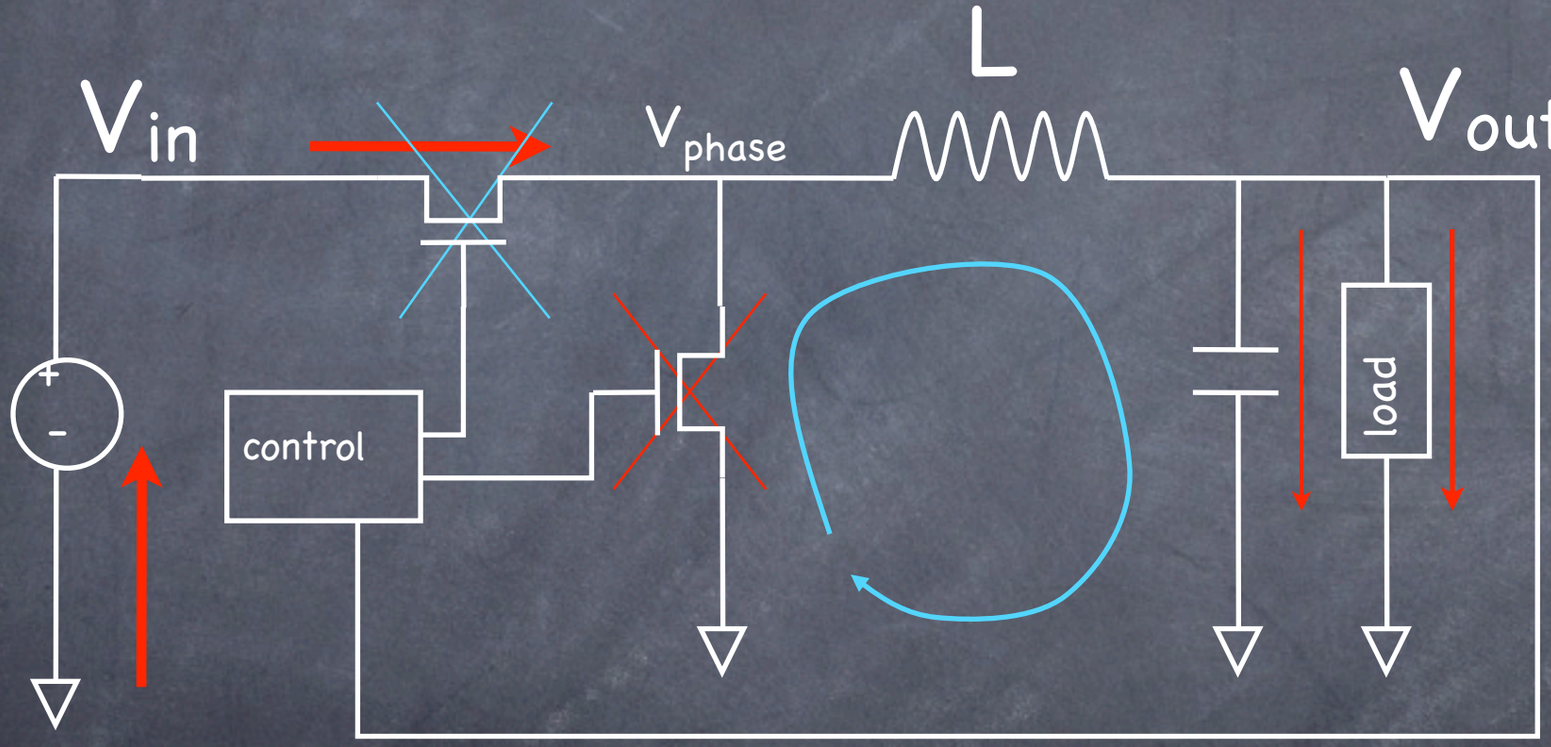
$P_{in}=V_{in}I_{cable}$ → DC/DC converter → $P_{out}=V_{Load}I_{Load}$

if $P_{in}=P_{out}$ and if $V_{in}>V_{Load}$, $I_{cable}<I_{Load}$

the DCDC needs to function in the radiation and magnetic field of the experiments

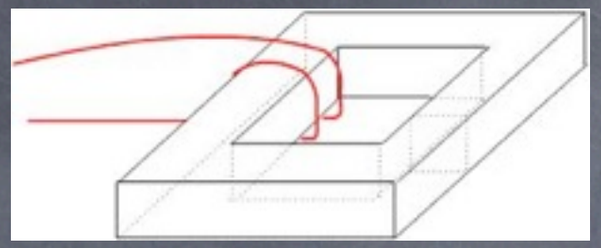


2
1

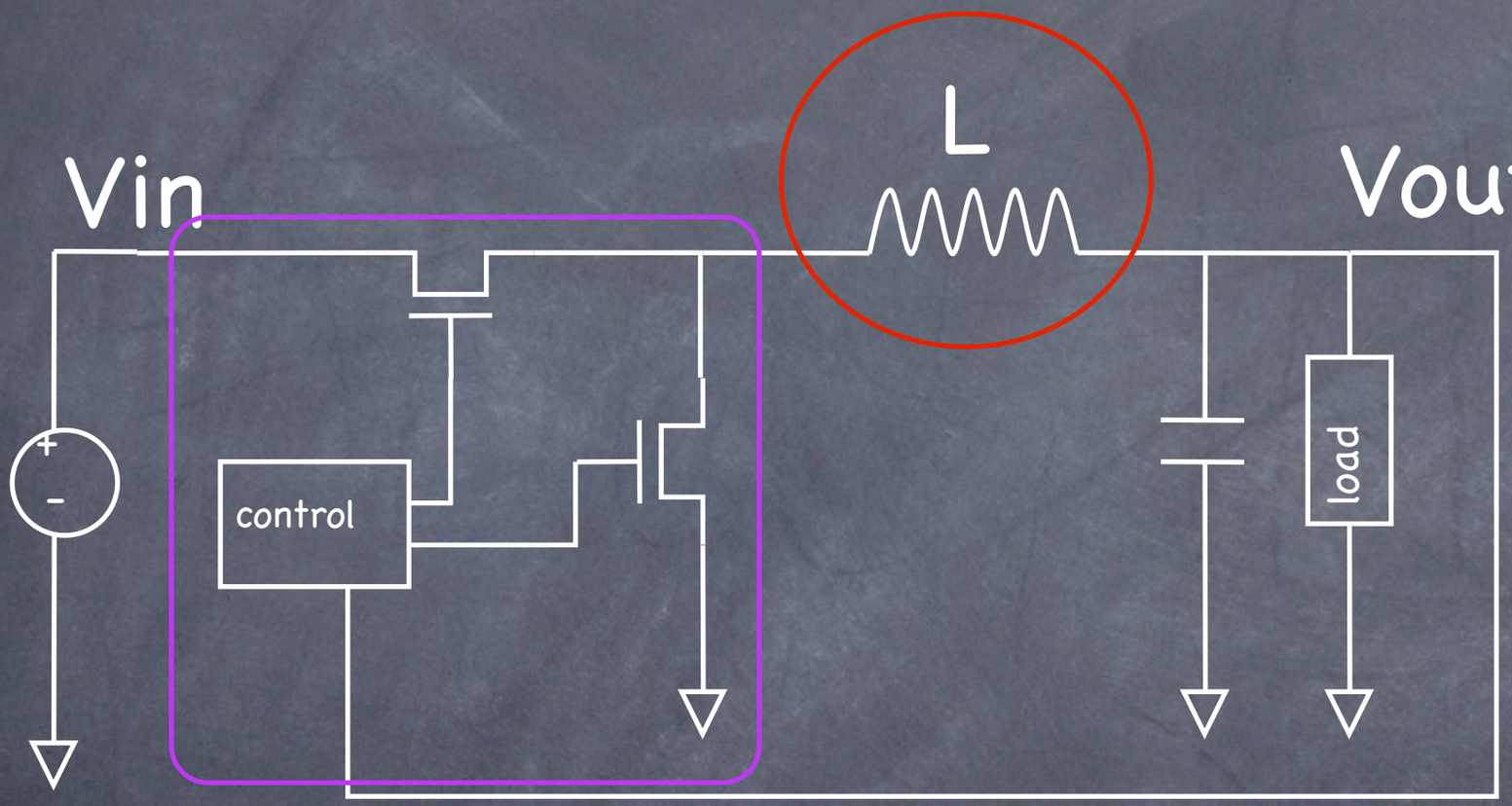


$$\frac{V_{out}}{V_{in}} = \text{Duty cycle}$$

Ferromagnetic core



Air core



Qualification required for radiation effects:
TID, displacement damage, SEEs

Electrical specs

Input voltage	10-12V
Output voltage	1.2-3.3V
Output current	up to 3A*
Efficiency	>80% (for V_{out}=2.5V)
Conducted and radiated noise compatible with installation in close proximity to FE electronics and detectors	

* We will know the real output current limit soon, with measurements of a mature ASIC in a realistic configuration (cooling)

Mechanical specs

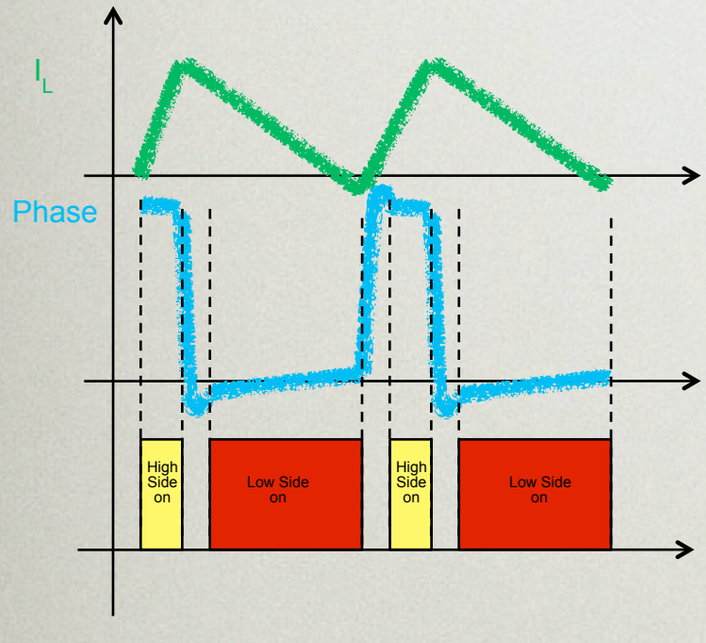
Small size (footprint, height)
Small contribution to material budget
Connectable to cooling system

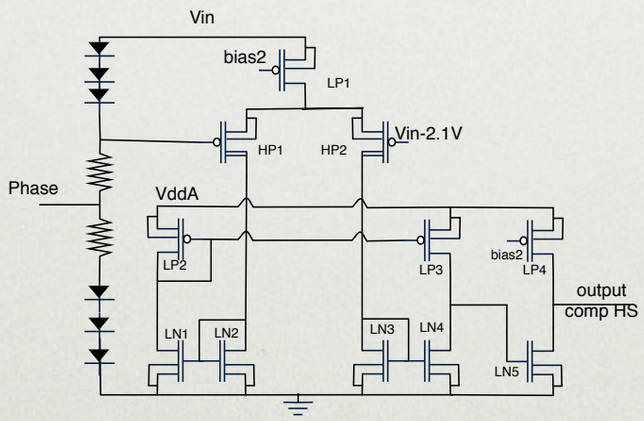
Environmental specs

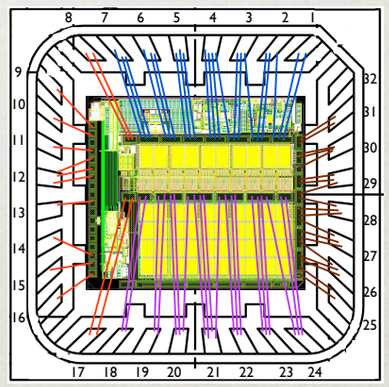
TID tolerance	250 Mrad
Displacement damage	$2.5 \cdot 10^{15}$ n/cm^2 (1MeV equivalent)
SEE	Absence of destructive SEEs and Vout transients when tested with heavy ions up to an LET of 30 MeVcm^{2}mg^{-1}
Magnetic field	4 T
Temperature of cooling pad	-30 to +10 °C

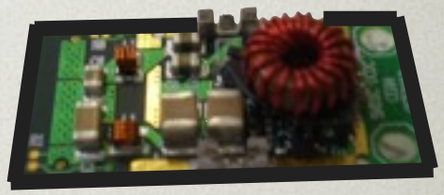
DCDC

???


I_L
Phase
High Side on
Low Side on
High Side on
Low Side on


Vin
bias2
LP1
HP1
HP2
Vin-2.1V
Phase
VddA
LP2
LP3
bias2
LP4
output
comp HS
LN1
LN2
LN3
LN4
LN5


8 7 6 5 4 3 2 1
9 10 11 12 13 14 15 16
32 31 30 29 28 27 26 25
17 18 19 20 21 22 23 24



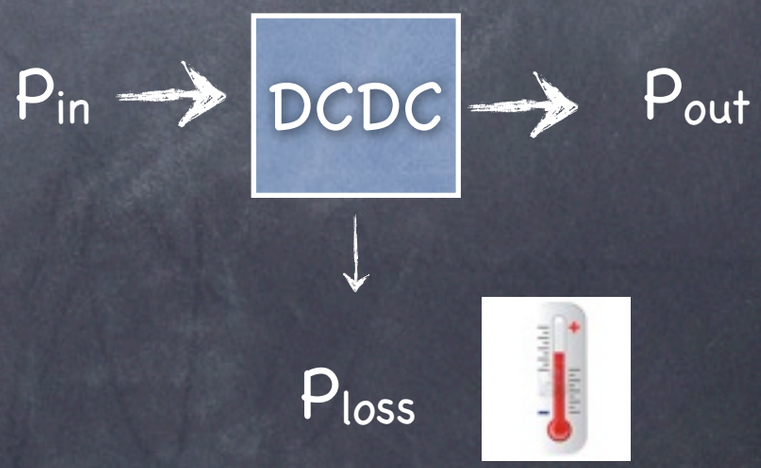
DC/DC ASIC design

Radiation tolerance:
Technology choice
HV transistors (10V)
LV transistors (control circuit)
Layout and design technique
(ELT, triplications)

2007-2009	pre-selection of CMOS technologies with HV extension
2008-2010	design of prototypes in the two pre-selected technologies (0.25 and 0.35um)
2010	SEE tests on the two technologies led to selection of 0.35um

Design for high efficiency:

$$efficiency = \frac{P_{out}}{P_{in}}$$

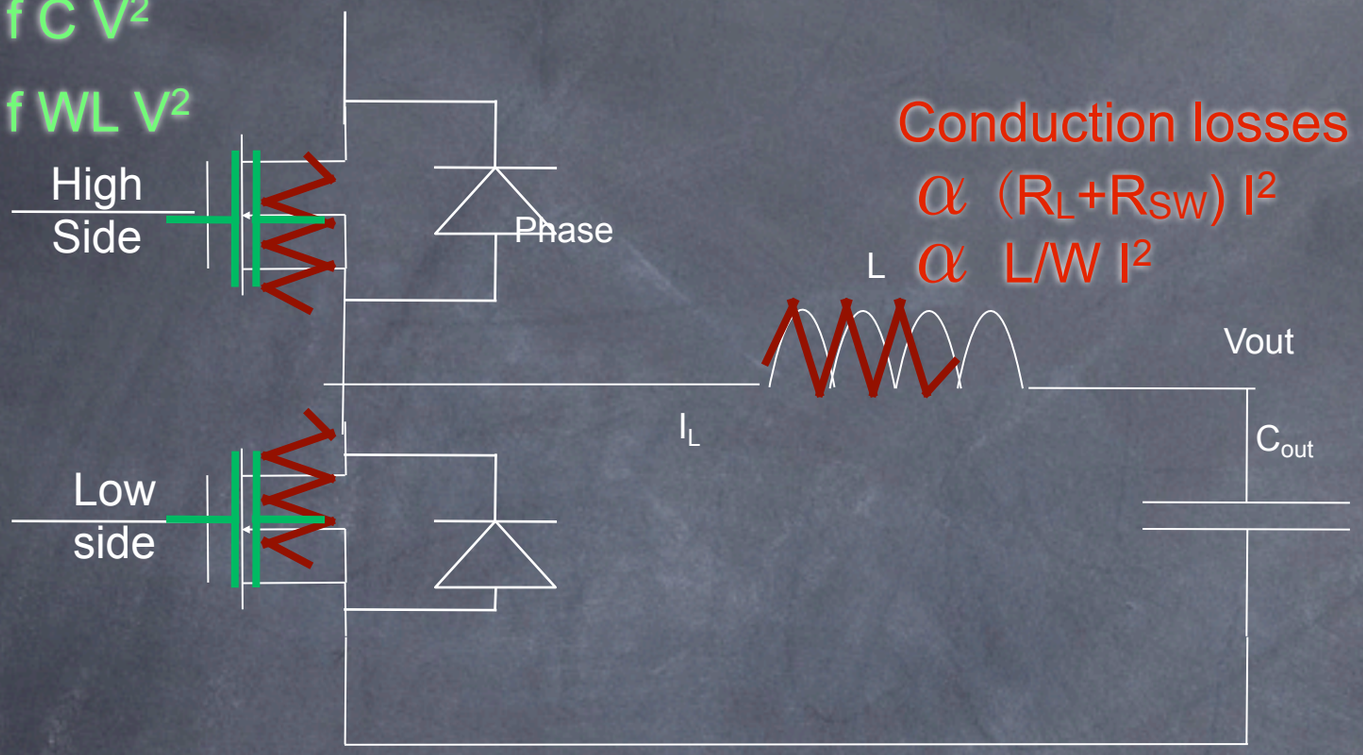


Losses in a converter

Driving losses

α f C V^2

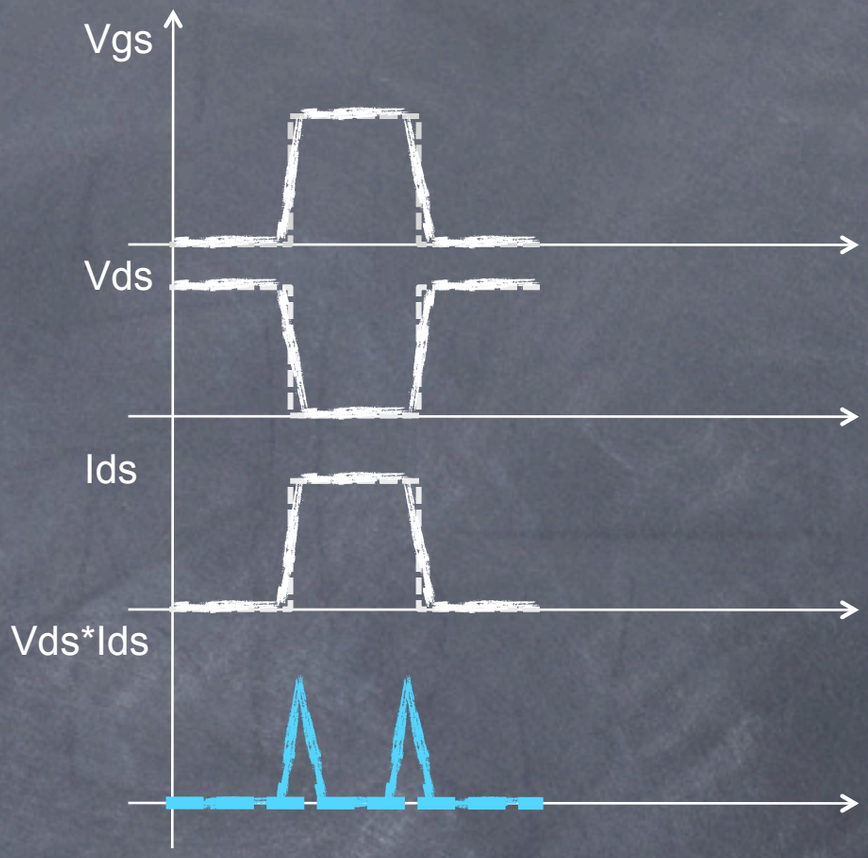
α f WL V^2



Conduction losses

α (R_L+R_{SW}) I^2

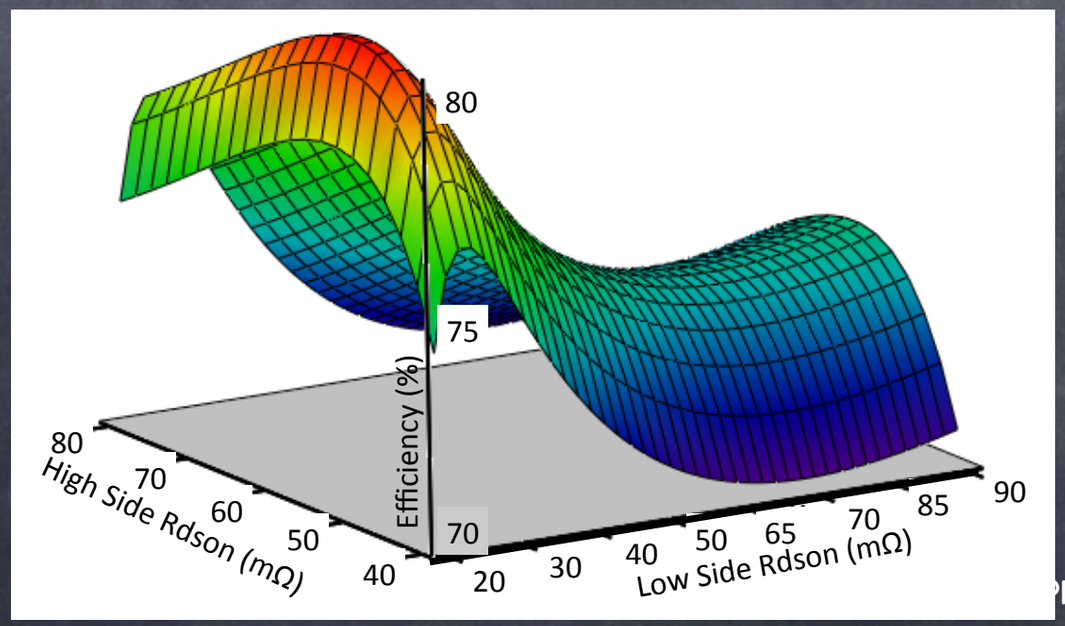
α L/W I^2



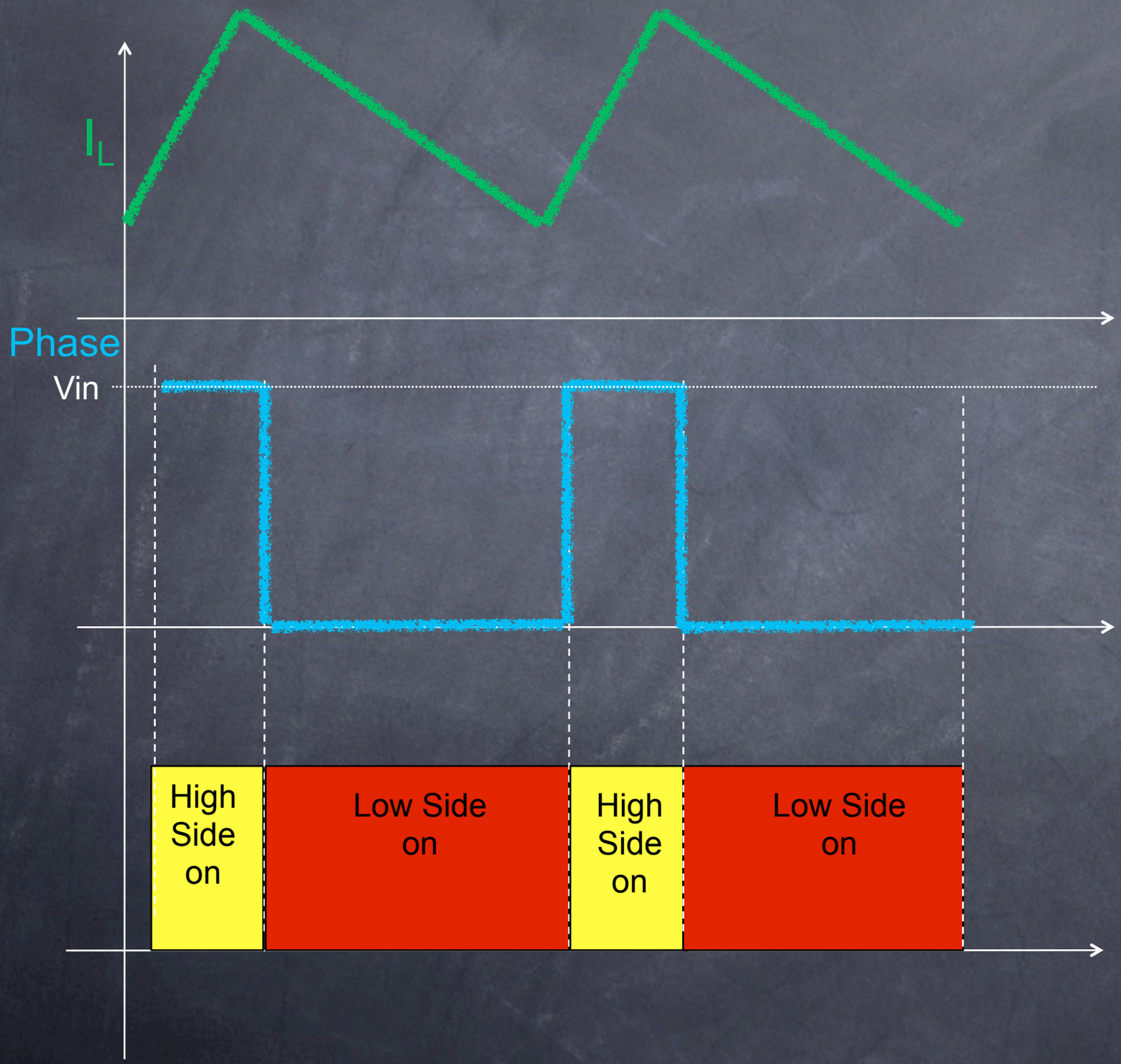
Switching losses

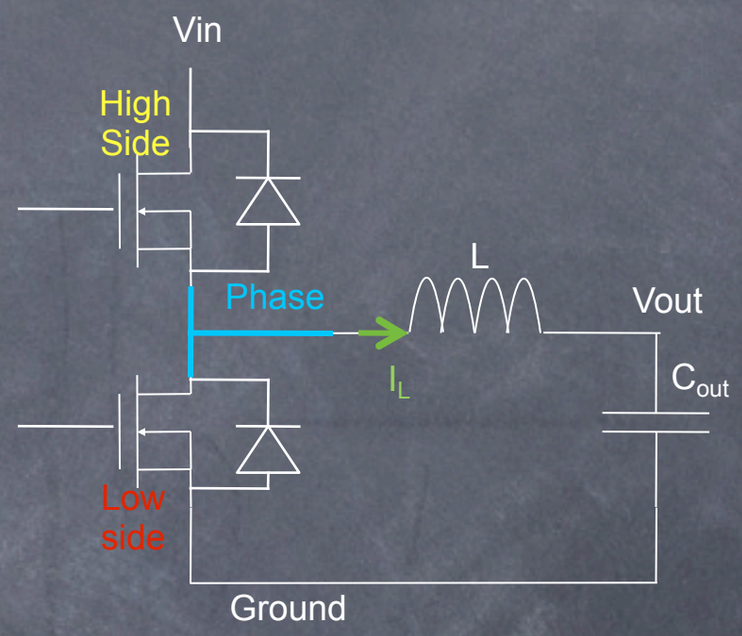
α f Vds Ids C

α f Vds Ids WL

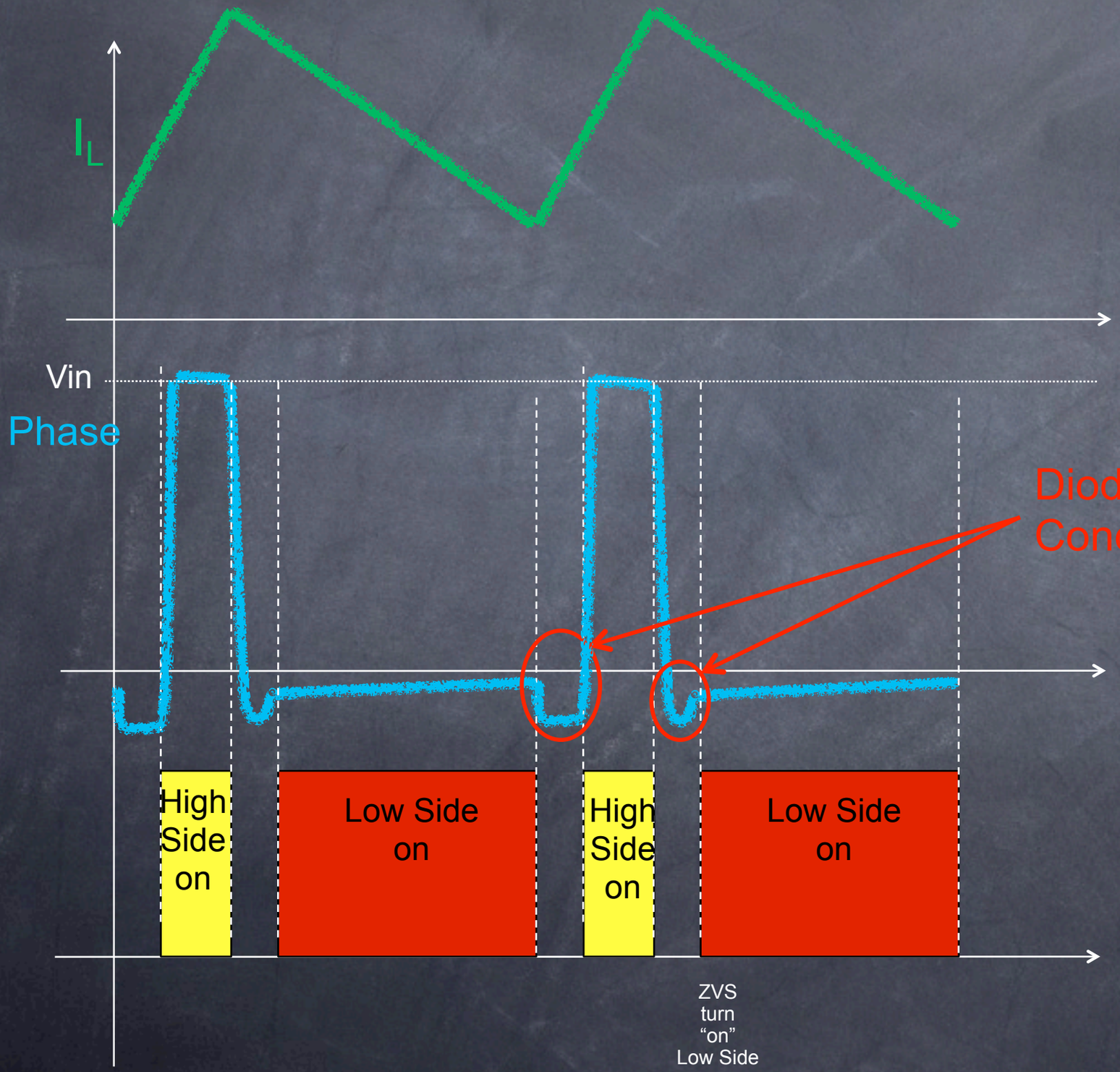


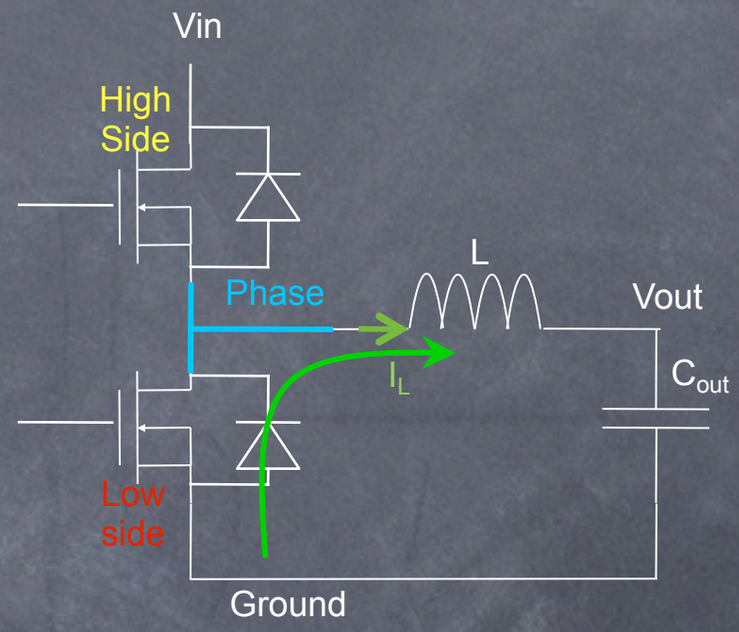
Ideal behavior



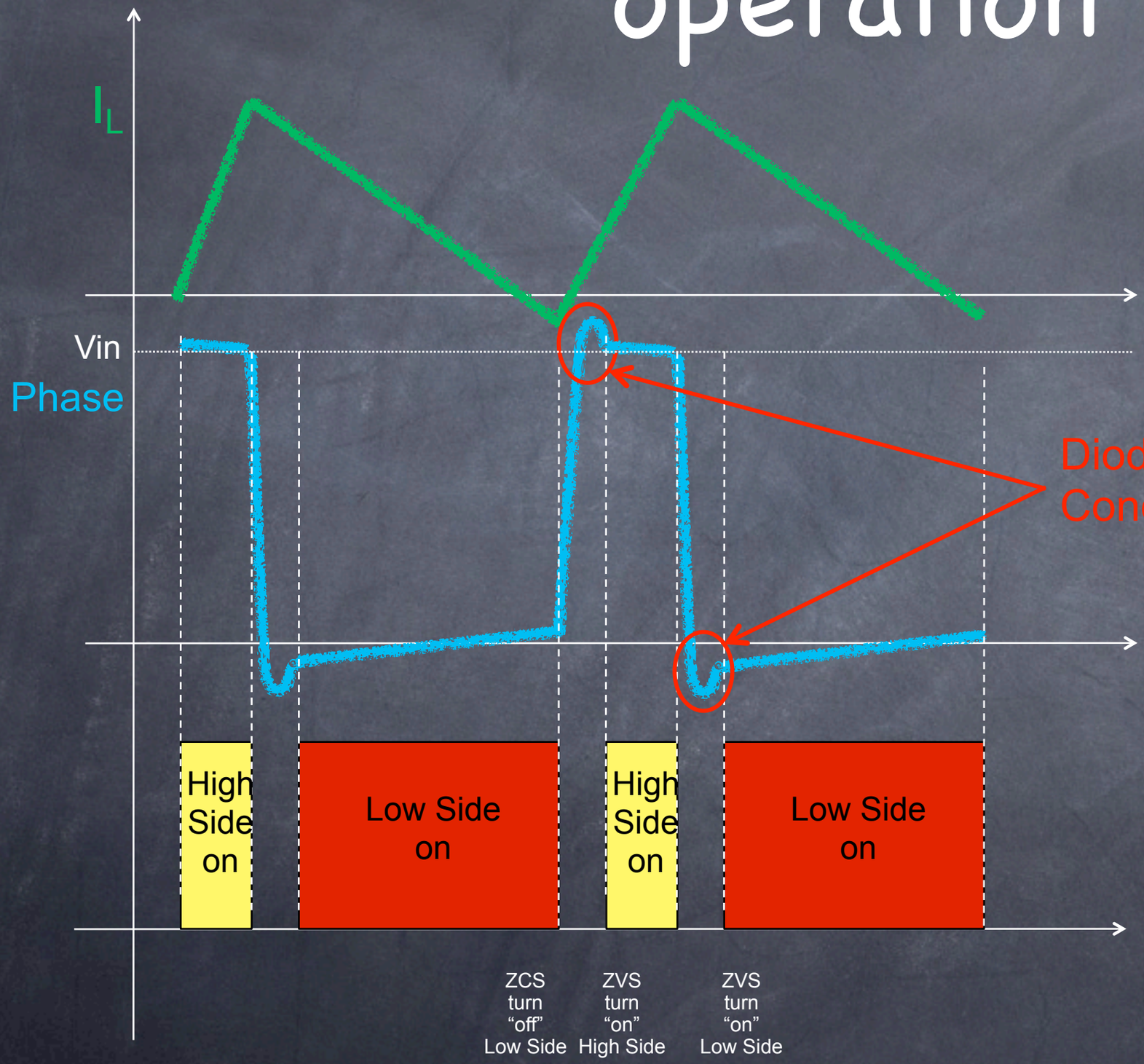


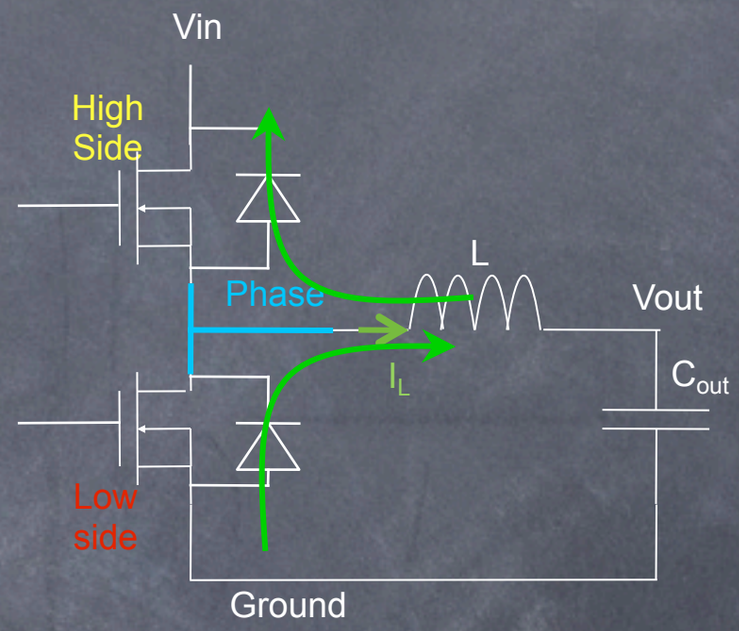
Fixed delay dead time





Quasi Square Wave (QSW) operation





Advantages:

- Smaller Switching losses

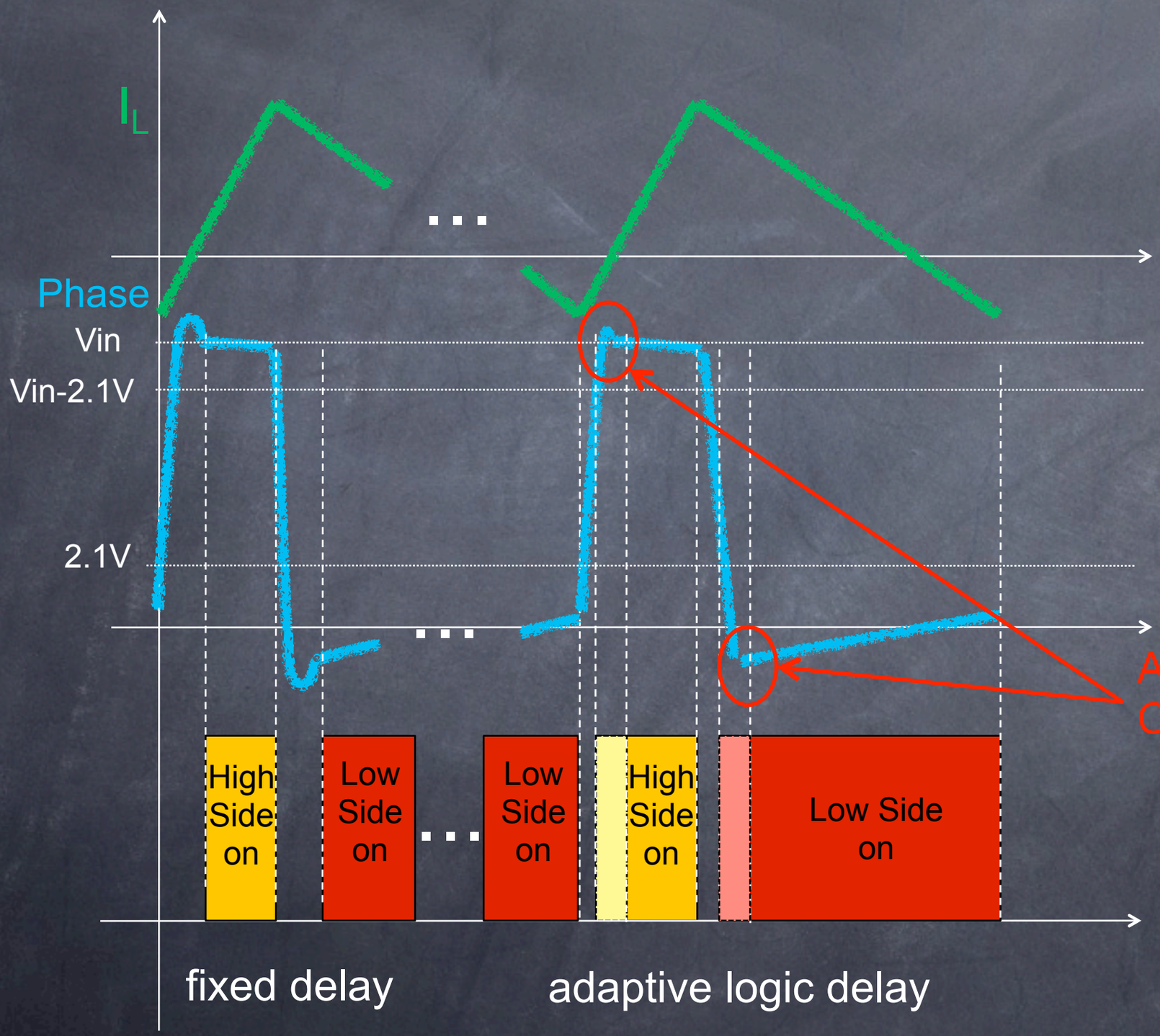
2 zero voltage switching (ZVS):
1 zero current switching (ZCS)

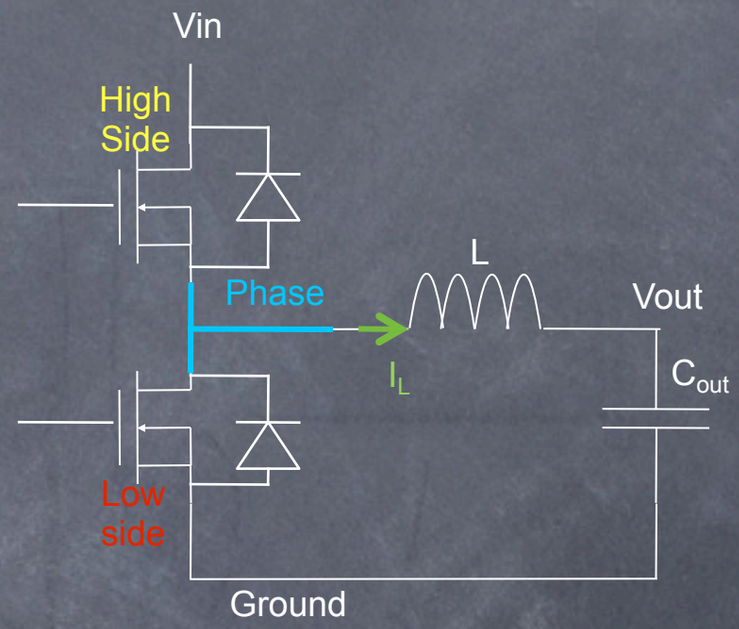
Disadvantages:

- Higher current ripple
- Diode conduction losses

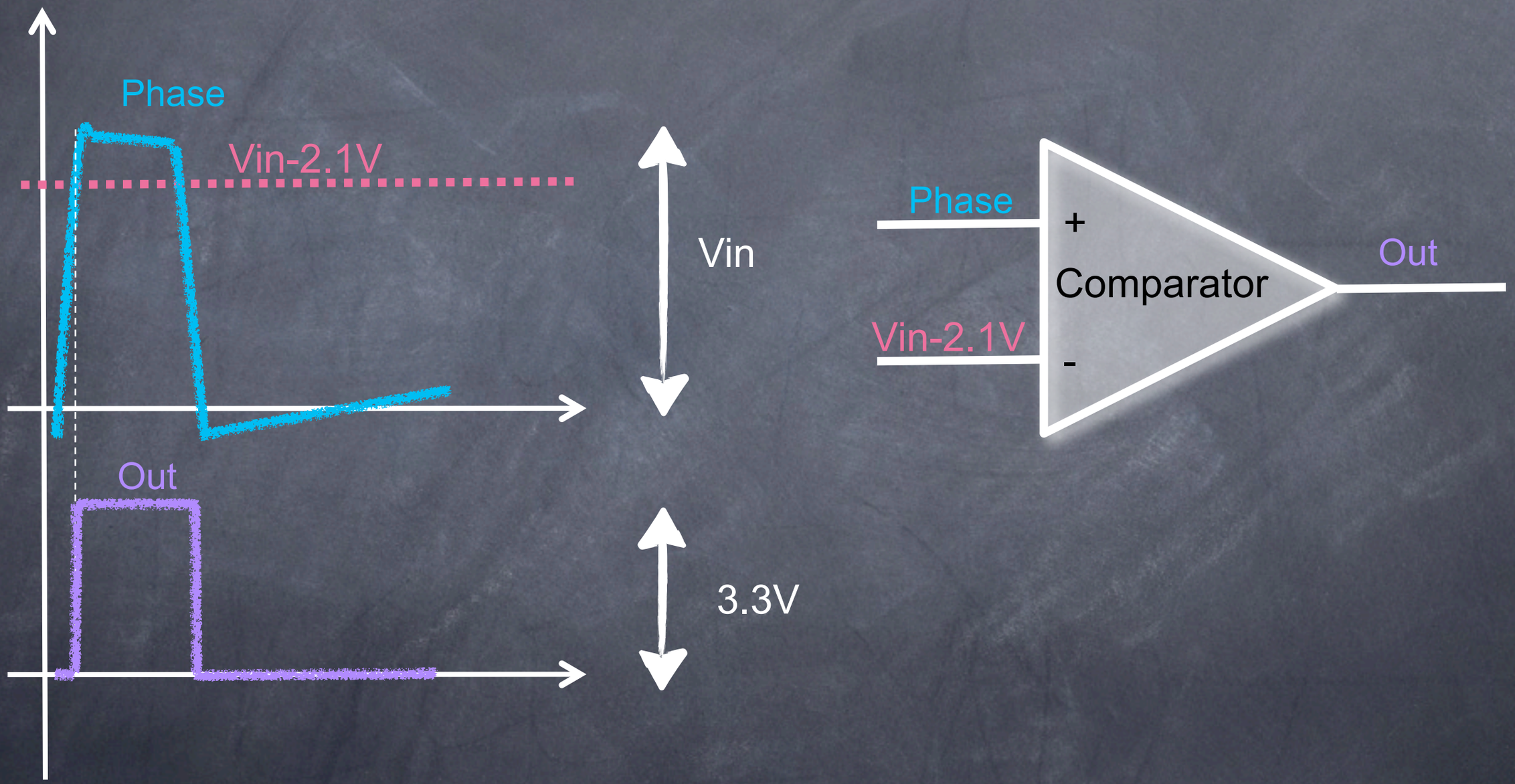
W_{diodes}=0.7*Ids

Adaptive Logic in QSW

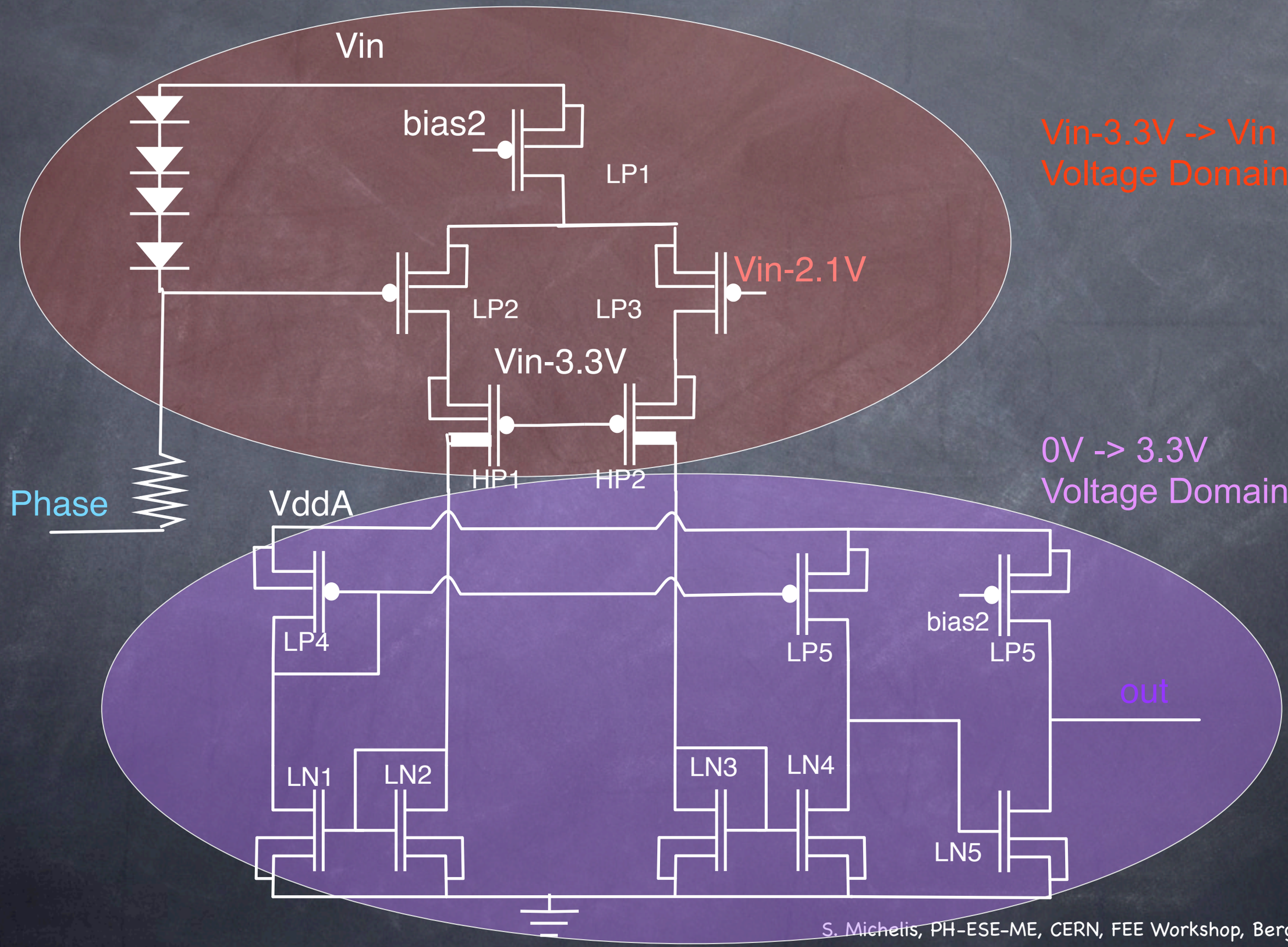




Vin-2.1V comparator



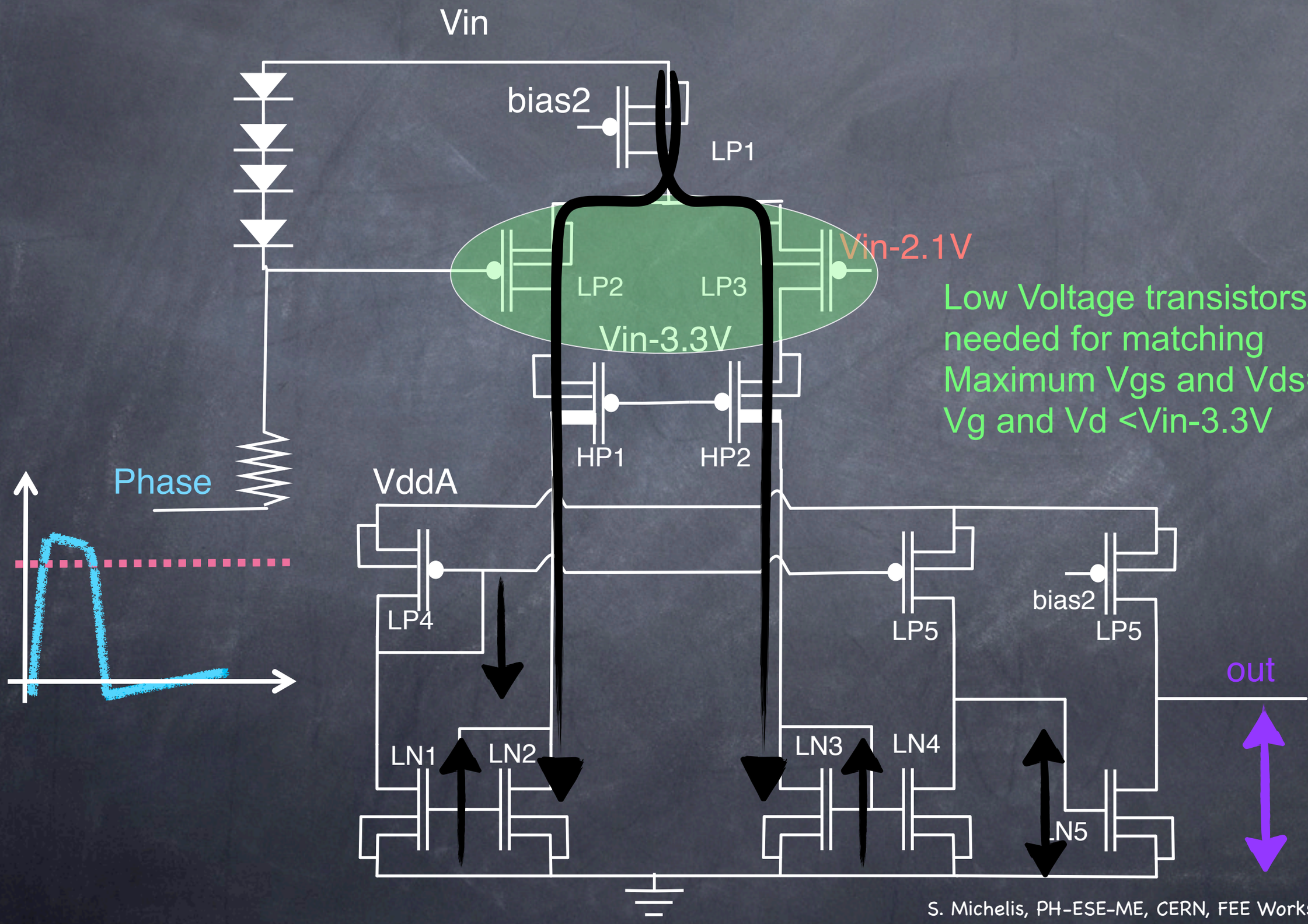
Vin-2.1V comparator



Vin-3.3V -> Vin
Voltage Domain

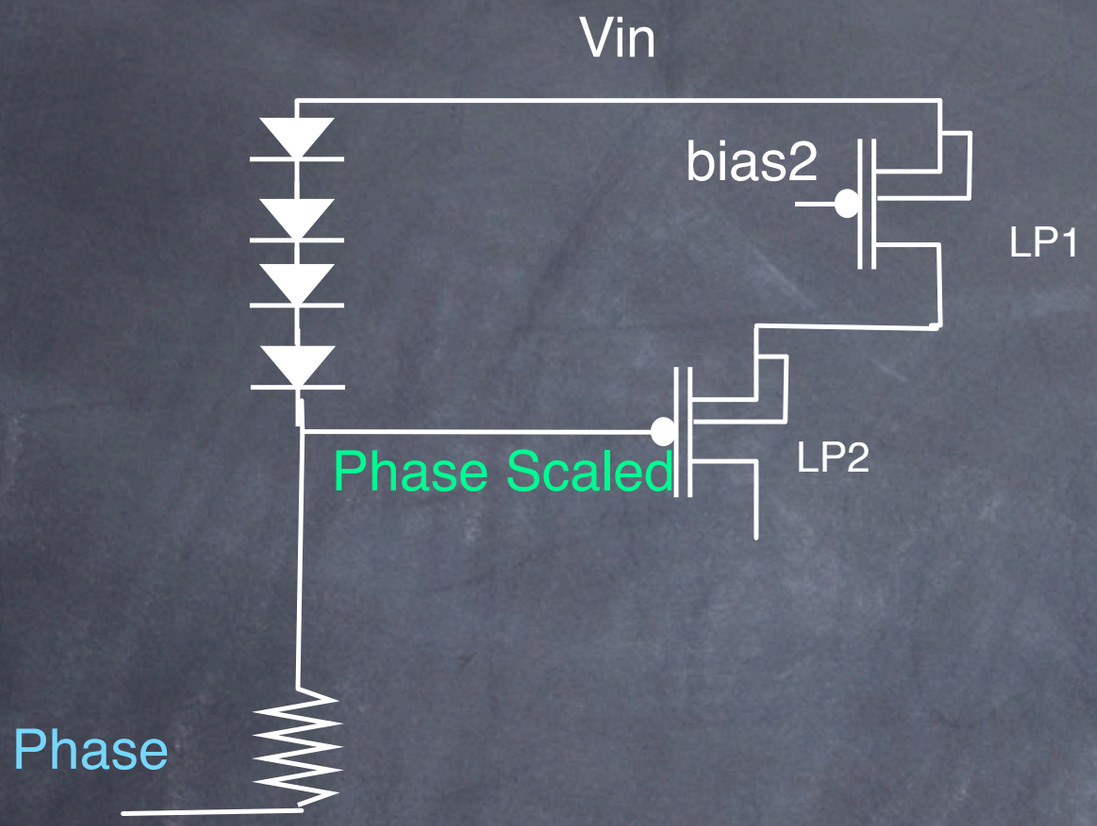
0V -> 3.3V
Voltage Domain

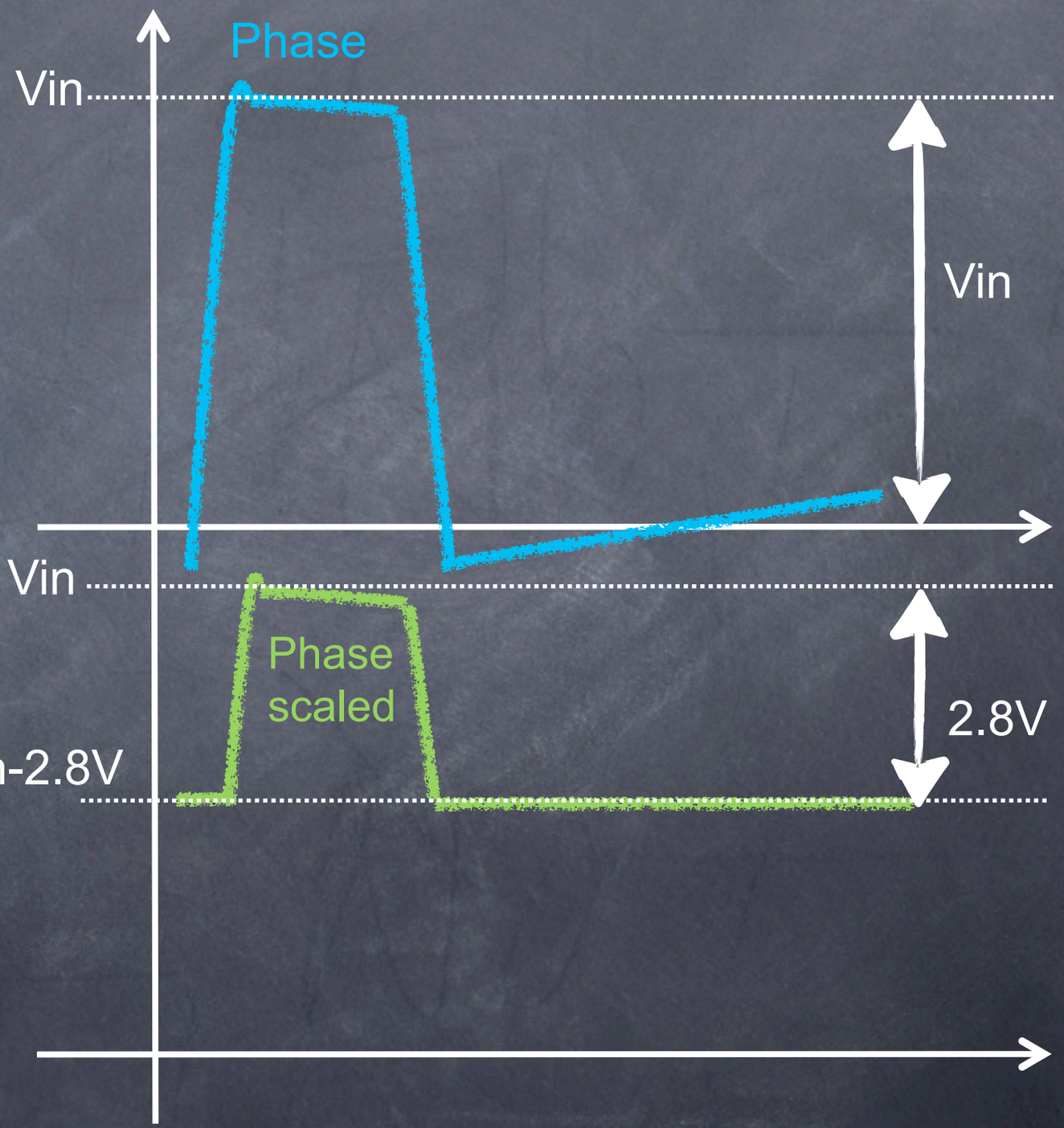
Vin-2.1V comparator



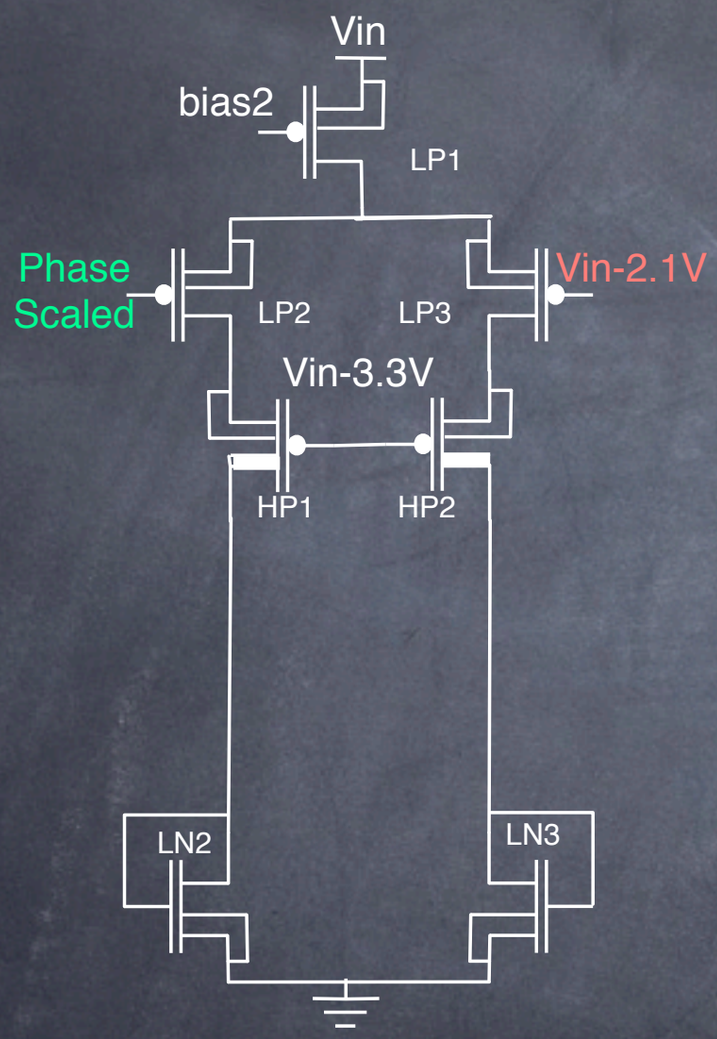
Low Voltage transistors needed for matching
Maximum Vgs and Vds=3.3V
Vg and Vd <Vin-3.3V

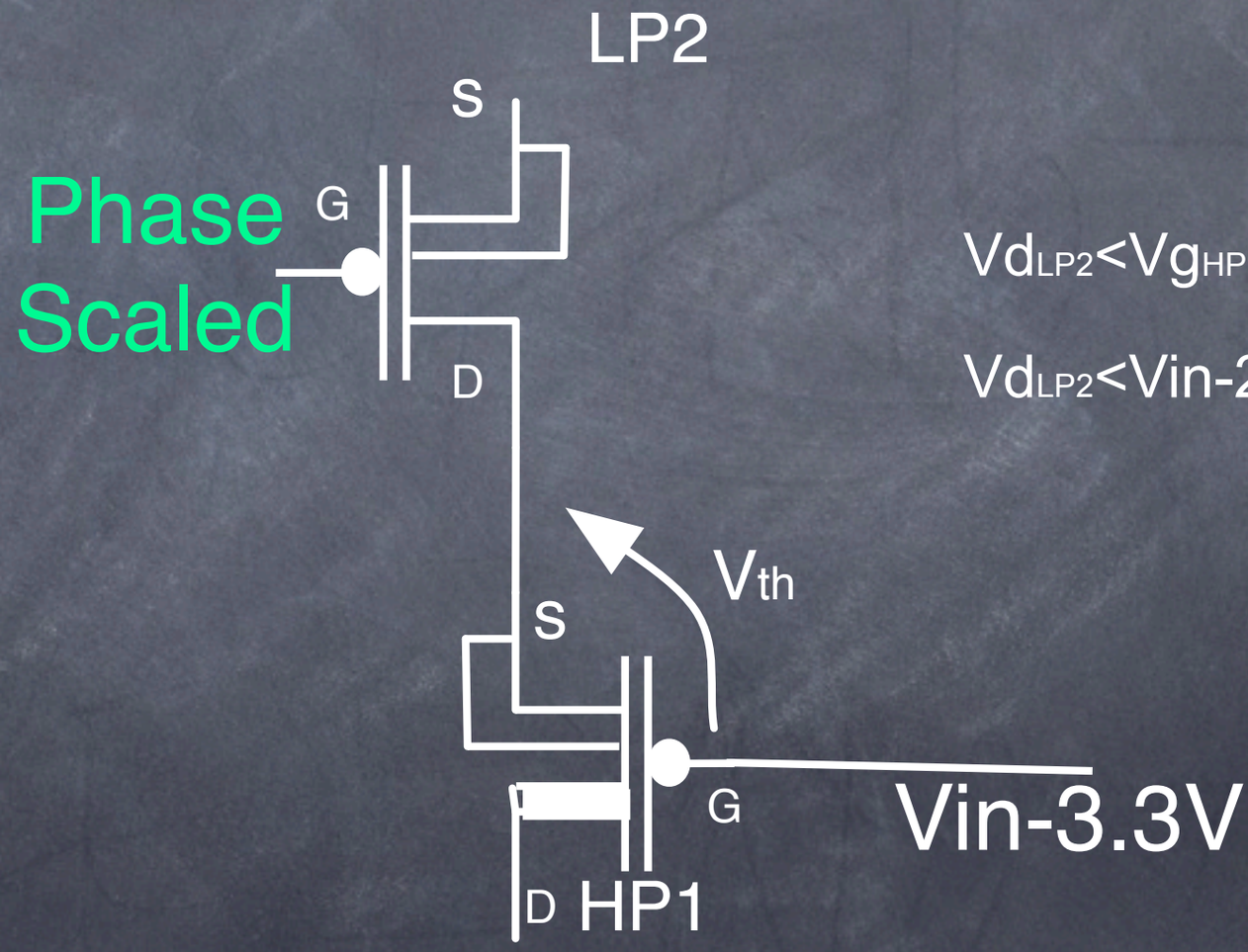
Gate Protection





Drain Protection



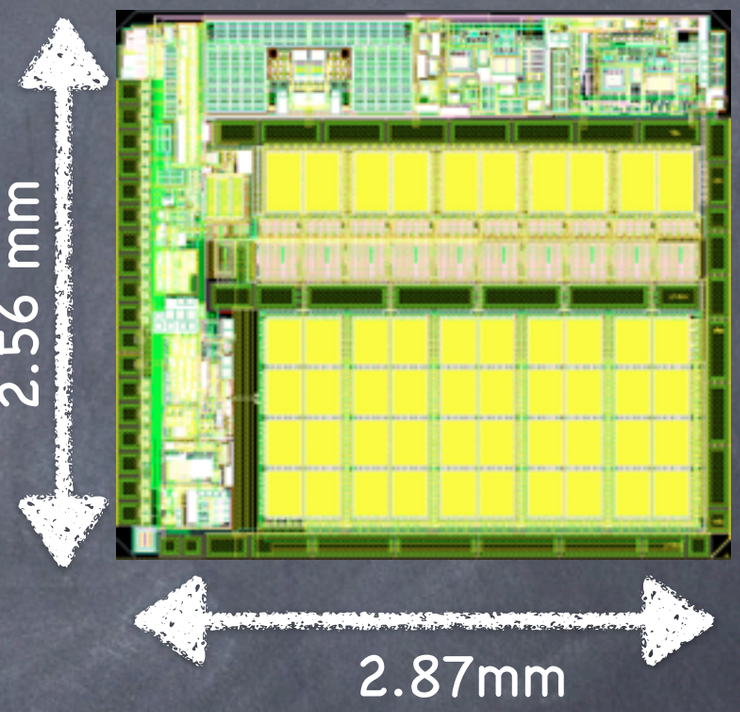


$Vd_{LP2} < Vg_{HP1} - Vth$

$Vd_{LP2} < Vin - 2.7V$

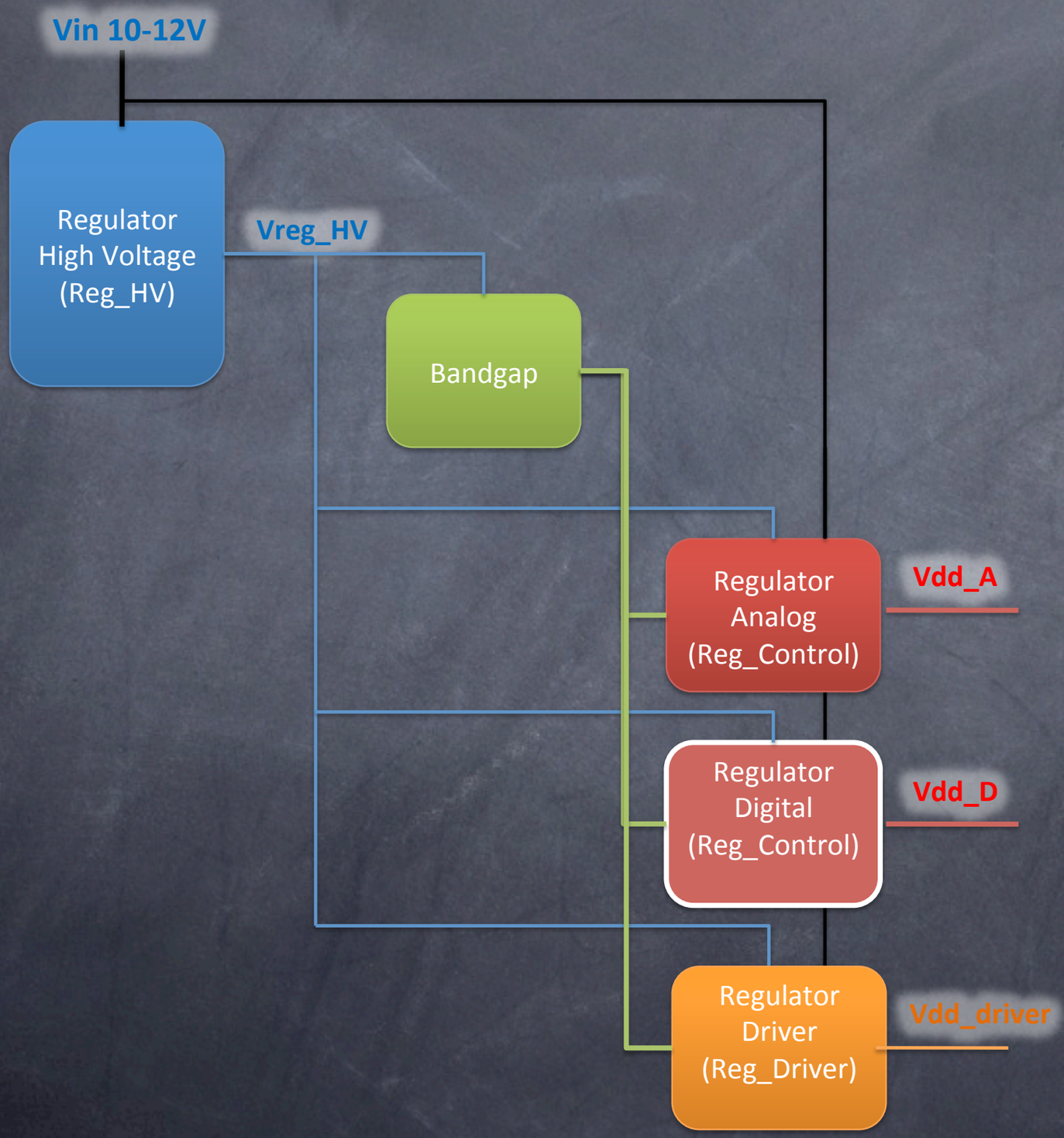
AMIS4

- Some features integrated in the prototype:
  - Bandgap
  - 4 linear regulators: Pre-Reg, Analog, Digital and Driver
  - Handling of the dead time with adaptive logic
  - Triplication and logic against SEU
  - Improved power transistors' design to reduce TID effects
  - Enablers
    - Complete circuit
    - Dimension of the power transistors



- External components needed:
  - Capacitor for Linear regulator
  - Capacitor for Bootstrap

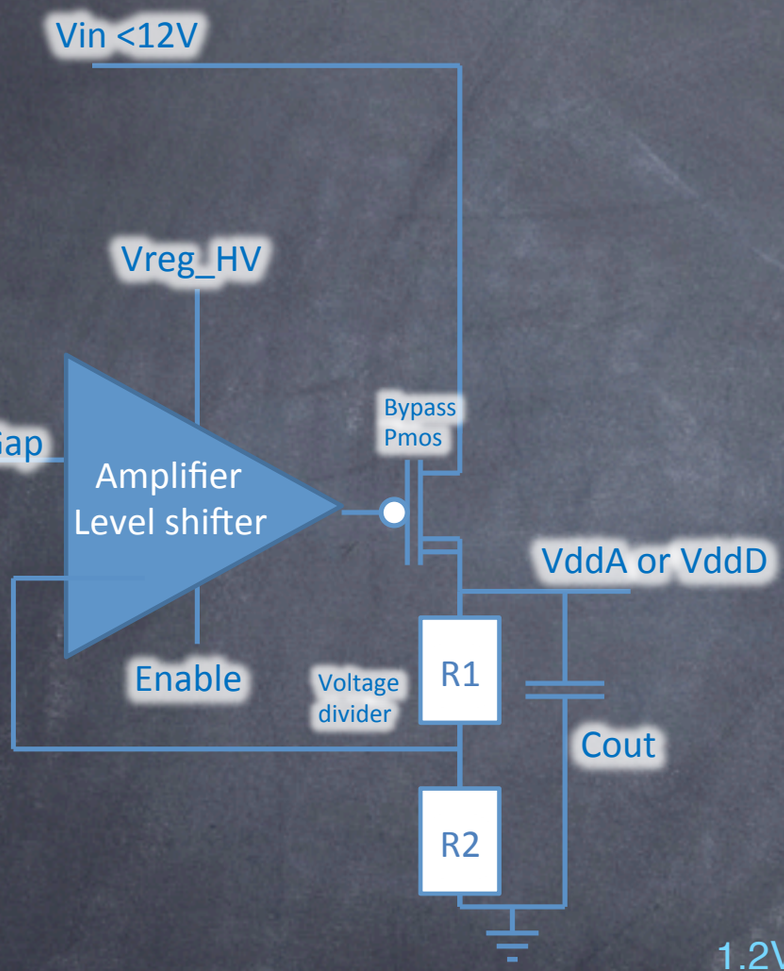
Linear regulators

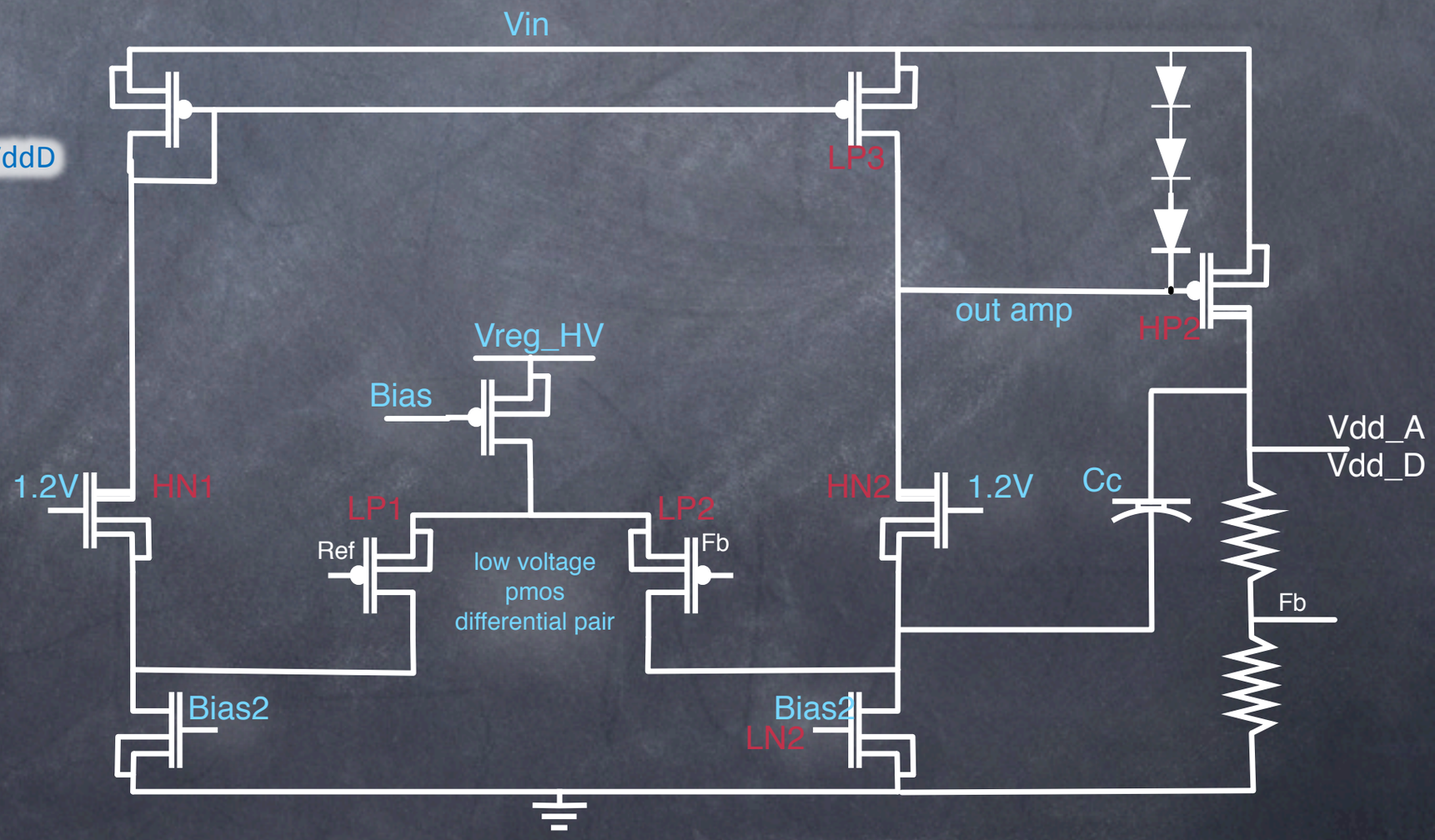


Reg_HV, Reg_Controls are designed with fully integrated output capacitor

Reg_Driver requires 100nF external capacitor

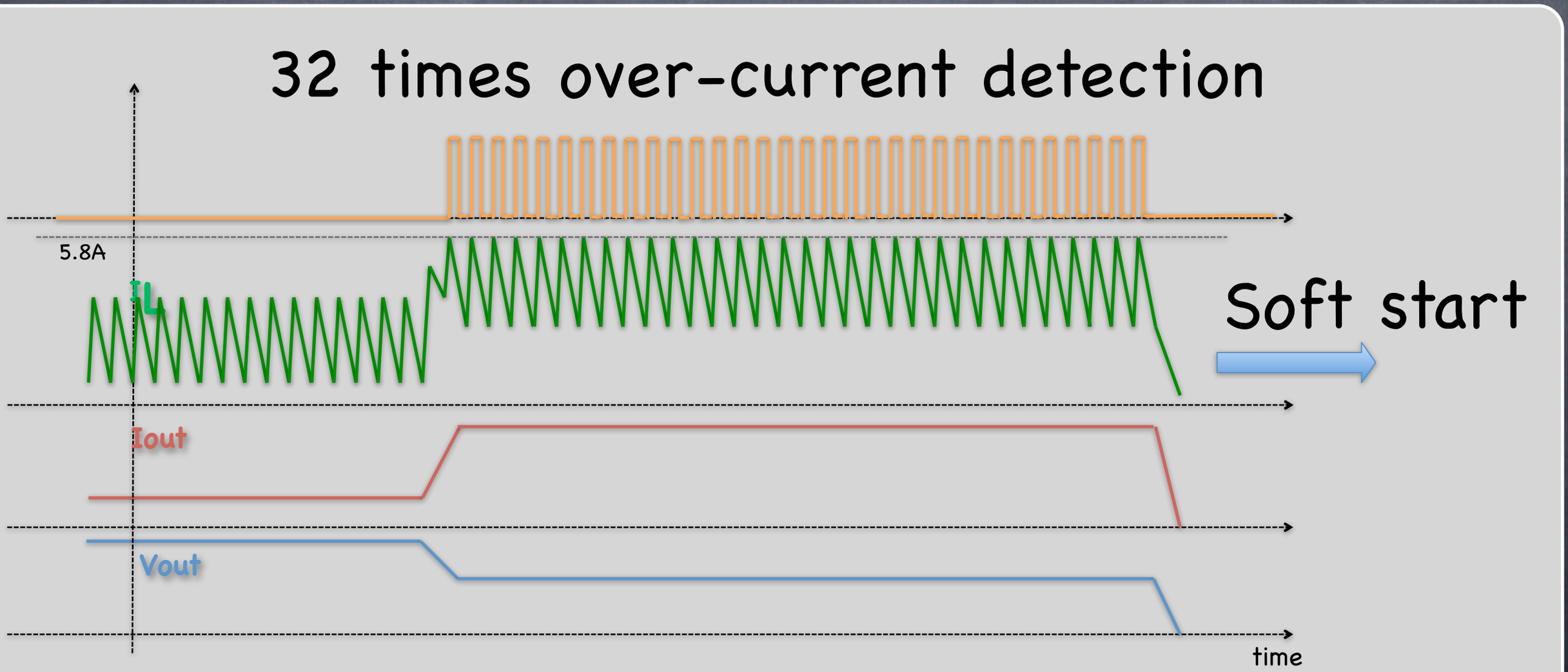
Linear regulator



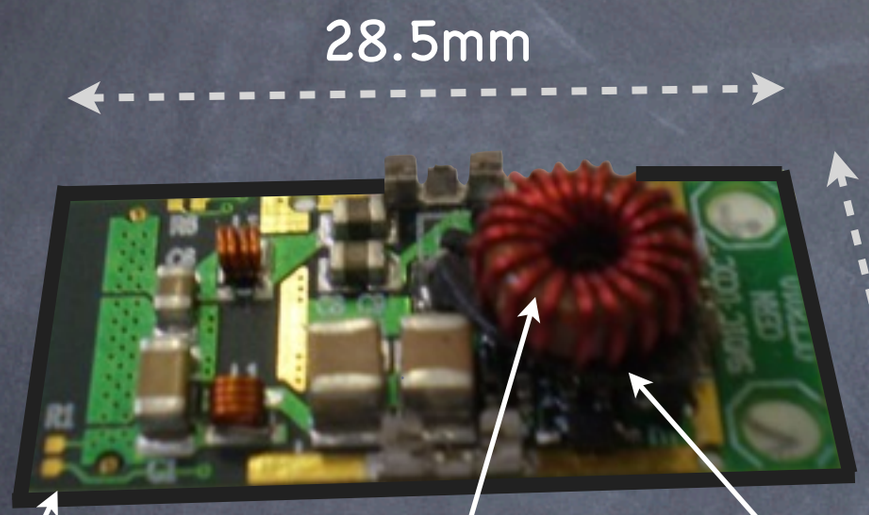


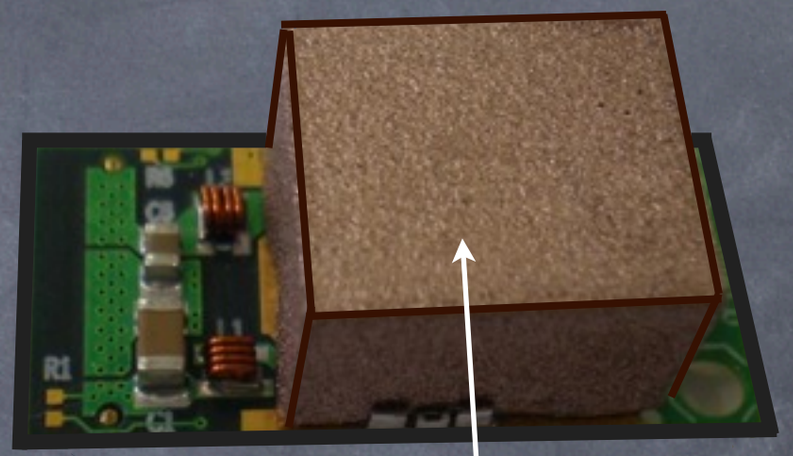
An embedded state machine handles the soft start procedure and the fault signals from the protection circuitry:

- Over-Current: if High Side current over 5.8A for 32 consecutive times
- Under-Voltage: control on Vin if lower than a threshold
- Over-Temperature: if T_{chip}>115°C
- Disable Buck: from external pin



Example prototype of a full DCDC





"optimized" PCB

Custom inductor

Converter ASIC
(commercial or
custom rad-tol)

Covering shield

Conclusions

- DCDC converters are required for the upgrade of the LHC experiments
- They enable power distribution at higher voltage, decreasing the current on the cables.
- The development of full DCDC converters required a technology with HV extension (with good tolerance to radiation)
- A fully integrated buck converter has been designed in this technology and design hints has been presented