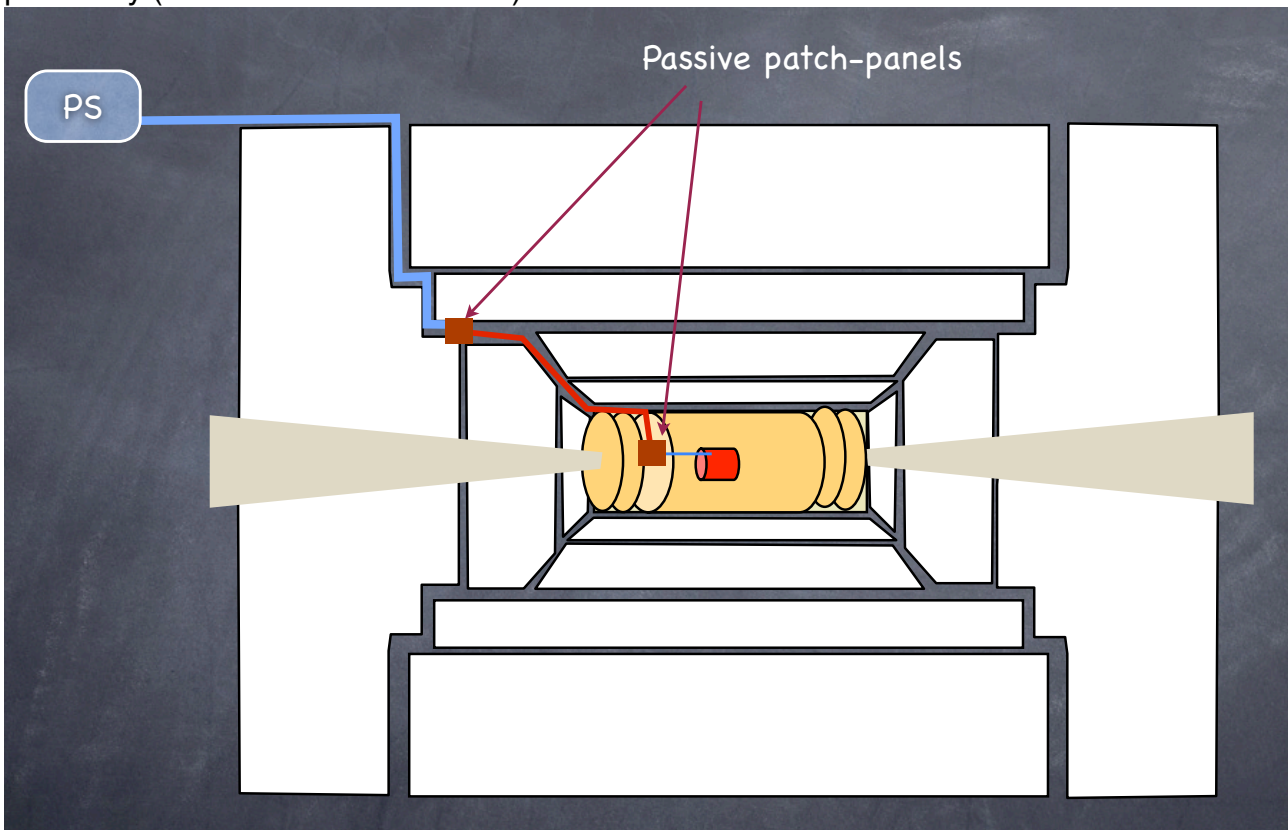


The first part of the talk is focused on the motivation of a development of a new power distribution scheme based on DC/DC converter, followed by the design of ASIC converter which satisfies the environmental constraints.

In the present experiment the current needed by the front end electronic is provided through long cables (up to hundreds of meters) from PS that are placed in the cavern (outside the experiment). In some cases some linear regulator are placed in the patch panel. The power dissipation in the cable is defined as  $RI^2$ , and  $R$  is related to the diameter of the cable. This value is a trade-off between material budget and cooling possibility (which add more material).



In the future design of experiment upgrade, where a ten-fold increase of the current is foreseen to have better resolution, this power distribution scheme is no more usable.

For this reason we are developing a new scheme based on DC/DC converters.

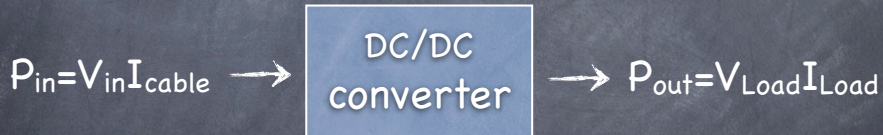
If we define  $P_{load}$  the power required from the front-end, and if an ideal converter is used before the front-end chip,  $P_{in} = P_{load}$ .

If  $V_{in} > V_{load}$  the resulting  $I_{in} < I_{load}$ . This means that the power losses in the cables are smaller in comparison with the present power distribution scheme.

The DC/DC converter should be placed close to the front end electronics, implying that it should be radiation hard and tolerant to the high magnetic field present in the experiments (4T).

Power loss in cables:  $P_{Loss}=R_{cable}I^2$

The electronics load (the FE boards) needs power at a precise voltage  $P_{Load}=V_{Load}I_{Load}$

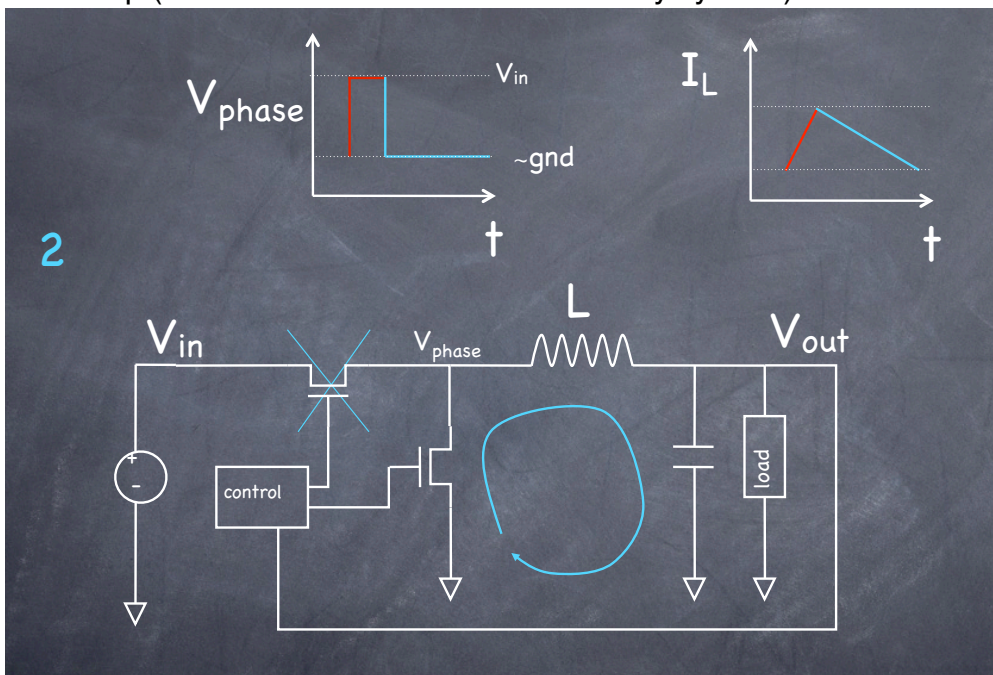


if  $P_{in}=P_{out}$  and if  $V_{in}>V_{Load}$ ,  $I_{cable}<I_{Load}$

the DCDC needs to function in the radiation and magnetic field of the experiments

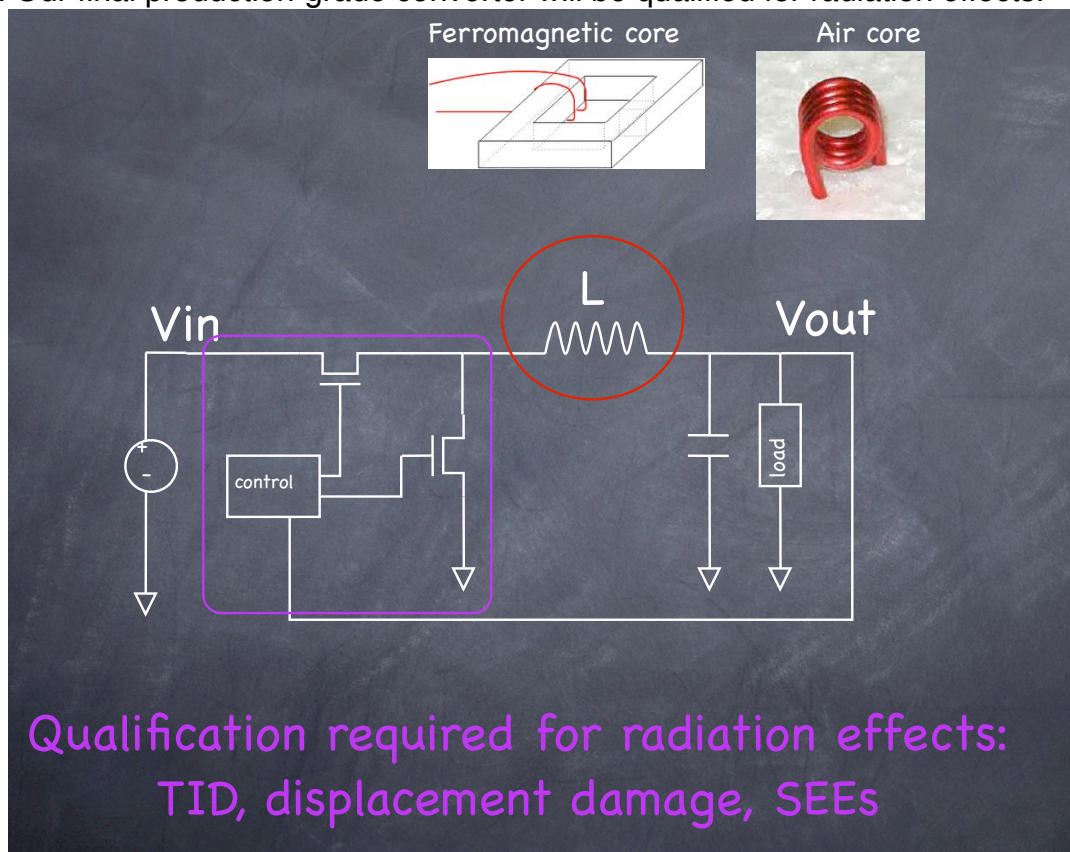
A DCDC converter transforms a DC input voltage into a DC output voltage. In our case, we need a step-down converter ( $V_{in} > V_{out}$ ). The simplest and most widely used type of converter is called 'buck'.

Converters are switching circuits: they cyclically operate at a frequency (fixed for the Pulse Width Modulation -PWM- converters like the one we are developing) and their duty cycle  $D$  determines the conversion ratio  $V_{out}/V_{in}$ . Buck converters use an inductor to store energy and filter a switching voltage to provide a DC output voltage. Energy is transferred from  $V_{in}$  when one of the two main switches (the 'high side' MOSFET transistor) is turned on, for a fraction  $D$  of the switching period. So the step-down conversion can be seen as a periodic transfer of energy from a source ( $V_{in}$ ) to a constant DC  $V_{out}$  which is regulated by an internal control loop (whose function is to decide the duty cycle  $D$ ).



Buck converters can be widely found in the marketplace. They use ferromagnetic inductors and commercial-grade semiconductor processes, without any precaution to protect them against radiation. With ferromagnetic cores, inductance values of several uH can be used

while keeping the parasitic resistance of the inductor very small (less than 10 mOhm). Ferromagnetic cores unfortunately saturate in the magnetic field of the LHC experiments, and in our application we necessarily need to use coreless (or air-core) inductors. Without the ferromagnetic core, the inductor requires many more turns to yield the same inductance, meaning a much longer wire needs to be wound. This leads to much larger parasitic resistance, and larger volume. To limit somehow these drawbacks, we limit the inductance value to below the  $\mu\text{H}$  - we choose 200-500 nH. This in turn determines a higher switching frequency for the converter - 1 to 4 MHz. The second fundamental difference from commercial products is that our converter is designed to survive to the HL-LHC trackers radiation environment. The semiconductor technology choice is determined by this requirements, and dedicated design and layout provisions are followed to ensure protection from cumulative and Single Event radiation effects. Our final production-grade converter will be qualified for radiation effects.



The full DCDC converter we are developing is a small plug-in PCB engineered to meet the typical specifications of HL-LHC experiments. They include:

## Electrical specs

Input voltage	10-12V
Output voltage	1.2-3.3V
Output current	up to 3A*
Efficiency	>80% (for $V_{out}=2.5V$ )
Conducted and radiated noise compatible with installation in close proximity to FE electronics and detectors	

\* We will know the real output current limit soon, with measurements of a mature ASIC in a realistic configuration (cooling)

## Mechanical specs

Small size (footprint, height)
Small contribution to material budget
Connectable to cooling system

## Environmental specs

TID tolerance	250 Mrad
Displacement damage	$2.5 \cdot 10^{15}$ n/cm <sup>2</sup> (1MeV equivalent)
SEE	Absence of destructive SEEs and $V_{out}$ transients when tested with heavy ions up to an LET of 30 MeVcm <sup>2</sup> mg <sup>-1</sup>
Magnetic field	4 T
Temperature of cooling pad	-30 to +10 °C

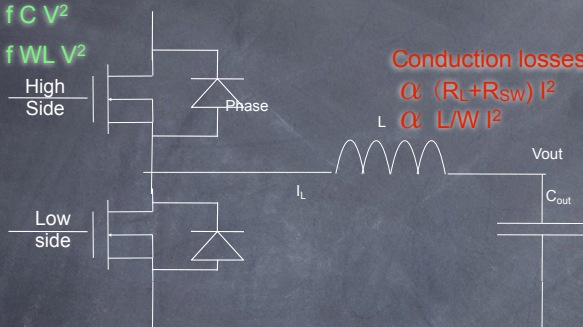
The design of the converter requires that a choice is made in terms of size of the power transistors and switching frequency. These can be chosen to optimise the efficiency that is calculated considering all the conversion losses: conductive (on parasitic resistance), switching (overlap of  $I_{ds}$  and  $V_{ds}$  during the switching time) and driving losses (charge and discharge of the power transistors' gate). All these losses are strongly technology dependent; therefore a complete parameter extraction of the selected technology was carried out to allow for a meaningful evaluation. They have been inserted in a mathematical model which allows to plot the efficiency vs the dimensions (or resistance) of the power switches.

## Losses in a converter

### Driving losses

$$\propto f C V^2$$

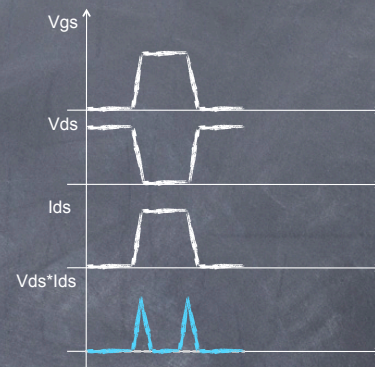
$$\propto f W L V^2$$



### Conduction losses

$$\propto (R_l + R_{sw}) I^2$$

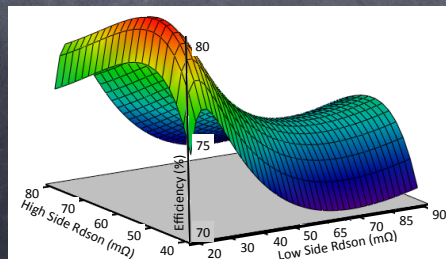
$$\propto L/W I^2$$



### Switching losses

$$\propto f V_{ds} I_{ds} C$$

$$\propto f V_{ds} I_{ds} W L$$

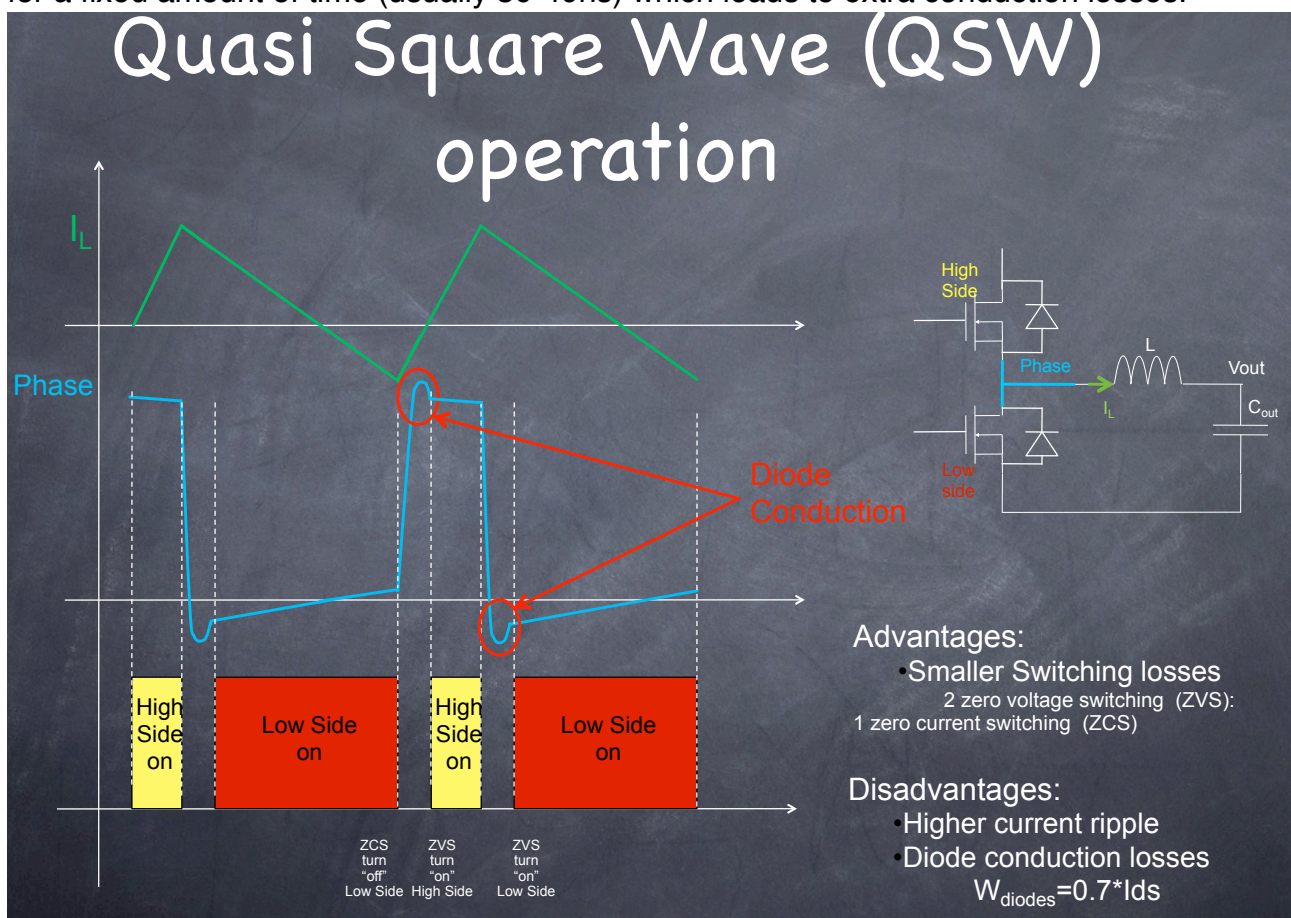


It appears that the best compromise is a switching frequency in the range 1-3 MHz and also that the converter should work in an mode called quasi-square-wave (QSW). This is a continuous mode with the inductor current that goes slightly negative. Leaving a delay between the gates of the two power switches, the inductive load forces the current circulating in their parasitic diodes. This allows having a low  $V_{ds}$  (equal to the forward voltage of the diode ( $\sim 0.7$  V), instead of  $V_{ds}=V_{in}$ ) during the switch-on of the power transistor, reducing in such a way the on-switching losses.

Three out of four commutations are “soft”: Zero Current Switching (ZCS) for low side turn-off and Zero Voltage Switching (ZVS) for high side and low side turn on.

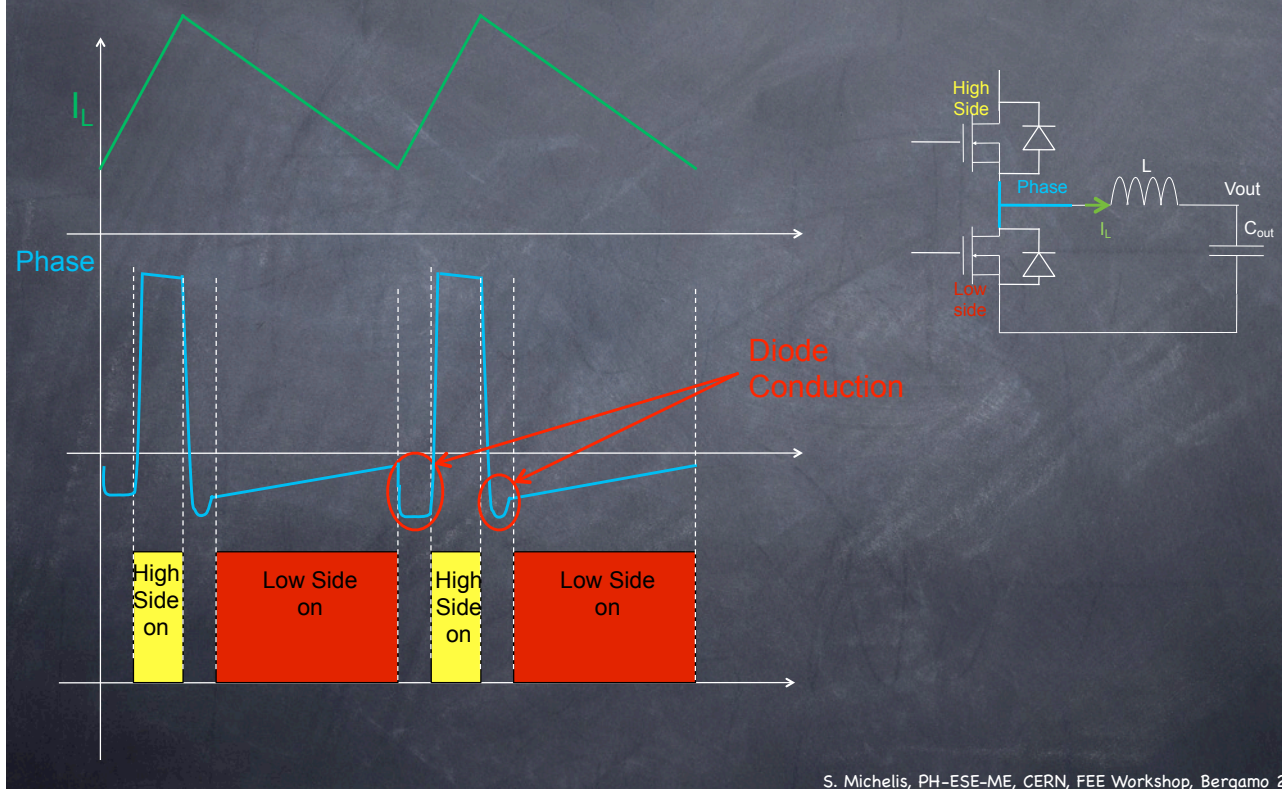
The drawback is a higher rms value of the inductor current that leads to an increase of the conductive losses.

If a fixed delay approach is used, the bulk diodes of the high side and low side will conduct for a fixed amount of time (usually 30-40ns) which leads to extra conduction losses.



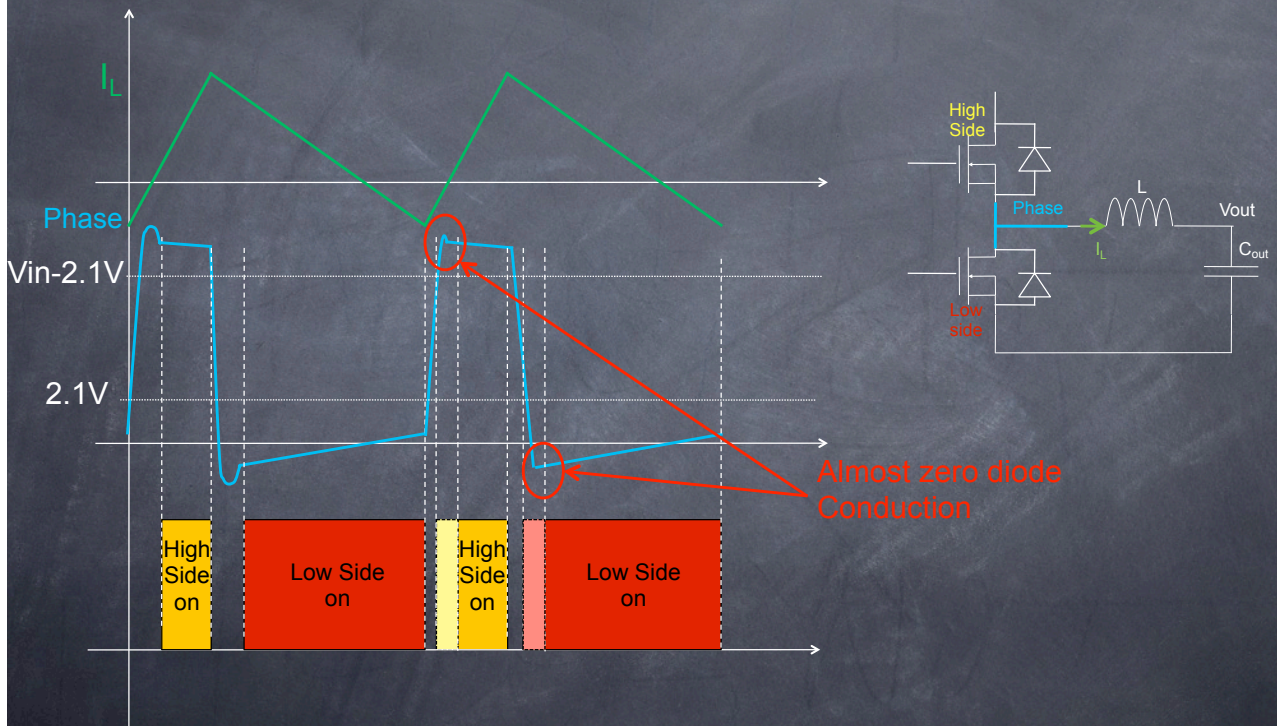
If the inductor current is always positive, then the converter is working in continuous mode (CCM). In this case three commutation are “hard” and only the turn on of the low side remains soft (ZVS). In CCM the low side bulk diode always carries the inductor current during the dead-time.

# Continuous (CCM) operation



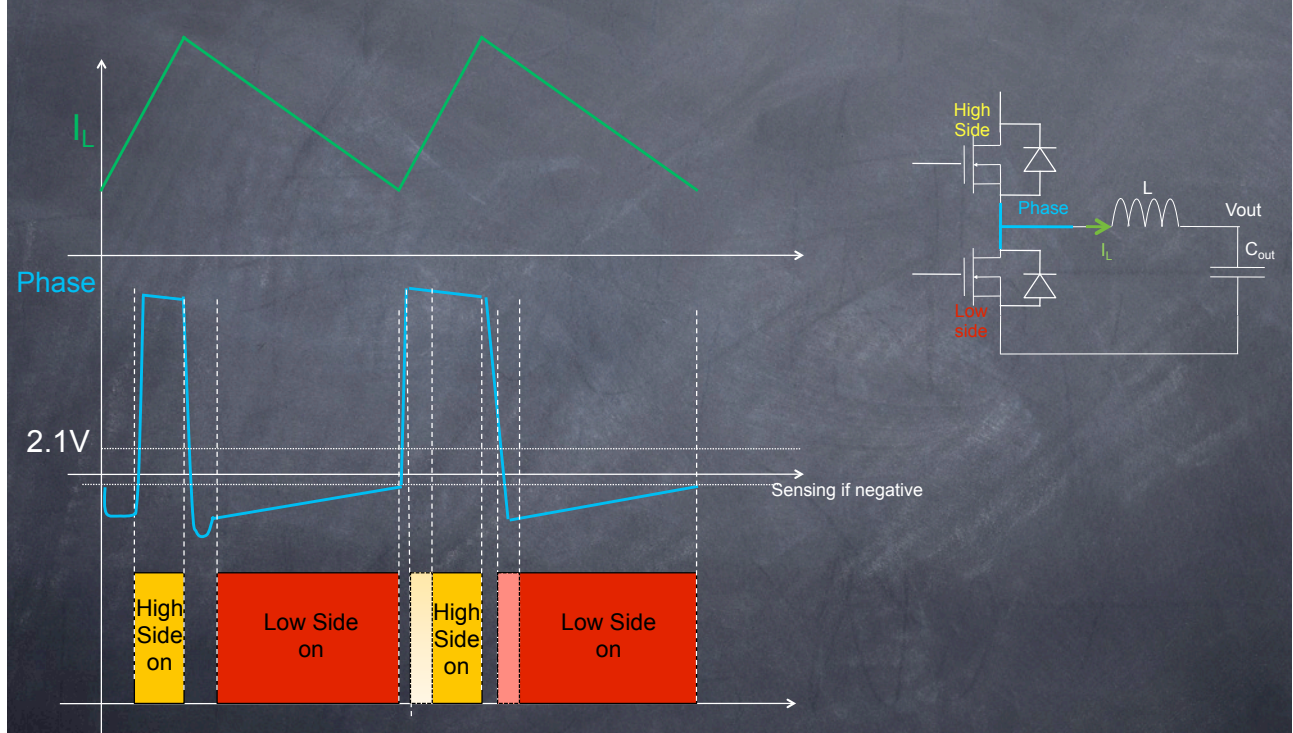
The diode conduction time can be reduced using a circuit called Adaptive Logic, which monitors the phase voltage. As soon as the phase voltage reaches  $V_{in} - 2.1V$ , the AdLog circuit enables the switching on of the high-side transistor. In the same way, when the phase falls under  $2.1V$ , the low-side transistor is switched on. This technique allows reducing the diode conduction, leading to a higher efficiency.

# Adaptive Logic in QSW



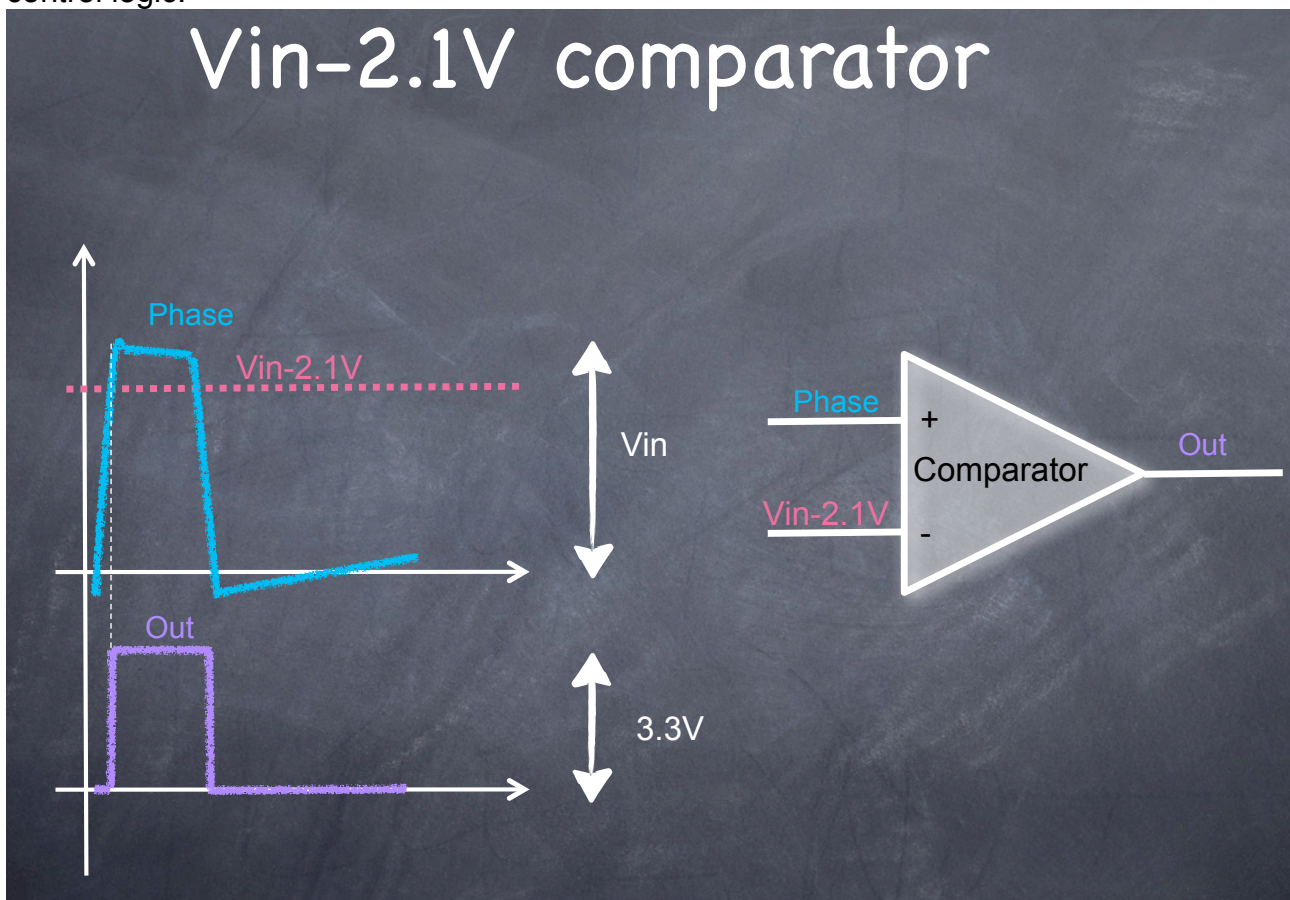
Also for CCM operation the diode conduction can be reduced. At the low side turn off, if the phase is negative, the adaptive logic enable the hard turn-on of the high side. The turn on of the low side works as in the QSW mode.

# Adaptive Logic in CCM



Now let's focus on the design of the  $V_{in}-2.1V$  comparator which includes the main design technique to cope with high voltages.

This circuit needs to compare a Phase signal (with swing from  $0 \rightarrow V_{in}$ ) with a signal fixed at  $V_{in}-2.1V$  and it provides an output voltage in the range  $0 \rightarrow 3.3V$  compatible with the control logic.

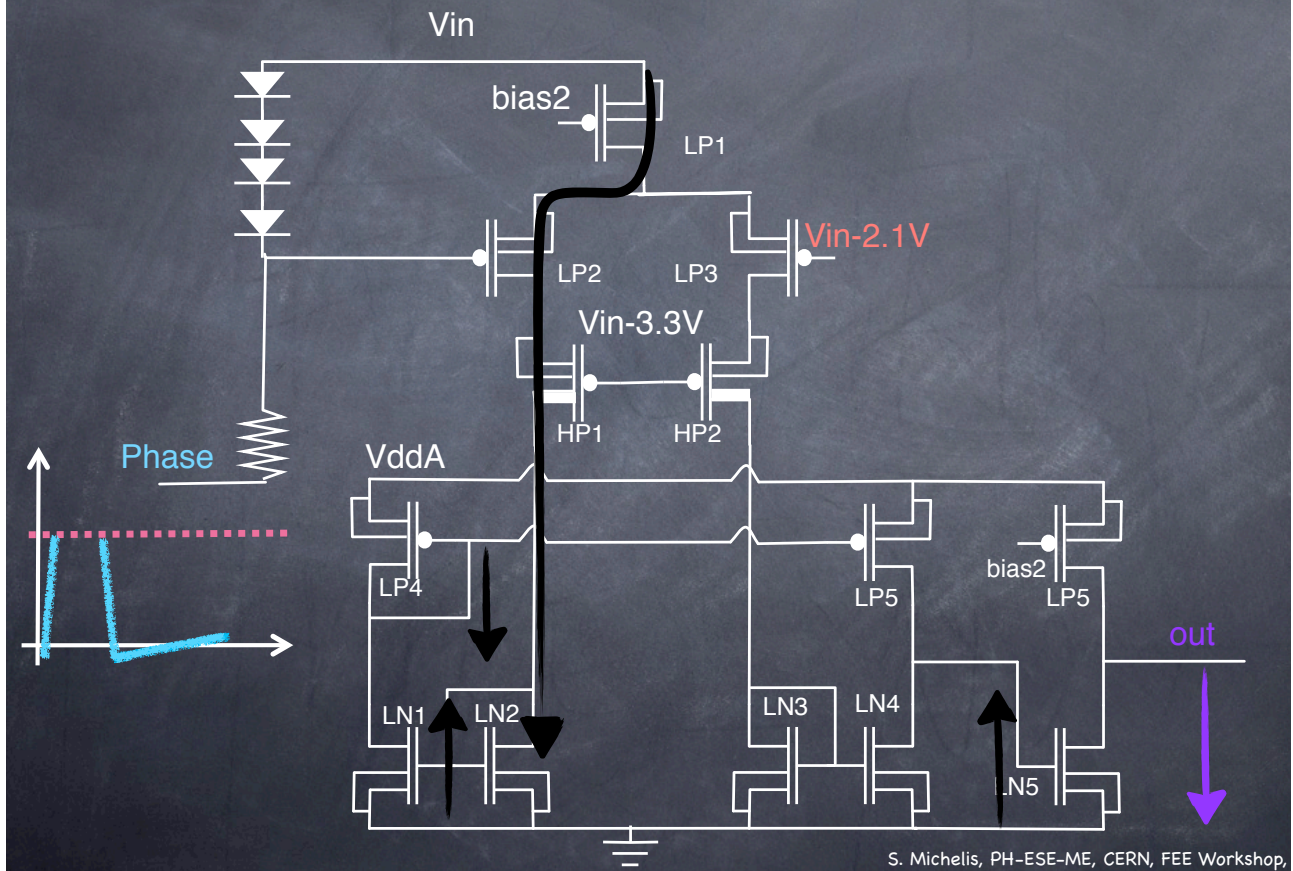


The comparator is divided in two parts, referred to two different voltage domains:  
 $V_{in}-3.3V \rightarrow V_{in}$  and  $0 \rightarrow 3.3V$



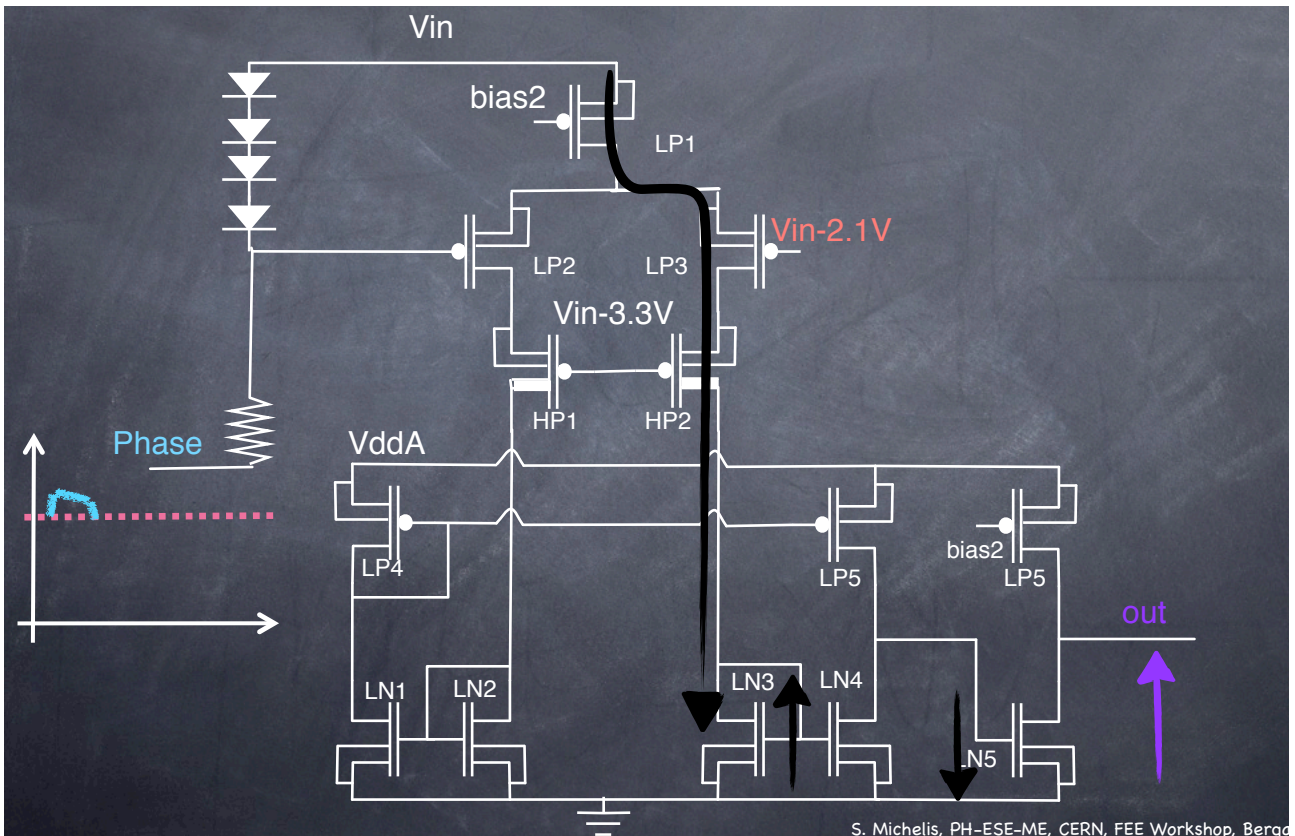


# Vin-2.1V comparator

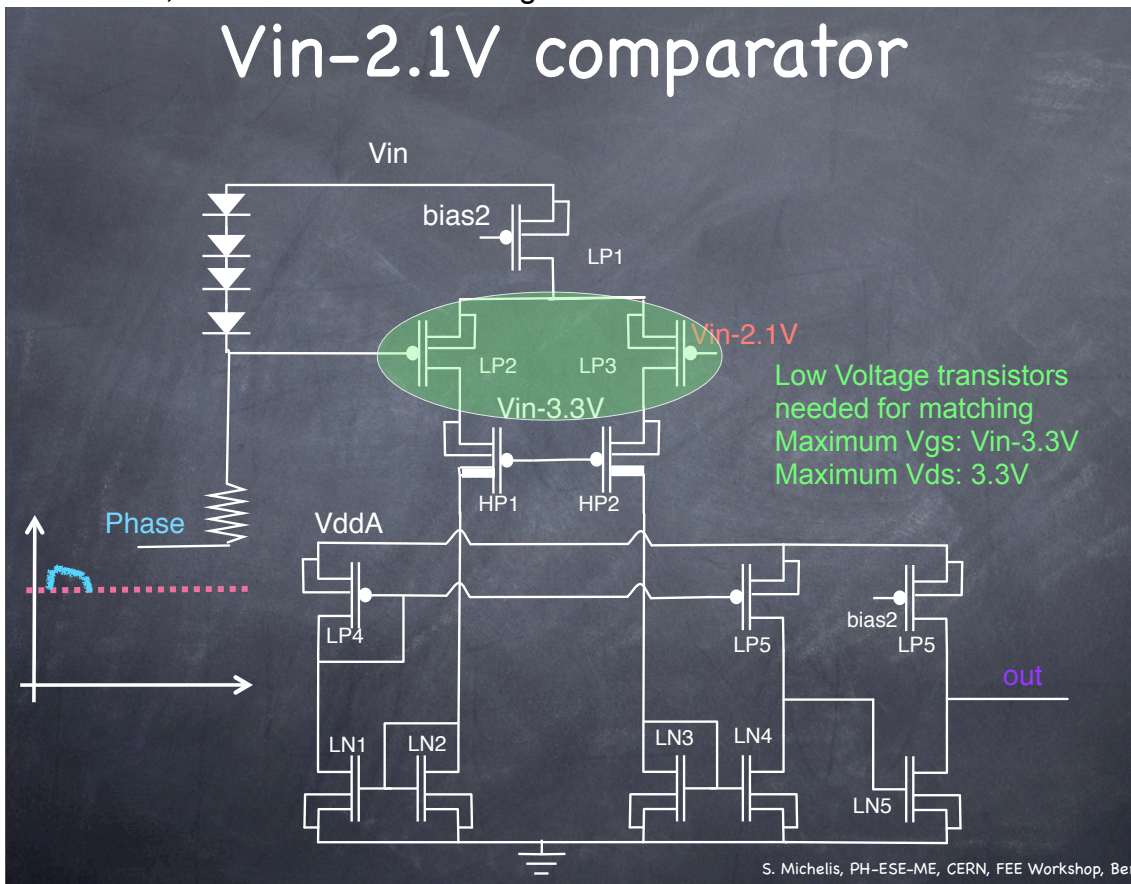


S. Michelis, PH-ESE-ME, CERN, FEE Workshop,

Similarly when the phase  $> V_{in-2.1V}$  the current will flow in LP3, turning on LN3 and LN4. The last pulls down the LN5 gate allowing the output to rise.



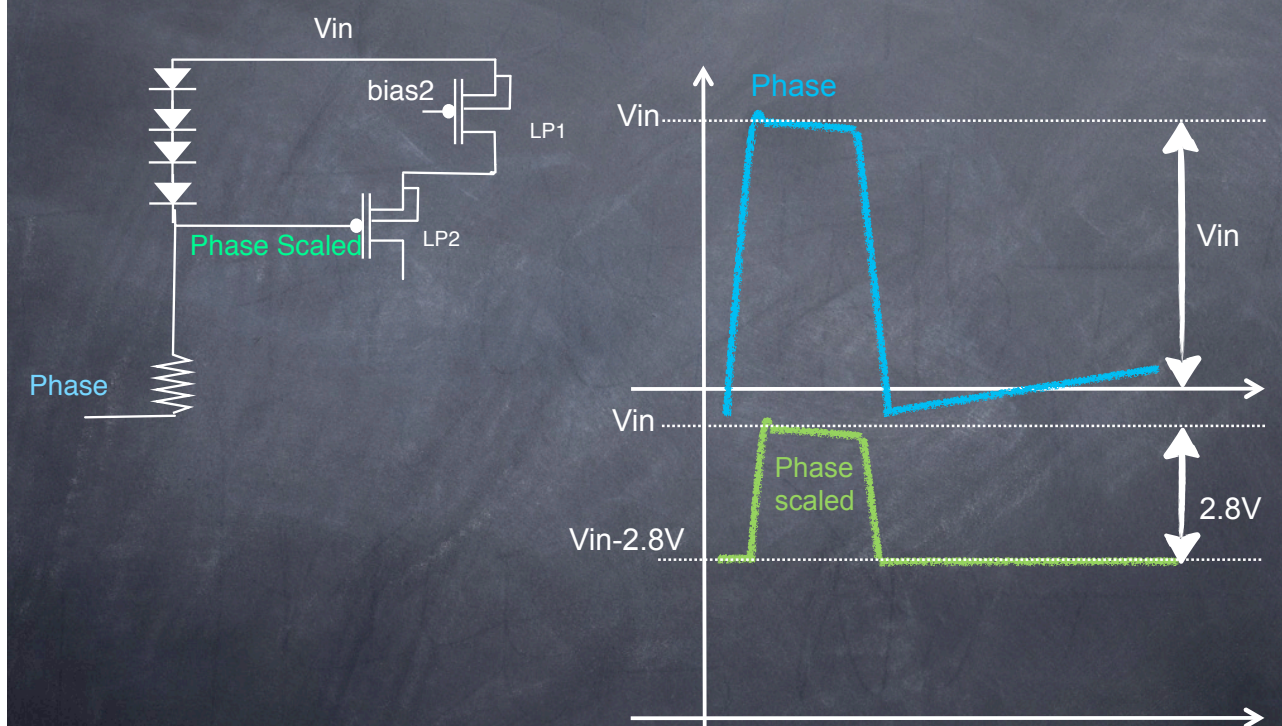
In order to have good matching on the differential pair, it is mandatory to use low voltage Pmos, which have maximum  $V_{gs}$  and  $V_{ds}=3.3V$ . Considering that the transistor is connected to  $V_{in}$ , its maximum  $V_{ds}$  and  $V_{gs}$  is  $V_{in}-3.3V$ .



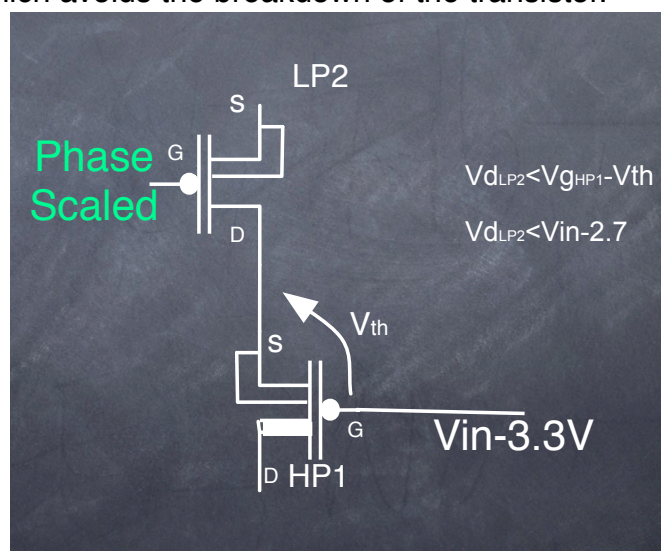
Monday, May 23, 2011

The Gate of LP2 can be then protected with diodes which will clamp the phase voltage to  $V_{in}-2.8V$  to avoid break down of the gate.

# Gate Protection

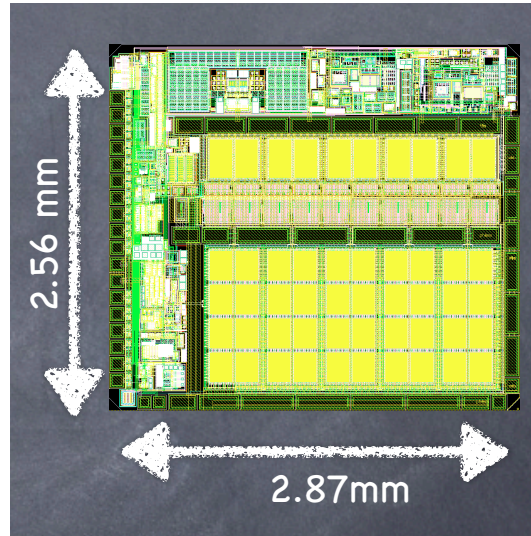


The drain of LP2 and LP3 can be protected with a high voltage transistor which will stand the high voltage. For example if HP1 source is connected to LP2 and the HP1 gate is connected to a  $V_{in}-3.3V$ , then its source potential cannot exceed the  $V_{gate}-V_{th}$  to allow a current flowing in the transistor. This means that HP1 source (and LP2 drain) voltage is limited to  $V_{in}-2.7V$  which avoids the breakdown of the transistor.



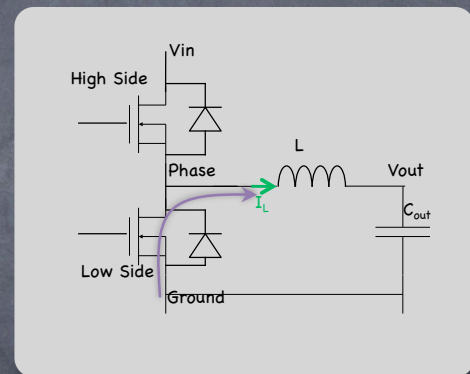
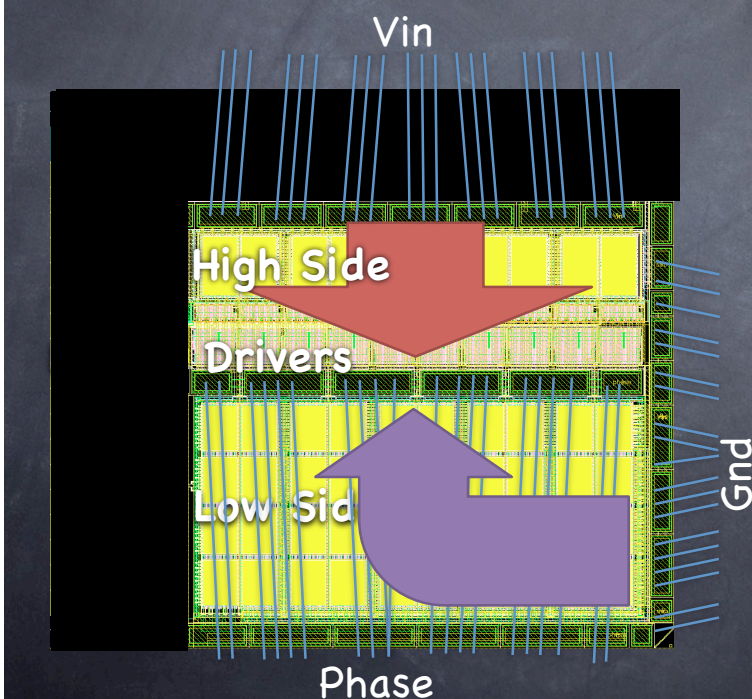
This circuit has been added in our last design, called AMIS4. It has been designed in the 0.35um technology. It includes 4 different linear regulators to provide the 3.3V for the control circuit and drivers, a bandgap and different features to limit radiation effect. Enclosed layout transistors have been used against TID, diodes have been designed with a squared shape to limit leakage currents and triplications techniques have been used to limit SEE.

A state machine is used to handle the soft start procedure and the faulty signal from the protection circuit.

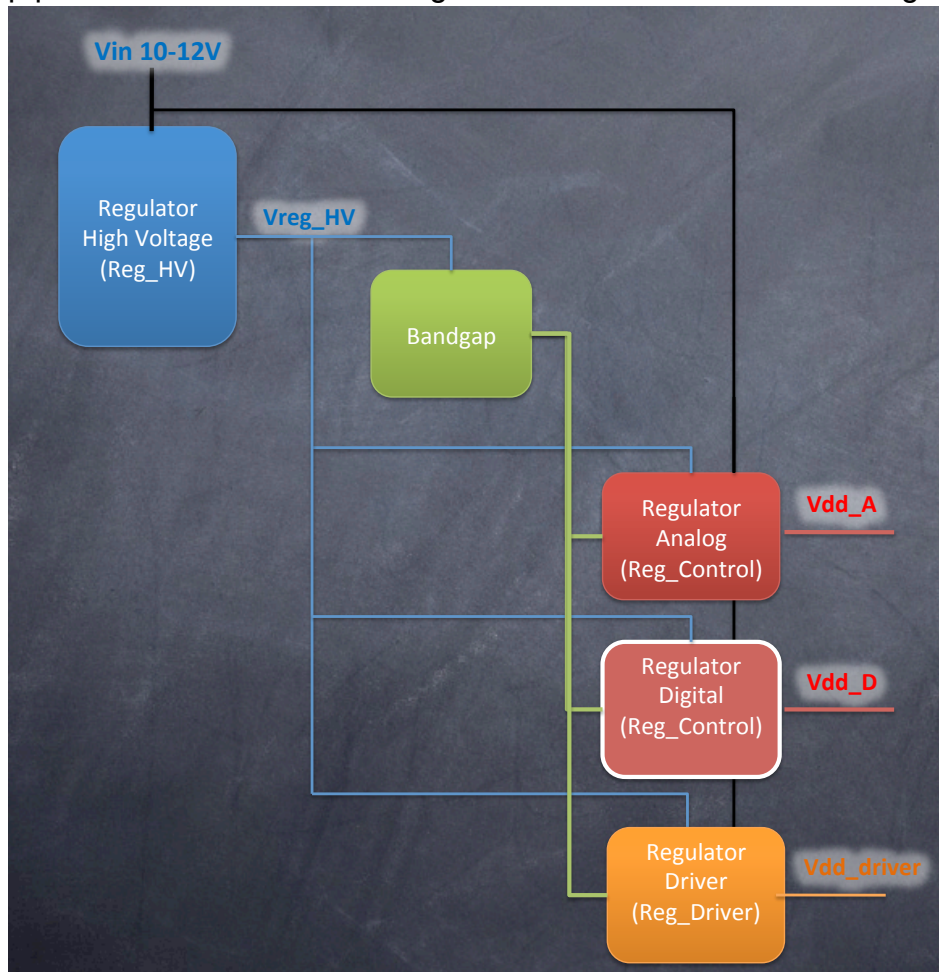


AMIS4 chip bonding diagram has been optimized for reducing the on-resistance of the switching. The Phase voltage is in the middle of the chip allowing a reduction of the metal squares.

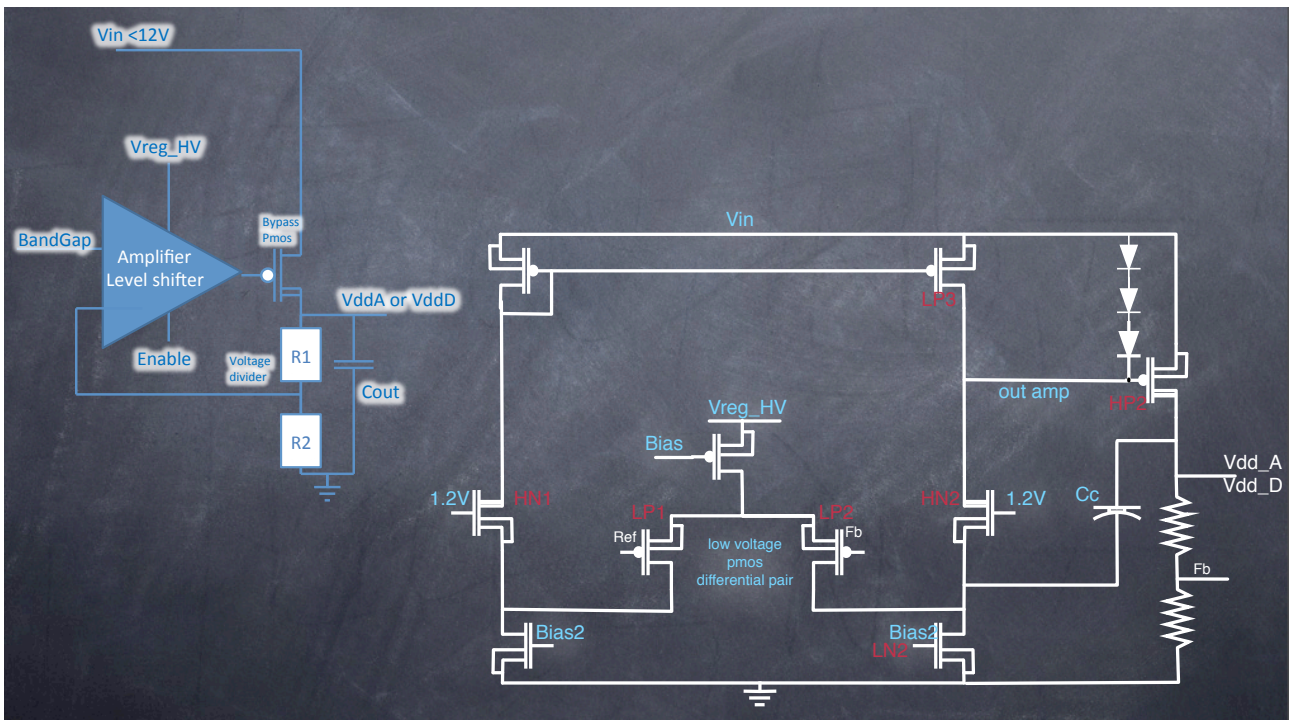
The pad layout (for QFN32) has been optimized for reducing the switch on-resistance



AMIS contains 4 different linear regulators: one pre-regulator completely biased from  $V_{in}$ , which supply the 3.3V for the Bandgap circuit and the regulators for the analog and digital circuitry and the regulator for the drivers. The bandgap provides the reference voltage for the three last mentioned regulators.



The Reg\_control schematic is presented in the figure below. It is composed by an amplifier and a bypass PMOS transistor HP2. The amplifier is composed by a folded cascoded OPA with low voltage input Pmos differential pair. The current signal is the sent to the  $V_{in}$  voltage domain through the two high voltage ILDMOS HN1 and HN2. A compensation capacitor  $C_c$  is connected between HP2 and the drain of LN2 (instead of the drain of LP3) to improve the PSR of the amplifier.



An embedded state machine handles the soft start procedure and the fault signals from the protection circuitry:

- Over-Current: if High Side current over 5.8A for 32 consecutive times
- Under-Voltage: control on Vin if lower than a threshold
- Over-Temperature: if  $T_{chip} > 115^{\circ}\text{C}$
- Disable Buck: from external pin

