

# Design of the **Timepix3**



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25<sup>th</sup> May 2011

8th International Meeting on Front-End Electronics



# Outline

- Introduction to Timepix3
- Timepix3 Analog Front-End
- Timepix3 readout architecture
- A new high density and low power digital Library
- Conclusions



# 2 Collaborations → 21 collaborating institutes

## Medipix2

- INFN Cagliari
- CEA-LIST Saclay
- CERN Geneva
- University of Erlangen
- University of Freiburg
- ESRF Grenoble
- University of Glasgow
- University of Houston
- IFAE Barcelona
- Mid Sweden University
- MRC-LMB Cambridge
- INFN Napoli
- NIKHEF Amsterdam
- INFN Pisa
- FZU CAS Prague
- IEAP CTU Prague
- SSL Berkeley

## Medipix3

- ALMOF Amsterdam
- University of Bogota
- University of Canterbury NZ
- CEA-LIST Saclay
- CERN Geneva
- DESY Hamburg
- Diamond Light Source
- University of Erlangen
- ESRF Grenoble
- University of Freiburg
- University of Glasgow
- ITER
- University of Karlsruhe
- Leiden University
- Mid Sweden University
- NIKHEF Amsterdam
- IEAP CTU Prague
- SSL Berkeley
- VTT Microsystems

<http://www.cern.ch/medipix>

# The Medipix Chips

Silicon, 3D, CdTe, GaAs,  
Amorphous Silicon, Gas  
Amplification, Microchannel  
Plates etc...

A philosophy of functionality built  
into the pixel matrix allows  
complex behavior with a minimal  
inactive region

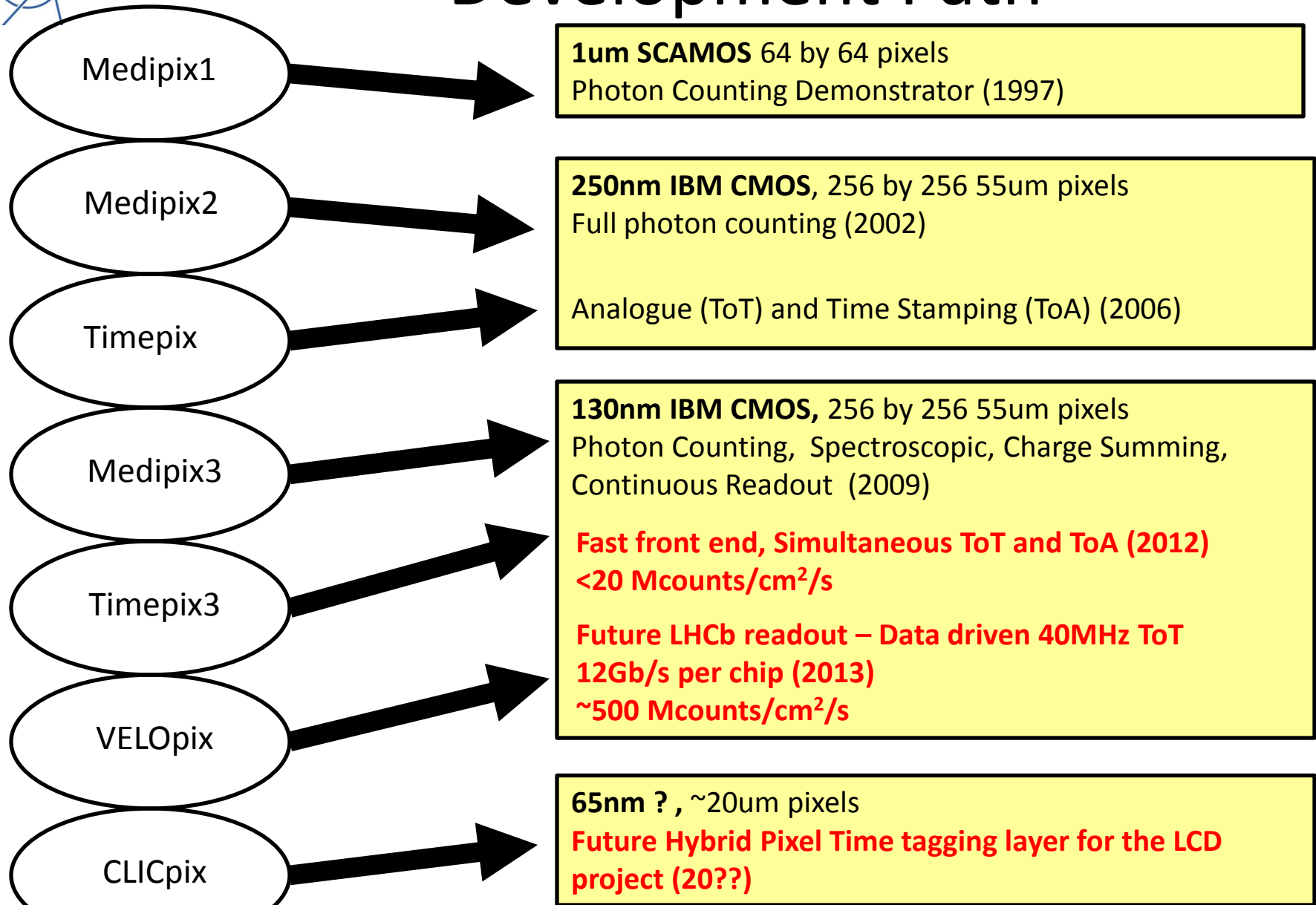
14 mm

55um square pixel matrix  
256 by 256

Configurable 'shutter'  
allows many different  
applications



# Development Path





# Timepix3 Scope

- Several groups in the Medipix3 collaboration have shown interested in a new version of the Timepix (2006) → Timepix3
- Large range of applications (HEP and non-HEP):
  - X-ray radiography, X-ray polarimetry, low energy electron microscopy
  - Radiation and beam monitors, dosimetry
  - 3D gas detectors, neutrons, fission products
  - Gas detector, Compton camera, gamma polarization camera, fast neutron camera, ion/MIP telescope, nuclear fission, astrophysics
  - Imaging in neutron activation analysis, gamma polarization imaging based on Compton effect
  - Neutrino physics
  - Main Linear Collider application: pixelized TPC readout
- Reuse many building blocks from Medipix3 chip (2009)
- Timepix3 is an approved project by the Medipix3 collaboration with an assigned budget (2-engineering runs)
- Design groups: NIKHEF, BONN, CERN

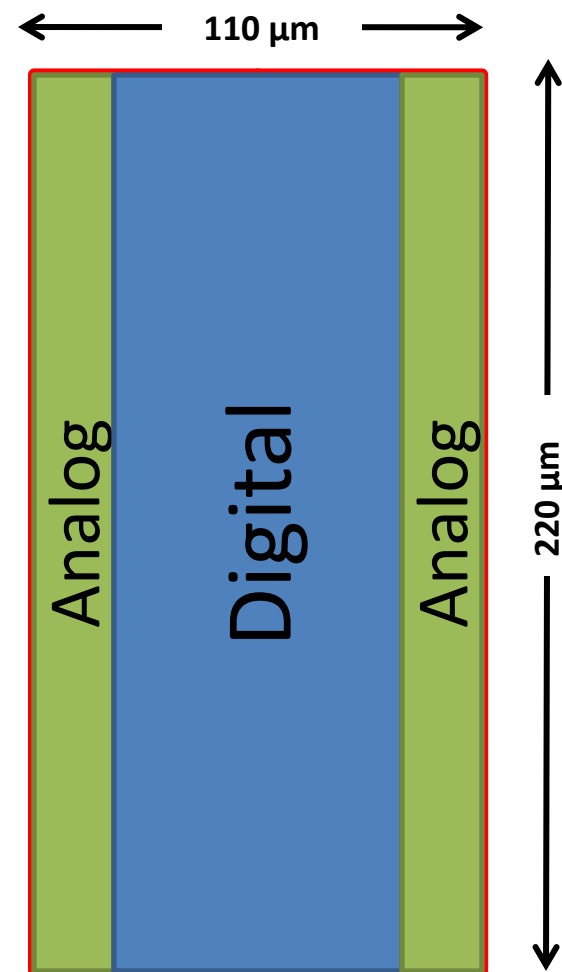


# Timepix3 Main Requirements

- Matrix layout: 256x256 pixels (Pixel size 55x55  $\mu\text{m}$ )
- Time stamp and TOT recorded simultaneously
  - 8-10 bit Energy Measurement (TOT)
    - Standard Resolution 25ns (@40MHz)
    - Energy Dynamic range from 6.4  $\mu\text{s}$  to 25.6  $\mu\text{s}$  (@40MHz)
  - 10-12 bits Slow time-stamp
    - Resolution 25ns (@40MHz)
    - Dynamic range 25.6  $\mu\text{s}$  (10 bit) to 102.4  $\mu\text{s}$  (12 bit)
  - 4 bits Fast time-stamp
    - resolution  $\sim 1.5\text{ns}$  (if using on-pixel oscillator running at 640MHz)
    - Dynamic range 25ns
- Sparse Readout
- Technology choice: IBM 130nm DM 3-2-3 or 4-1

# The Timepix3 Chip

<b>Readout Chip</b>	TIMEPIX3 (beginning of 2012)
<b>Pixel size</b>	55 x 55 $\mu\text{m}^2$
<b>Pixel arrangement</b>	256 x 256 (2x4 superpixels)
<b>Sparse readout</b>	YES
<b>PC, TOA or TOT recorded simultaneously</b>	YES (2 at a time) ~40 bit/Hit
<b>Minimum threshold</b>	> 500 e <sup>-</sup> (1.8 keV)
<b>TOA resolution</b>	> 1.5 ns
<b>Peaking time</b>	< 25 ns
<b>TOT resolution</b>	< 5% channel to channel spread
<b>Technology</b>	IBM 130nm DM 3-2-3 or DM 4-1-3
<b>Power consumption ON</b>	<700 mW (~20 $\mu\text{W}/\text{pixel}$ ) @1.2 V
<b>Power consumption OFF</b>	<10 mW (Power Pulsing)
<b>Target floorplan</b>	3 sides buttable and minimum periphery
<b>TSVs possibility</b>	YES. Multi-dicing scheme as Medipix3
<b>Count Rate</b>	20x 10 <sup>6</sup> x-rays/cm <sup>2</sup> /s



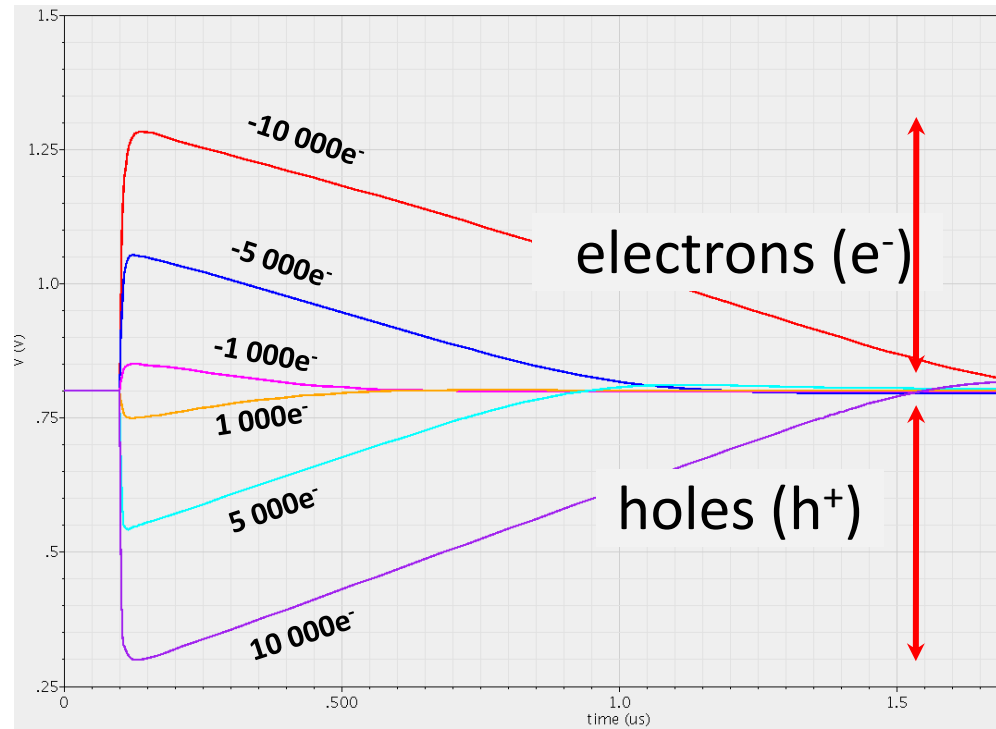
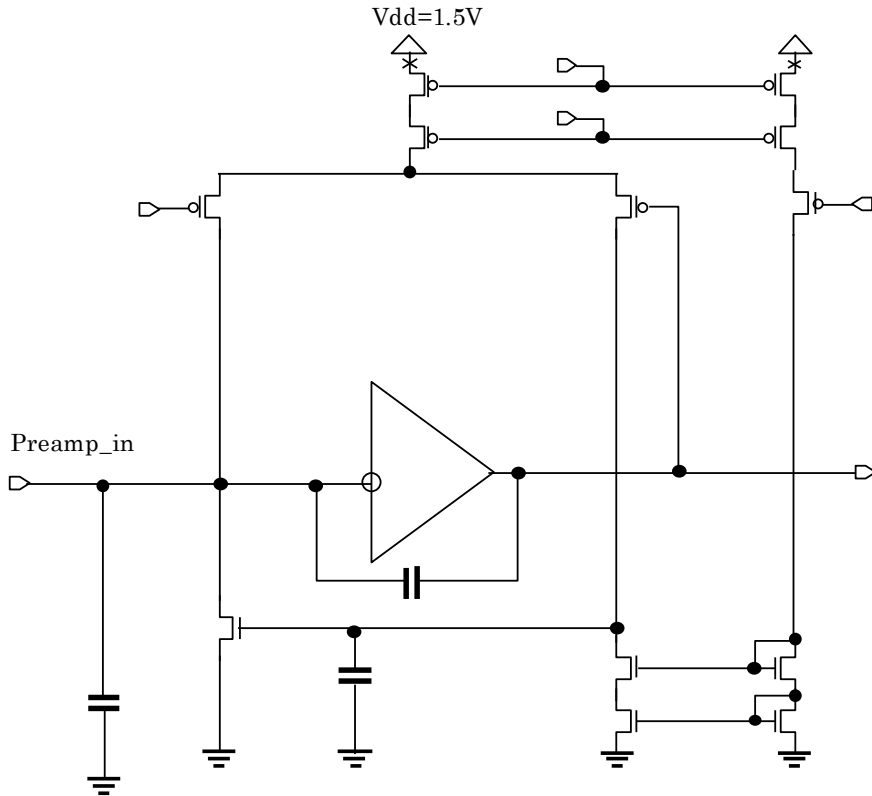
# **TIMEPIX3 ANALOG FRONT END**



# Timepix3/VeloPIX pixel FE

- Timepix3 and VeloPix chips can use the same front-end design
- Main requirements:
  - Bipolar input with DC leakage current compensation
  - Small and low power →  $55 \mu\text{m} \times [10\dots20] \mu\text{m}$  and  $< 10 \mu\text{W}$
  - TimeWalk  $< 25\text{ns}$  → Fast peaking time in Preamp and Fast discriminator (power penalty)
  - Full chip minimum detectable charge as low as possible ( $< 500e^-$ ) → 4 bits threshold tuning and low Preamp Noise (ENC)
  - Precise TOT measurement → Minimize Preamp Noise (ENC)
- An advance version of the schematic has been designed (CERN and NIKHEF)
- Simulation based results are shown in following slides

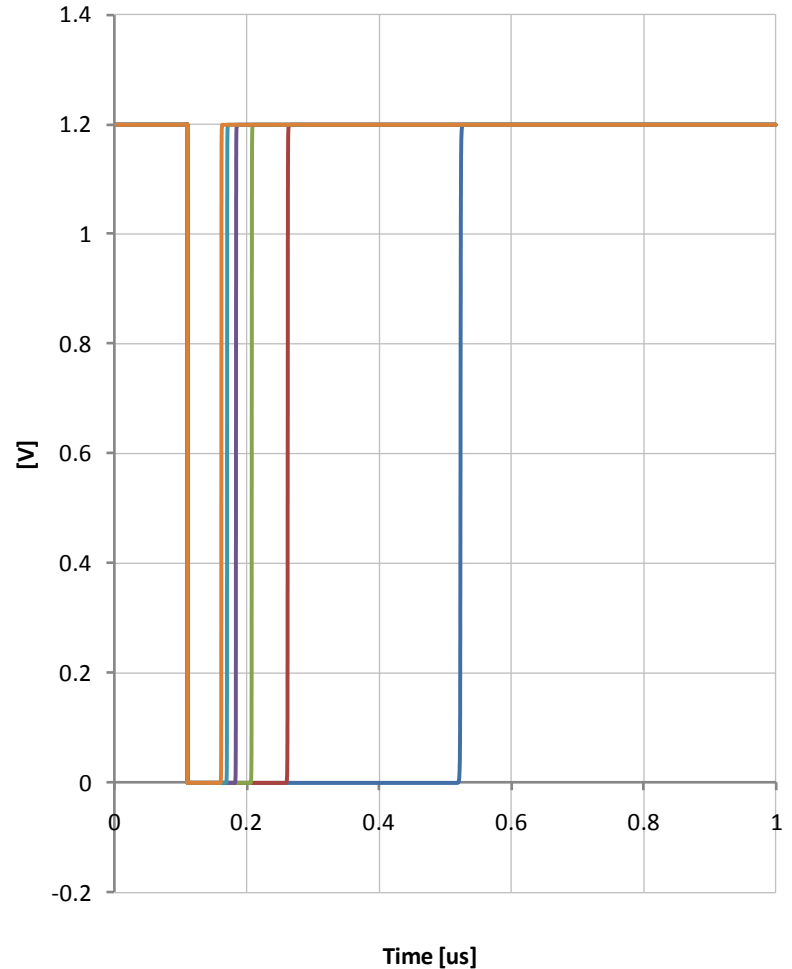
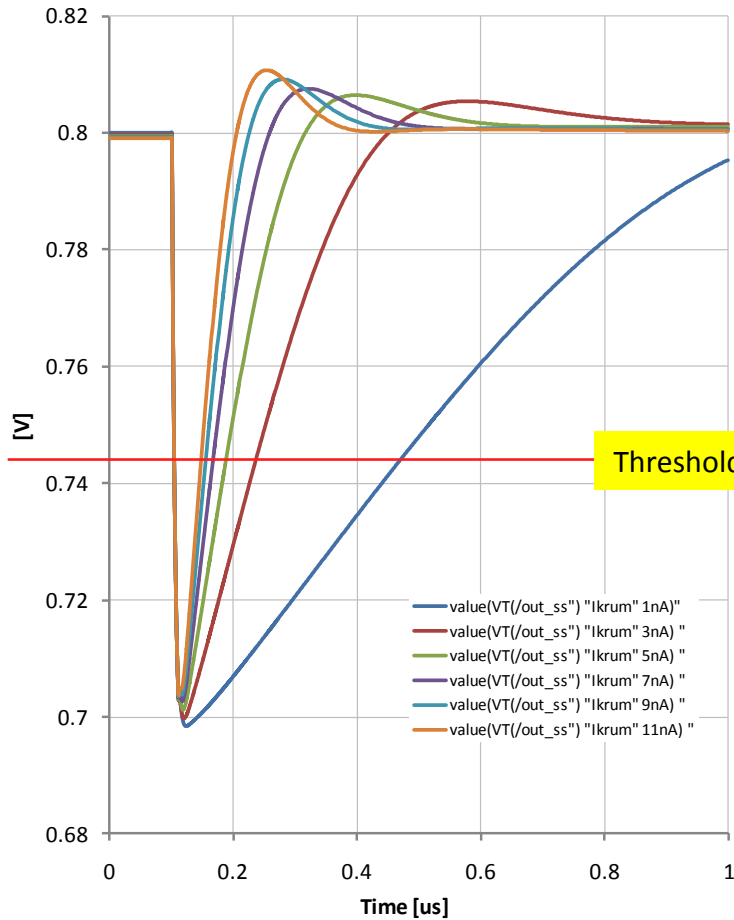
# FE of Timepix3



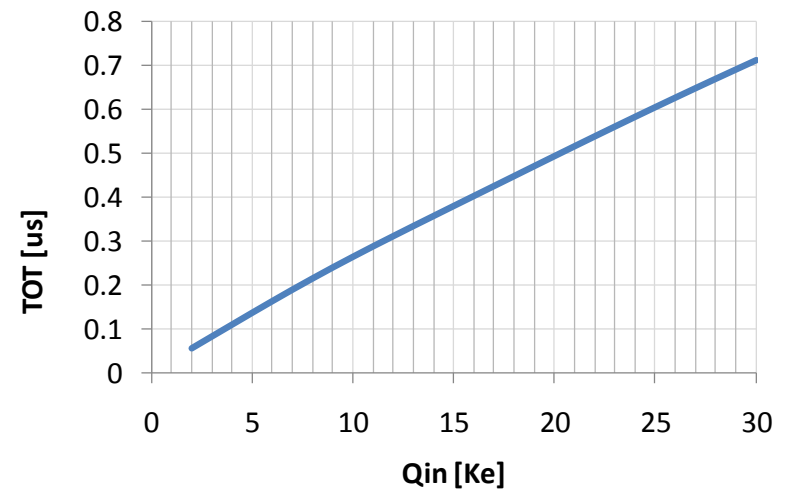
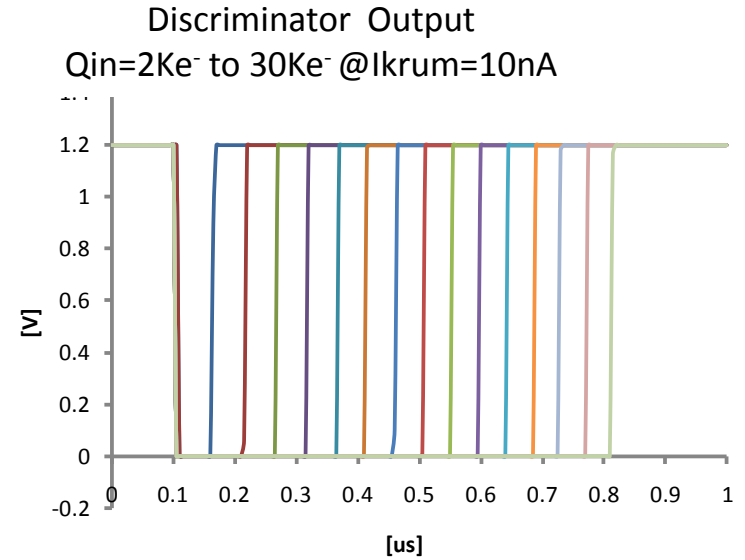
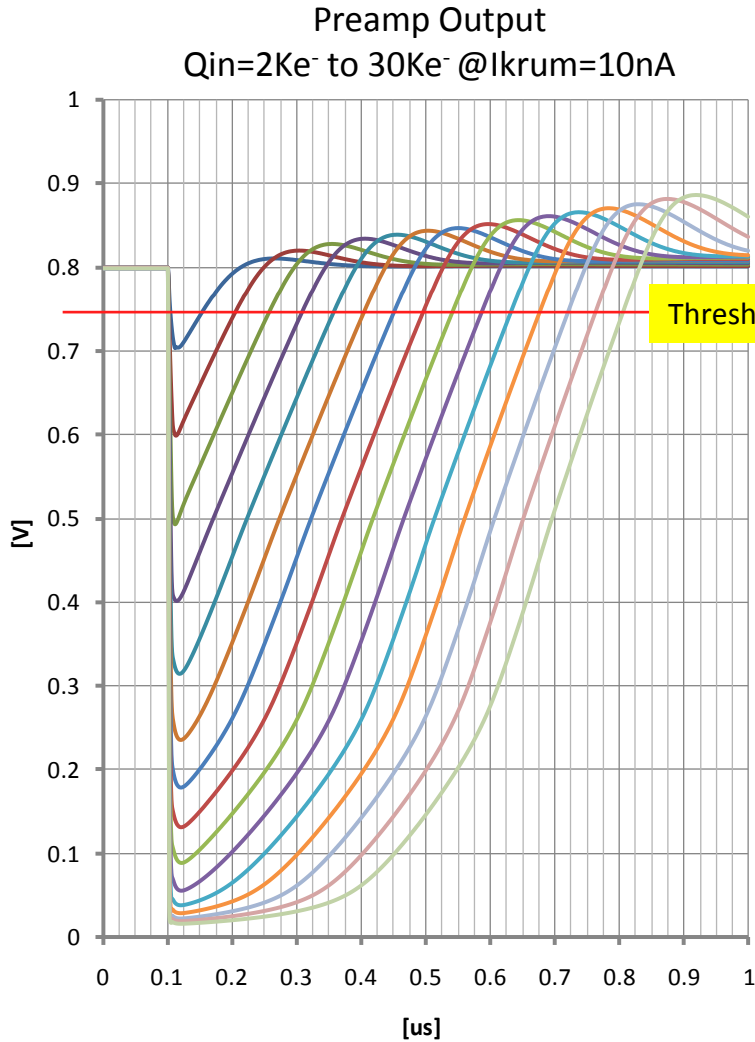
- The design of Timepix3/Velopix FE is based in the Krummenacher FE architecture

# Tunable return to zero ( $V_{out}$ vs $I_{krum}$ )

$Q_{in} = 2ke^-$

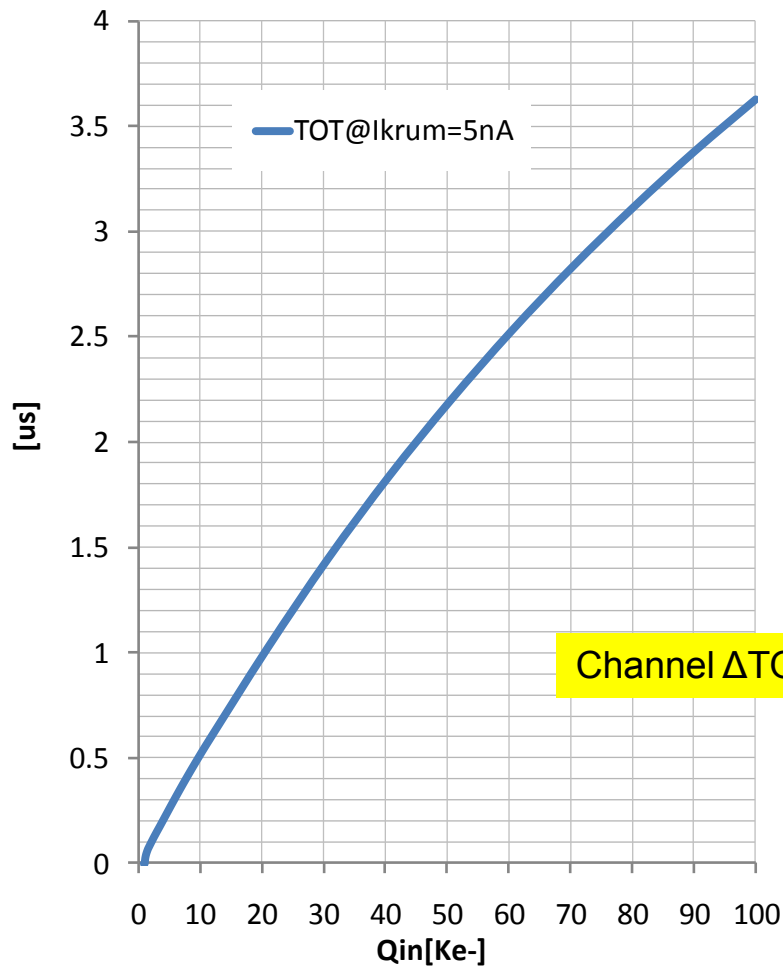


# Time-over-threshold response

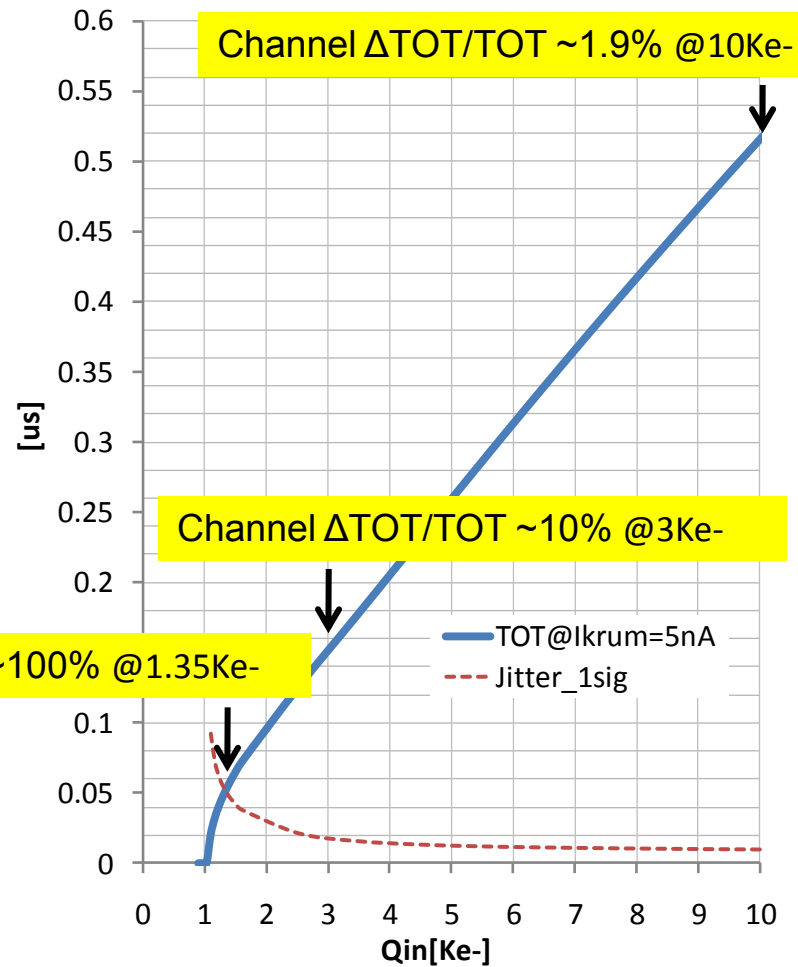


# TOT linearity and $\Delta\text{TOT}/\text{TOT}$

Threshold=1ke<sup>-</sup>

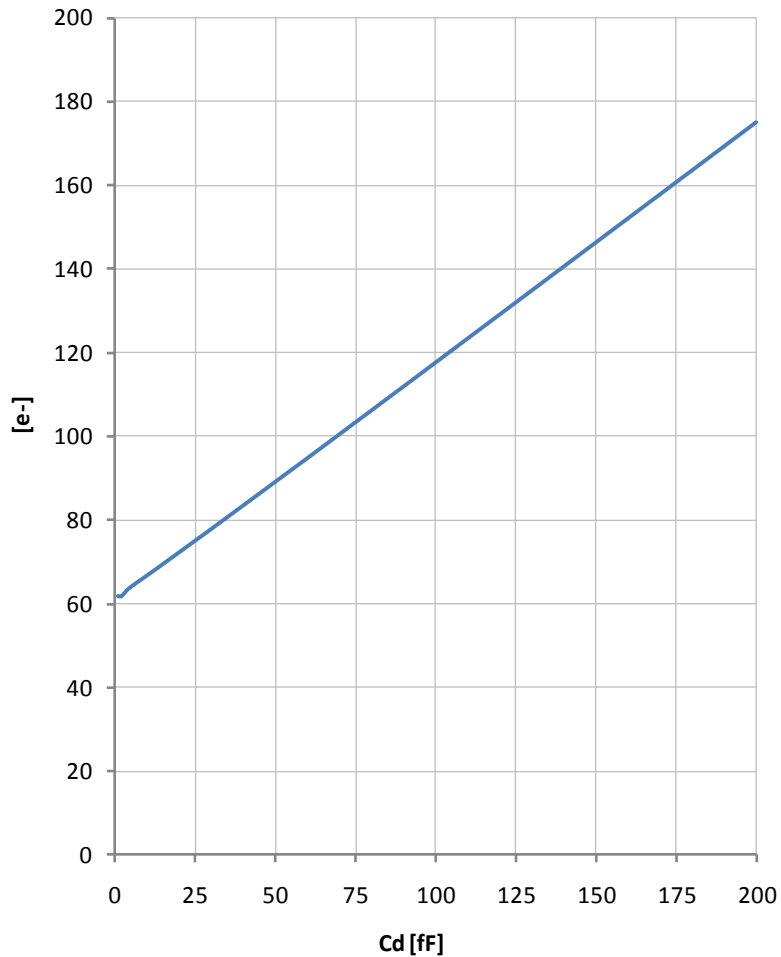


Channel  $\Delta\text{TOT}/\text{TOT} \sim 100\%$  @1.35Ke<sup>-</sup>

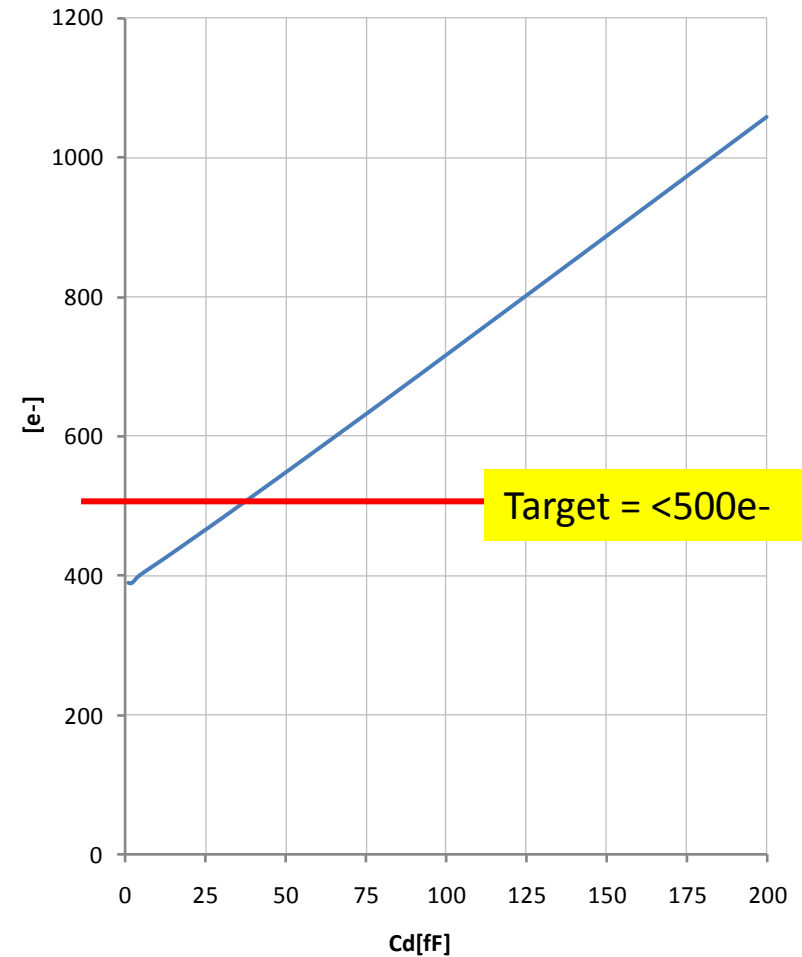


# Channel Noise and Minimum detectable Charge

Pixel noise (ENC) vs Cd[fF]

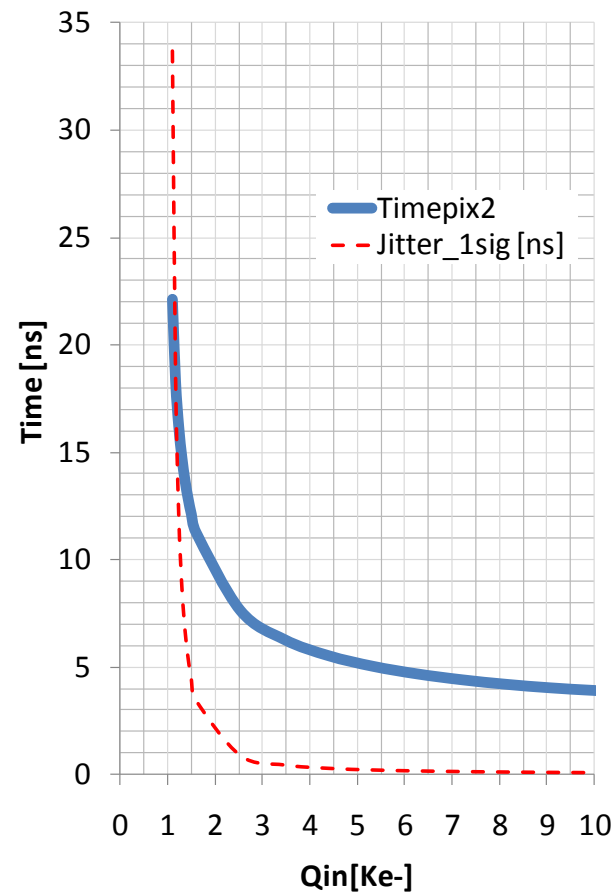
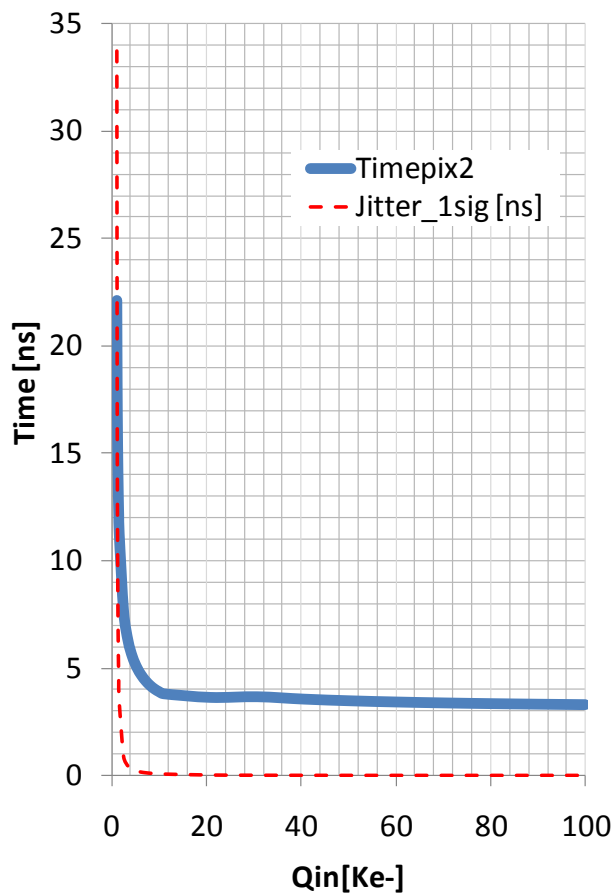
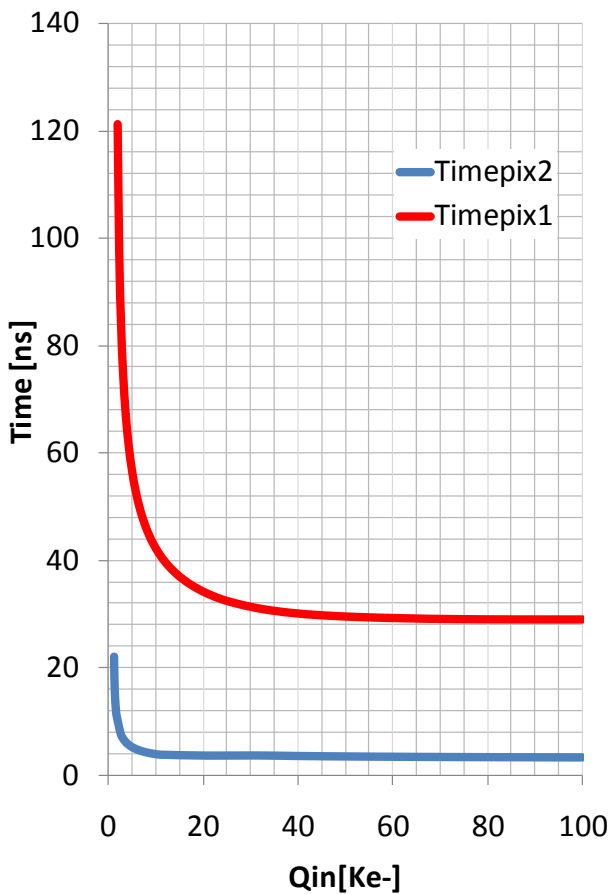


Minimum detectable charge



# TimeWalk Simulations

Threshold=1ke<sup>-</sup>

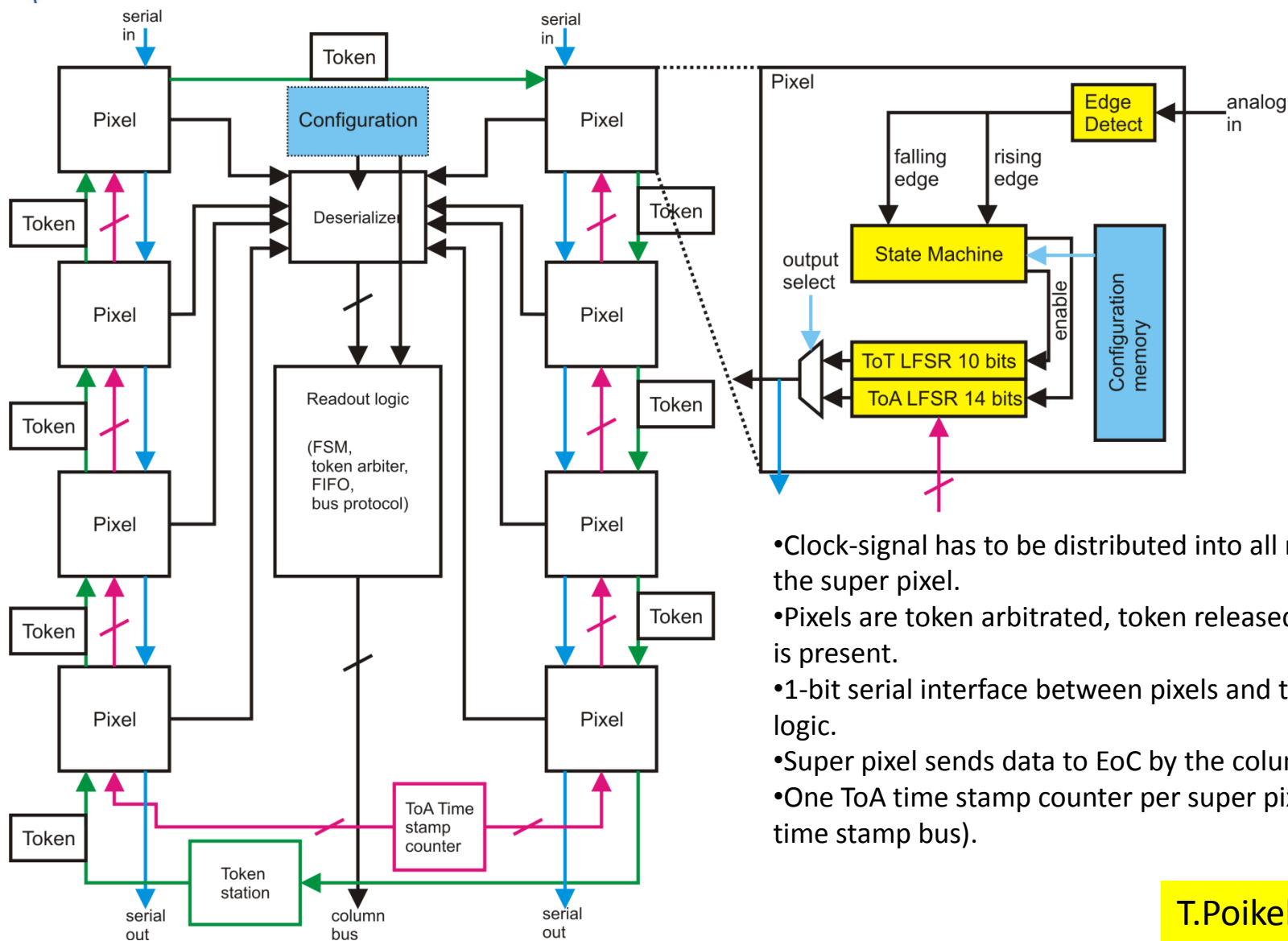


# Simulations Summary

	Simulation Results
Pixel size	55 $\mu\text{m}$ x 55 $\mu\text{m}$
Analog pixel area	55 $\mu\text{m}$ x [10...20] $\mu\text{m}$
Pixel matrix	256 x 256
Input charge	Bipolar ( $\text{h}^+$ and $\text{e}^-$ )
Leakage current compensation	YES
Detector capacitance (Planar detector)	< 50 fF
Peaking time	<25ns if Cd<70fF
Preamp output linear dynamic range	< 15 $\text{Ke}^-$
Timewalk	<25ns [@ $Q_{\text{in}}$ >Threshold]
Return to zero (Tunable)	YES ( $\Delta I_{\text{krum}}$ )
TOT linearity and range	Monotonic up to $\sim 150 \text{ Ke}^-$ @ $I_{\text{krum}} 10\text{nA}$
Return to zero full chip spread (TOT spread)	< 5%
ENC ( $\sigma_{\text{ENC}}$ )	$0.57 \cdot \text{Cd}[\text{fF}] + 61 [\text{e}^-] \rightarrow \sim 75 \text{ e}^-$ @ Cd=25fF
# Thresholds	1
Discriminator response time	<5ns [if $Q_{\text{in}}$ >Threshold + 5 $\text{Ke}^-$ ]
MC simulated Threshold spread	$\sim 200 \text{ e}^-$
Threshold spread after tuning (4 bits)	$\sim 20 \text{ e}^-$
Full chip minimum detectable charge	$6 \cdot \sqrt{\text{ENC}^2 + \text{Threshold\_mismatch}^2} \rightarrow \sim 475 \text{ e}^-$ @ Cd=25fF
Pixel analog power consumption	8.4 $\mu\text{W}$ static (Preamp 3.6 $\mu\text{W}$ and 4.8 $\mu\text{W}$ Discriminator) 2.4 $\mu\text{W}$ dynamic (only @ HIT)

# **TIMEPIX3 READOUT ARCHITECTURE**

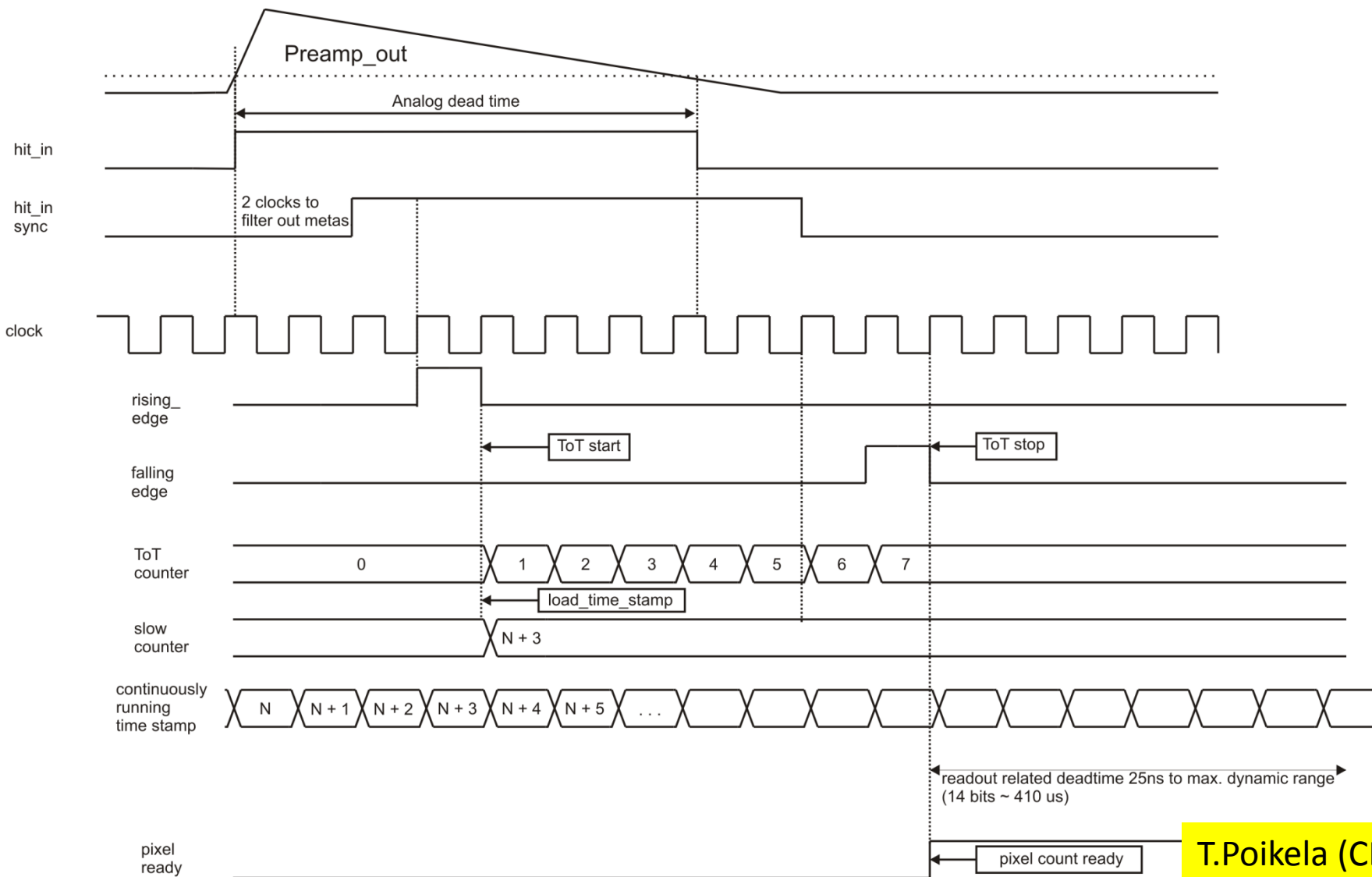
# Super Pixel and Pixel



- Clock-signal has to be distributed into all modules in the super pixel.
- Pixels are token arbitrated, token released when a hit is present.
- 1-bit serial interface between pixels and the readout logic.
- Super pixel sends data to EoC by the column bus.
- One ToA time stamp counter per super pixel (or global time stamp bus).

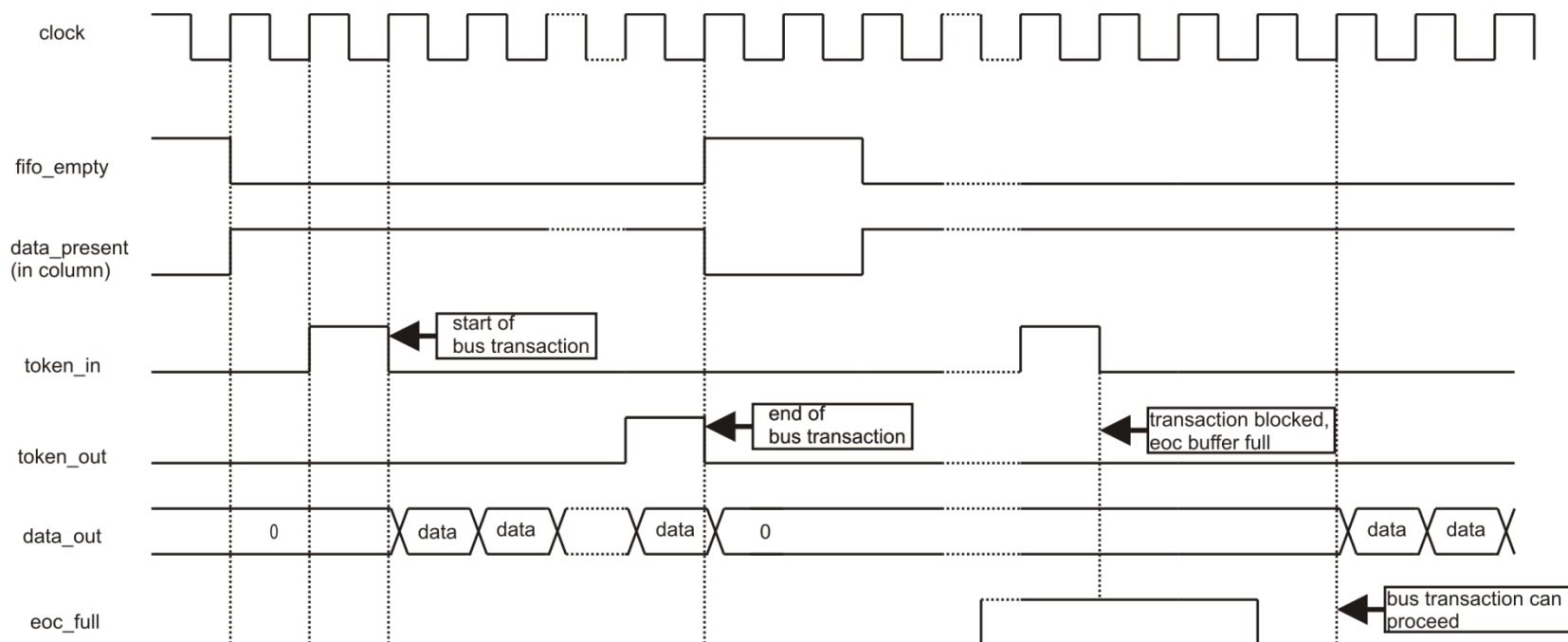
T.Poikela (CERN)

# Timing Diagram of Digital Pixel



T.Poikela (CERN)

# Super Pixel-to-EoC data transport



- Bus protocol does not allow any data overflows in the periphery. If EoC is full, no data is transmitted.
- Protocol requires a counter in the super pixel to count the number of words per bus transaction (max 3-bit counter)
- Global signals in Double Column:

Data bus	5b/9b (not fixed yet)
EoC Full	1b
DataPresent	1b
RefClk	1b
Reset	1b
Shutter	1b
Time stamp	14b (or implemented with local counter)
Total	10b – 28b

T.Poikela (CERN)



# To sum it up: Pixel/ Super Pixel Features

Feature	Description
ToT Counter 10 bits (Pixel)	Resettable LFSR for ToT/ event count.
ToA Counter 14 bits (Pixel)	Resettable LFSR / parallel load register (40MHz)
Fast ToA Counter 4 bits (Pixel)	Binary Counter (640MHz)
Event count/Integral ToT mode	Event count 10 bits, ToT 14 bits in this mode.
Configuration Register (~10 bits) (Pixel)	Size depends on the features in a pixel.
Fast counter reset (Pixel)	Reset in 24 clock cycles (600 ns).
Shutter-signal (Pixel)	Controls data taking. (See Timepix1)
Adjustable ToT/ToA clock. (Pixel?/Super Pixel?/EoC?)	Make ToA/ToT independent of each other.
Output select (either from 10b/14b/both counters)	Makes it possible to read out only ToA or ToT information if required.
Configurable pixel-to-super pixel FIFO dead time.	Done by adjusting the shift counter of deserializer in the super pixel.
User-enabled readout mode (Super pixel)	Closing the shutter starts the readout in user-enabled mode (Event count mode).
Continuous readout mode (Super pixel)	Readout operates independently of shutter-signal.

# **A HIGH DENSITY AND LOW POWER STANDARD CELL LIBRARY**



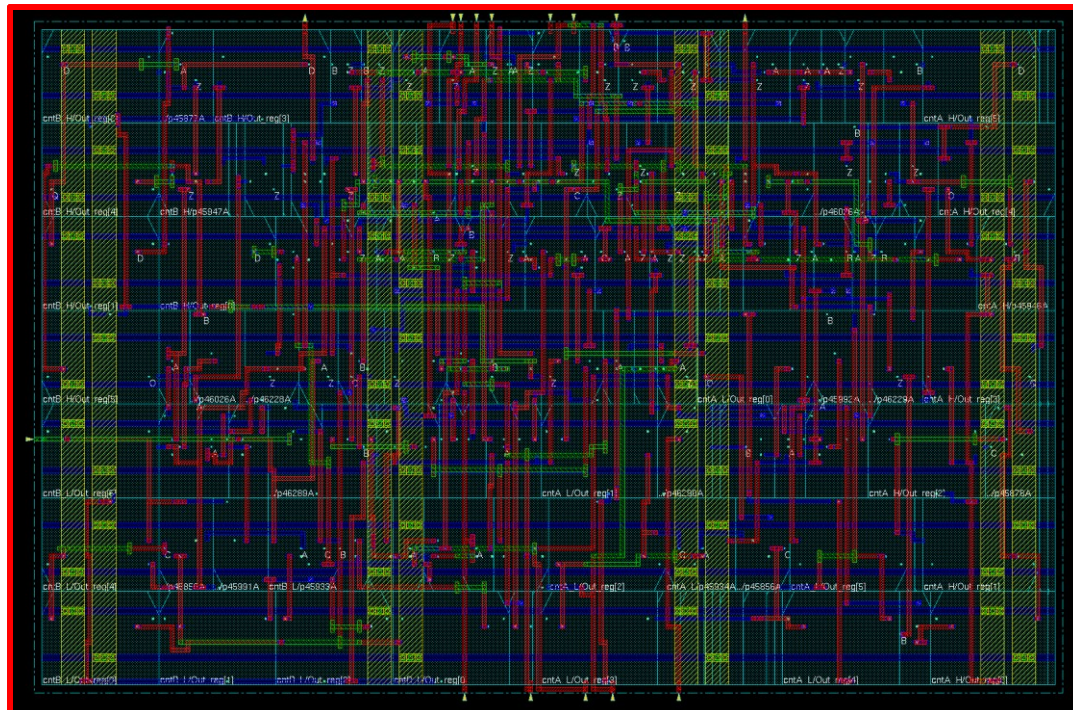
# An high density low power 130 nm digital library

- The design of the Timepix3 goes in parallel with the Medipix3.2 design
- The Medipix3.2 redesign requires significant changes in the digital part of the pixel (designed as a full custom layout)
- Can we use CERN default standard cell 130nm library at the pixel level?
  - **Too big:** @CERN the default library has **large cells** since is targeted for ~800MHz !!
  - **Too much leakage power:** @CERN the default library is **not low-power**
- A custom made high density library (SC\_130nm\_XL) design has been done with the initial idea of using it in Medipix3.2 pixel but with a huge potential impact in later developments (Timepix3, Velopix...)
- Main actions:
  - Reduce cells height → We don't need big buffers (speed)
  - Keep all transistor small or minimum size ( $W/L=0.28/0.12$ )
  - ADD NV and PV layers → Low power transistors (no area penalty)

# Medipix3 pixel counter (24 bits) + control logic

← 55 μm →

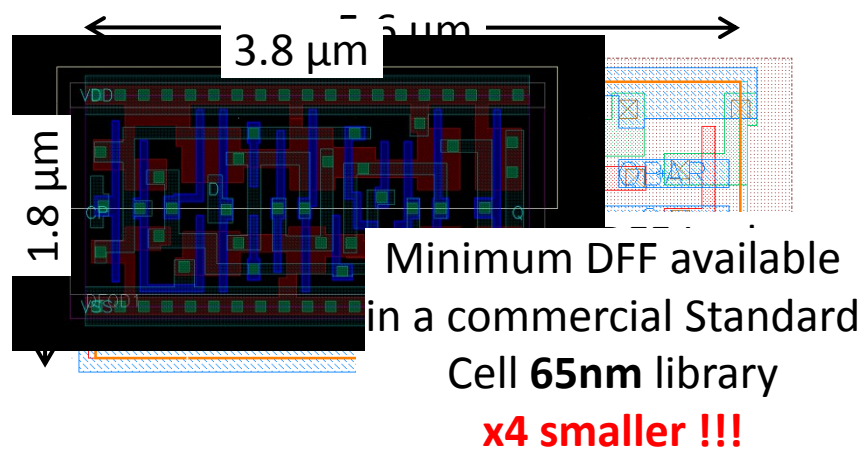
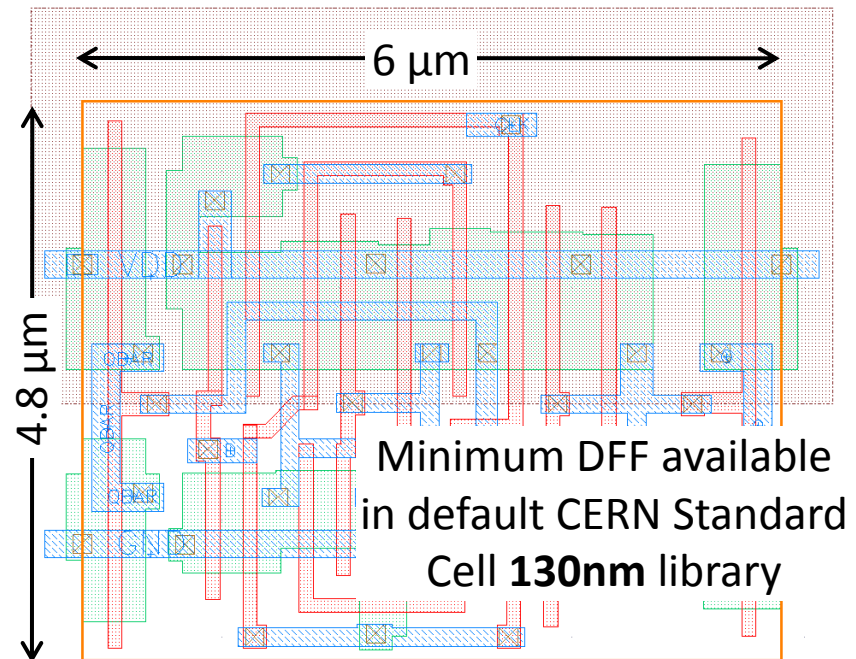
- Synthesized using the CERN IBM 130nm Standard Cell Library (CMOS8RF)
- Area is too big (52 x 33.6) → ~60% pixel area
- High static (leakage) power consumption:



VDD	Temp	Leakage in cell	leakage In Chip
1.4 V	125 C	22.5 μW	<b>1.5 W !!!</b>
1.5 V	25 C	223 nW	<b>14.6 mW</b>
1.6 V	-55 C	470 pW	<b>30 μW</b>

# SC\_130nm\_XL Library

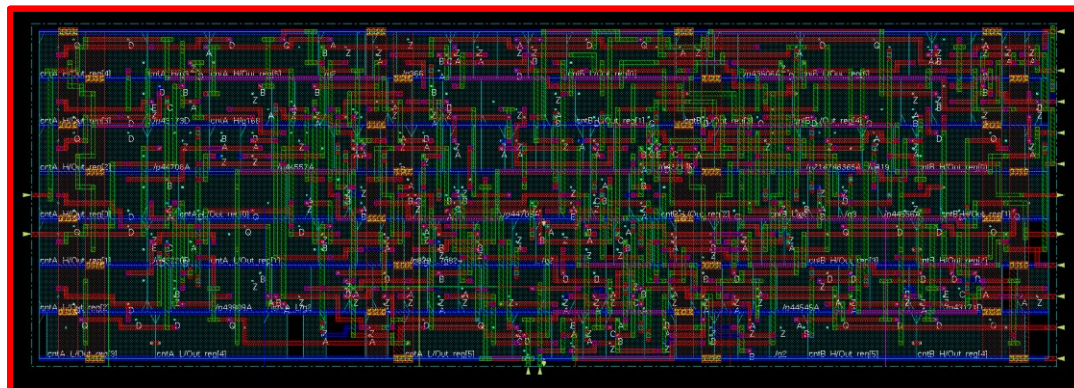
- Row Height is fixed to 2.4  $\mu\text{m}$
- Well Tap library
- Maximum frequency  $<\sim 350$  MHz
- Low power transistors
- $\sim 45$  cells are available in the library (growing fast...)
  - No SEU registers (so far)
- Encounter Library Characterizer (ELC) has been used to fully characterize the library in different corners
  - Full Synopsis library
  - Verilog library
  - LEF files



# Medipix3 pixel counter (24 bits) + control logic

← 55 μm →

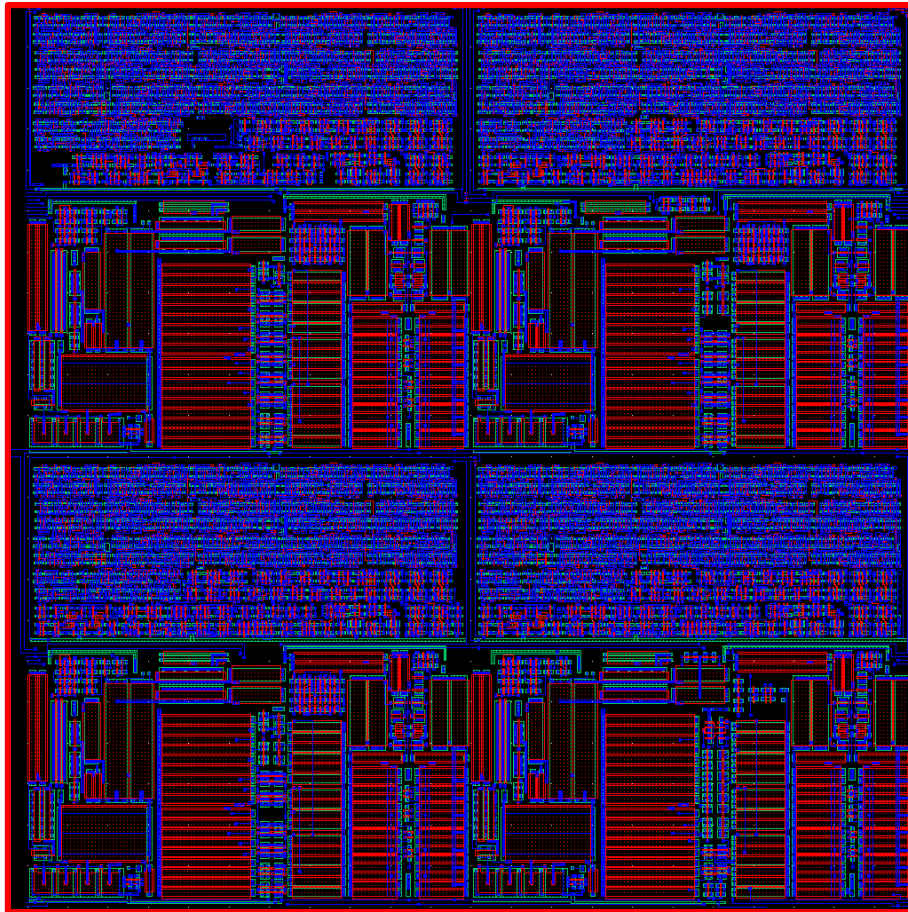
- Synthesized using the SC\_130nm\_XL library
- Area (52 x 16.8) → ~29% pixel area
- Low cell leakage power



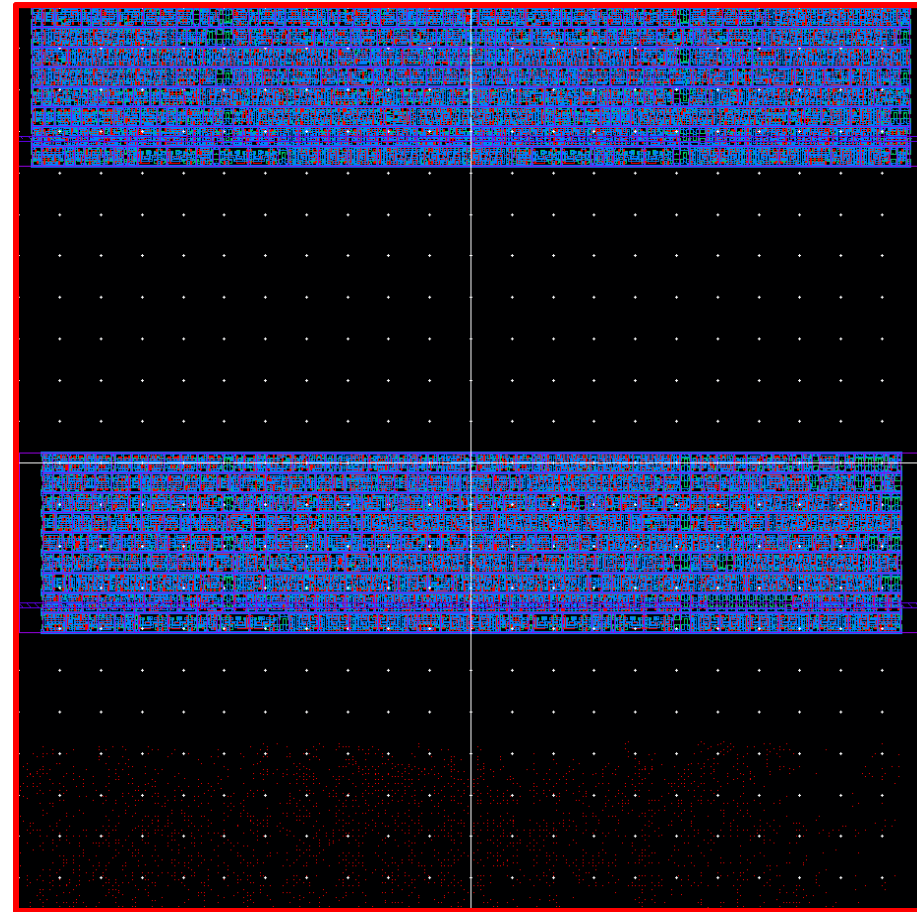
VDD	Temp	Leakage in cell	leakage In Chip
1.5 V	25 C	2.5 nW	<b>163 μW</b>
1.2 V	25 C	1.15 nW	<b>75.3 μW</b>

# Comparison between old and new counter

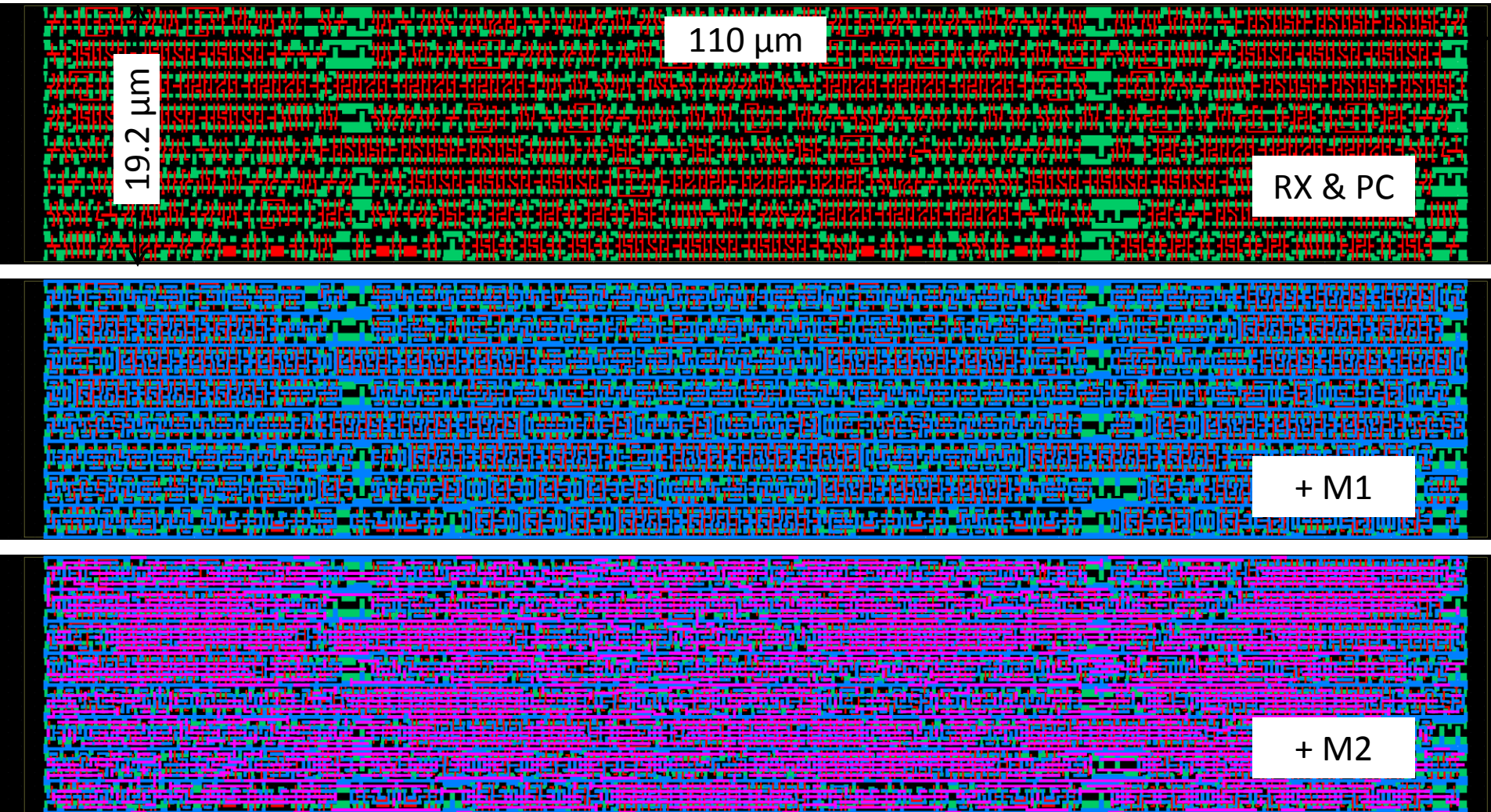
Medipix3.0 (2009)



Medipix3.2 (2011) using SC\_130nm\_XL



# Medipix3.2 counter using SC\_130nm\_XL library



# CONCLUSIONS

# Conclusions

- The Timepix3 will be the next chip in the Medipix family
  - TOT and TOA simultaneously
  - Sparse and data driven readout
- The use of a new high density and low power digital library helps to optimize the pixel digital area
- Submission of the Timepix3 chip is expected by beginning of 2012

