CMOS Pixel Sensors adapted to Tracking Devices

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- coll. with IRFU-Saclay -

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  - ⋇ general remarks on highly pixelated and thin sensors
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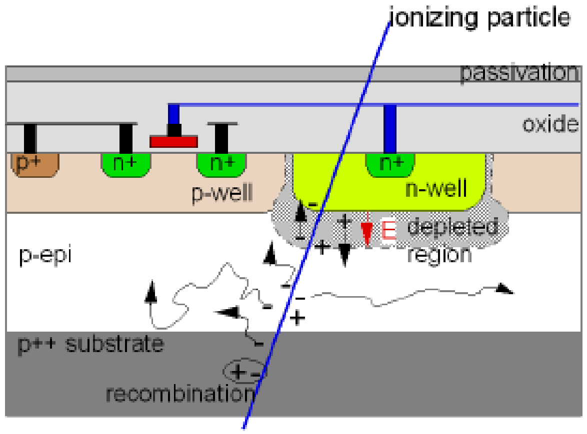
  - ⋇ applications under way or under study
  - ⋇ trend of development : smaller feature size, larger pitch, larger sensors, ...
- *Summary*

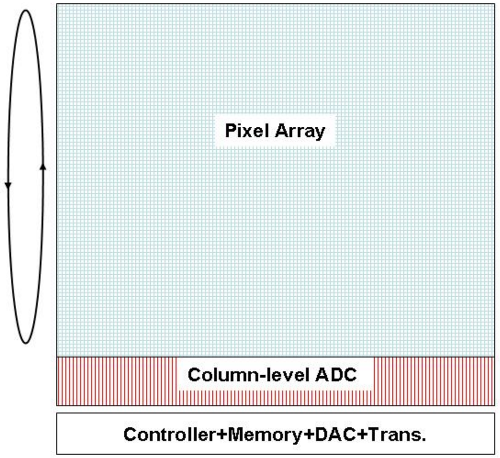
CMOS Pixel Sensors: State of the Art

- **Prominent features of CMOS pixel sensors:**
  - ✳ high granularity $\Rrightarrow$ excellent (micronic) spatial resolution
  - ✳ very thin (signal generated in 10-20 μm thin epitaxial layer)
  - ✳ signal processing μ-circuits integrated on sensor substrate
    - $\Rrightarrow$ impact on downstream electronics ($\Rrightarrow$ cost)



- **Organisation of MIMOSA sensors:**
  - ✳ manufactured in 0.35 μm OPTO process
  - ✳ signal sensing and analog processing in pixel array
  - ✳ mixed and digital circuitry integrated in chip periphery
  - ✳ read-out in rolling shutter mode

    (pixels grouped in columns read out in //)
    - $\Rrightarrow$ impact on power consumption



Granularity versus Speed

- **Impact of high granularity:**
  - ⁎ large number of pixels $\Rrightarrow$ handicap for read-out speed of the full pixel array
  - ⁎ **but:** slow down of detector read-out frequency compensated by accuracy
    - ↪ single point resolution and material budget :
      - ⊸ improved neighbouring hit separation on each detector layer
      - ⊸ improved track extrapolation accuracy during track reconstruction from layer to layer
      - ⊸ effect enhanced by small material budget
      - ⊸ strategy option: connect CMOS pixels sensors to 2-layer fast&thick detector
  - ⁎ **global effect :** improved track reconstruction capability in high density conditions
    - $\Rrightarrow$ data rate handling capability not really downgraded (but track rec. SW needs to be adapted)

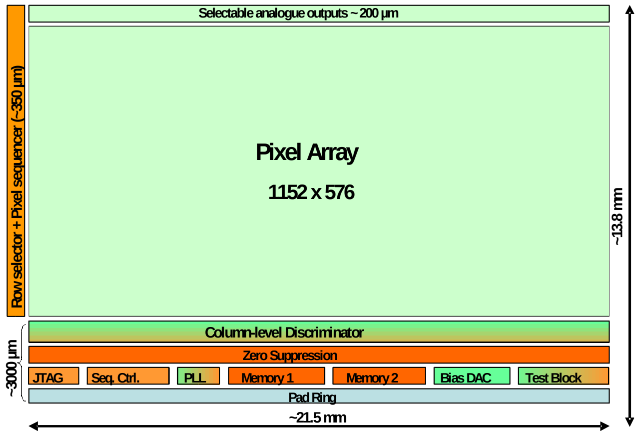
- **Illustration with CMOS pixels (20×20 μm^2) :**
  - ⁎ $>$ 60 times smaller than ATLAS pixels (50×425 μm^2)
  - ⁎ $\gtrsim$ O(10-100) times more accurate track extrapolation for hit search

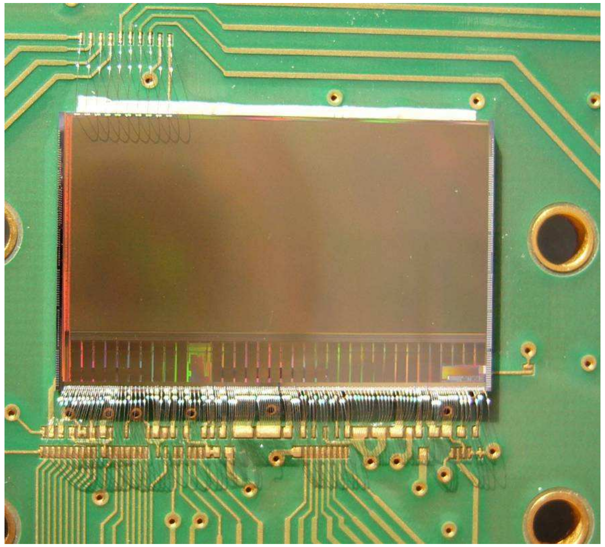
$\Rrightarrow$ $\sim$ **3 ordres of magnitude improvement in hit rate handling capability**

- ↪ single CMOS pixel layer in a tracker does not provide all added value of granular & thin sensors
- ↪ large particle rate does not necessarily imply priority to r.o. speed

CMOS Pixel Sensors: State of the Art

- **Main characteristics of MIMOSA sensor equipping EUDET BT:**
  - 0.35 μm process with high-resistivity epitaxial layer
    (coll. with IRFU/Saclay)
  - column // architecture with in-pixel amplification (CDS)
    and end-of-column discrimination, followed by $\emptyset$
  - active area: 1152 columns of 576 pixels (21.2$\times$10.6 mm^2)
  - pitch: 18.4 μm $\rightarrowtail$ $\sim$ 0.7 million pixels
    charge sharing $\Rrightarrow$ $\sigma_{sp} \lesssim$ 4 μm
  - t$_{r.o.}$ $\lesssim$ 100 μs ($\sim$10^4 frames/s)
    $\Rrightarrow$ suited to $>$10^6 part./cm^2/s
  - $\sim$ 250 mW/cm^2 power consumption (fct of N$_{col}$)

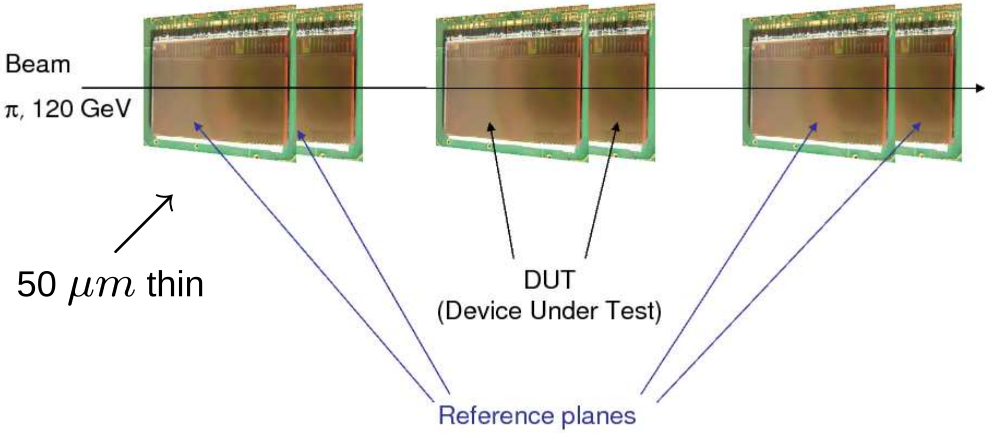




High-Resistivity CMOS Pixel Sensors

- **M.i.p. detection with LOW & HIGH resistivity CMOS sensors combined in a Beam Telescope (BT)**
  - 4 EUDET ref. sensors & 2 sensors under test
  - June 2010 at CERN-SPS ($\sim$ 120 GeV pions)
  - sensor variants : standard epitaxy (14 μm thick)

    & high-resistivity epitaxy (10 & 15 μm thick)



- **Main Results:**
  - det. eff. $\sim$ 100 % (SNR $\sim$ 40) for very low fake rate:
    - ▷ plateau until fake rate of few 10^{-6}
  - single point resolution $\lesssim 4\ \mu m$
  - det. eff. still $\sim$ 100 % after exposure

    to fluence of $1\cdot10^{13} n_{eq}/cm^2$

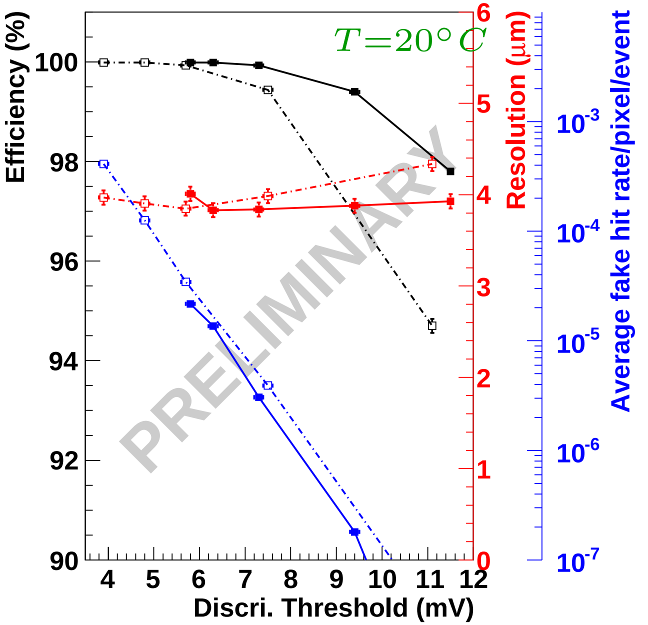
$\Rightarrow$ **Excellent detection performances**

with high-resistivity epitaxial layer

despite moderate resistivity (400 $\Omega \cdot cm$)

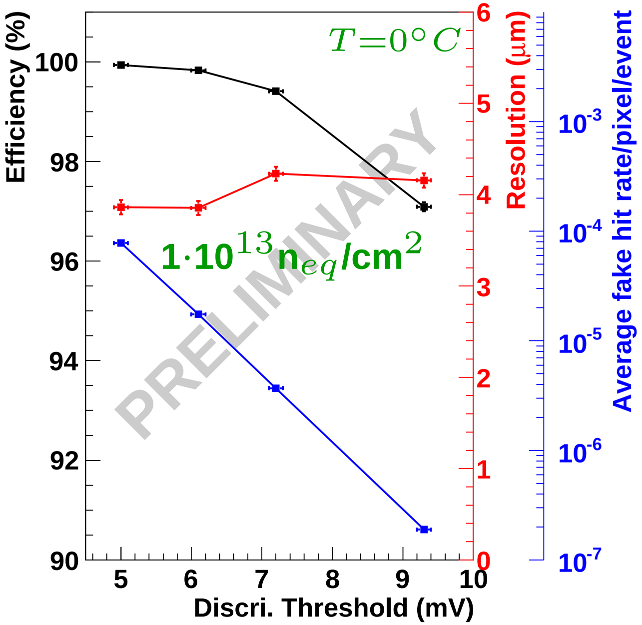
and poor depletion voltage ($<$ 1 V)

Mi26 HR-15 and HR-10 Efficiency, Fake rate and Resolution



Mi26 HR-15 Efficiency, Fake rate and Resolution

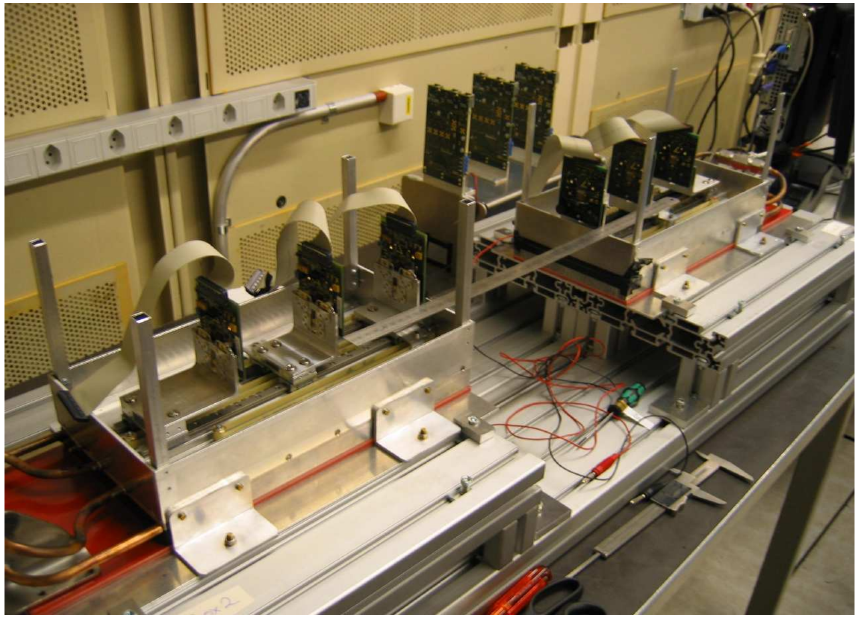
for a chip irradiated with a $1.10^{13}N_{eq}$ dose at T_{op} ~ 0° C



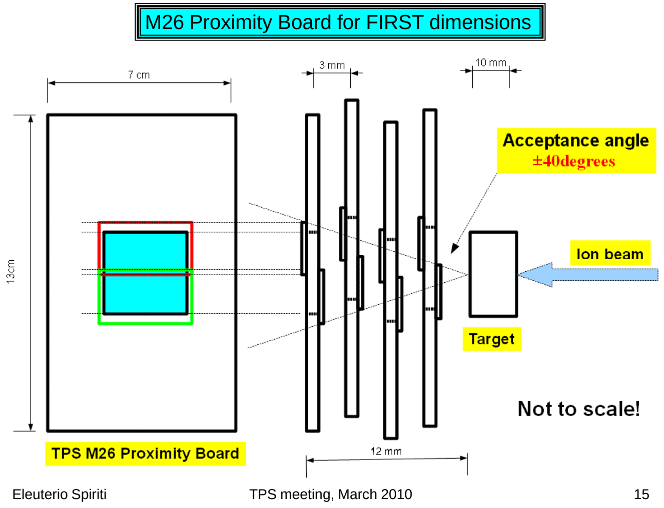
$\Rightarrow$ **Tolerance to $\gtrsim$ O(10^{14})n_{eq}/cm^2 seems within reach (study under way)**

Direct Applications of MIMOSA-26

- Beam telescope of the FP6 project EUDET
  - 2 arms of 3 planes (plus 1-2 high resolution planes)
  - MIMOSA-26 thinned to 50 μm
  - $\sigma_{extrapol.} \sim$ 1-2 μm EVEN with e$^-$ (3 GeV, DESY)
  - frame read-out frequency O(10^4) Hz
  - running since '07 (demonstrator: analog outputs) at CERN-SPS & DESY (numerous users)

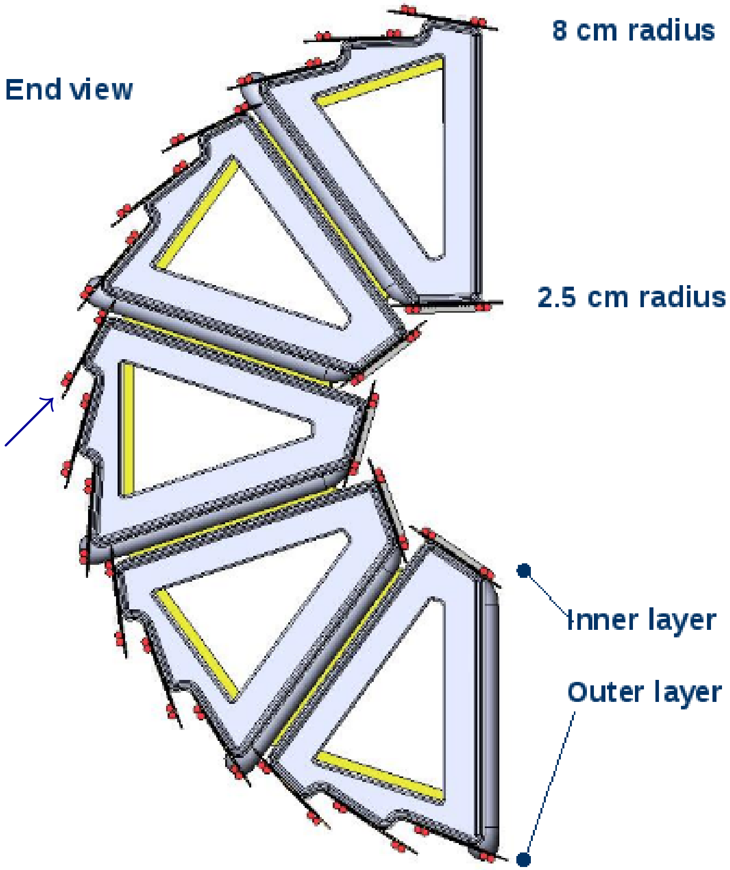


- **Spin-offs :**
  - **Several BT copies :** foreseen for detector R&D
  - **BT for channelling studies, mass spectroscopy, etc.**
  - **CBM (FAIR) :** MVD demonstrator (2-sided layers) for CBM-MVD (HP-2 project)
  - **FIRST (GSI) :** VD for hadrontherapy $d\sigma/d\Omega$ measurements ▷▷▷



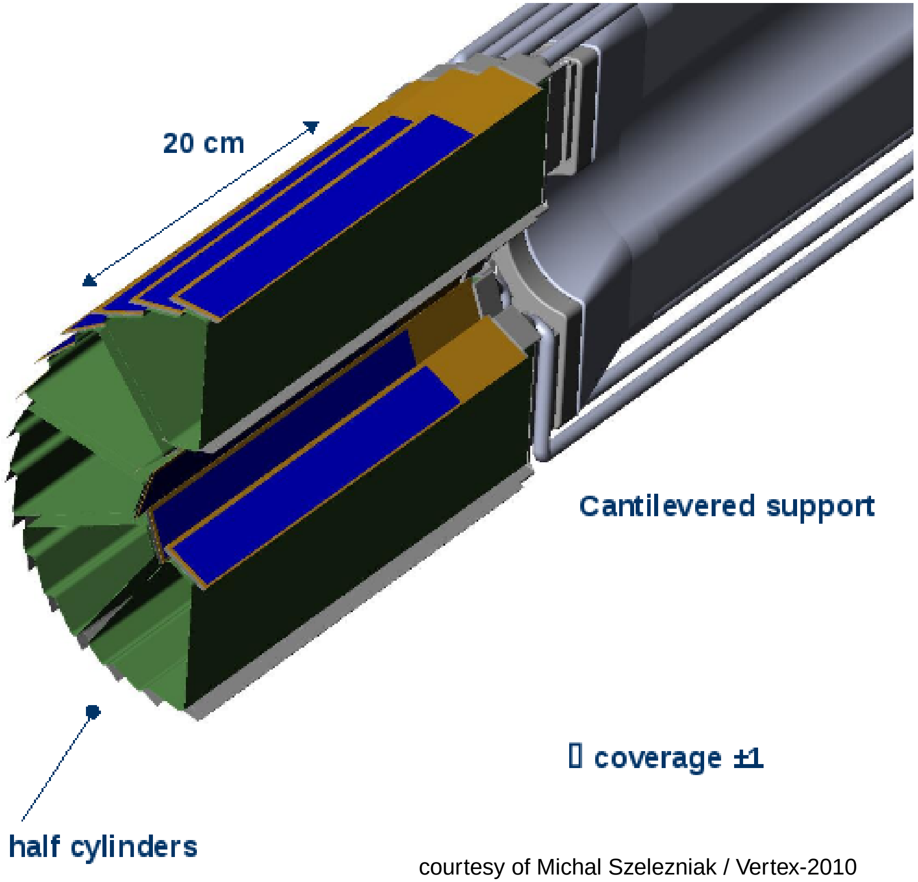
Application of CMOS sensors to the STAR-PXL

The detector ladders are 50 µm thinned silicon, on a flex kapton/aluminum cable.



0.37 % X_0/ladder

Total: 40 ladders

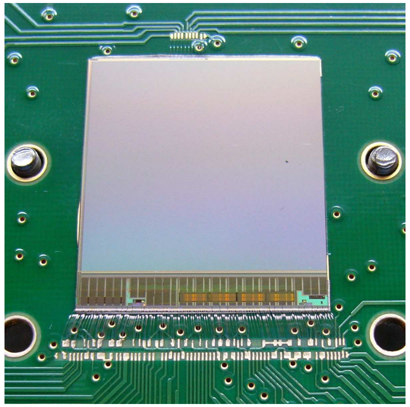


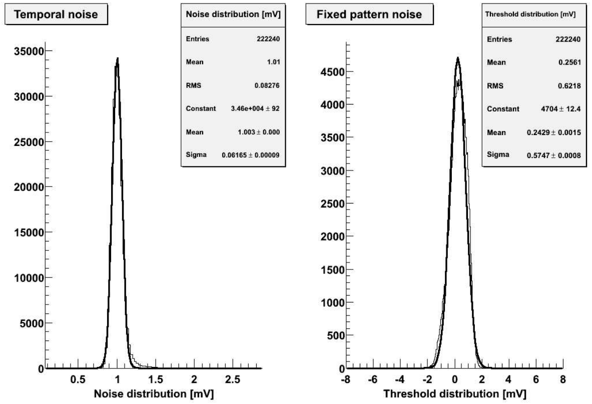
courtesy of Michal Szelezniak / Vertex-2010

▷▷▷ **1st vertex detector equipped with CMOS pixel sensors** ⟶ **1st data taking in 2013**

STAR-PXL Detector : MIMOSA-28

- **Use ULTIMATE sensor (alias MIMOSA-28) equipping STAR-PXL detector**
  - ▷ derived from MIMOSA-26 equipping EUDET BT
- **Main characteristics of ULTIMATE:**
  - ⋇ 0.35 μm process with high-resistivity epitaxial layer
  - ⋇ column // architecture with in-pixel cDS & amplification
  - ⋇ end-of-column discrimination and binary charge encoding, followed by $\emptyset$
  - ⋇ active area: 960 columns of 928 pixels (19.9$\times$19.2 mm^2)
  - ⋇ pitch: 20.7 $\mu m \rightarrowtail \sim$ 0.9 million pixels
    - $\hookrightarrow$ charge sharing $\Rrightarrow$ $\sigma_{sp} \sim$ 3.5 μm expected
  - ⋇ t$_{r.o.} \lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s)
    - $\Rrightarrow$ suited to $>$10^6 part./cm^2/s
  - ⋇ 2 outputs at 160 MHz
  - ⋇ $\lesssim$ 150 mW/cm^2 power consumption

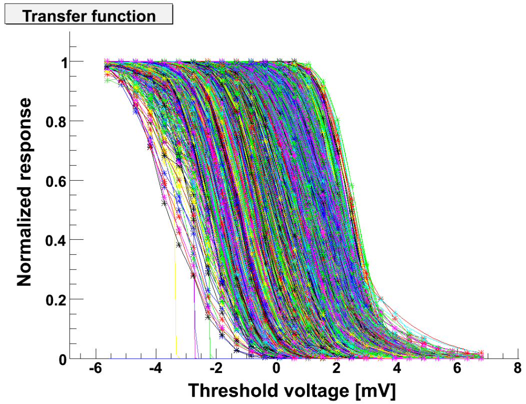




▷▷▷ Chip back from foundry $\Rrightarrow$ lab tests under way since early April :

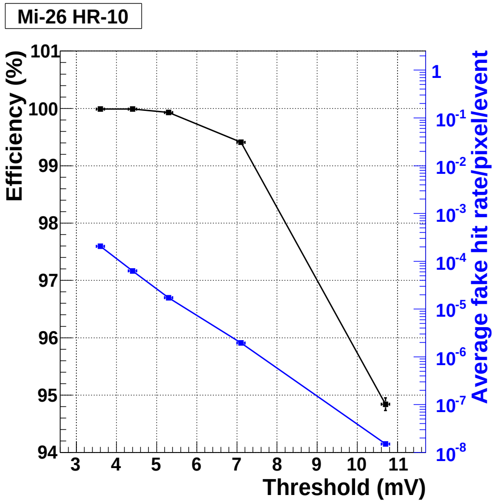
- ⋇ N $\lesssim$ 15 e$^-$ENC at 30-35°C (as MIMOSA-22AHR)
- ⋇ CCE (^{55}Fe) similar to MIMOSA-22AHR

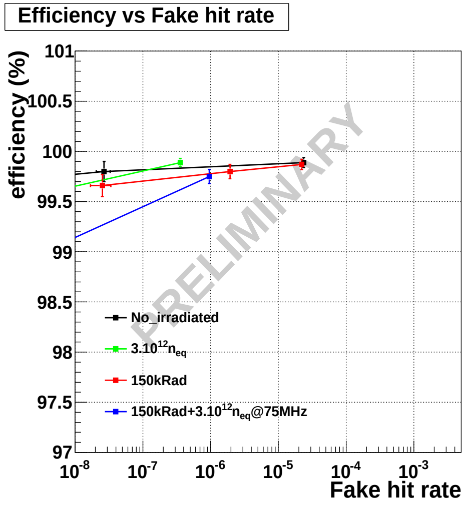
—○ **m.i.p. detection assessment at CERN-SPS in June-July ’11**



Expected M.I.P. Detection Performances of MIMOSA-28

- **Expected m.i.p. detection performances** determined with MIMOSA-26 and with medium size MIMOSA-22AHR prototype of ULTIMATE/M28 at SPS with $\sim$ 100 GeV π^- (Summer '10)





- **Detection efficiency vs fake hit rate :**

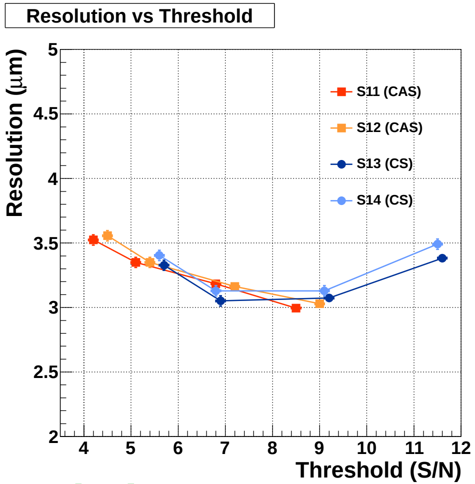
  sensor works with high detection efficiency and

  marginal contamination by noise fluctuations (fake hits)

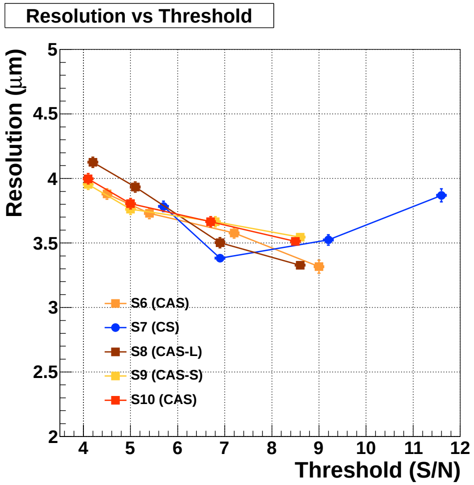
- **Single point resolution :**

  ※ 18.4 μm pitch (MIMOSA-26) $\rightarrowtail$ $\sigma_{sp} \sim 3\ \mu m$

  ※ 20.7 μm pitch (ULTIMATE) $\rightarrowtail$ $\sigma_{sp} \sim 3.5\ \mu m$



Pitch : 18.4 μm

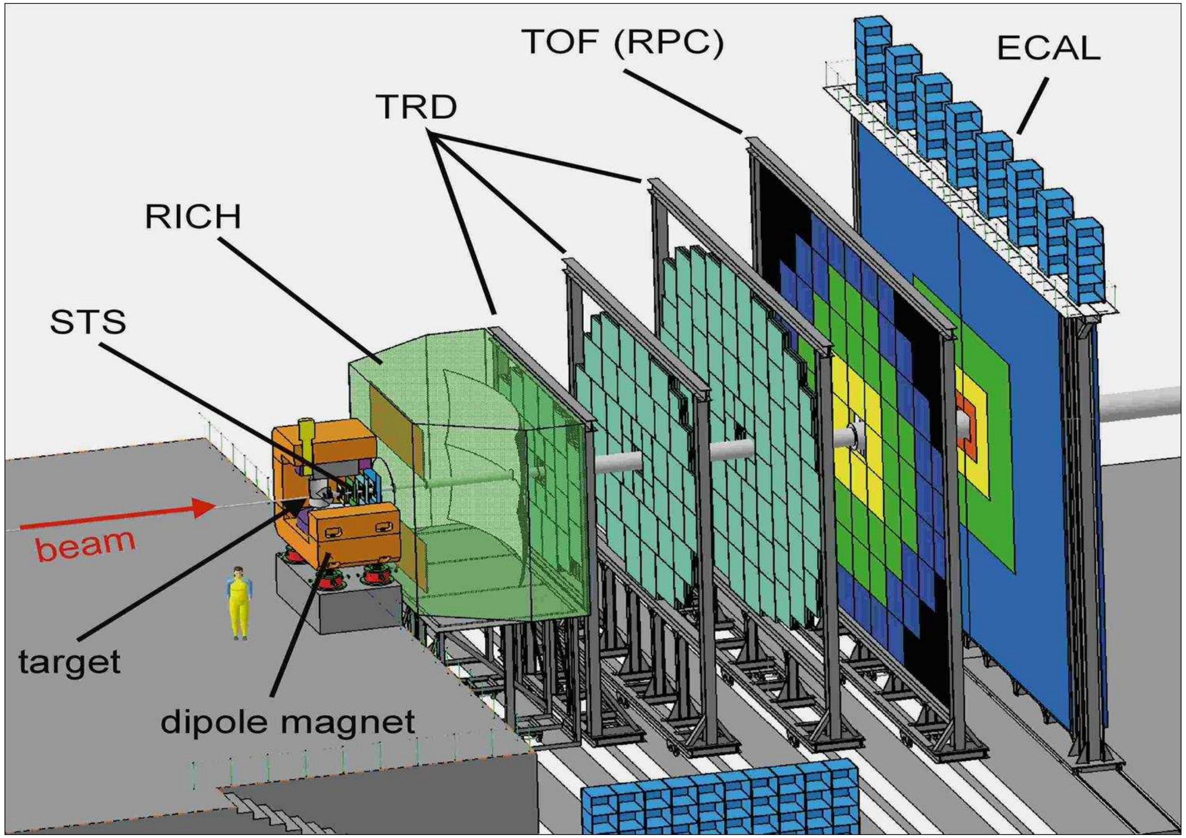


20.7 μm

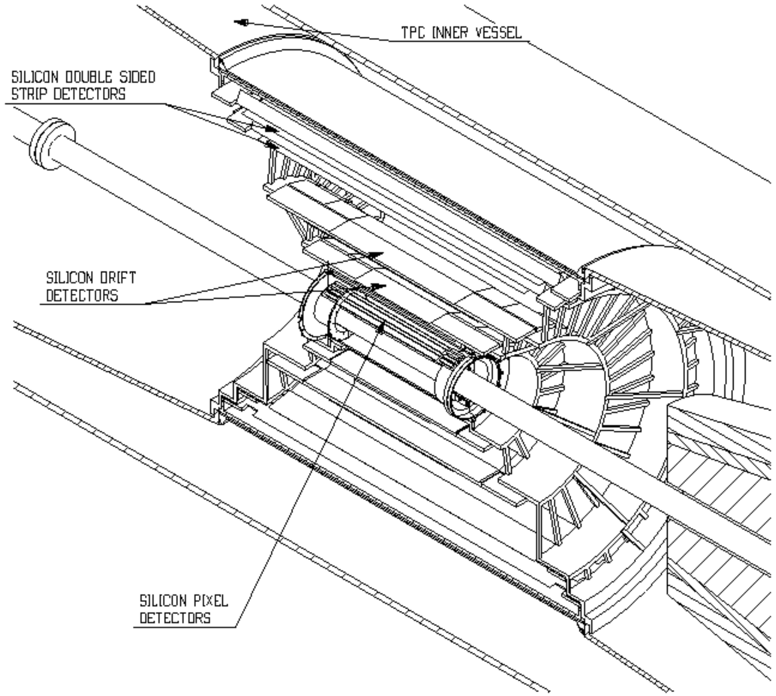
Application of CMOS Sensors to the CBM Experiment

- **Cold Baryonic Matter (CBM) experiment at FAIR:**
  - Micro-Vertex Detector (MVD) made of 2 of 3 stations located behind fixed target
  - double-sided stations equipped with CMOS pixel sensors)
  - **operation a negative temperature in vacuum**
  - each station accounts for $\lesssim$ 0.5 % X_0
  - sensor architecture close to ILC version

- **Most demanding requirements :**
  - ultimately ($\sim$ 2020): 3D sensors
    $\lesssim$ 10 μs, $>$ 10^{14}n$_{eq}$/cm^2, $\gtrsim$ 30 MRad
  - intermediate steps: 2D sensors
    $\lesssim$ 30-40 μs, $>$ 10^{13}n$_{eq}$/cm^2, $\gtrsim$ 3 MRad
  - 1st sensor for SIS-100 (data taking $\gtrsim$ 2016)

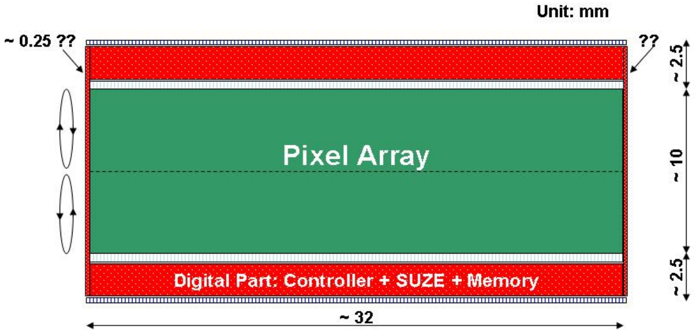


Upgrade of ALICE-ITS



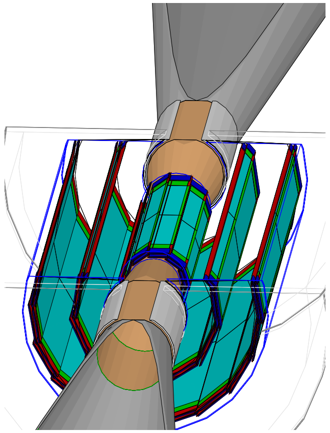
- **ITS upgrade :** envisionned for ”2016” LHC long shutdown
  - exploits space left by replacement of beam pipe
    with small radius (19 mm) section
  - consists (at least) in introducing L0
    $\equiv$ additionnal layer at $\lesssim$ 25 mm radius
    (potentially : replace part of the ITS)
  - 2 main pixel options considered :
    - ◇ Hybrid pixels with reduced material budget & pitch
    - ◇ CMOS pixel sensors derived from STAR-PXL (ULTIMATE/M-28)

- **Differences w.r.t. ULTIMATE/M-28 :**
  - $>$ 1 MRad & 10^{13}n$_{eq}$/cm^2 at T = 30°C (target values)
    $\hookrightarrow$ 0.18 μm triple-well HR-epi techno. (instead of 0.35 μm double-well hR-epi)
  - $\sim$ 1$\times$3 cm^2 large sensitive area (instead of 2$\times$2 cm^2)
  - double-sided read-out (instead of single-sided)
  - 1 or 2 output pairs at $\gtrsim$ 200 MHz (instead of 1 output pair at 160 MHz)
  - two $\lesssim$ 200 μm wide raw sequencers (instead of one 350 μm wide)
    - ▷ potentially : raw sequencers moved to bottom (requires $\sim$ 6 ML)
  - possibly: 2-sided ladder derived from PLUME ($<$ 0.5 % X$_0$) $\rightarrowtail$ see W.Dulinski’s talk

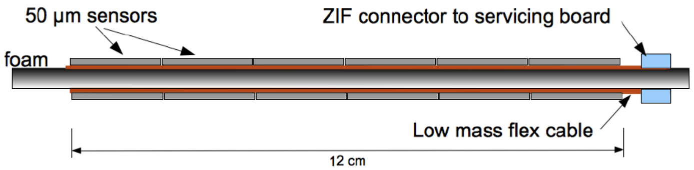


▷▷▷ **Technical Proposal due for 2011**

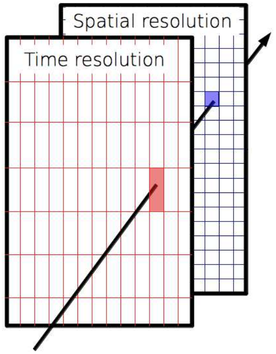
CMOS sensors for the ILD-VTX



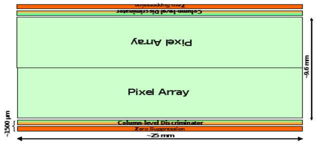
- **Two types of sensors :**
  - ⋇ Inner layers ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - $\hookrightarrow$ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - $\hookrightarrow$ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 5 μm
  - ⋇ Outer layers ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - $\hookrightarrow$ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - $\hookrightarrow$ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm

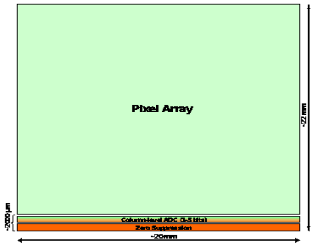


- **2-sided ladder concept for inner layer** (see W.Dulinski's talk) **:**
  - ⋇ square pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} < 3\ \mu m$)
    & elongated pixels (16×80 μm^2) on external ladder face ($t_{r.o.} \sim 10\ \mu s$)



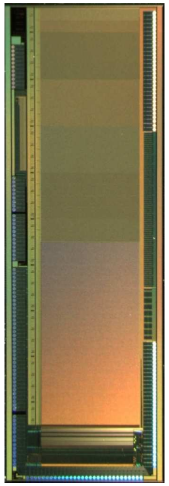
- **Sensor prototyping :** design under way
  - ⋇ MIMOSA-30: inner layer prototype with 2-sided read-out
    - $\hookrightarrow$ one side : 256 pixels (16×16 μm^2)
      other side : 64 pixels (16×64 μm^2)
  - ⋇ MIMOSA-31: outer layer prototype
    - $\hookrightarrow$ 48 col. of 64 pixels (35×35 μm^2) with 4-bit ADC

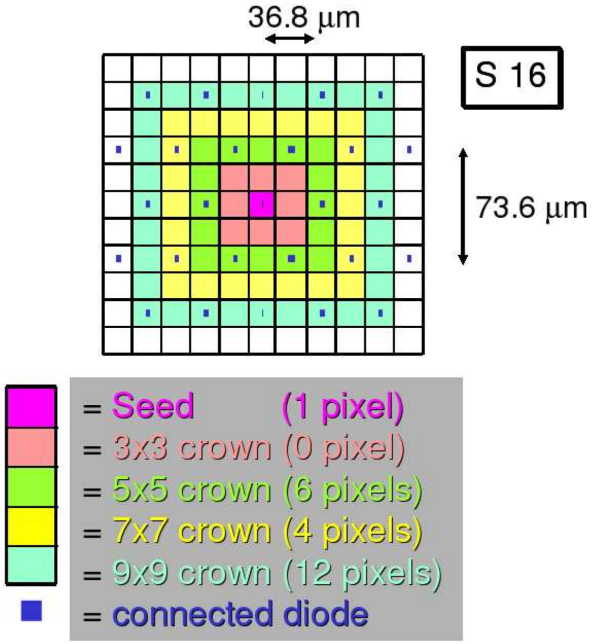




Towards a Large Pitch

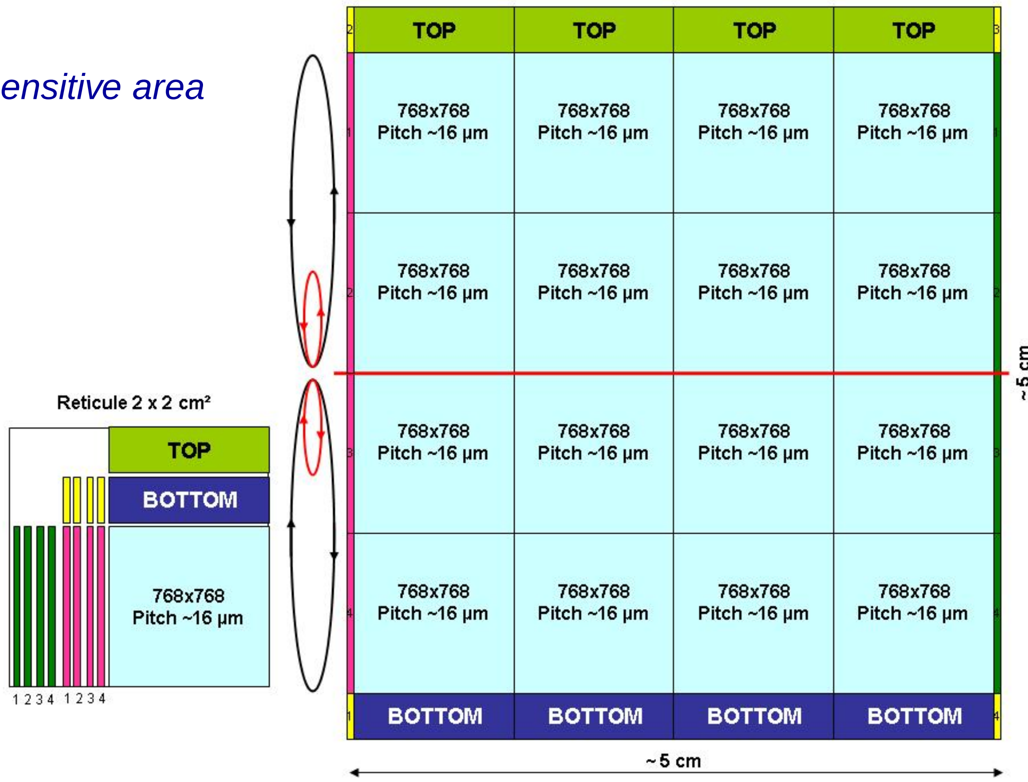
- **Large pitch : Motivations**
  - ⋇ trackers require $\sigma_{sp} \gtrsim 10\ \mu m$ ⋇ calorimeters require O(100×100) μm^2 cells
    - $\Rightarrow$ minimise number of pixels for the sake of power dissipation, integration time and data flow
- **Large pitch : Limitations**
  - ⋇ DANGER: increasing distance inbetween neighbouring diodes
    - $\Rightarrow$ particles traversing sensor ”far” from sensing diodes may not be detected because of e^- recombination
  - ⋇ ”fragile” detection efficiency, exposed to losses due to irradiation, high temperature operation & slow read-out
- **Elongated pixels : Test results**
  - ⋇ elongated pixels allow minimising the drawbacks of large pitch
  - ⋇ concept evaluated with MIMOSA-22AHR prototype, composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⋇ m.i.p. detection performances assessed at CERN-SPS (T $\sim$ 15°C)
    - —o $\epsilon_{det} \sim$ 99.8 %
    - —o $\sigma_{sp} \sim$ 5-6 μm (binary charge encoding)
- **Square pixels : prototype under fabrication**
  - ⋇ MIMOSA-29 being fabricated on high-res epitaxy
  - ⋇ pixels of $\leq$ 80×80 μm^2





Investigating Large Area Sensors

- **Prototype multireticule sensor for ”large” area detectors:**
  - ⋇ *2304/3072×2304/3072 pixels (22/16 μm pitch)* ⇛ *5×5 cm^2 sensitive area*
  - ⋇ *requires combining several reticules*
    - ⇛ *stitching process* ⇛ *establish proof of principle*
  - ⋇ *2-sided read-out of 1152/1536 rows in 200-300 μs*
    - ⇛ *Large Area Telescope for AIDA project*
      (EU-FP7 approved recently)
  - ⋇ *windowing of $\lesssim$ 1×5 cm^2 (collim. beam)*
    - ⇛ *$\lesssim$ 50–60 μs r.o. time*
  - ⋇ *50-100 μm pitch variants under consideration*
    - ⇛ *trackers & FW disks (e.g. VD for EIC)*



- **Submission expected in 2014:**
  - ⋇ bonus: avoid paving ”large” areas with reticule size sensors ⇛ dead zones, material, connectics/complexity
  - ⋇ synergy with tracker layers and forward disk projects on collider & fixed target experiments
  - ⋇ 3 sensors will compose a beam telescope at CERN (AIDA project deliverable)
    - ▷ few ns time stamping resolution associated to each hit by TLU (scintillator)

SUMMARY

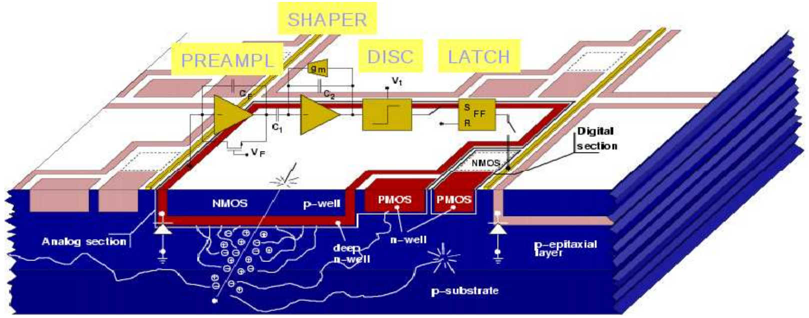
- **CMOS sensor technology continues extending its domins of applications :**
  - ⁜ well suited for specifications governed by granularity, material budget, power consumption, ... (large surfaces ?), ...
  - ⁜ excellent performance record with beam telescopes (e.g. EUDET project)
  - ⁜ 1st vertex detector experience will be gained with STAR-PXL, starting data taking in $\lesssim$ 2 years
    - ↪ well adapted running conditions: 30-35°C, 100 kRad, 10^{12}n$_{eq}$/cm^2, 200 μs

- **Next steps :**
  - ⁜ CBM-MVD : 2013/14 sensor with 40-50 μs r.o. time and several MRad $\oplus$ 10^{13} n$_{eq}$/cm^2
    - ↪ also considered as an option for the upgrade of ALICE-ITS $\Rrightarrow$ Techical Proposal for end ’11
  - ⁜ Large pitch : developments under way for trackers (e.g. external layers of inner trackers) and EM calorimetres (ALICE-FOCAL)
  - ⁜ Large sensors : 2013/14 ▷ 5×5 cm^2 sensors for forward disks (e.g. EIC vertex detector)
    - ↪ will also equip large area telescope of EU-AIDA project
  - ⁜ Faster 2D sensors (with in-pixel FEE) : $\geq$ 2015 ▷ 1-2 μs read-out time $\rightarrowtail$ SuperB fact. ?

- **Full potential of technology far from being exploited :**
  - ⁜ important 1st step (2011) : move to 0.18 μm feature size
  - ⁜ far future ($>$ 5 years) : multi-tier (3D) sensors using vertical integration

Perspectives: Fast 2D sensors

- **Evolve towards feature size $<<$ 0.35 μm :**
  - ⋇ μcircuits : smaller transistors, more Metal Layers, ... ⋇ sensing : triple well, depleted sensitive volume, ...
- **Benefits :**
  - ⋇ faster read-out $\Rrightarrow$ improved time resolution
  - ⋇ higher μcircuit density $\Rrightarrow$ higher data reduction capability
  - ⋇ thinner gates, depletion $\Rrightarrow$ improved radiation tolerance
- **On-going R&D (examples) :**
  - ⋇ *APSEL* sensor (130nm) for SuperB & ILC Vx Det. :
    - —○ in-pixel pre-amp + shaping + discri. ▷▷▷
    - —○ sensing through buried n-well
    - —○ shallow n-well hosting P-MOS T
  - ⋇ *LePIX* project (90 nm) for sLHC trackers :
    - —○ large pixels connected individually to peripheral FEE (fast !)
    - —○ high-resistivity substrate, high depletion voltage



- **Main limitations :**
  - ⋇ VDSM technologies not optimised for analog μcircuits (low V !) $\Rrightarrow$ reliability
  - ⋇ conflict between speed (e.g. 10 ns) and granularity (e.g. 20$\times$20 μm^2 pixels)

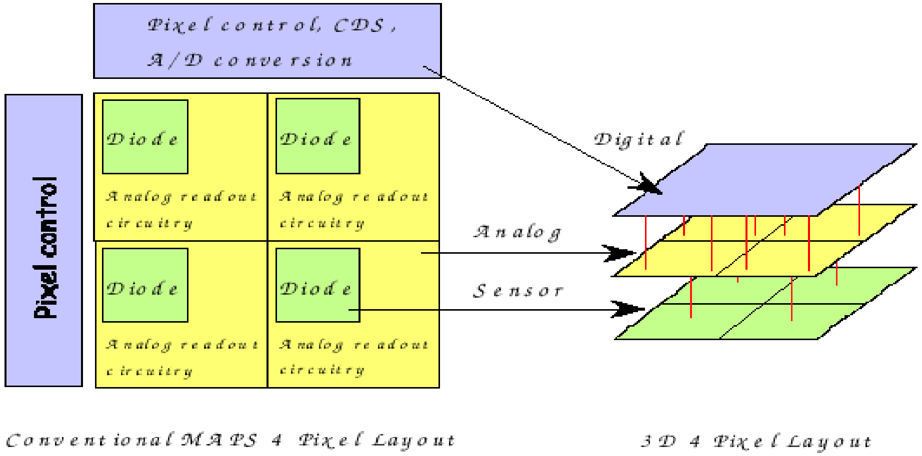
$\Rrightarrow$ **Natural trend : chip stacking**

Using 3DIT to reach Ultimate CMOS Sensor Performances

- 3D Integration Technologies allow integrating high density signal processing μcircuits inside **small** pixels by stacking ($\sim$ 10 μm) thin tiers interconnected at pixel level

- 3DIT are expected to be particularly beneficial for CMOS sensors :
  - ⋇ combine different fab. processes $\Rrightarrow$ chose best one for each tier/functionnality
  - ⋇ alleviate constraints on peripheral circuitry and on transistor type inside pixel, etc.

- Split signal collection and processing functionnalities :
  - ⋇ *Tier-1: charge sensing*
  - ⋇ *Tier-2: analog-mixed μcircuits*
  - ⋇ *Tier-3: digital μcircuits*



- **The path to nominal exploitation of CMOS pixel potential :**
  - ⋇ fully depleted 10-20 μm thick epitaxy $\Rrightarrow$ $\lesssim$ 5 ns collection time, rad. hardness $>$ Hybrid Pixel Sensors ???
  - ⋇ FEE with $\leq$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???

- **3DIC $\equiv$ consortium coordinated by FermiLab has already produced 1st generation of chips**

The Quadrature of the Vertex Detector