ADVANCED CMOS-BASED PIXEL SENSORS

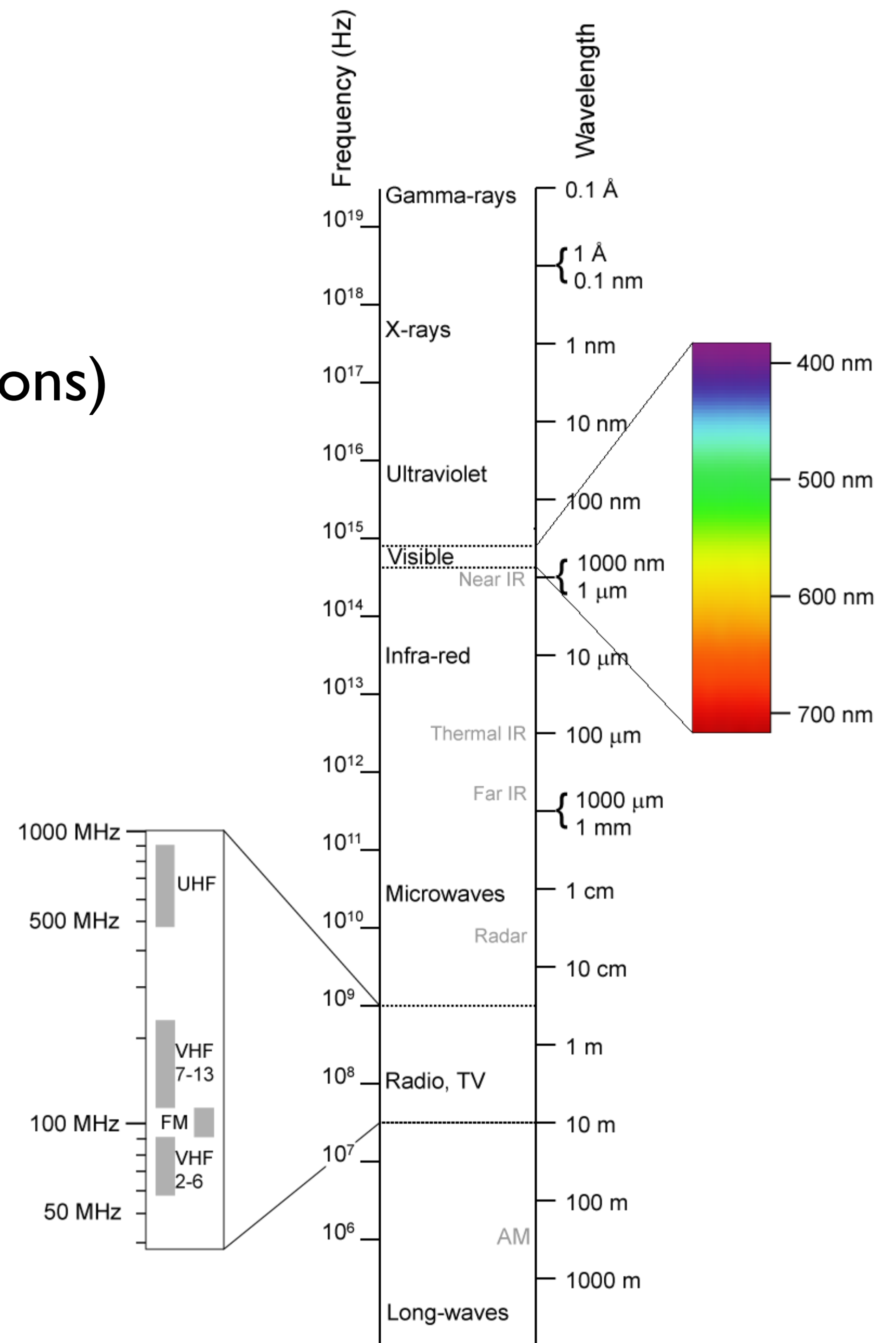
PIET DE MOOR

OUTLINE

- introduction: (Si) imagers
- design
- technology: CMOS + ...
- roadmap
- examples
- conclusion

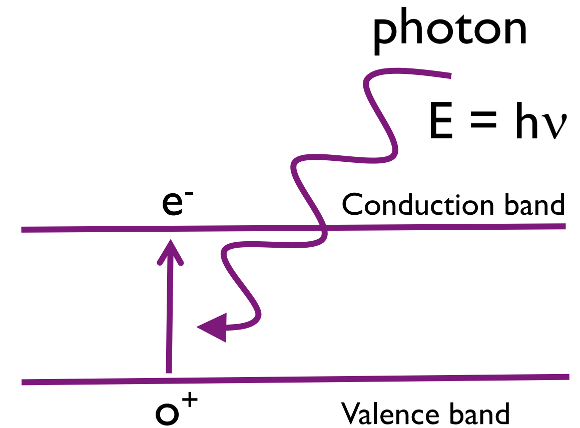
INTRODUCTION: IMAGER ?

- = detector, sensor for
  - electromagnetic radiation (photons)
  - particles
- visible spectrum:
  - consumer applications
  - CCD – 'vanilla' CMOS CIS
- other: high-end/scientific
  - CMOS + ...



SEMICONDUCTOR IMAGER BASICS

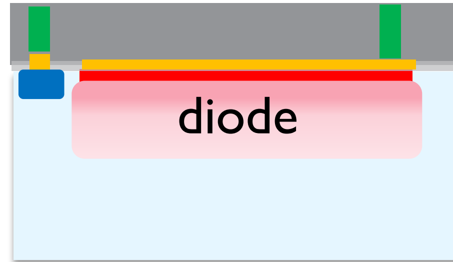
- detection in semiconductors:
  - photon absorption causes creation of electron-hole pair(s)
    - photon energy must be larger than bandgap
  - diode collects charges



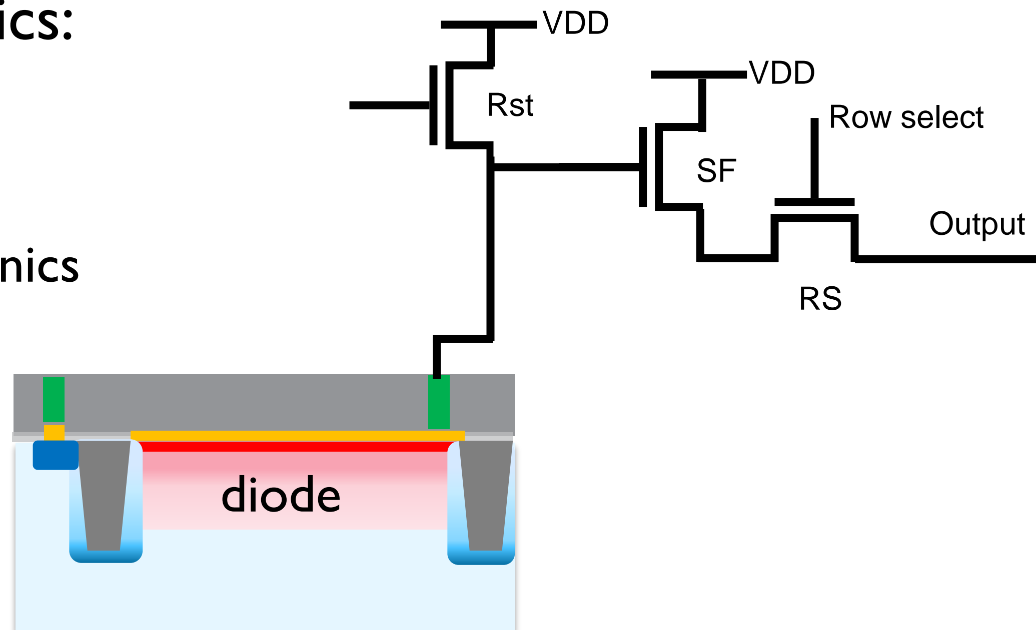
- **Si** has a combination of unique properties:
  - right bandgap to detect visible light
  - absorption of visible light in a few micron thickness
  - the best/most practical semiconductor material for integrated circuits

IMAGER PIXEL

- passive pixel:
  - single photodiode

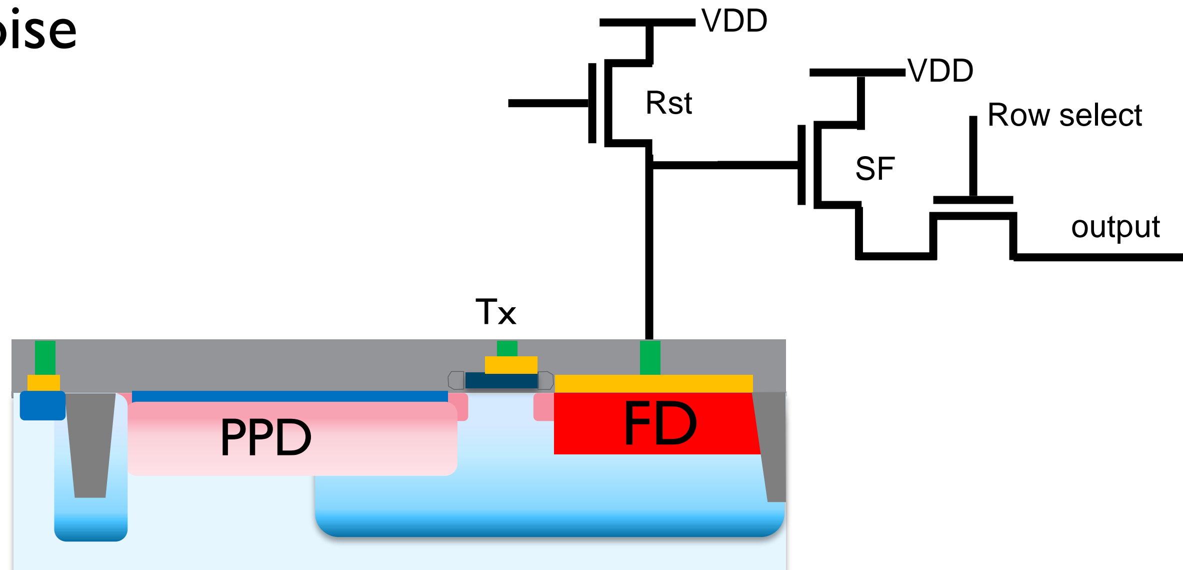


- active pixel:
  - photodiode
  - connected to pixel electronics:
    - source follower (SF): '3T pixel'
    - CTIA
    - additional analog/digital electronics



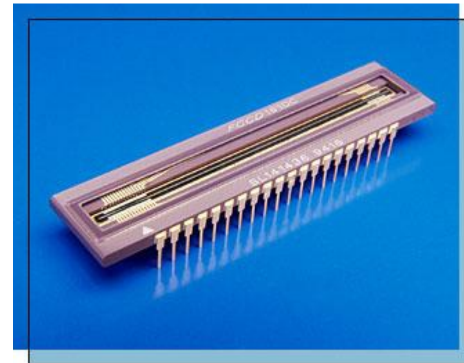
IMAGER PIXEL

- active pixel: 4 T(transistor) pixel:
  - = 3T pixel connected to a floating diffusion node (FD)
  - extra transfer gate (Tx) between photodiode and FD node
  - 'pinned' photodiode
- advantages:
  - lower dark (leakage) current
  - lower noise

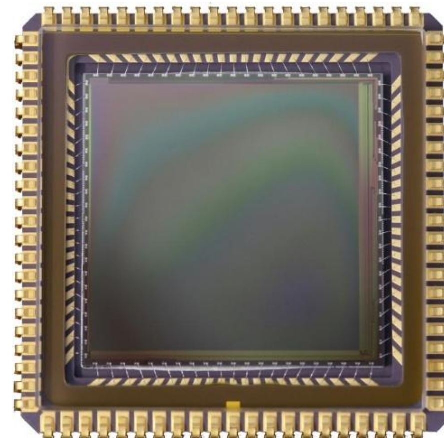


SI BASED IMAGER BASICS

- readout of many pixels requires **microelectronics fabrication technology**:
  - dedicated imager technology: **Charge Coupled Device (CCD)** – Nobel Prize 2009
    - excellent optical properties

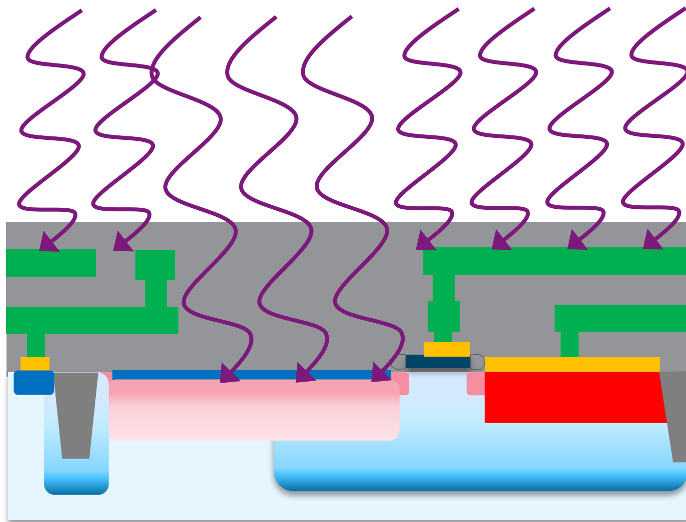


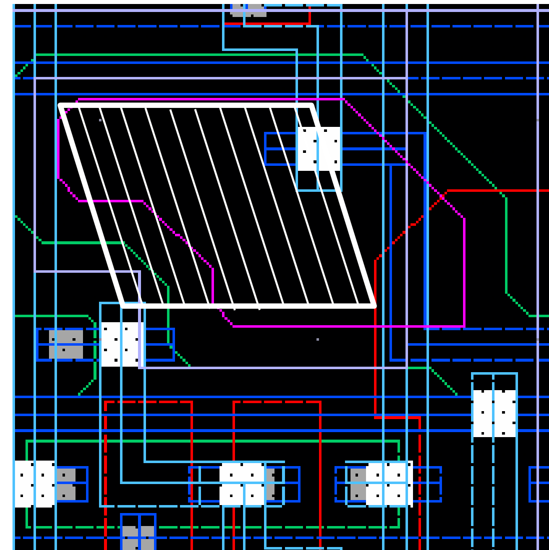
  - **CMOS image sensors (CIS):**
    - advantages of CMOS scaling:
    - integration of electronics, low power, ...



IMAGER PARAMETERS: FILL FACTOR

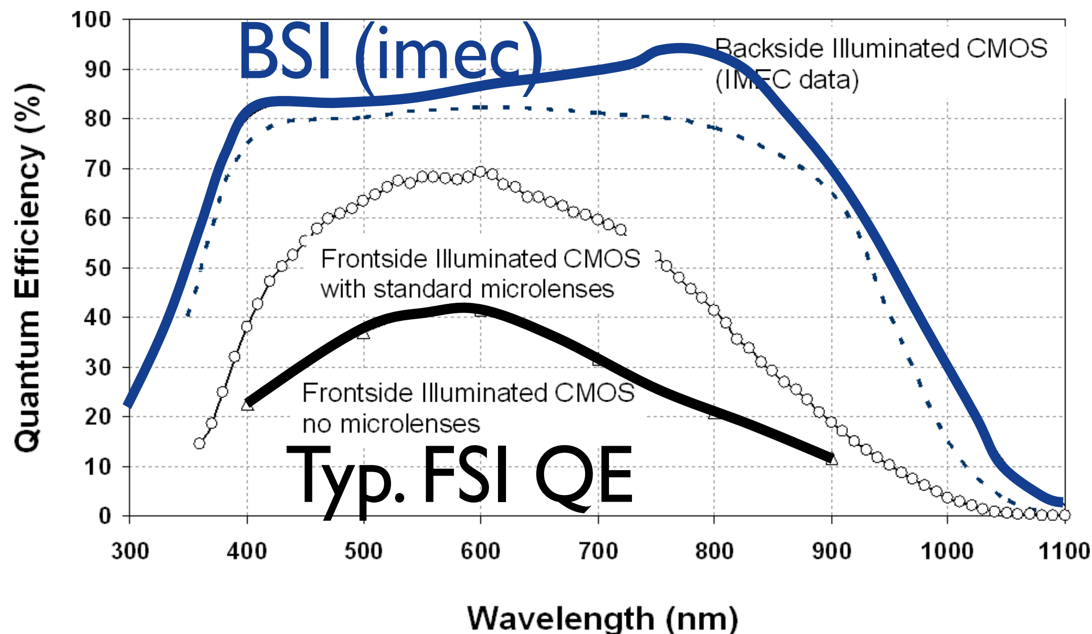
- = relative area of the pixel that is **sensitive**
- reasons:
  - shielding/reflection of light/paritcles by metal interconnects
  - size of the diode vs. pixel transistors





IMAGER PARAMETERS: QUANTUM EFFICIENCY (QE)

- **= intrinsic sensitivity**
- = number of collected charges per incoming photon/particle
  - particle/energy/wavelength dependent
- typical numbers :
  - technology dependent



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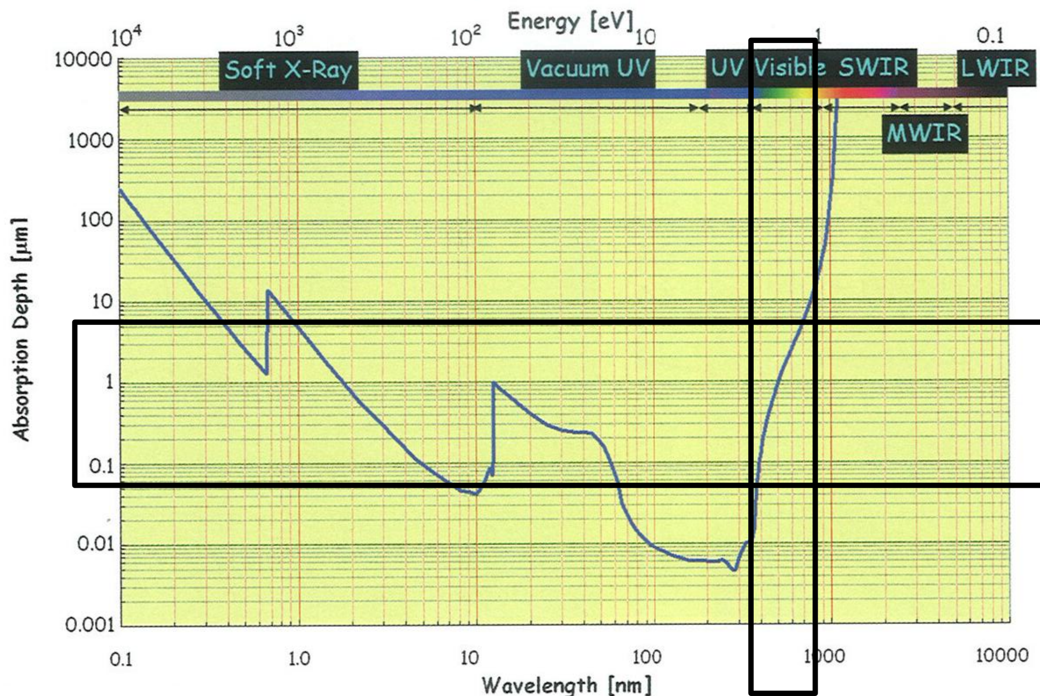
ABSORPTION

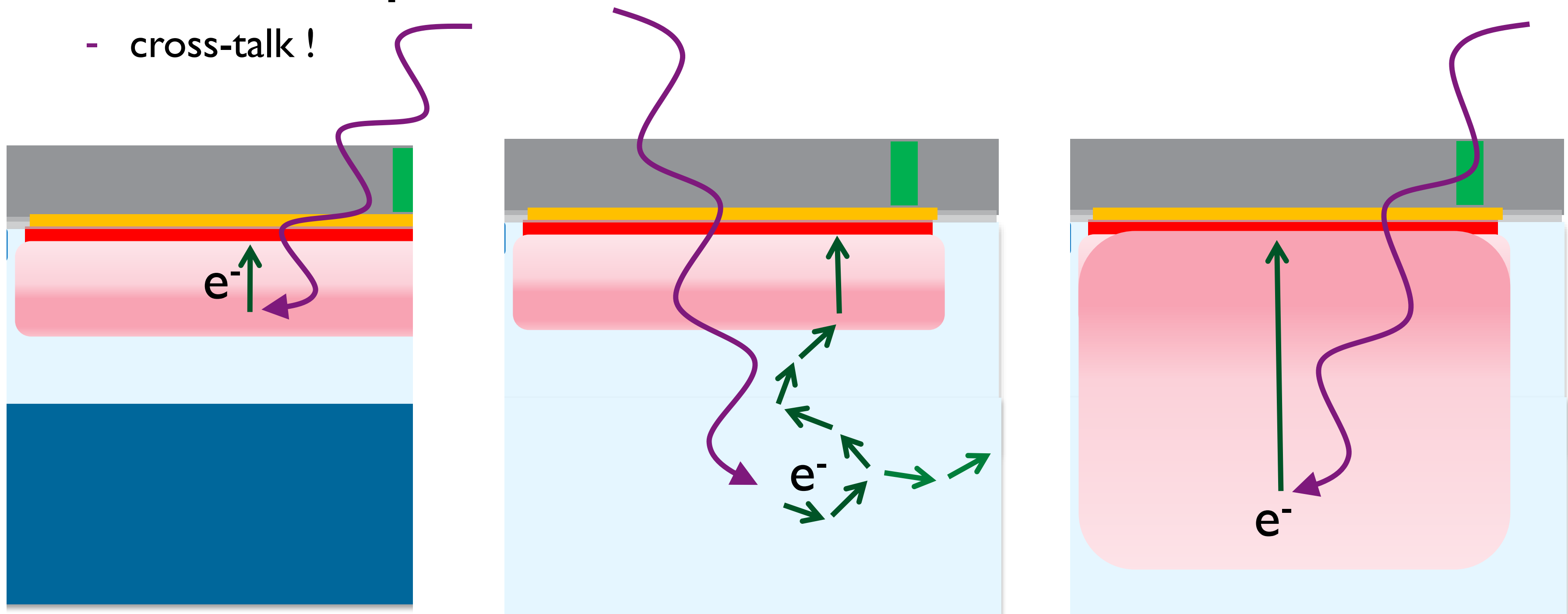
- penetration depth is dependent on:
  - wavelength (photons)
  - particle type & energy
- examples:



Type of radiation	Penetration depth	Challenge ?
visible light, soft X-rays	few micron	easy
near UV, low E electrons, molecules	few nanometers	difficult: surface passivation
high energy photons, particles	(much) larger than 10 um	difficult: large collection depth

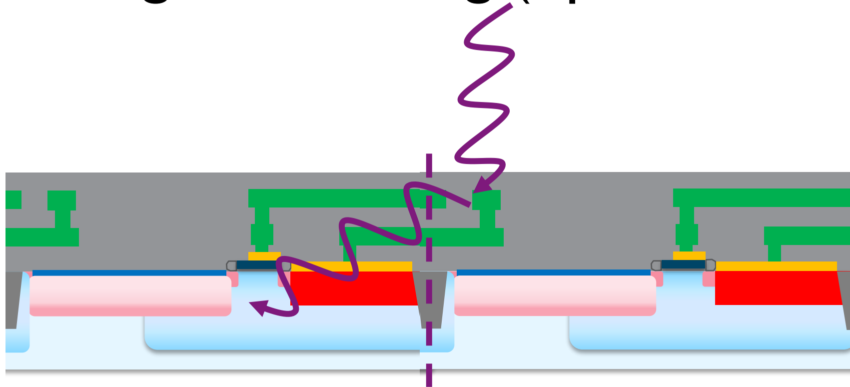
CHARGE COLLECTION

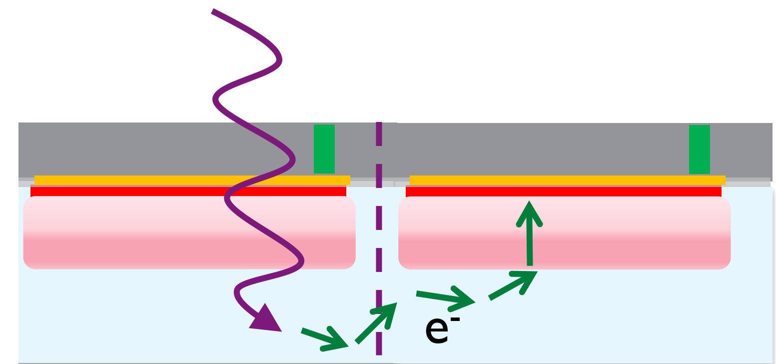
- requires low dopant (= high resistive) Si part:
  - epi layer on bulk (highly doped) Si
  - high resistivity substrates
- mechanism:
  - electric field/depletion: **directional**
  - diffusion: **isotrope**
    - cross-talk !



IMAGER PARAMETERS:
CROSS-TALK

- = light/particle incoming in a pixel, charges collected in other pixel
- reasons:
  - light scattering (optical cross-talk) and/or charge diffusion





- impact:
  - loss of effective resolution
- quantitative:
  - Modulation Transfer Function: MTF

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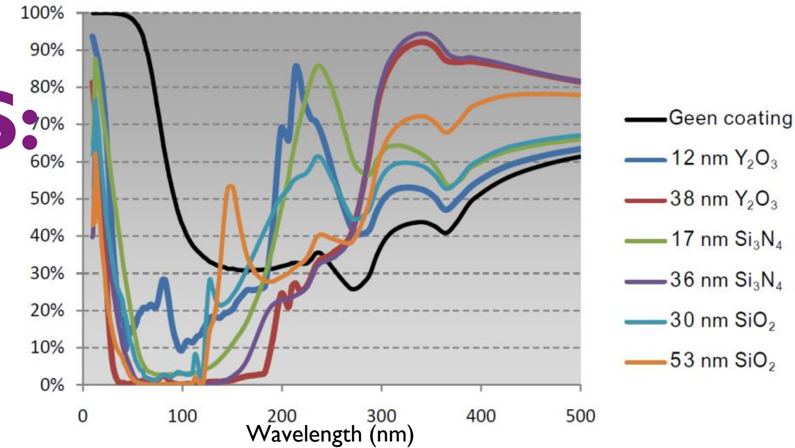
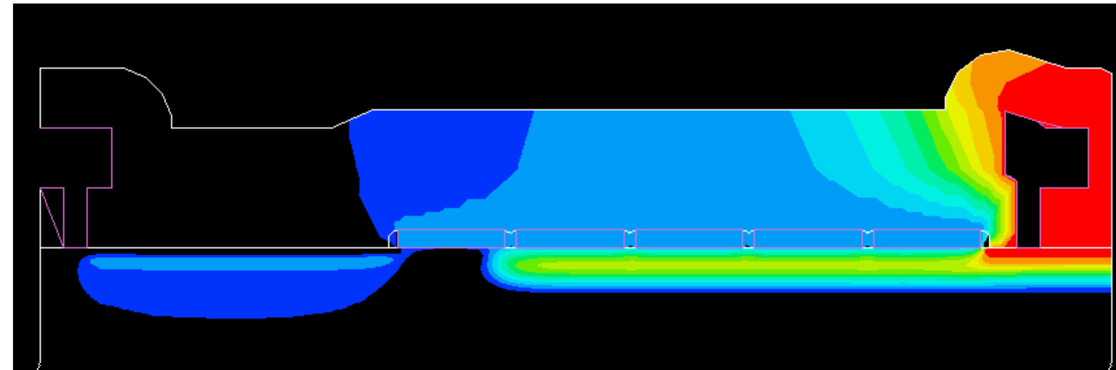
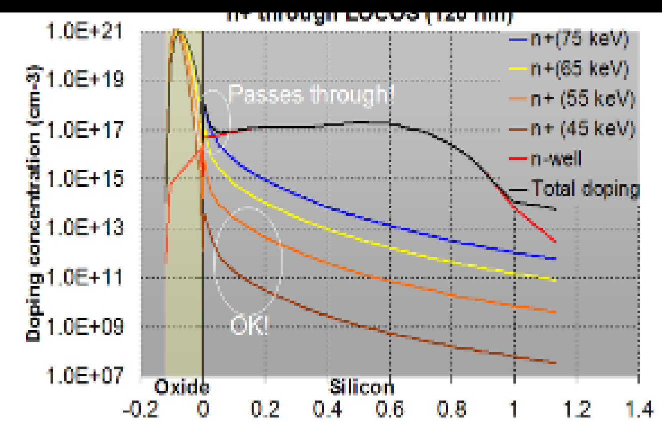
DESIGN COMPETENCES:
DEVICE SIMULATION



- 'optical':
  - reflection/transmission/absorption
- electrical:
  - electric field
  - charge transport
  - depletion



- process:
  - implantation and anneal conditions
- tools:
  - Sentaurus, Medici, Tsuprem, Matlab



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200 MM FLEXIBLE 0.13 UM PLATFORM

- pixel
  - pinned Photodiode: option (in development)
  - CCD in CMOS option (in development)
  - dual gate process, 3.3V/1.2 V operation
- analog & I/O
  - MIM capacitor
  - high precision resistor
- digital:
  - low Operating Power (LOP) optimized transistor
  - low Vdd operation
- outsourcing of color filters & micro lenses

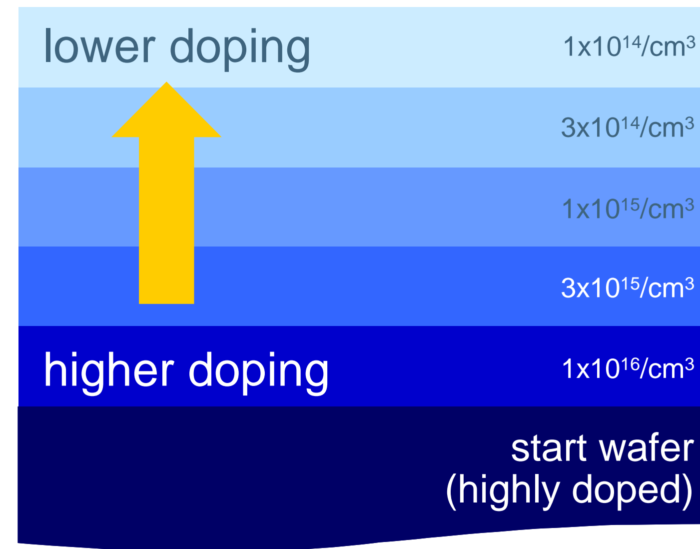
+ flexibility to non-standard processing

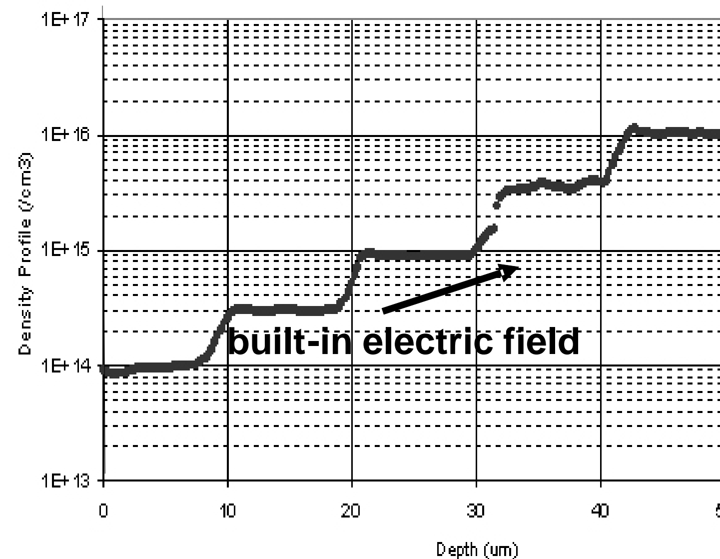
FLEXIBLE 0.13 UM PLATFORM:
SPECIAL SUBSTRATES

- epitaxial layers:
  - thick:
    - up to 50 um demonstrated

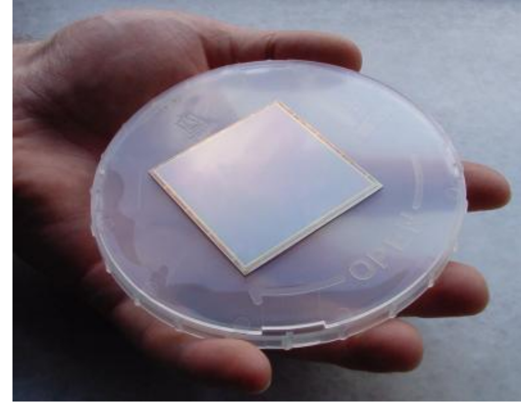
      for enhanced red response
  - graded dopant concentration
    - for directional carrier transport

      = lower cross-talk
- high resistivity substrates:
  - both n and p-type
  - resistivity > 1kOhm.cm
  - solution for chucking in imec fab



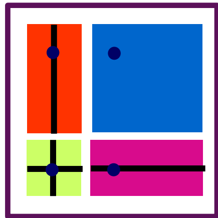


FLEXIBLE 0.13 UM PLATFORM: STITCHING

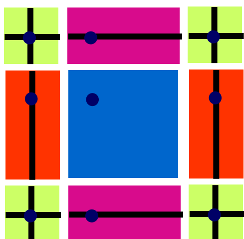


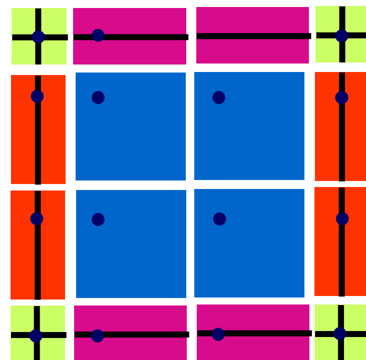
- stitching allows large area imagers:
  - up to 1 imager per wafer
- different imager sizes on one wafer demonstrated:
  - 12×12 mm^2, 25×25 mm^2 and 50×50 mm^2
- application: e.g. large area X-ray

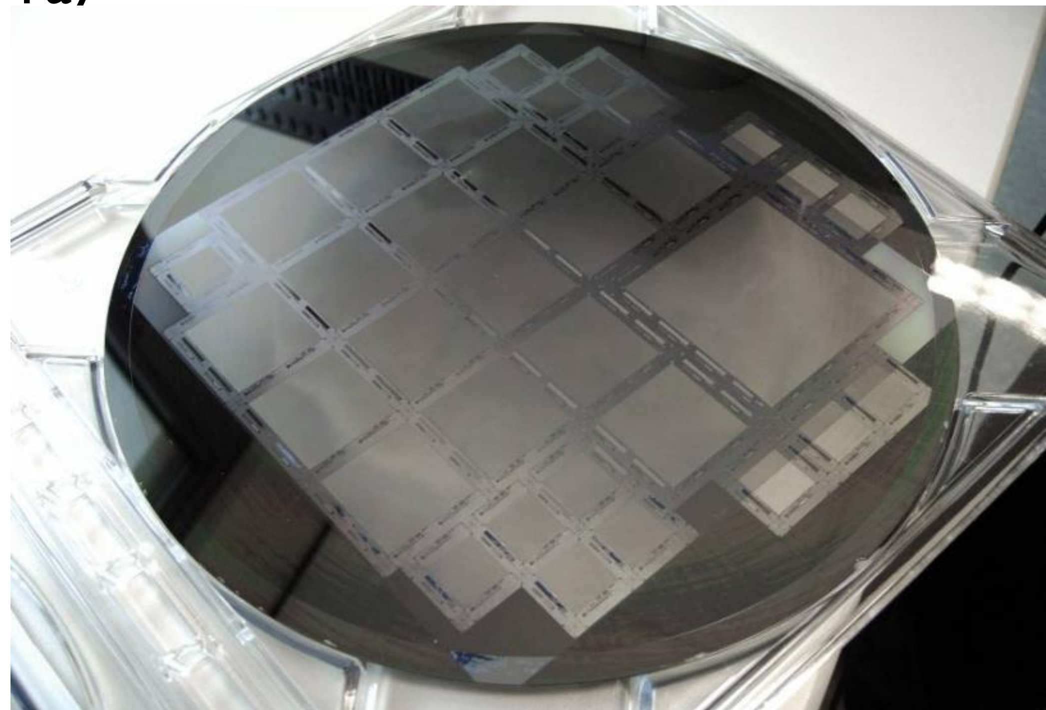
on reticle



on wafer







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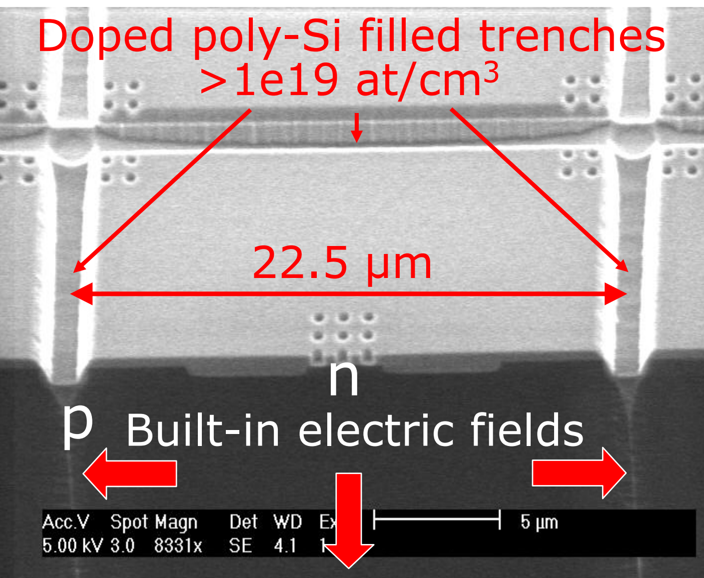
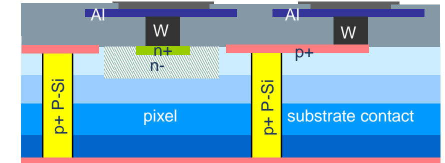
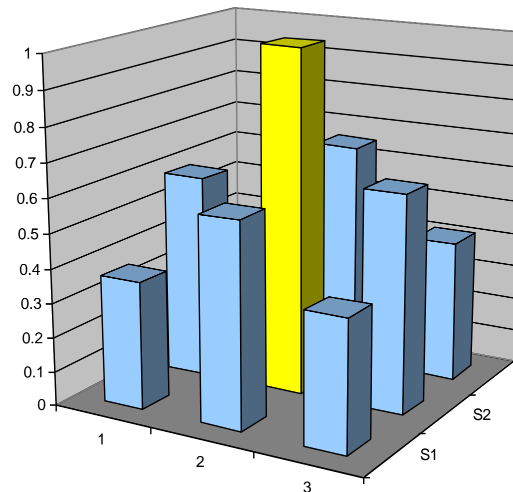
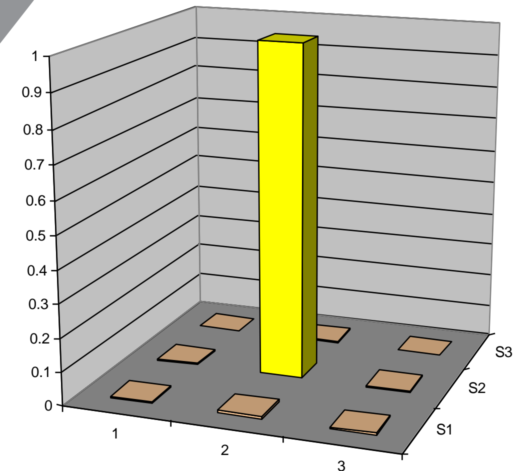
FLEXIBLE 0.13 UM PLATFORM: TRENCHES FOR ZERO CROSS-TALK

- poly-Si doped trenches separating pixels:
  - advantage: no cross-talk
- demonstrated using laser point source
- impact on (blue) QE





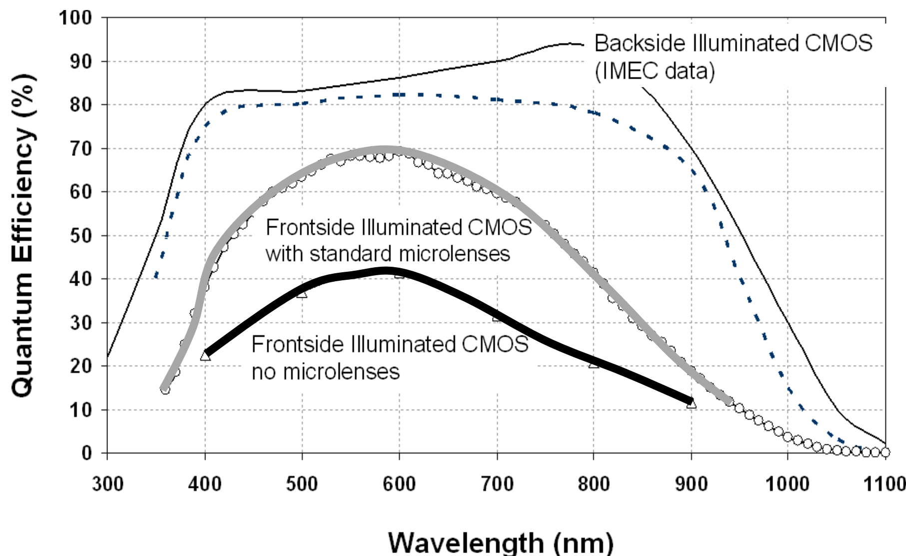




FLEXIBLE 0.13 UM PLATFORM: FRONTSIDE ILLUMINATED IMAGERS

- limited fill factor:
  - caused by metal interconnects
  - enhancements using micro-lenses
- limited QE:
  - absorption in BEOL dielectrics

- standard CMOS process



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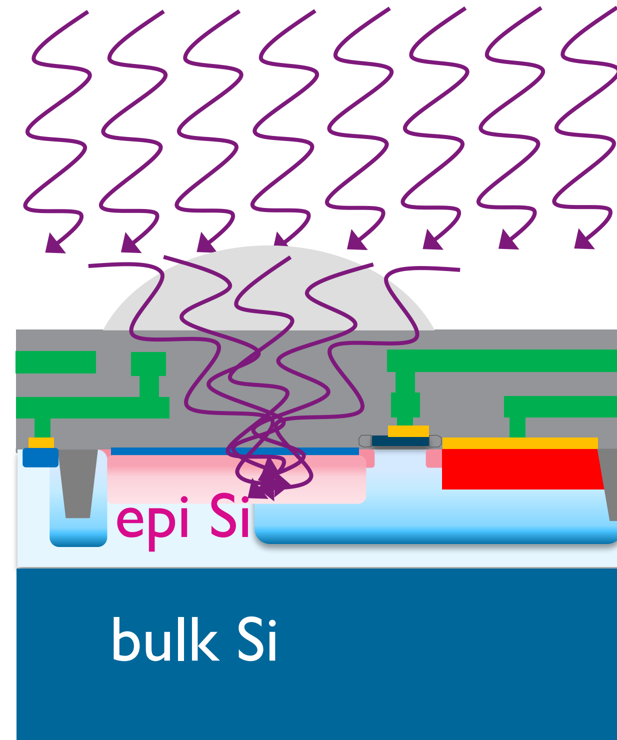

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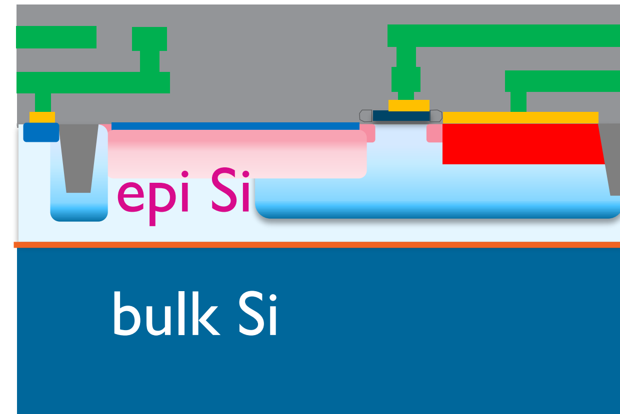
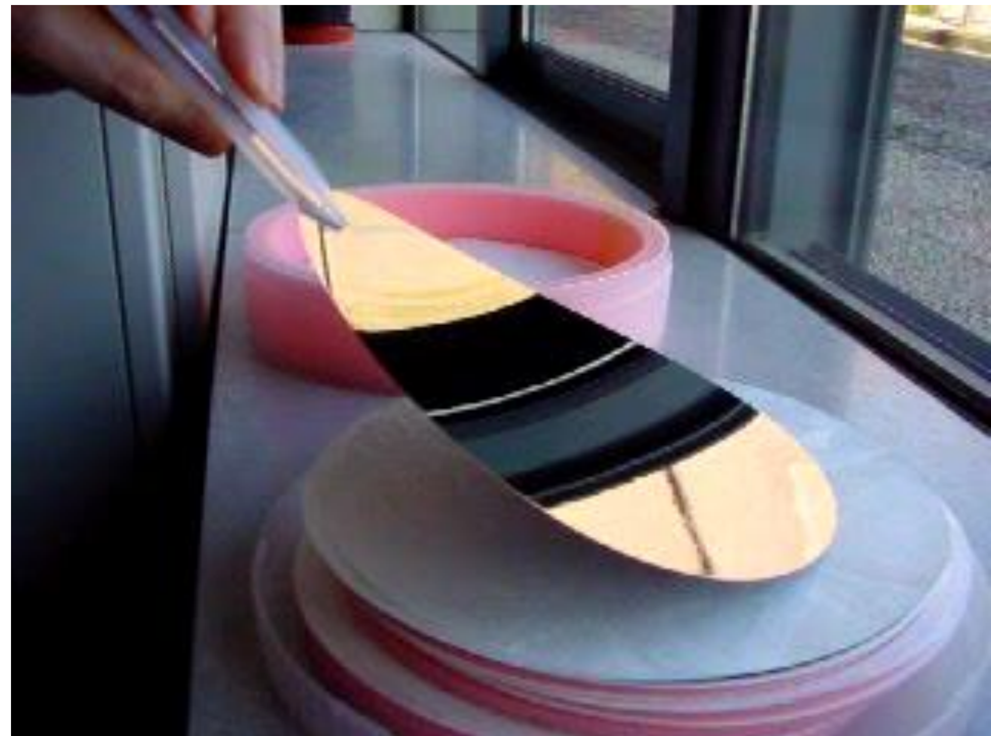
FLEXIBLE 0.13 UM PLATFORM: THINNING

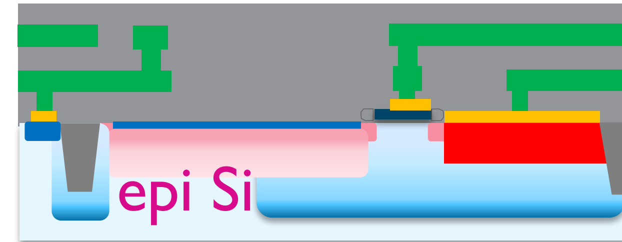
- solution:
  - backside thinning
- technology:
  - course + fine grinding
- challenges:
  - wafer handling:
    - use of carrier wafers and temporary wafer (de-)bonding technology
  - thinning damage, impact on devices:
    - damage removal
    - backside passivation: implant + laser annealing

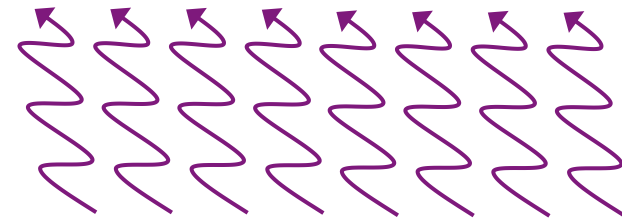


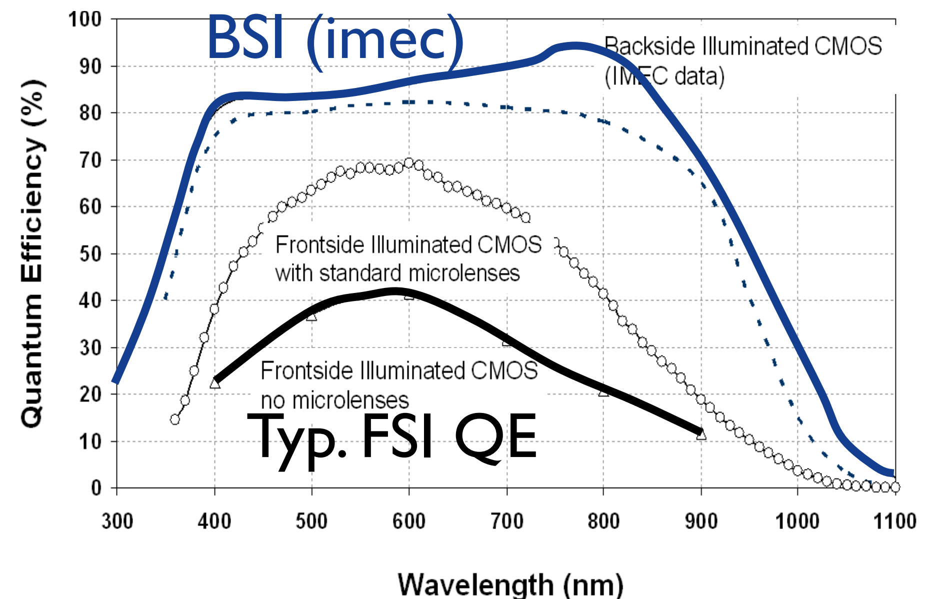


FLEXIBLE 0.13 UM PLATFORM: BACKSIDE ILLUMINATED IMAGERS

- 100% fill factor: no metal interconnects
- maximal QE:
  - no BEOL dielectric absorption
  - broader wavelength range (i.e. in near UV)
- enables the detection of particles with very shallow penetration in Si:
  - low energy electrons
- enables very thin detectors with minimal particle scattering:
  - tracking detectors







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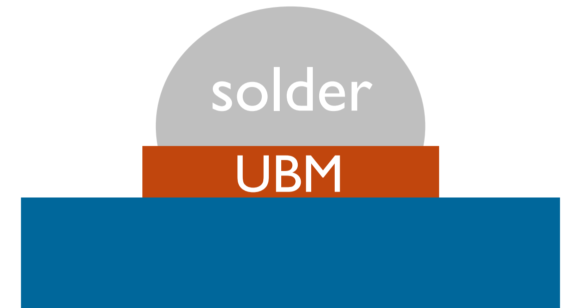
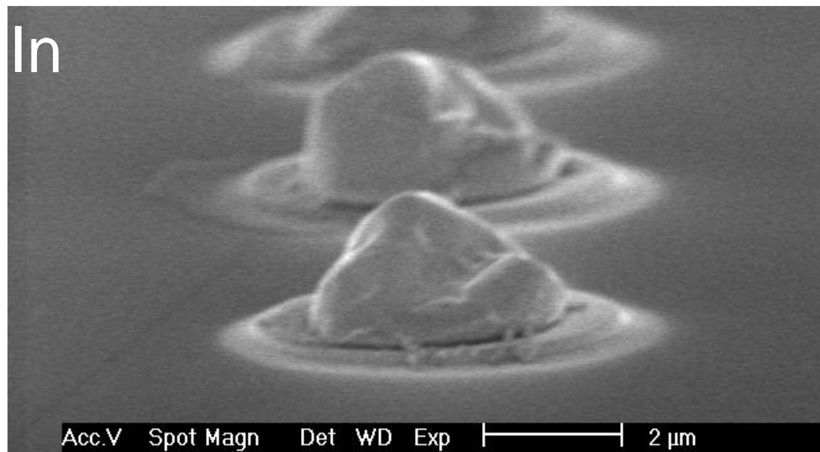
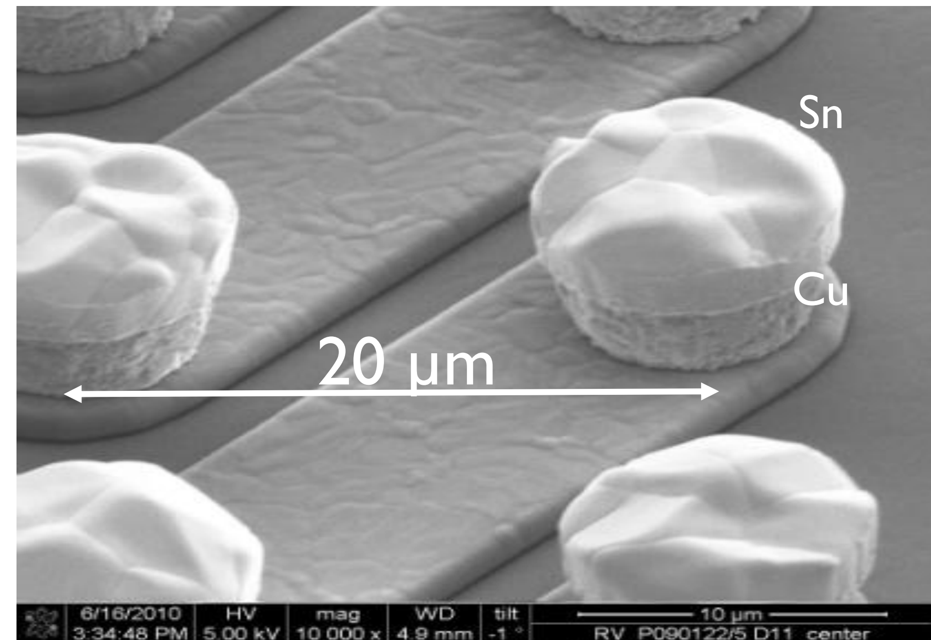
FLEXIBLE 0.13 UM PLATFORM: HIGH DENSITY BUMPING

- In and CuSn microbumps:
  - post-process at wafer level for both sides:
    - under-bump metallization (UBM) & patterning
    - solder deposition & patterning
  - smallest pitch:
    - 20 um
    - 10 um under development

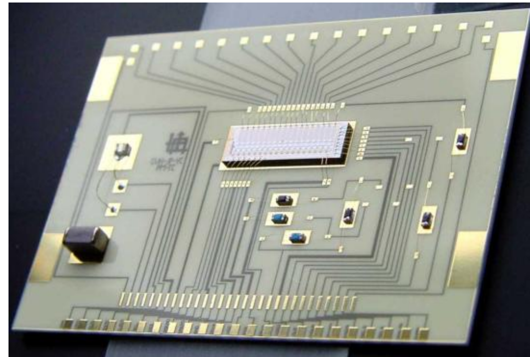
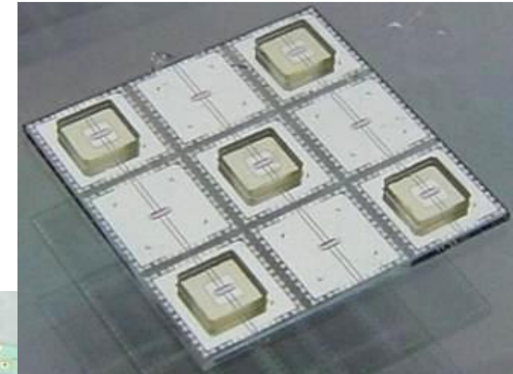
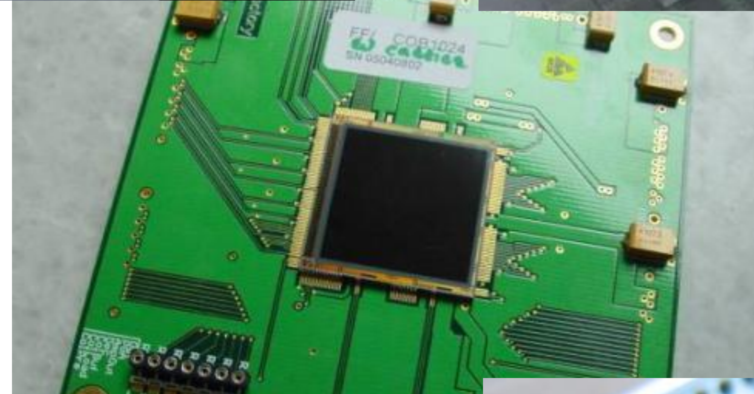
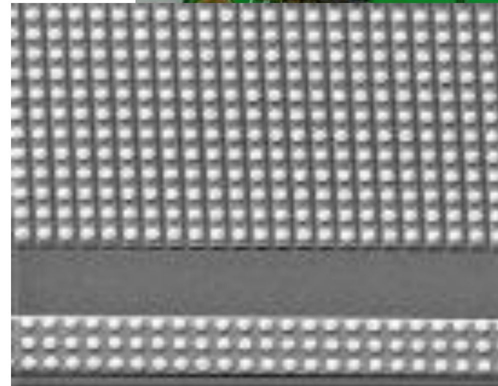
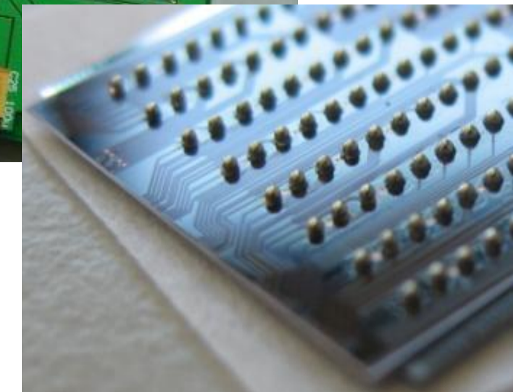






ADVANCED ASSEMBLY AND PACKAGING

- dicing
- wire bonding
- die attach
- bump placement:
  - Au stud ball bumping
  - solder bumping
- flip-chip:
  - high density bump assembly
  - glass capping
- underfill
- pick and place
- PCB/ceramic boards

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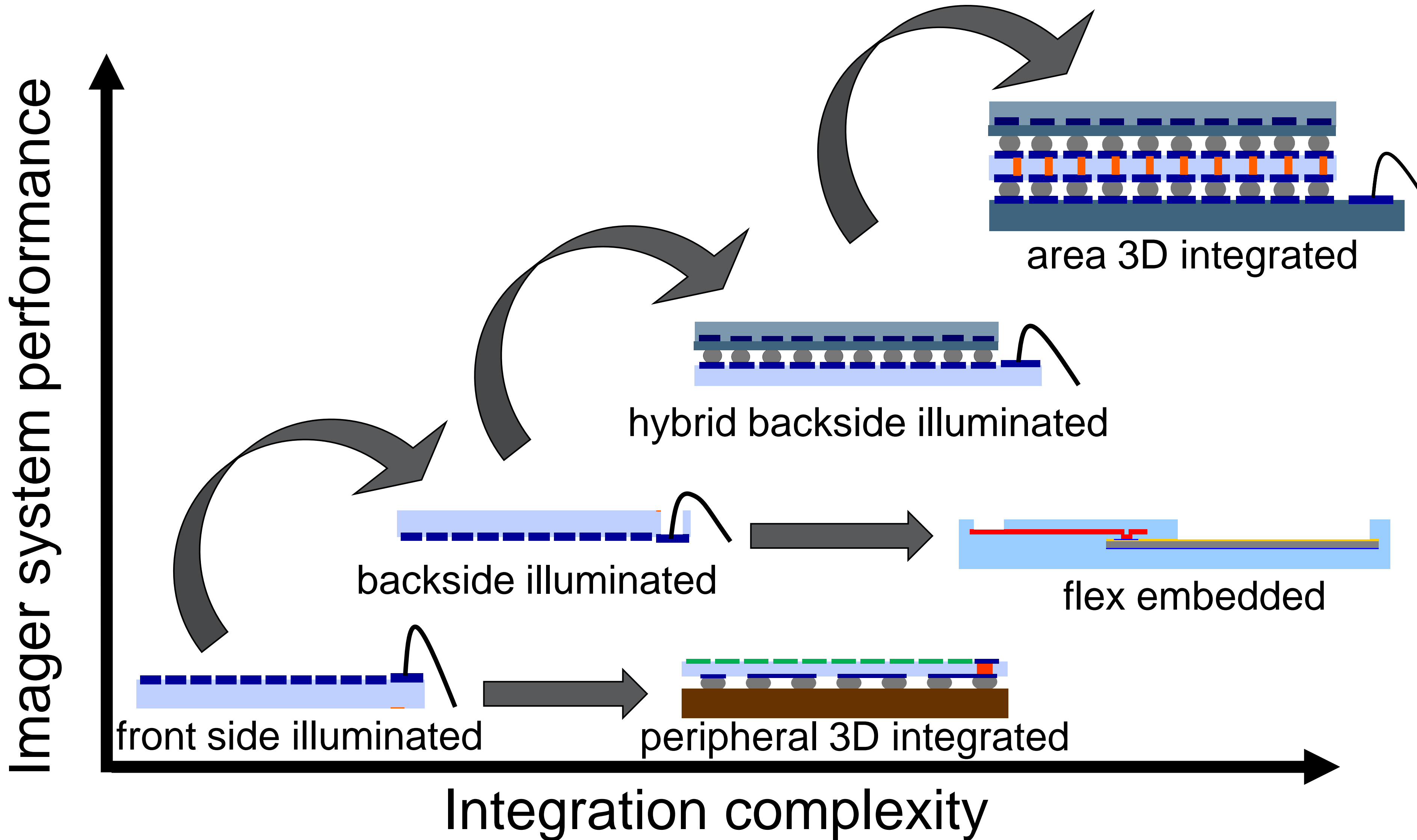
3D INTEGRATED IMAGERS ROADMAP



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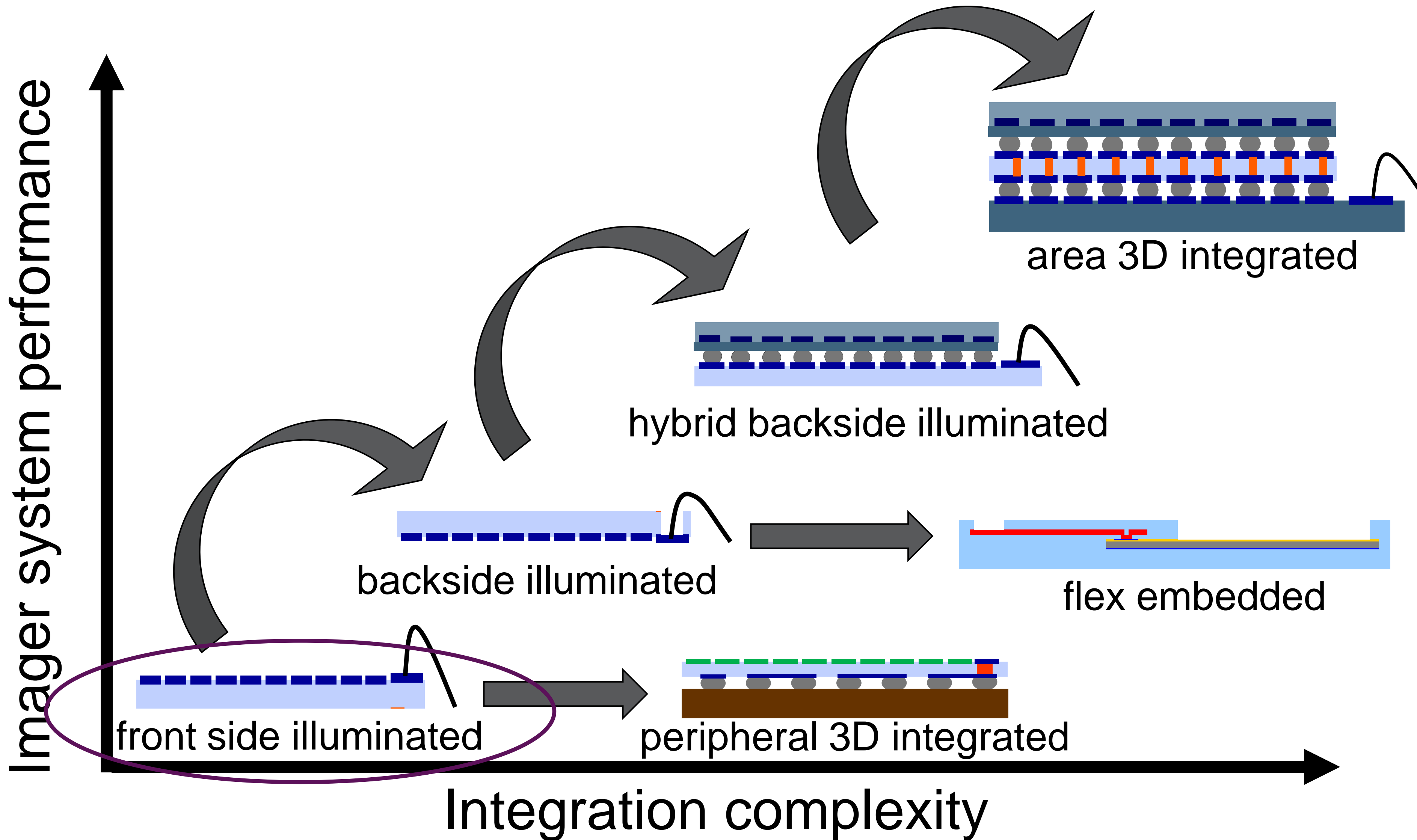
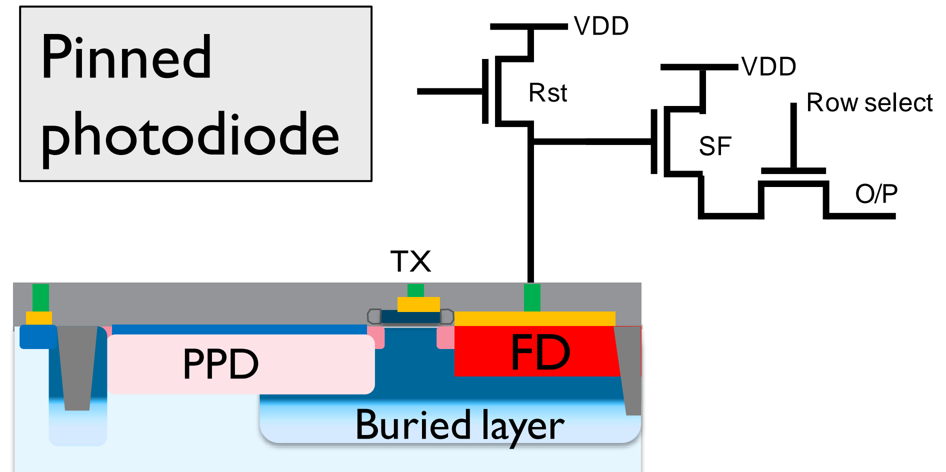
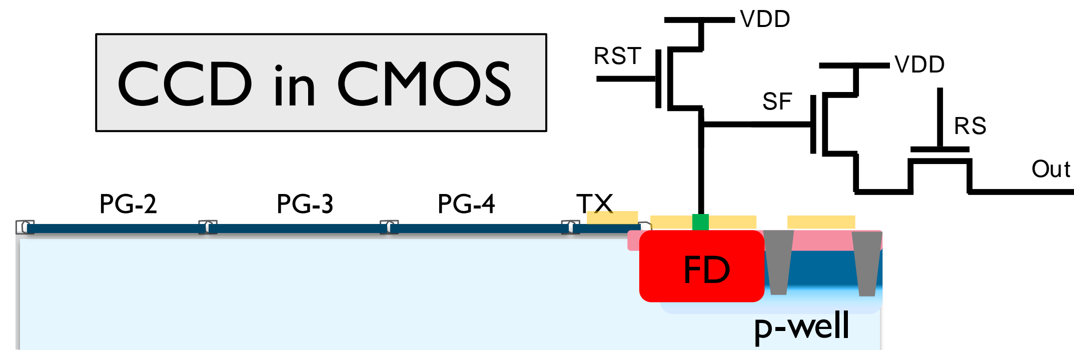


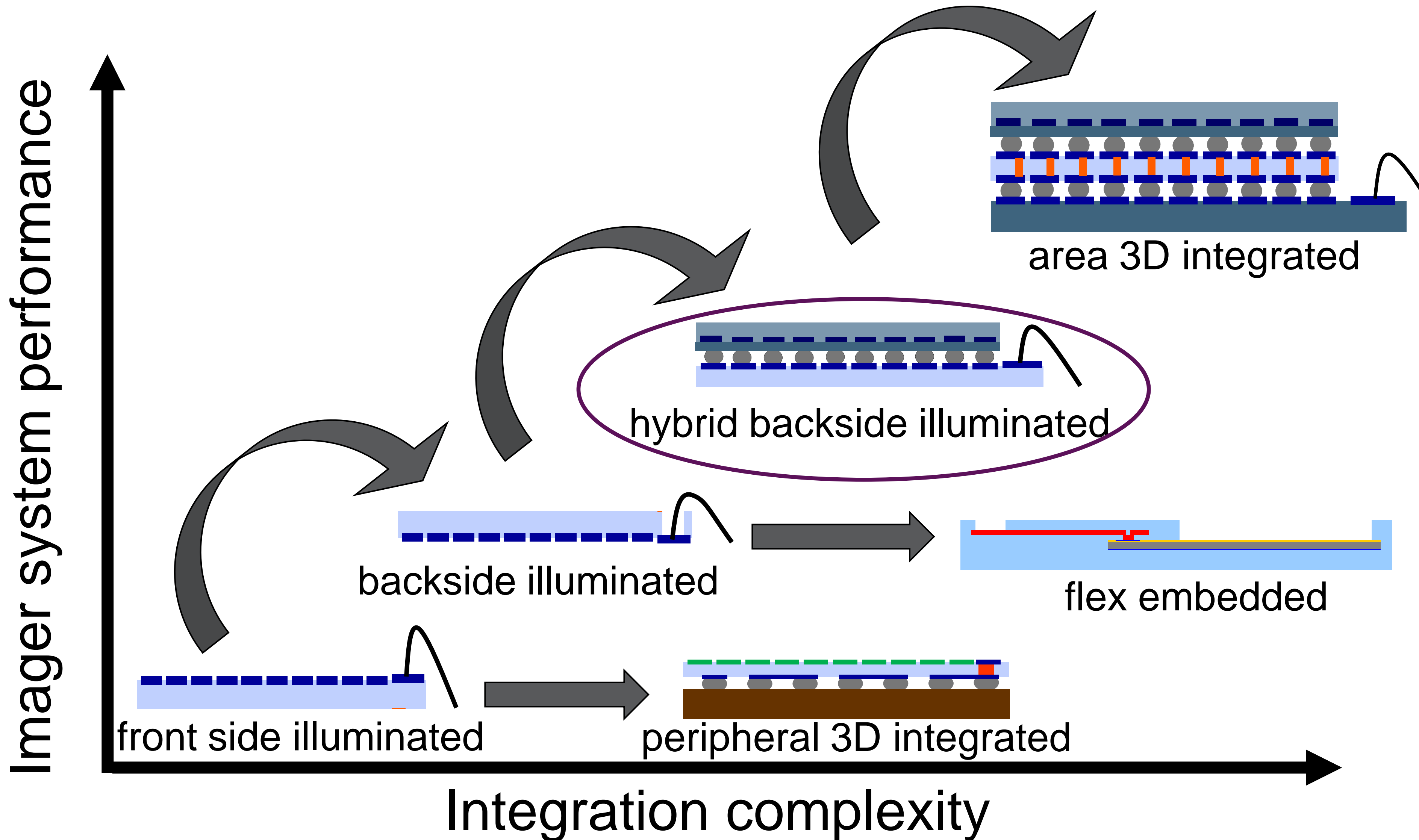
IMEC 0.13 UM CMOS CMOS IMAGERS

- CIS test chip:
  - 4T pixel with pinned photodiode
  - shared FD node
  - yield optimization
- eCCD:
  - CCD pixel structure embedded in CMOS
  - best of 2 worlds:
    - CCD operation of pixels, in charge domain
    - flexible CMOS read-out electronics



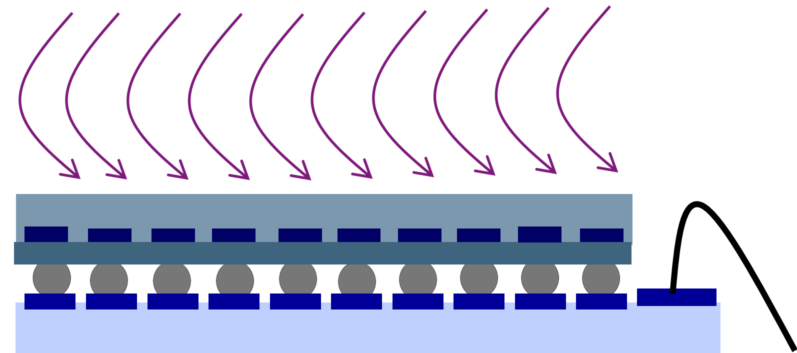


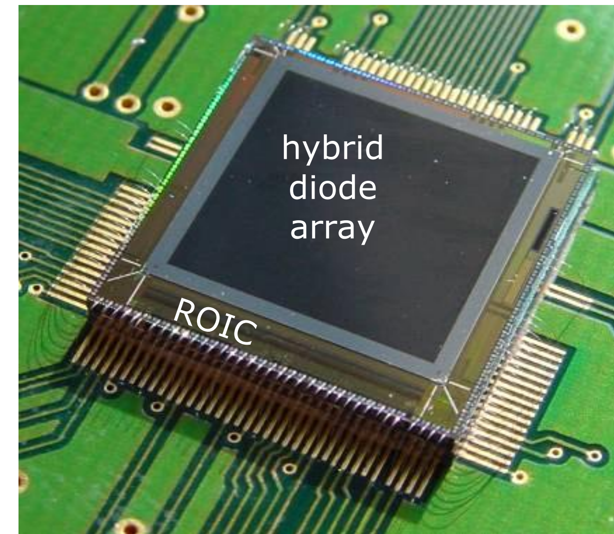
3D INTEGRATED IMAGERS ROADMAP



HYBRID BACKSIDE ILLUMINATED IMAGER: 'HYBRID APS'

- specifications:
  - 22.5 um pitch
  - stitched design: 512x512, 1024x1024
  - **QE> 80% from 400 – 850 nm**
  - thick epi: final thickness ~ 12-35 um
- passive photodiode array (including trenches for X-talk reduction, graded epi) designed and fabricated @ **imec**
- ROIC designed by **FillFactory/Cypress**, fabricated in CMOS 0.35um **commercial foundry** process
- backside thinning, backside passivation, hybridisation @ **imec**





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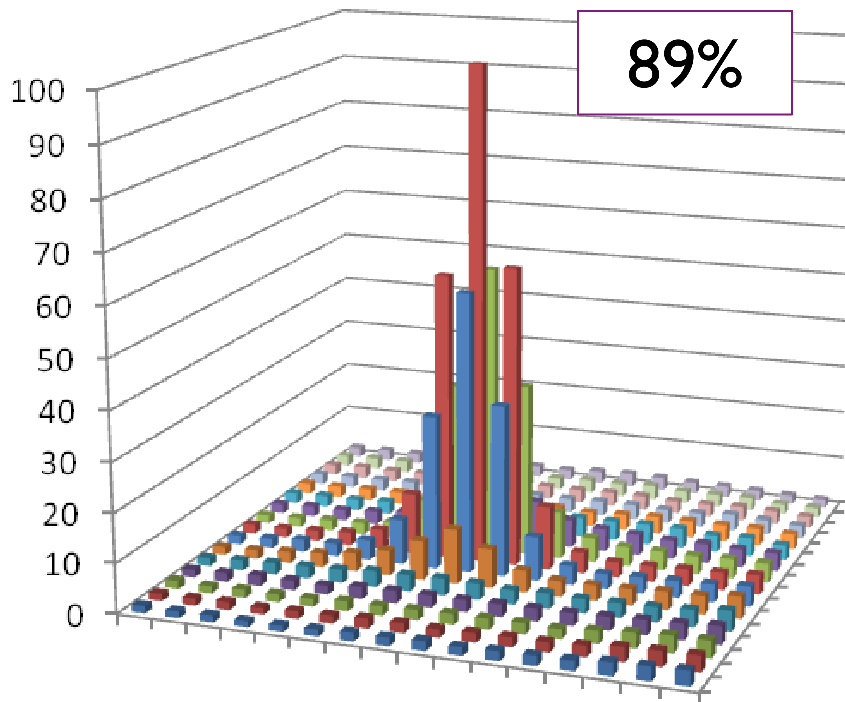
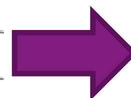
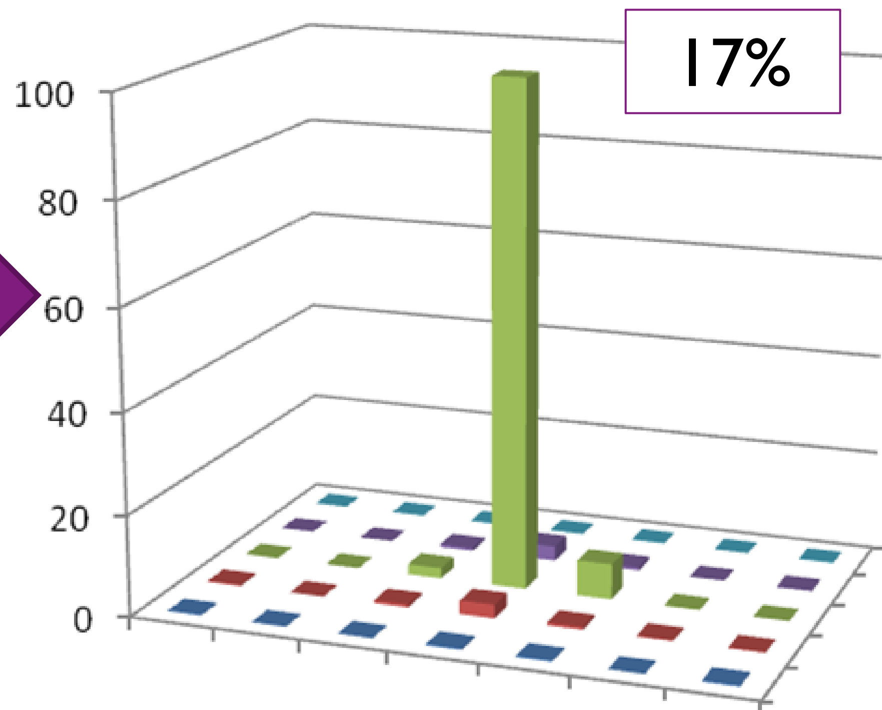
HYBRID BACKSIDE ILLUMINATED IMAGER:
LOW CROSS-TALK WITH GRADED EPI PROFILE

- decrease in cross-talk demonstrated on BSI hybrid imagers using optimized graded epi and reduced thickness
- total charge spreading to neighbors using (laser) point source:





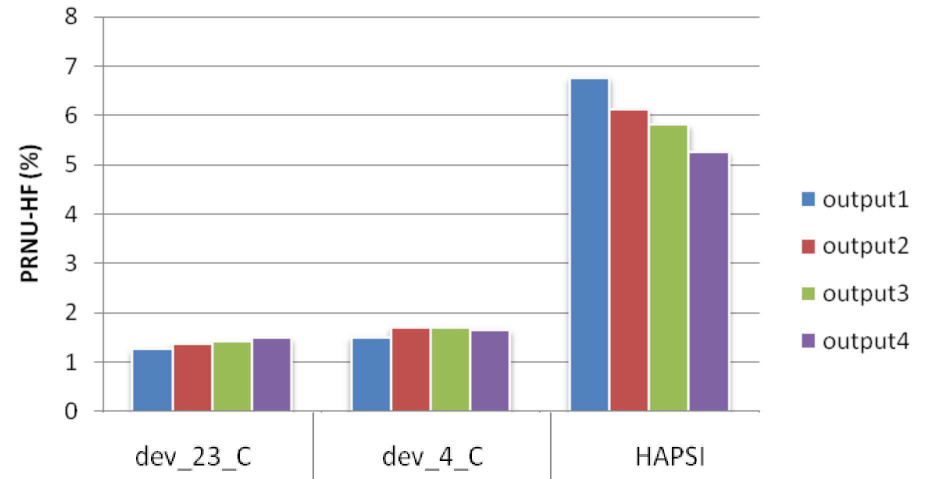


generation 1 graded epi, 35 um

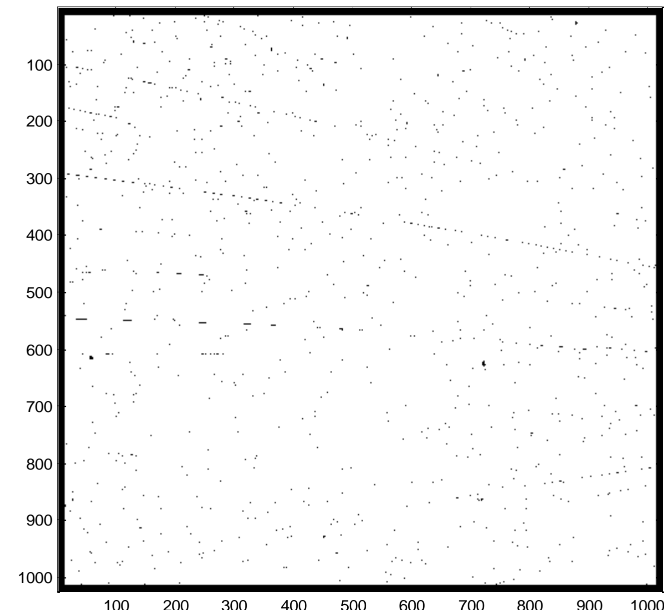
generation 2 graded epi, 12 um

HYBRID BACKSIDE ILLUMINATED IMAGER: UNIFORMITY & DEFECT PIXELS

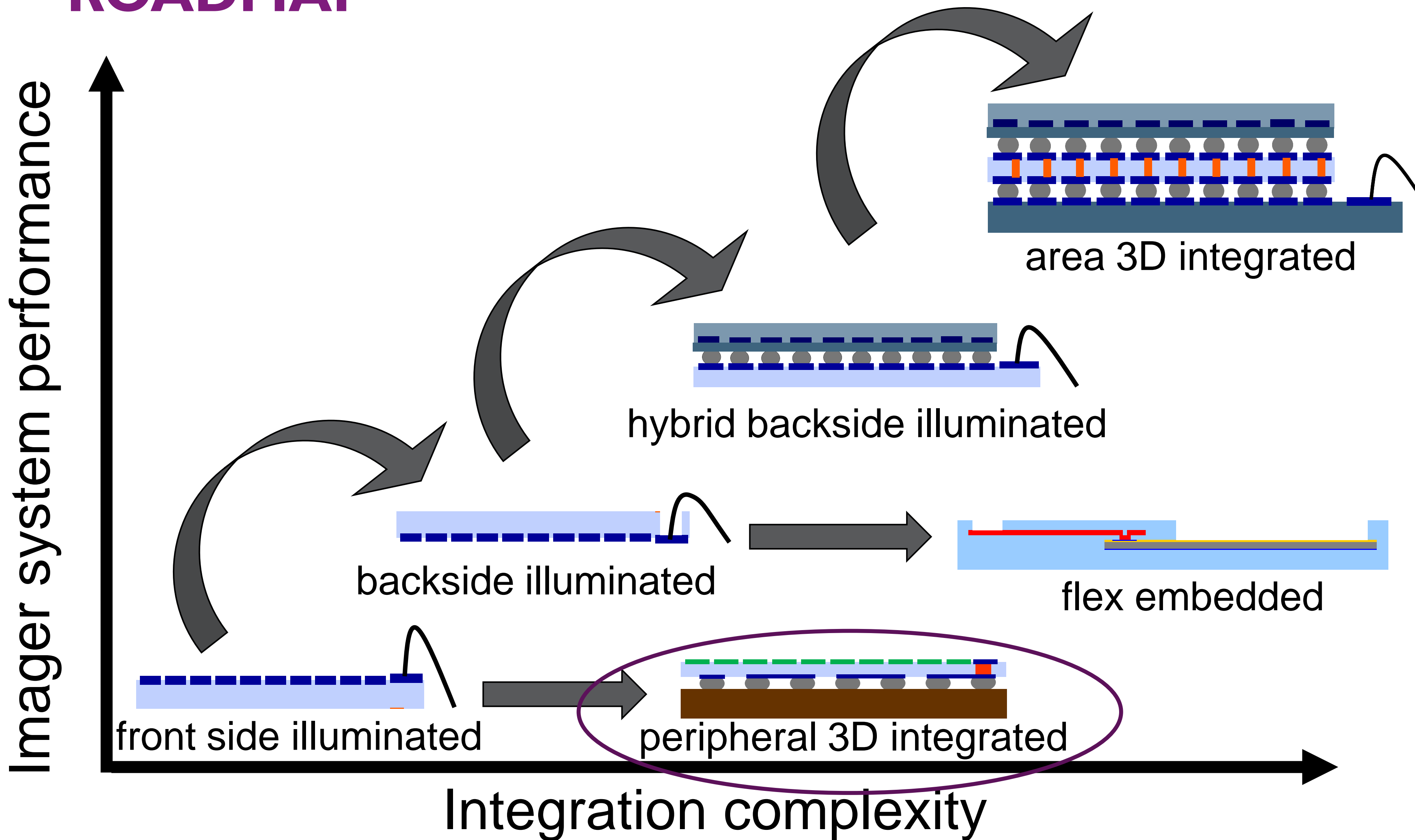
- pixel response non-uniformity (PRNU):
  - high frequency/ short distance
  - < 2%
  - very uniform process



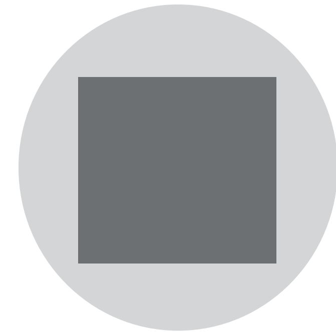
- defect pixels:
  - = pixel response outside +/- 20 % average response
  - < 0.5 %



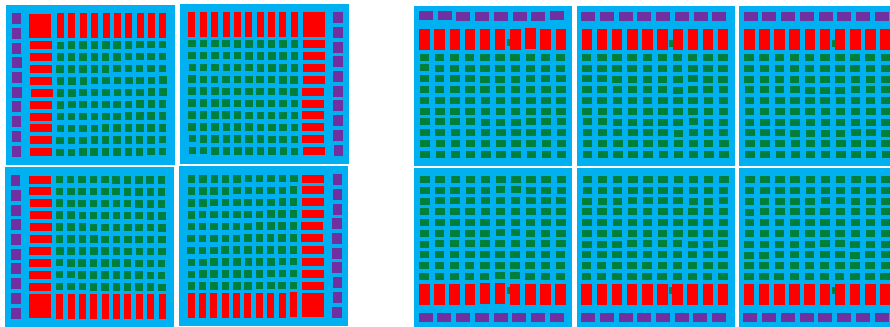
3D STACKED IMAGERS:
ROADMAP

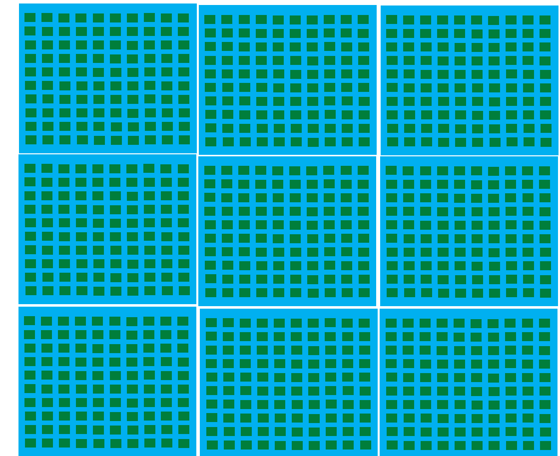


PERIPHERAL 3D INTEGRATED IMAGERS:
TILING FOR LARGE AREA IMAGERS

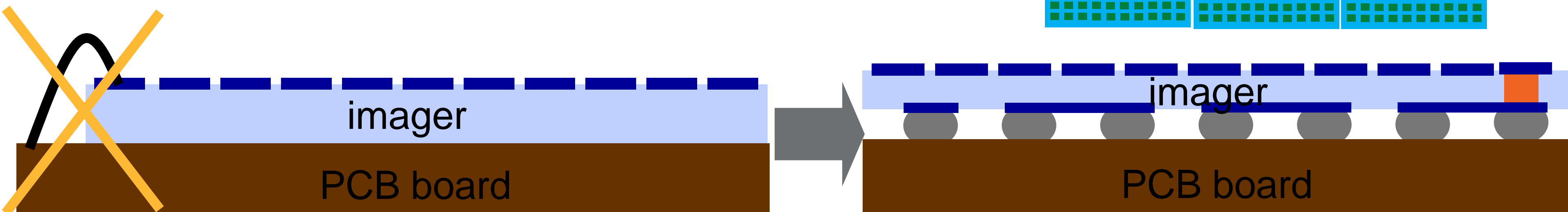


- stitching: yield problem, area limit
- 2-side/3-side buttable/tiling: area limit





- solution = 4-side buttable using 3D integration
  - minimal non-sensitive area thanks to vertical interconnection



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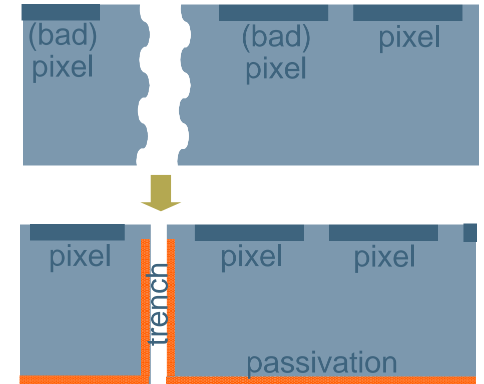
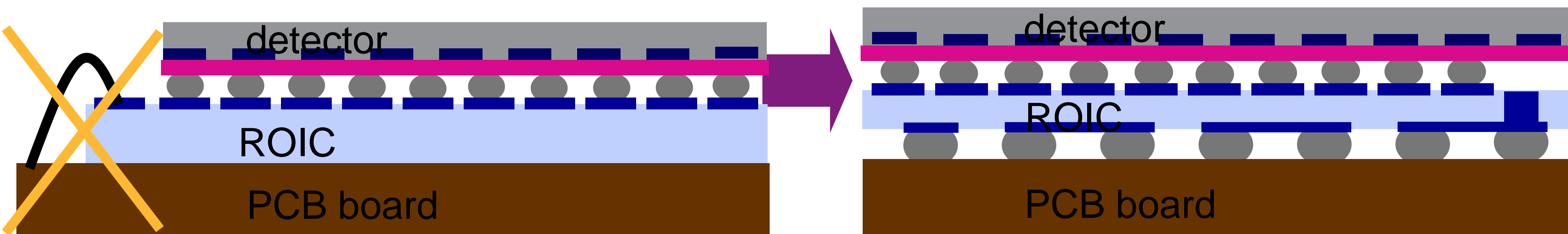
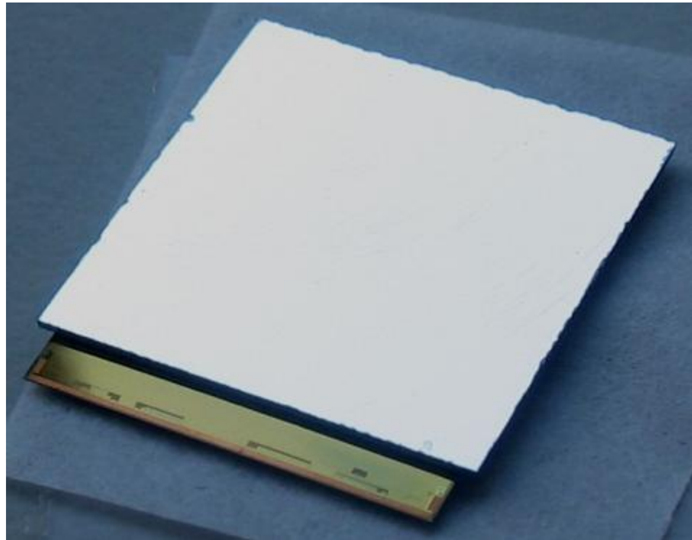
PERIPHERAL 3D INTEGRATED IMAGERS: RELAXD: LARGE AREA X-RAY DETECTION

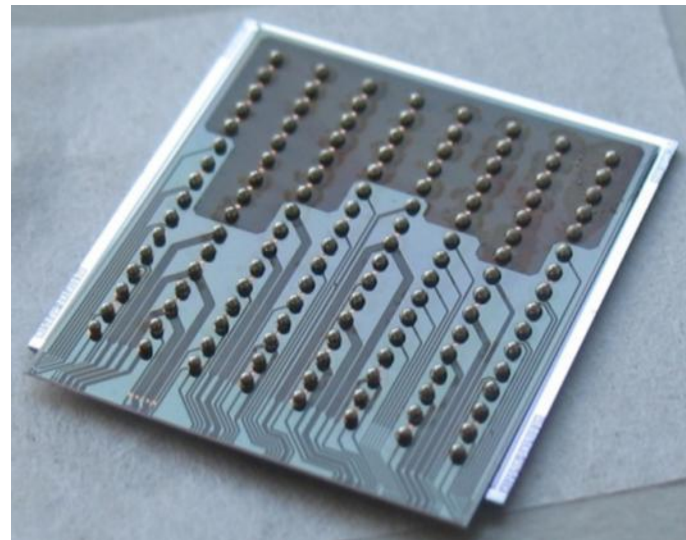
- 4-side buttability using TSV at bondpad level
- edgeless imagers:
  - advanced singulation close to active pixels:
    - dicing by grinding
    - side wall passivation
- status:
  - demonstrators built
  - functionality test ongoing

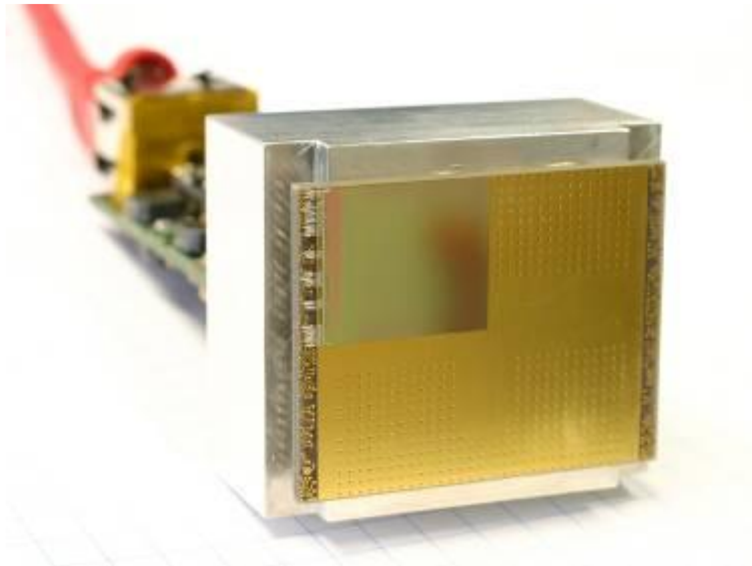


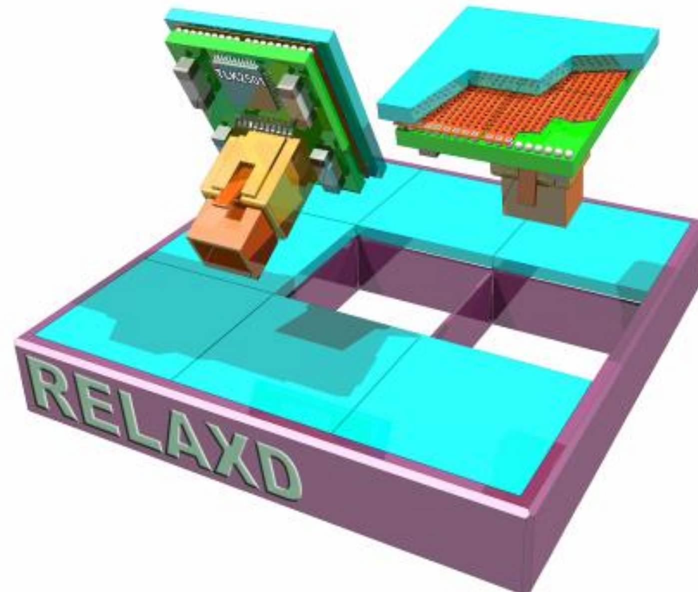


PERIPHERAL 3D INTEGRATED IMAGERS: RELAXD: LARGE AREA X-RAY DETECTION

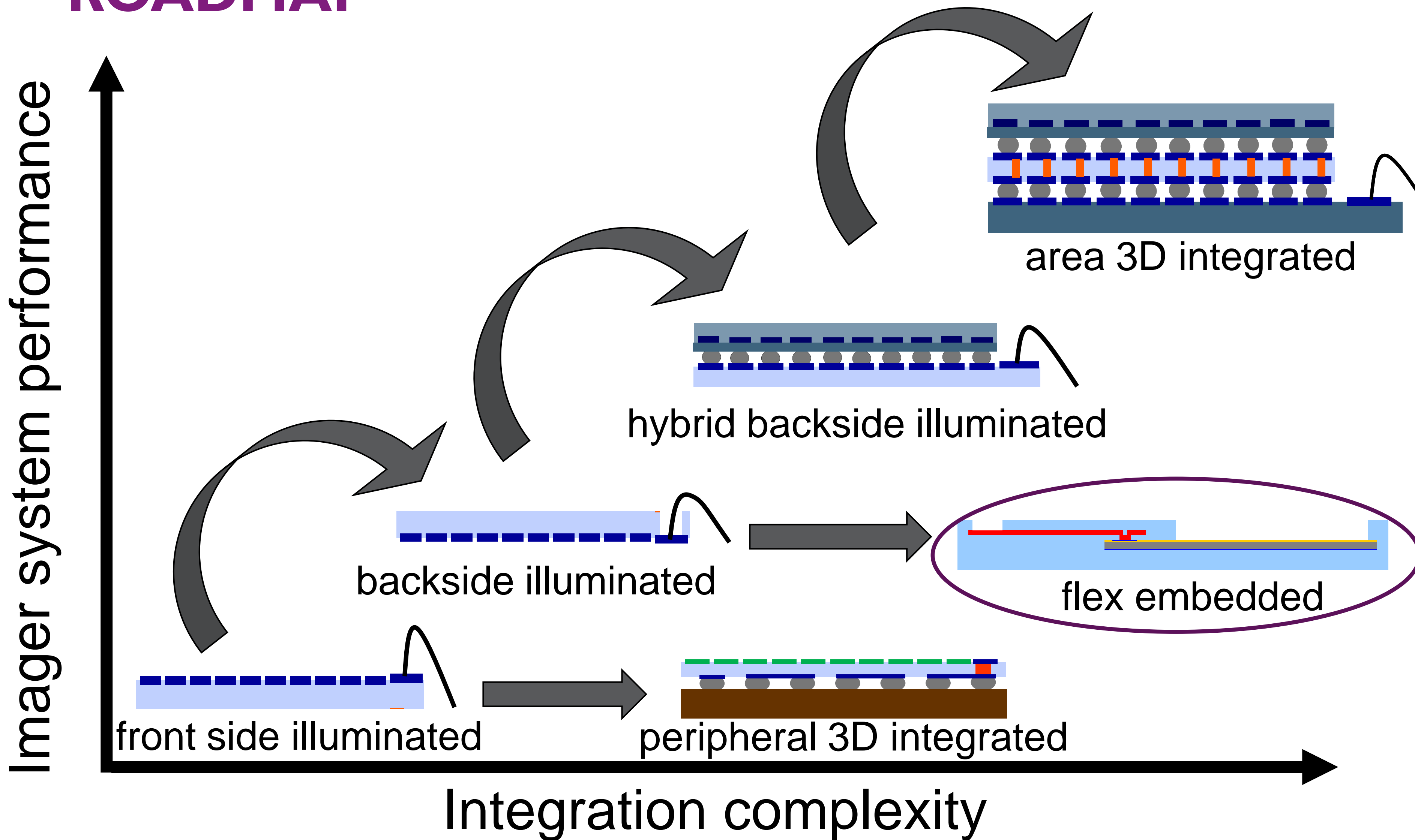




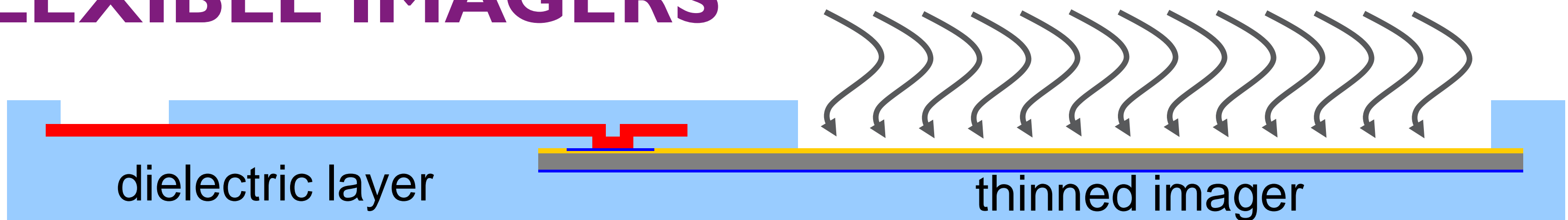




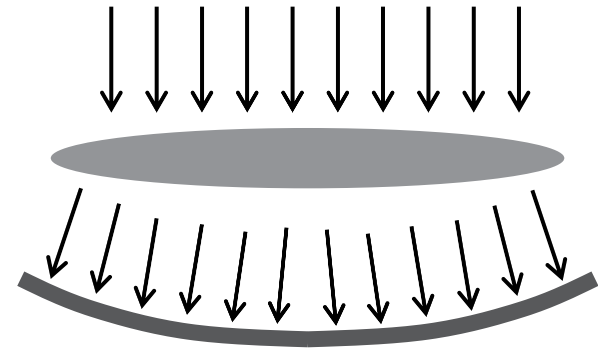
3D STACKED IMAGERS:
ROADMAP

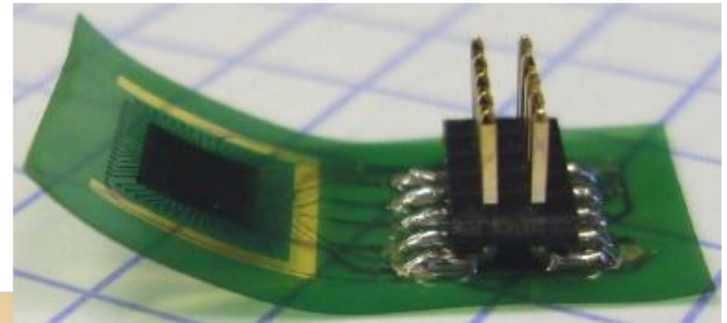


FLEXIBLE IMAGERS



- curved imager concept:
  - embedding of a thinned imager in a flexible foil
  - thin Si (~ 20 um)
- application examples:
  - non-planar focal plane, allowing easier/enhanced optics
  - on/in the body radiation monitoring for cancer therapy
  - tracking detectors for high energy particles
- example of IMEC techno:
  - functional microcontroller in flex substrate





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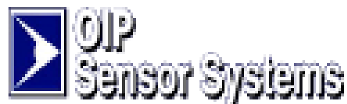
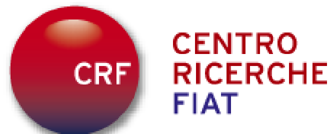
CONCLUSION

- many competences under one roof:
  - flexible 0.13 um CMOS
  - (pixel) design know-how
  - qualification know-how

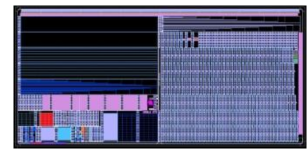
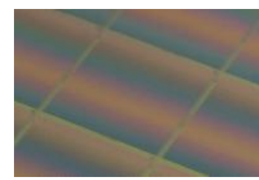
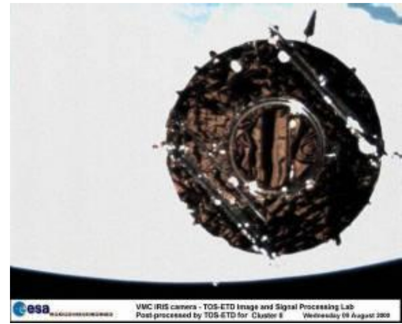
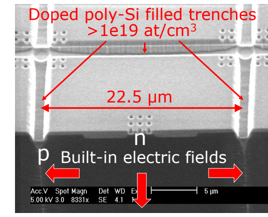
- enable state-of-the art image sensors:
  - R&D projects
  - DoD (Development-on-Demand)
  - LVP (Low Volume Production)

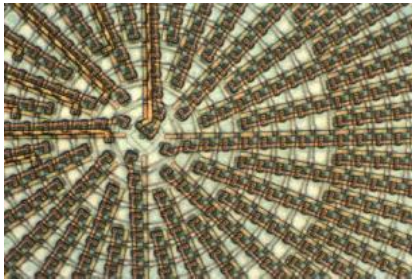
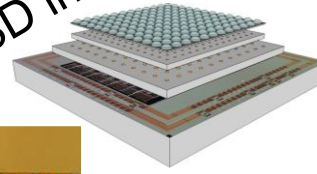
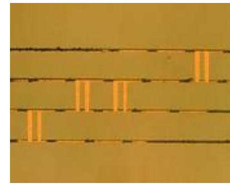
IMEC IMAGER PARTNERS

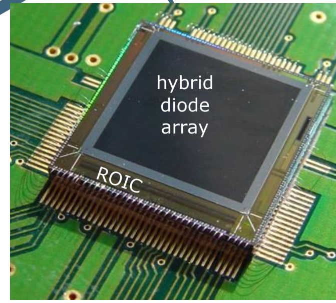


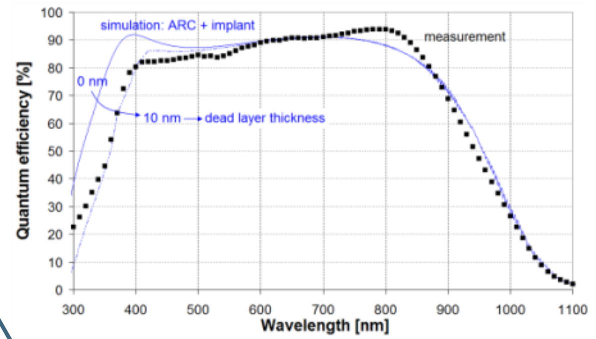


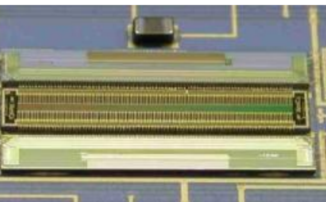
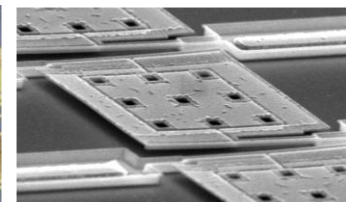
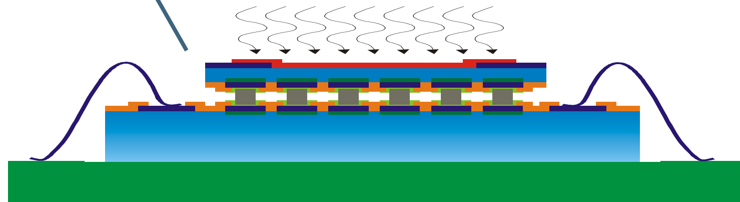
25 YEARS OF IMAGING





1985
CCDs
1990
1995
CMOS
2000
frontside illuminated
2002
2004
2006
2008
Hyper-
spectral
2010
Imec
0.13 um CIS
2012
infrared
Hybrid backside
illuminated
3D integrated

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ACHIEVE

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