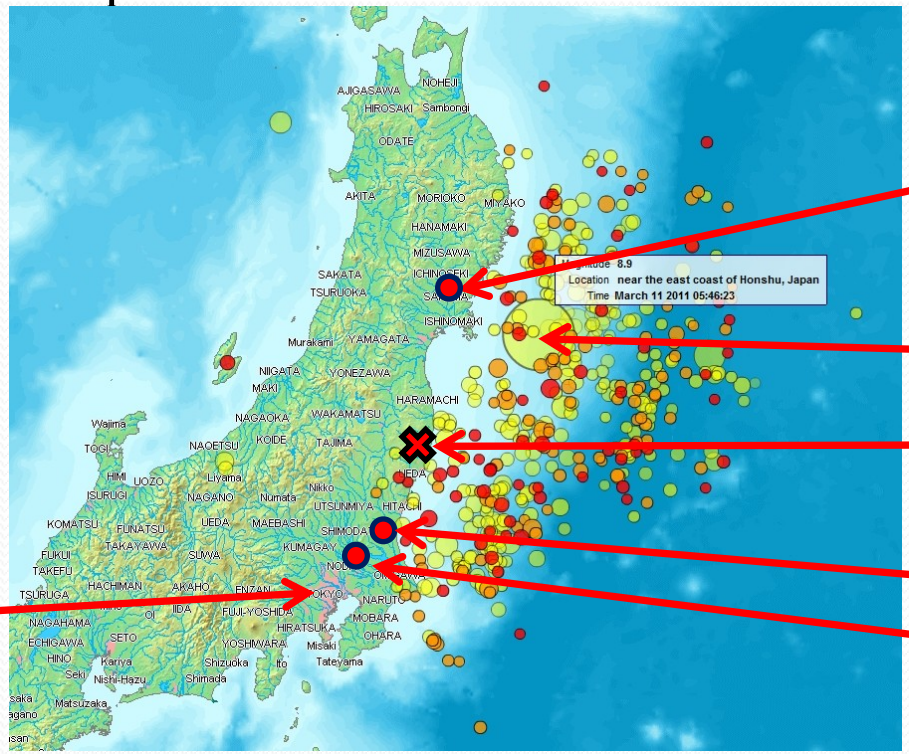
Recent progress on SOIPIX project

Ryo Ichimiya (KEK/IPNS)
on behalf of the SOIPIX collaboration
http://rd.kek.jp/project/soi/

Earthquake, Tsunami and recovery…

- On March 11th 2011 14:47 JST, Magnitude 9.0 earthquake hit East-Japan.
- Collaborating OKI Semiconductor Miyagi Fab. locates very near from the source of the earthquake.



OKI Semi. Miyagi Fab.

the source of the earthquake

Fukushima dai-ichi NPS

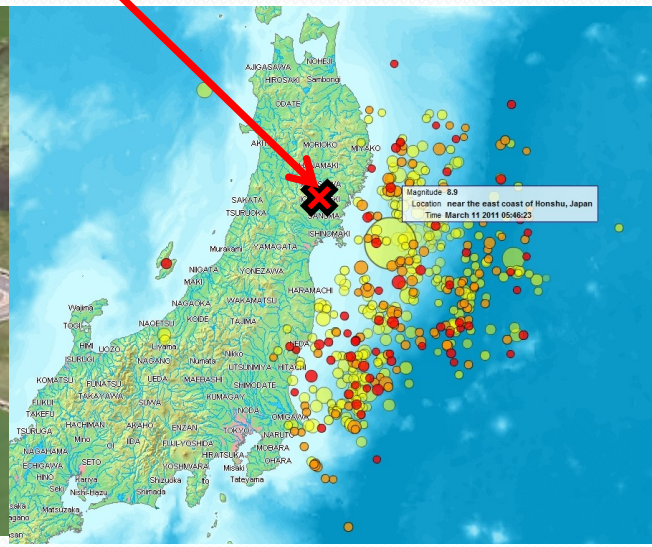
J-PARC

KEK

Tokyo

Our big thanks to colleagues and friends outside Japan who support us and are giving warm words. They are highly appreciated. We'd like to keep them in our heart forever.

OKI Semiconductor Miyagi



- OKI Semiconductor Miyagi, in which the SOIPIX is fabricated, has severe damage by the Earthquake and subsequent Water and electrical power stop.
- On April 15th, it resumed operation and now it produces products at 95% of normal level.
  - Fortunately, our MPW run wafers (submitted on this Janually) were safe and are scheduled to ship in mid-July.

KEK (Tsukuba)+J-PARC(Tokai)

8-GeV Injector Q-Magnet(Tsukuba)

Groundwater discharges… (Tsukuba)

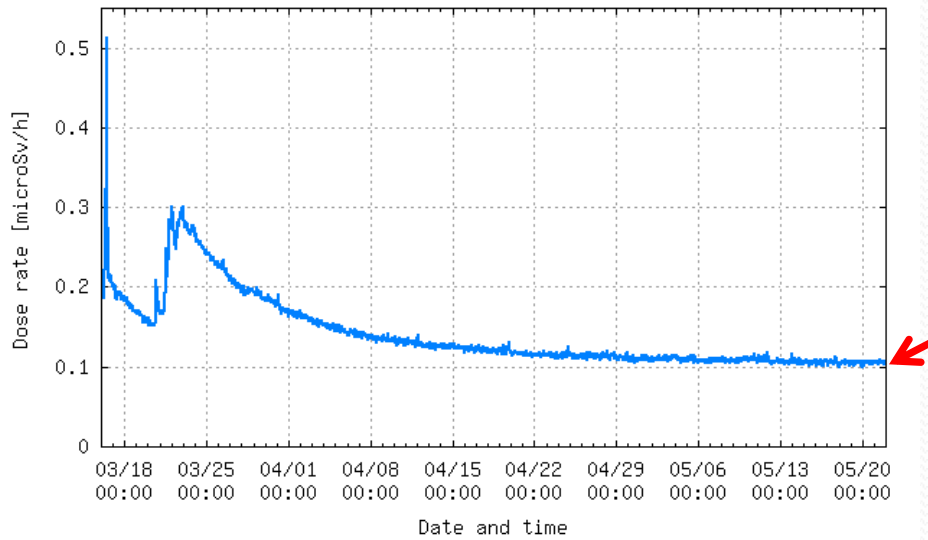
Linac building entrance (J-PARC)

NU Target Station Building (J-PARC)

KEK recovery and response

- No human injured or casualties. Material damage are being assessed and will be recovered.
- Fortunately, we can resume to use our laboratory from the April 6th.

- KEK radiation safety division has began real-time radiation monitoring just after electrical power recovered and made it publically viewable at KEK site: http://rcwww.kek.jp/norm/



Radiation level is almost back to normal; it's safe!!

KEK Web page: http://www.kek.jp/intra-e/

KEK
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION

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DG's Corner

09 May 2011

Damage caused by the recent earthquake and recovery prospects

First of all, I would like to express my deepest appreciation for the messages of concern, sympathy and encouragement that we received from all over the world since the major earthquake of March 11th. We are working to restore KEK as quickly as possible to its original condition so it can once again function as the exceptional research facility it was hitherto. Your messages do help a great deal in this difficult time.

Both the KEK-Tsukuba and KEK-Tokai (J-PARC) sites experienced tremors exceeding 6 on the Japanese seismic intensity scale, even though we are some 300 km away from the epicenter. This has caused a significant amount of damage to both facilities. In the Tsukuba-campus, components of accelerators, detectors and peripheral became detached and fell to the ground or collided with each other. Infrastructures such as the substation to ...

Atsuto Suzuki
Director General

more

- Earthquake Emergency Response Team
- Radiation Monitoring in Tsukuba
- For Personnel and Users

Announcement

8th report on radiation monitoring released
13 May 2011

KRS will be accessible from 13:00 on April 18.
15 Apr 2011

archive

Feature

Highlights

Conference & Seminars

(Cancelled)ILD Workshop 2011
23 May 2011 - 25 May 2011
Kobayashi Hall

Fundamental aspects of Time in Quantum Mechanics and Meson Phenomenology
31 May 2011 13:30 - 14:30
Kenkyu Honkan 3F, Room 322

Exploring Hadron Physics in Black Hole Formations: a New Promising Target of Neutrino Astronomy
31 May 2011 16:00 - 17:00
Laboratory No.4, Room 345

more
archive

Press & Topics

Press
Photon Factory secures research opportunities for its users
13 May 2011

Press
Call for Nomination for Next Director-General of KEK
10 May 2011

Topics
Donation from CERN goes to orphans of the earthquake
09 May 2011

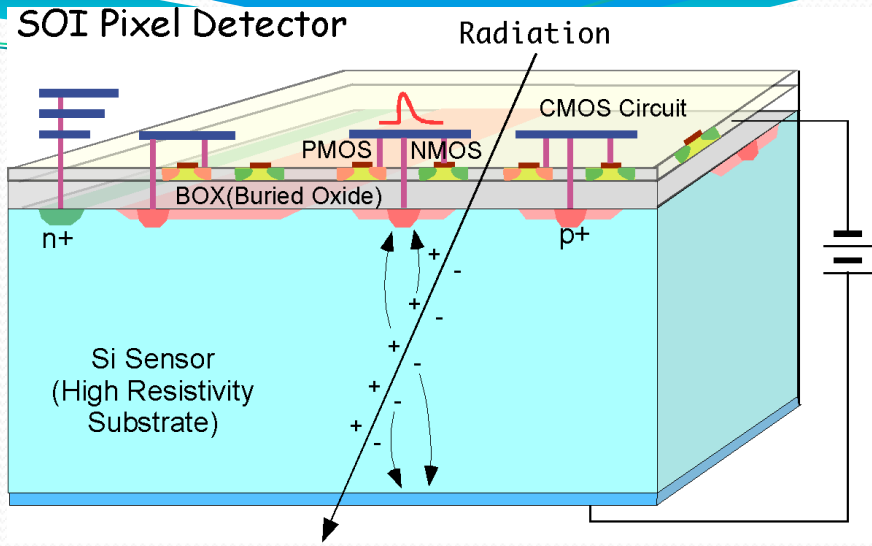
Press
Director of Photon Factory reports the damages of the recent earthquake and its recovery prospects
28 Apr 2011

Outline

1. SOIPIX technology
2. Recent Test Results
3. Issues & Solutions
4. Summary

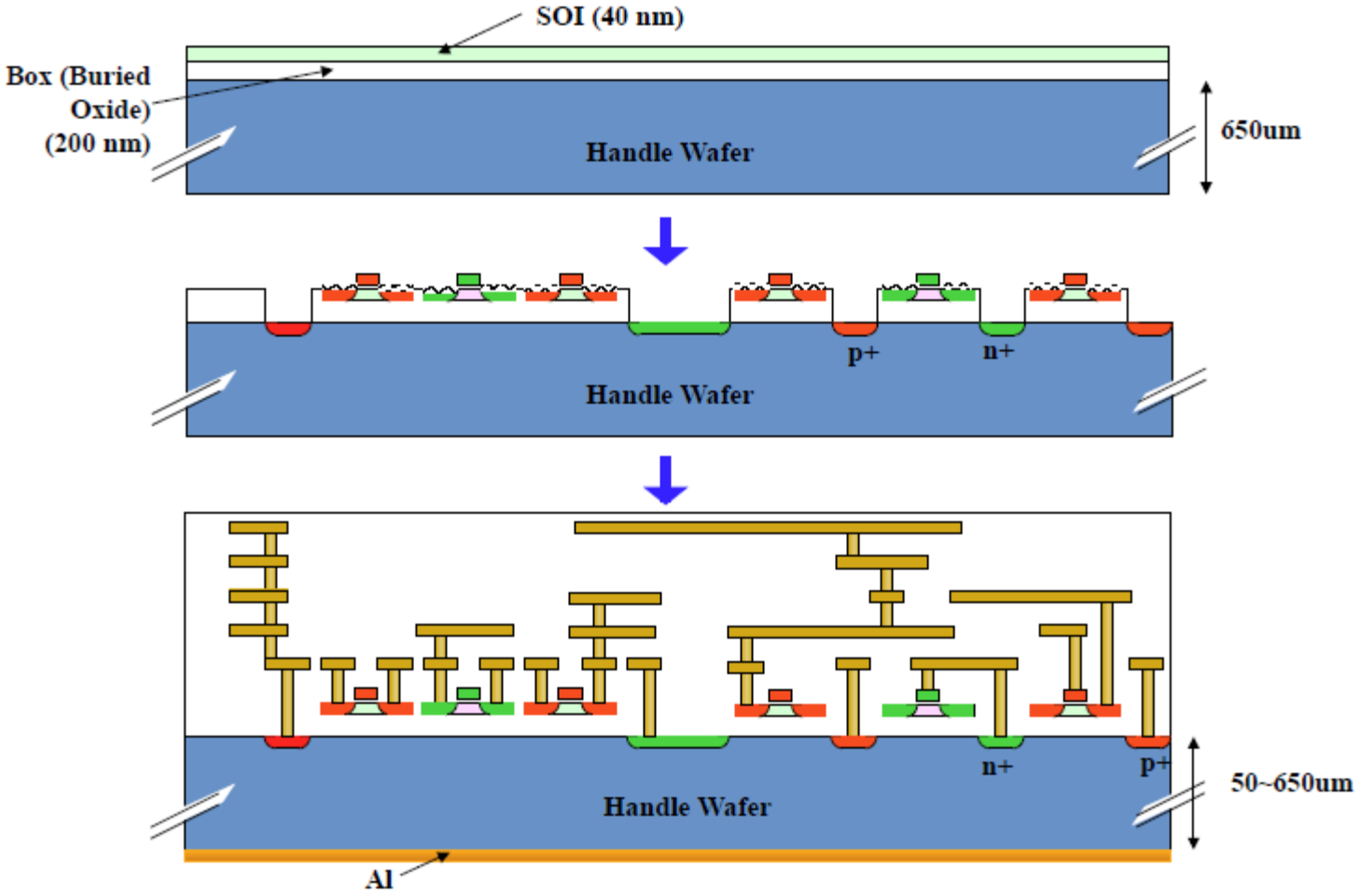
SOI pixel detector

Monolithic detector using Bonded wafer (SOI : Silicon-on-Insulator) of
Hi-R (sensor) and Low-R (circuit) Si layers.



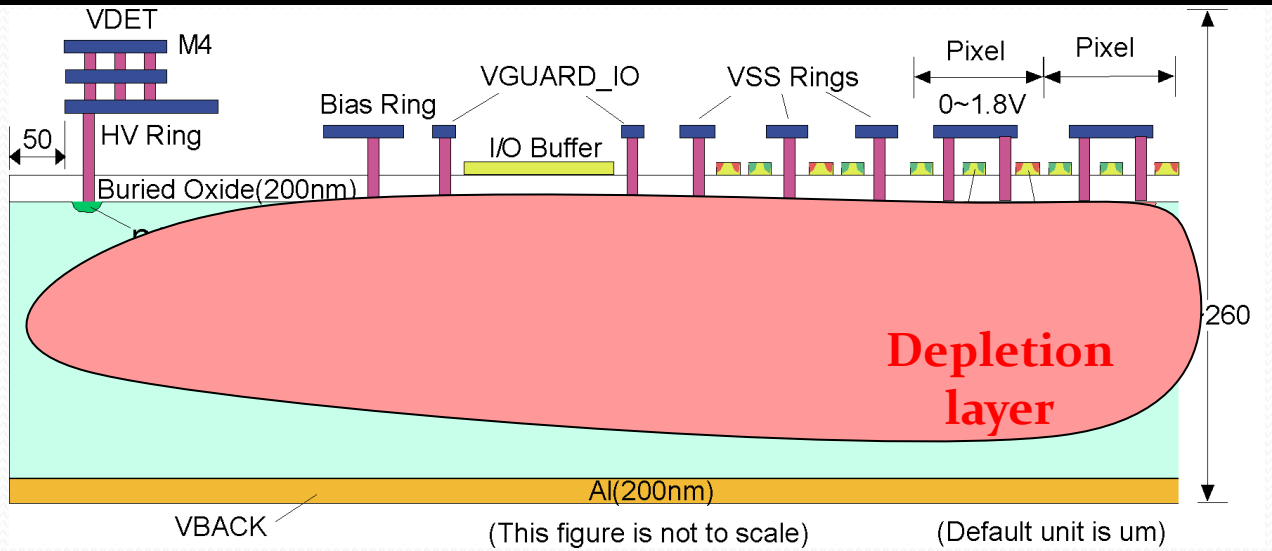
- No mechanical bump bondings
  -> High Density(pitch <5μm), Low material budget
  -> Low parasitic Capacitance, High Sensitivity
- Fast signal and High resolution (Full Depletion: >200μm Si)
- Standard CMOS circuits can be built.
- Thin active Si layer (~40 nm)
  -> No Latch Up, Small SEE Cross section, larger LET threshold.
- Based on Industrial standard technology
  -> Fabricate in a commercial fabrication plant

SOI Pixel Process Flow



OKI 0.2μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4 (5) Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz ~700 Ω-cm (*n-type)*, FZ: ~10kΩ-cm (n-type, p-type) up to 725 μm thick
Backside	Thinned to 260 μm and sputtered with Al (200 nm).



An example of a SOI Pixel cross section

Recent Process Improvements

- Increase No. of Metal Layer: 4 -> 5 layers
  --> Better Power Grid and Higher Integration

- Shrink MIM Capacitor Size: 1.0 -> 1.5 fF/μm^2
  --> Smaller Pixel size become possible

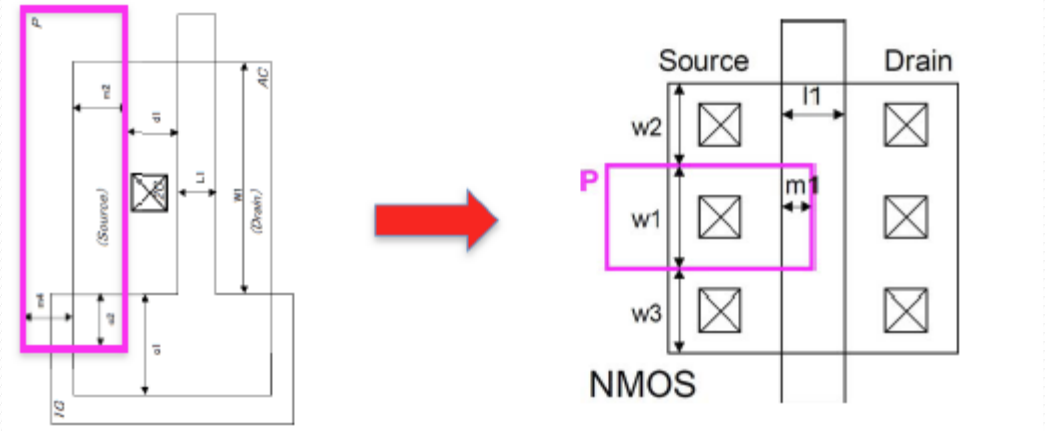
Recent Process Improvements(cont'd)

- Relax drawing rule: 30˚ ,45˚ -> Circle

  --> Smooth field and Higher breakdown Voltage

- Introduction of source-inserted body contacts

  --> Better body contacts (Less kink and history effects, Lower noise).



Target Applications

- High Energy Physics
  - Vertex detector – Belle II @ KEK, ILC, sLHC,...
- Material Research
  - X-ray Free Electron Laser (XFEL) @SPring-8
  - Time resolved XAFS (X-ray absorption fine structure)

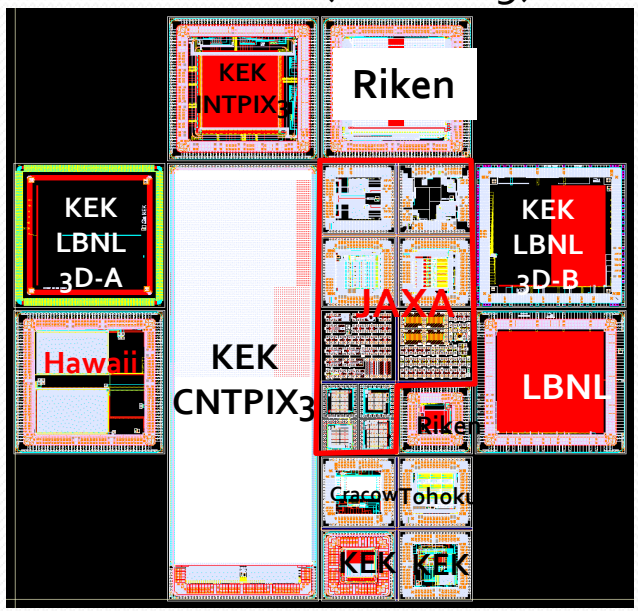
  ...
- Astrophysics
  - X-ray Imaging detector, Infrared detector
- Medical
  - Mammography, CT, PET, Hadron Therapy,...
- Electron Microscopy
- Industrial
  - X-ray Inspection System

Advantage: High density, Low material, Advanced functionality in each pixel.

Multi Project Wafer (MPW) run

- KEK organizes MPW runs (2005-)
- **Twice a year since 2009.**
  - **This year: we have only one MPW run; tentatively scheduled on October.**
- OKI Semiconductor Co. / Ltd. OKI Semiconductor Miyagi Co. Ltd. / T-Micro Co. Ltd.

MPW FY08(Feb.2009)

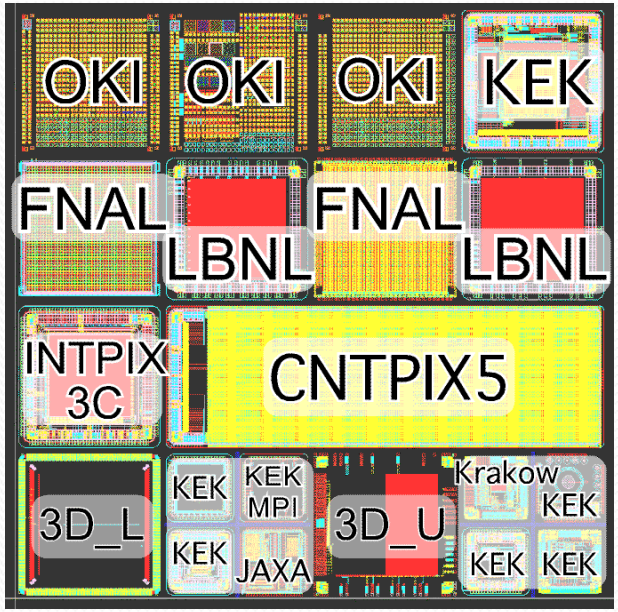


KEK, LBNL, Hawaii, Cracow, Tohoku, JAXA, Riken/SPring-8

MPW FY09-1 (Aug. 2009)

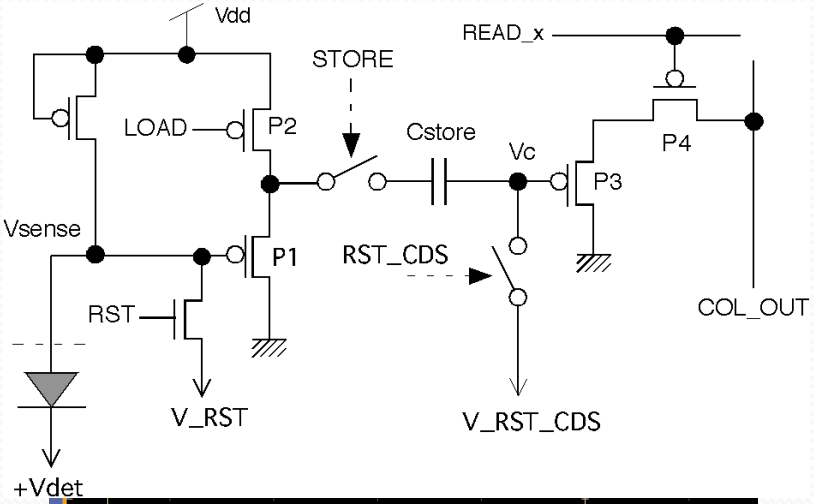
KEK, Riken, Cracow, FNAL, Kyoto, Hawaii

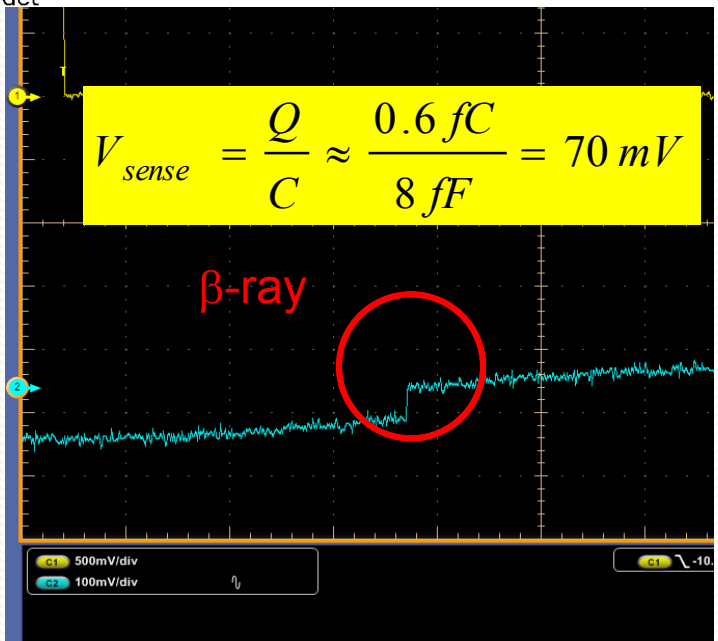
MPW FY09-2 (Jan. 2010)

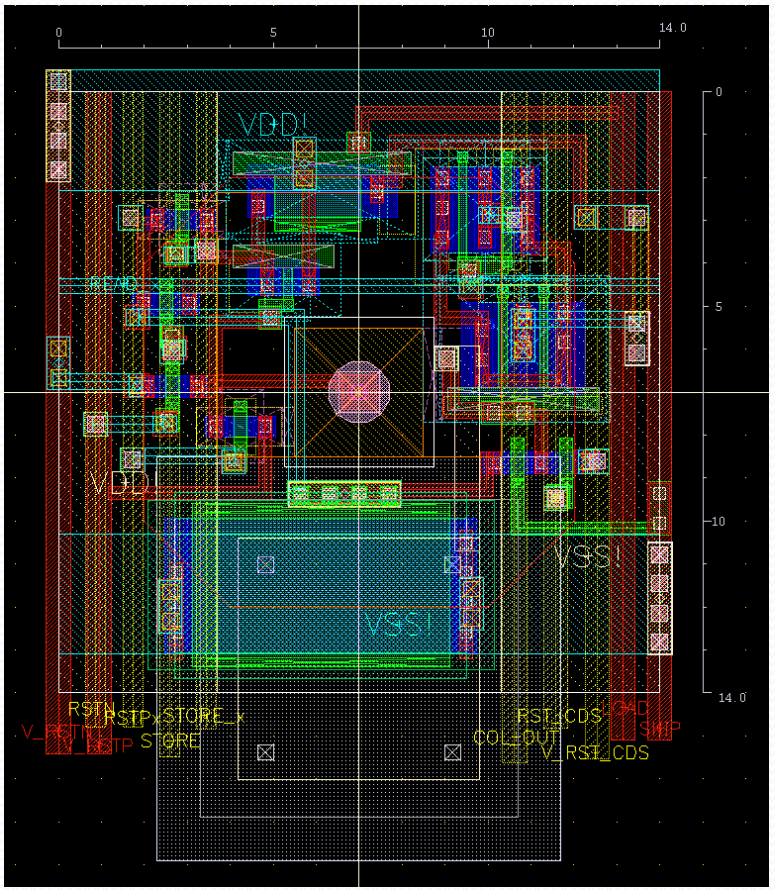


KEK, Riken, FNAL, LBNL, JAXA, KEK-MPI

Integration type pixel (INTPIX)



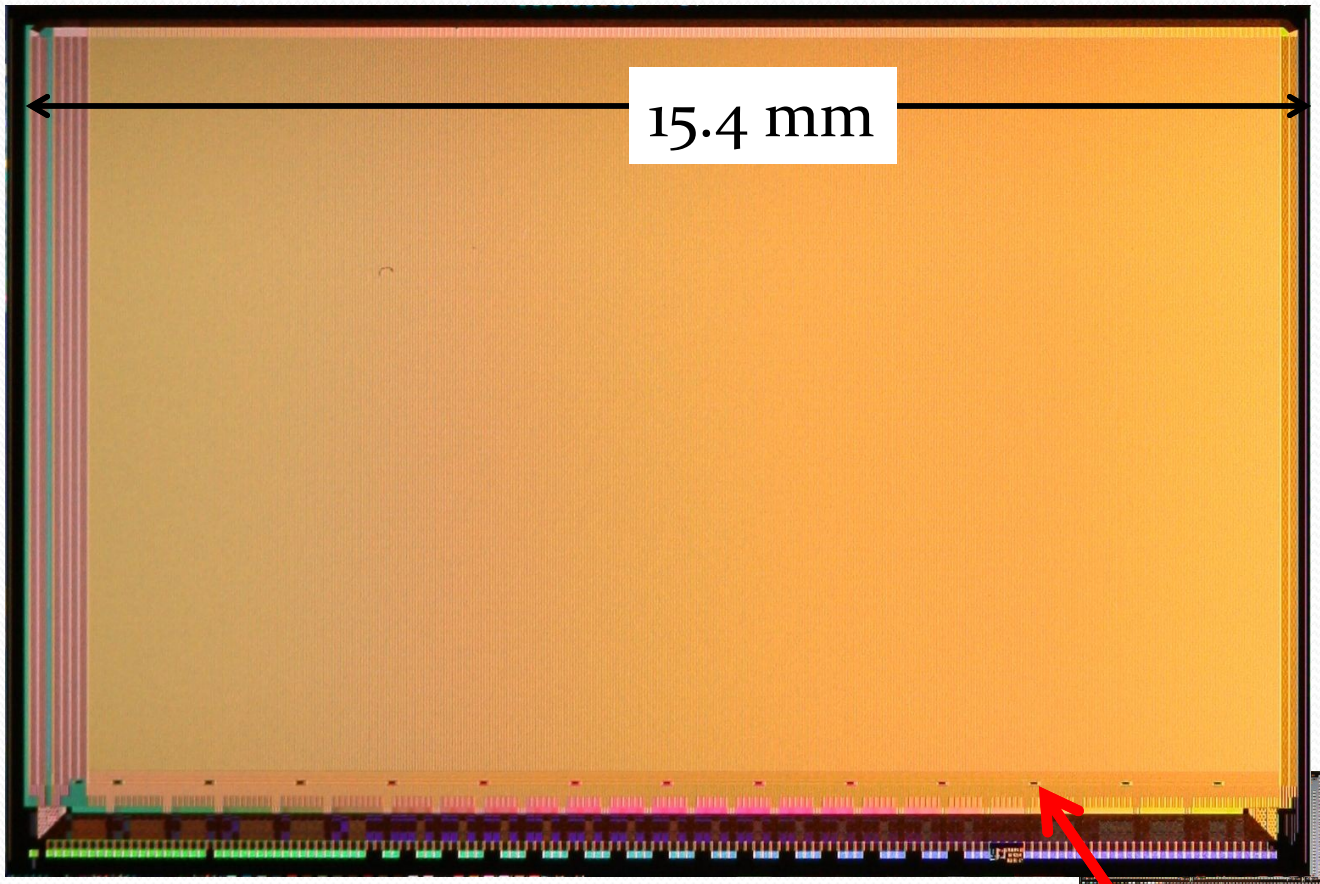




Size : 14 μm x 14 μm
with CDS circuit

Integration Type Pixel (INTPIX4)

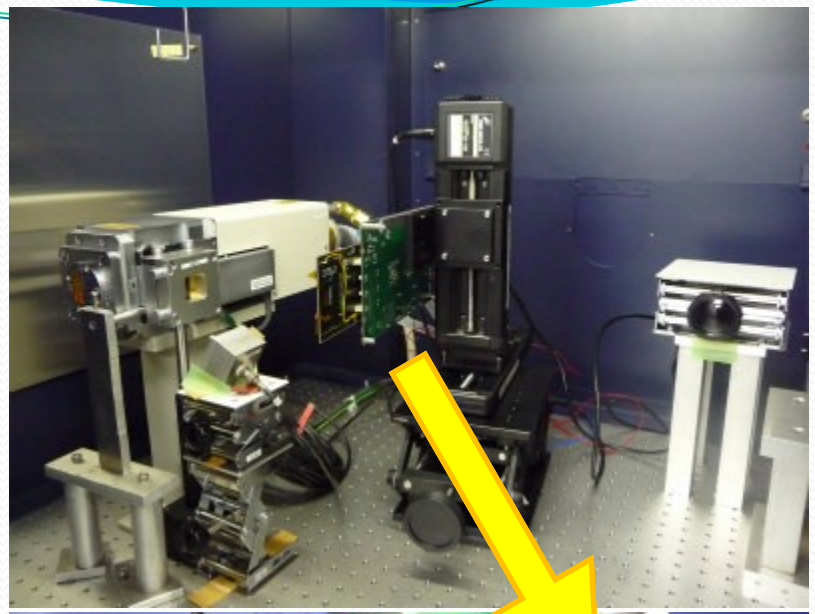
Largest Chip so far.

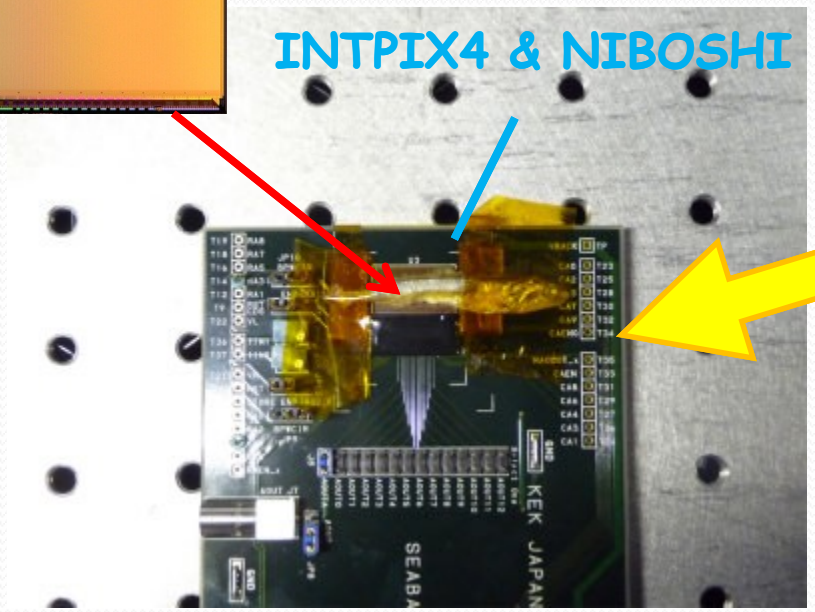


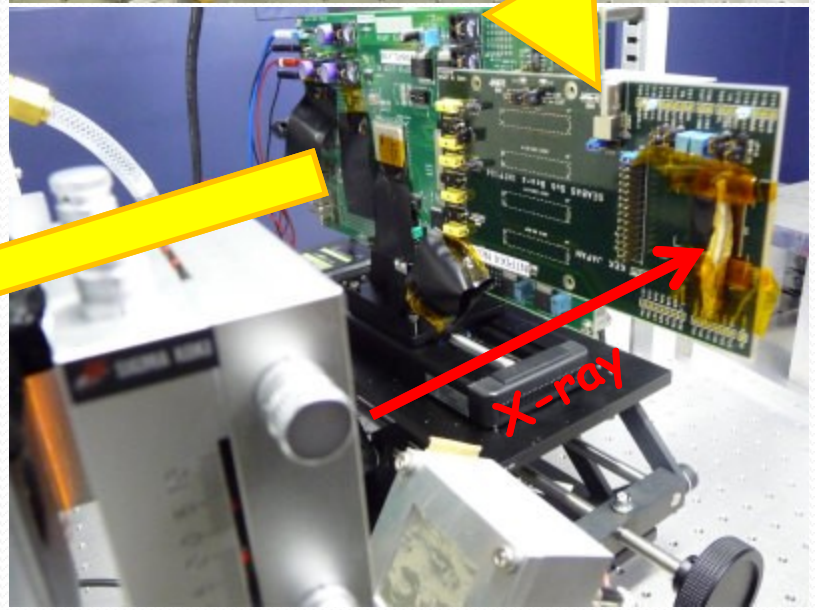
17x17 μm, 512x832 (~430k) pixels,
13 Analog Out,
CDS circuit in each pixel.

X-ray imaging test of INTPIX4

- A small dried sardine (“Niboshi” in Japanese) is used.
  - Bias Voltage: 200V (V_{back})
  - 500 frame obtained
  - Integration time: 250μs
  - X-ray tube(Mo): 20kV, 5mA







X-ray imaging test of INTPIX4(cont'd)

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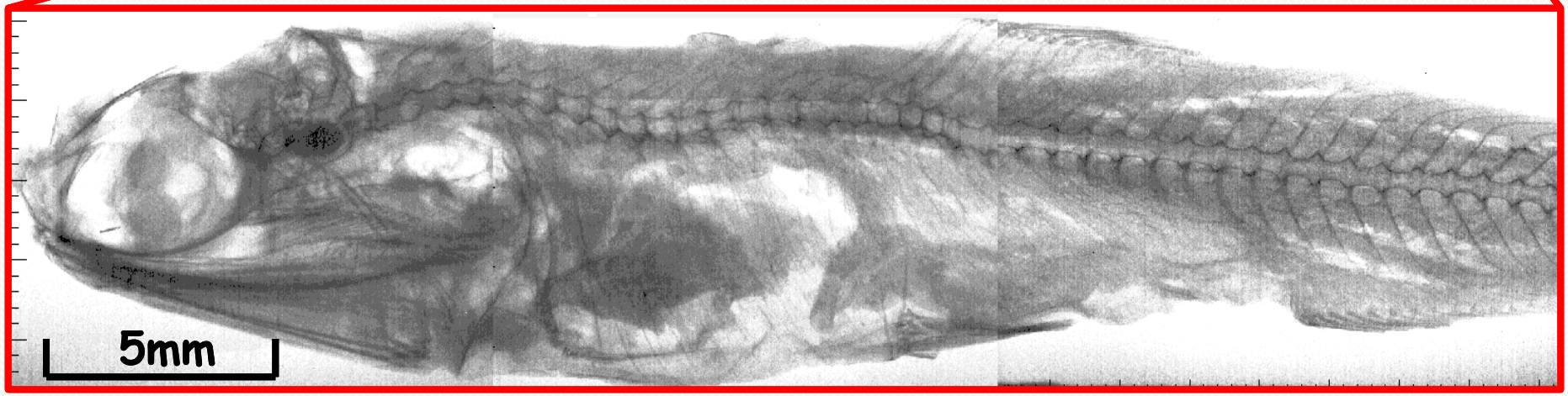
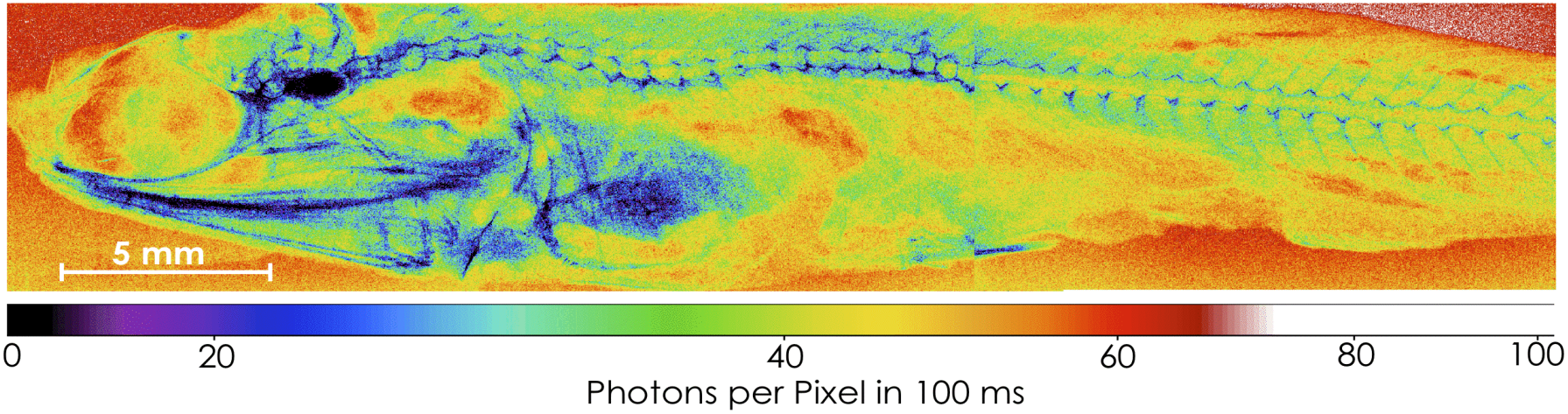
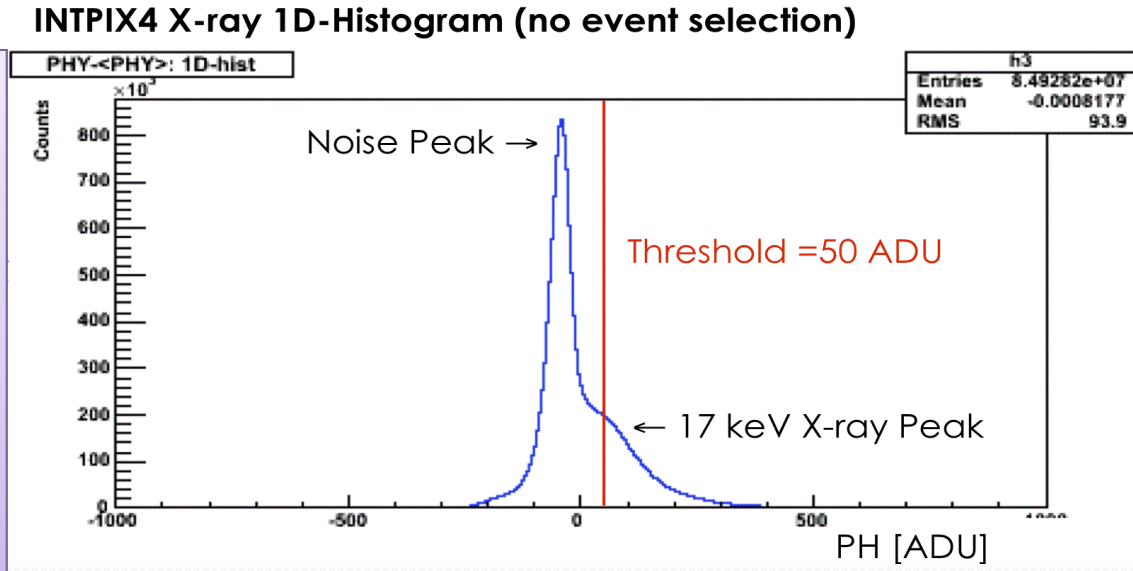


Pseudo-photon counting by INTPIX4

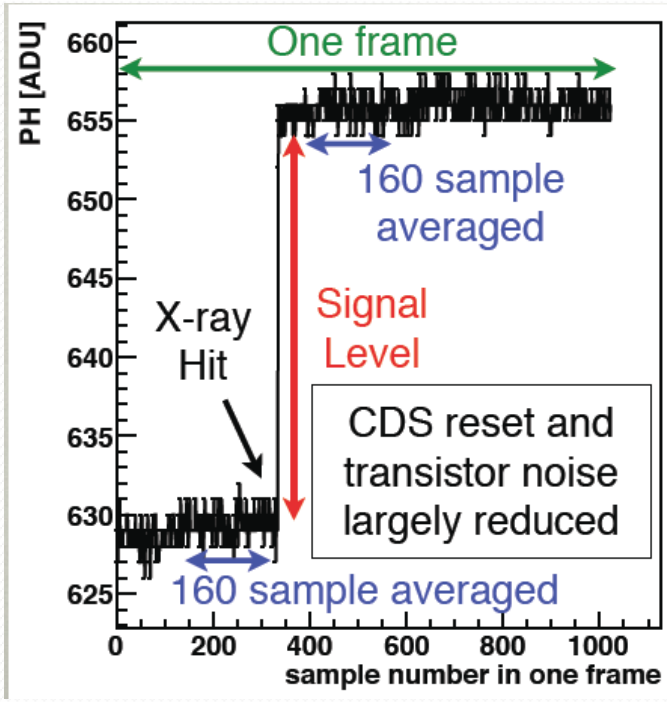


- How to create above map:
  - Calculate pulse height (PH) in each pixel
  - Set threshold as 50 ADU
  - In each pixel frame, evaluate threshold(hit)
  - Create count map (counts/pix)



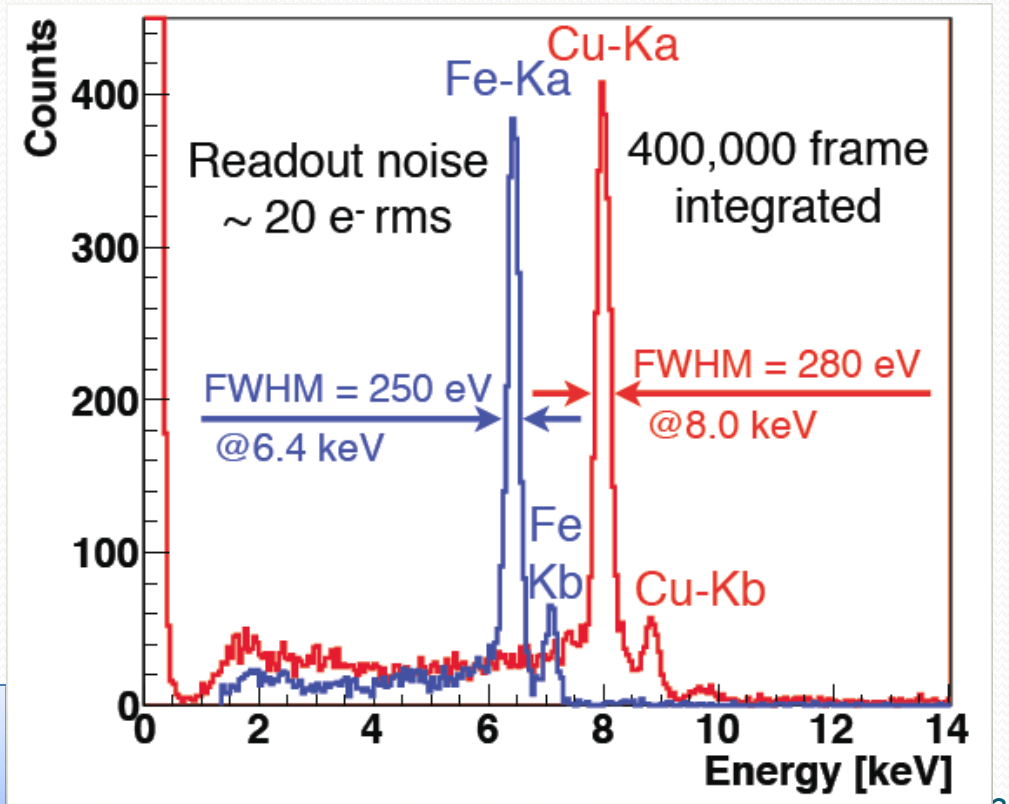
Energy Resolution

- Study of the limits of the energy resolution: single pixel readout mode
- During exposure, 1024 times samples sampled (scan interval=1μs)
- Signal level is calculated by difference between averaged 160 samples after X-ray hit and before hit.

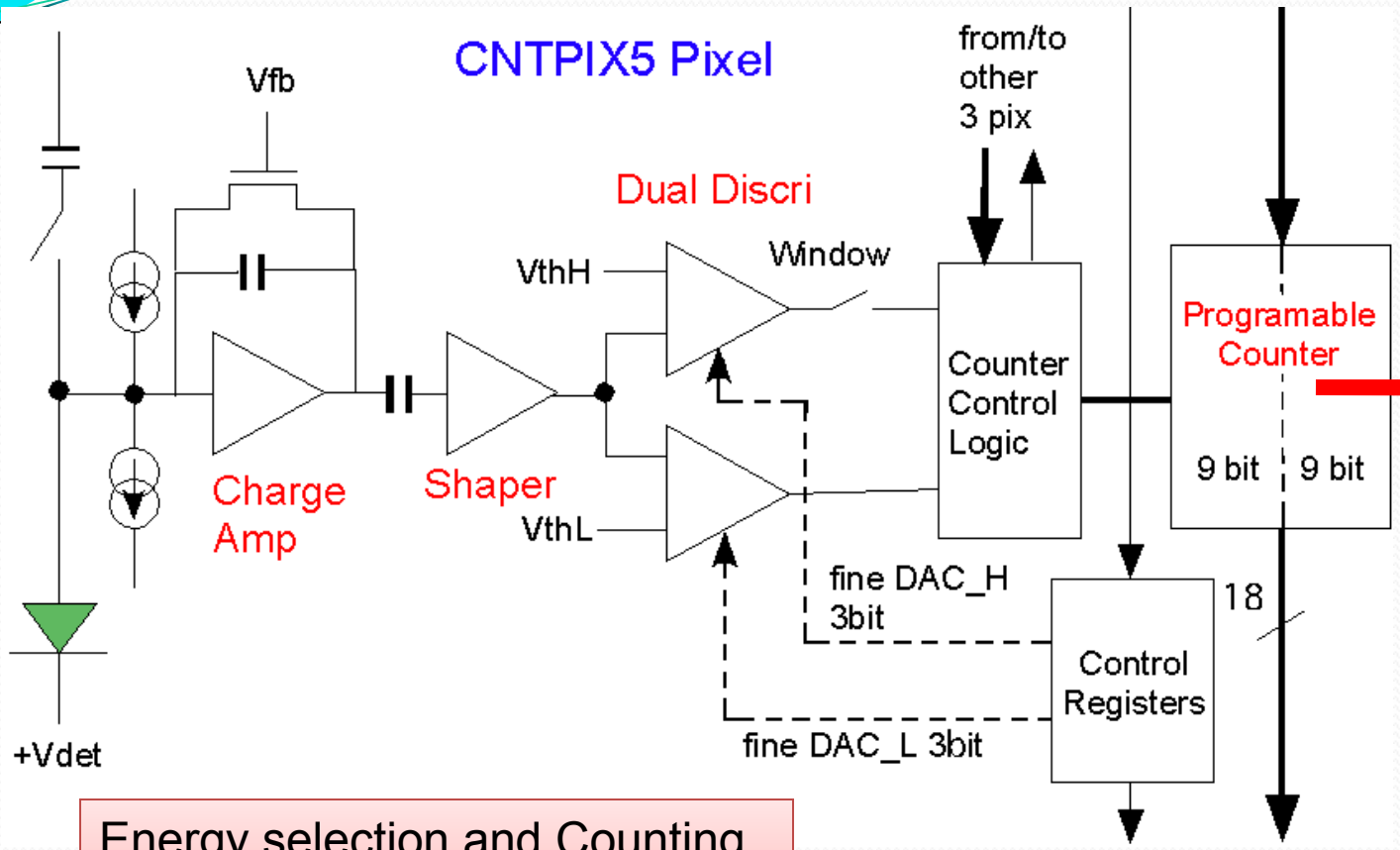


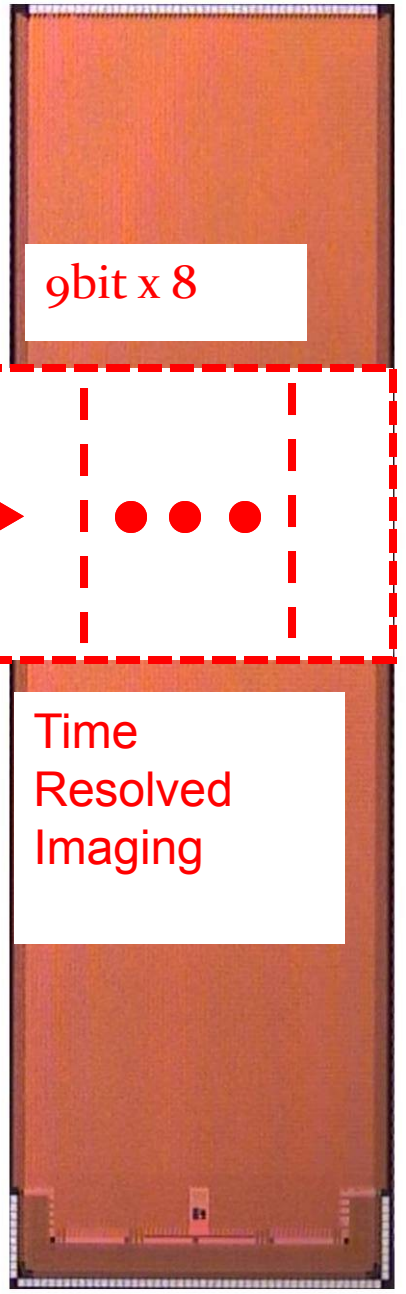
Need to reduce noise, especially at read-out circuit.

Energy Resolution



Counting Type Pixel (CNTPIX5)



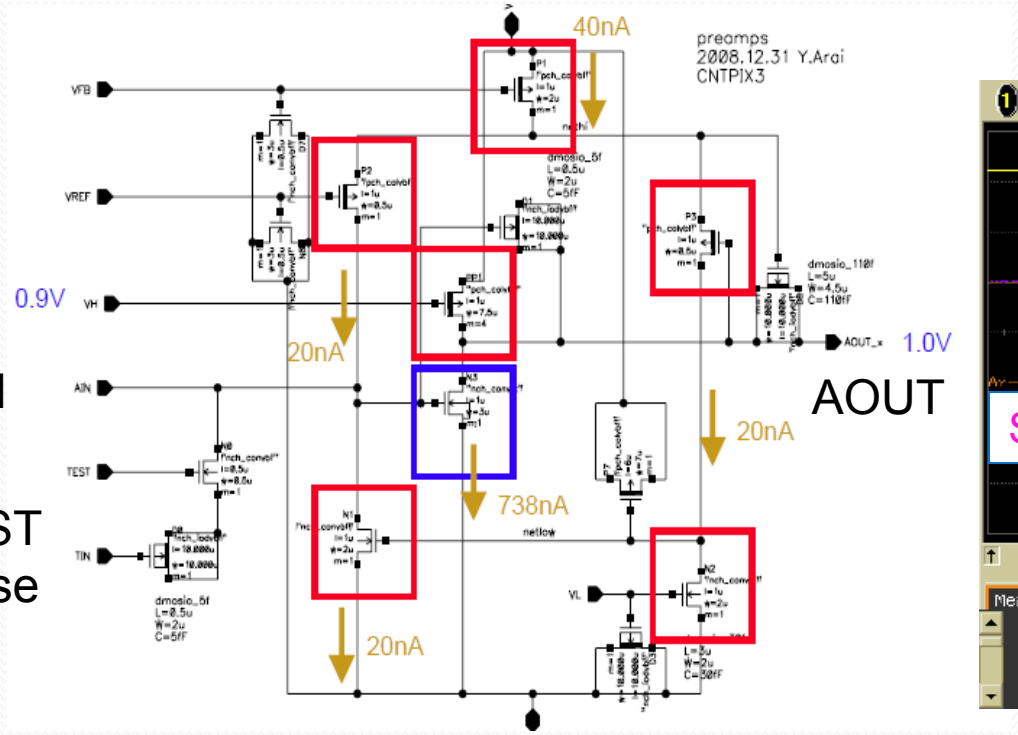


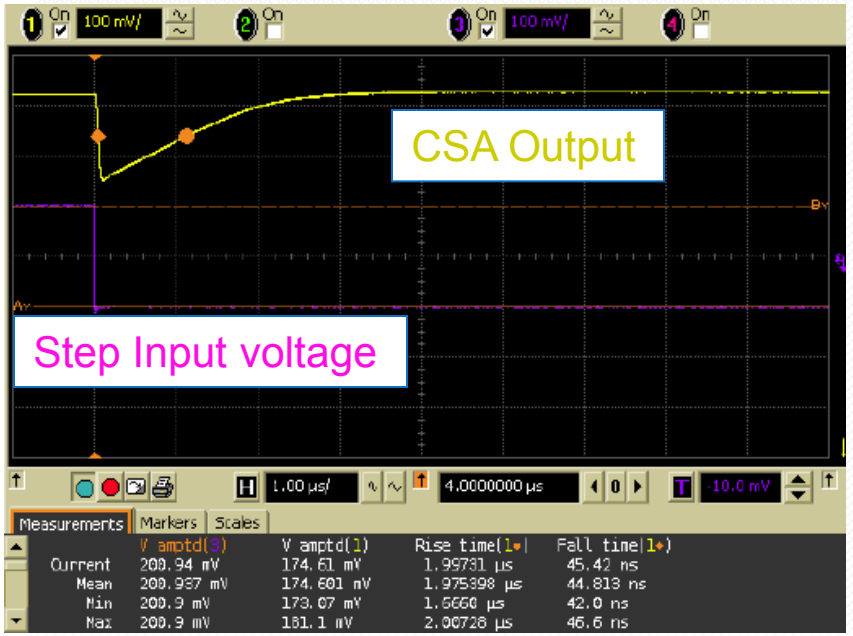
Energy selection and Counting in each pixel

Same architecture with HEP/NP pixels -> We are developing a prototype for next Belle II detector (SBPIX1).

5 x15.4 mm^2
72 x 212 pixels
64um x 64 um pixel

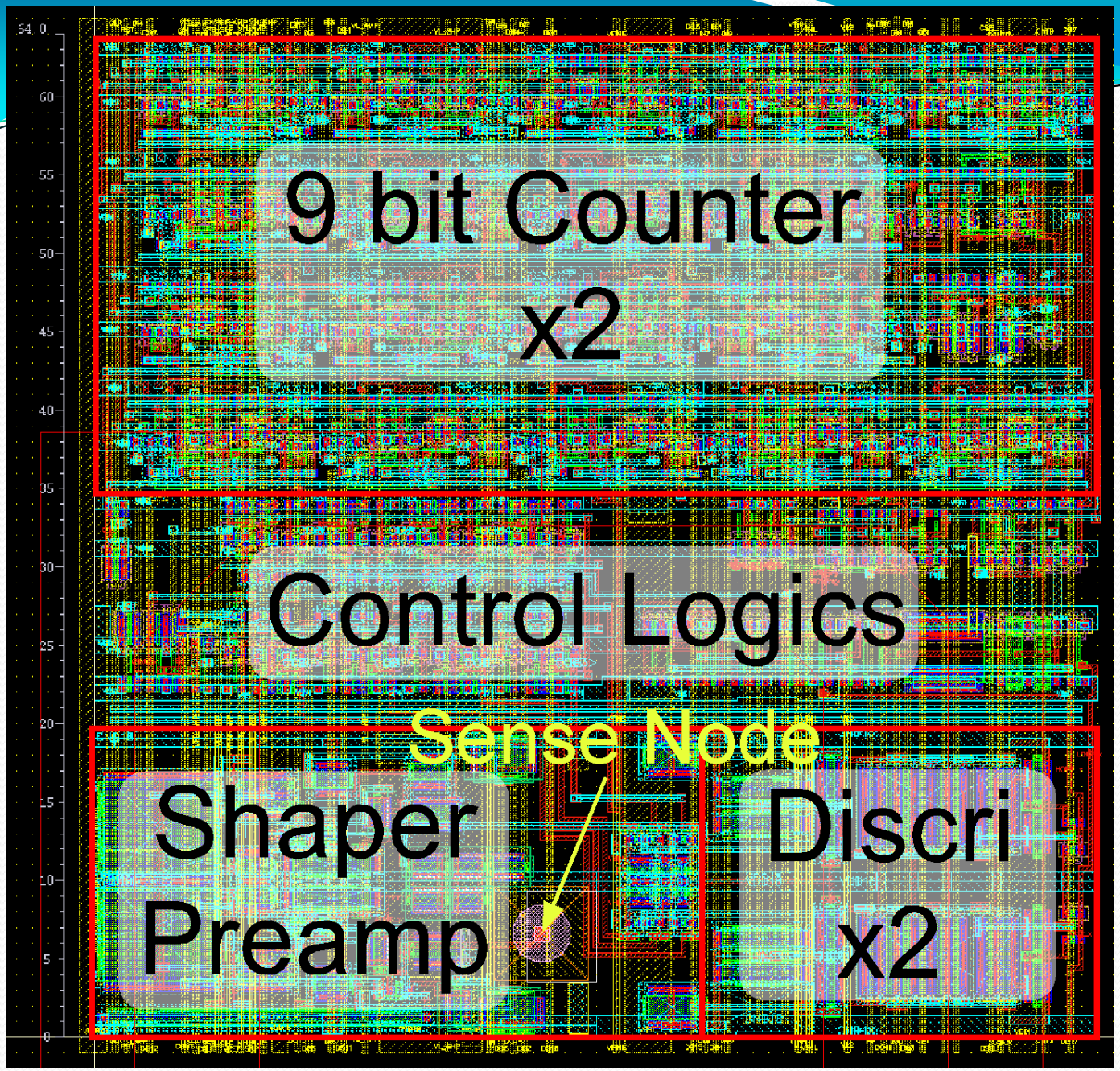
Counting Type Pixel –preamps(CSA)-





TEG31

- Charge Sensitive Amp with sensor leakage current compensation circuit (F.Krummenacher, NIM **A**305 (1991) 527-532)
- Gain : 23.4μV/e^-, ENC: 61.2e^-

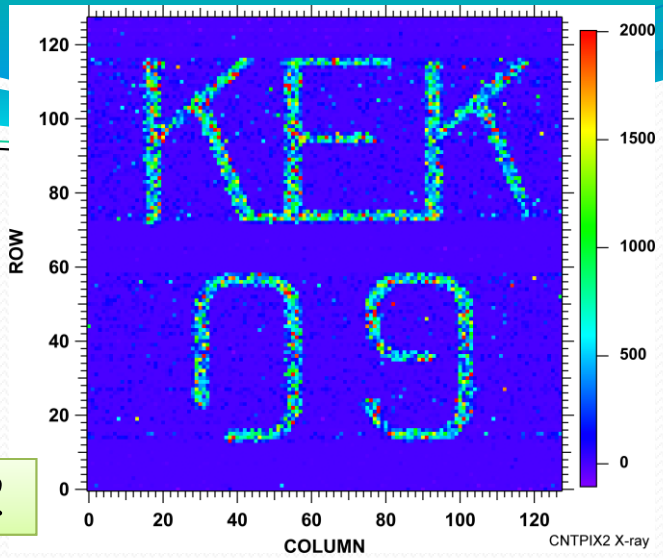


CNTPIX5
Pixel Layout

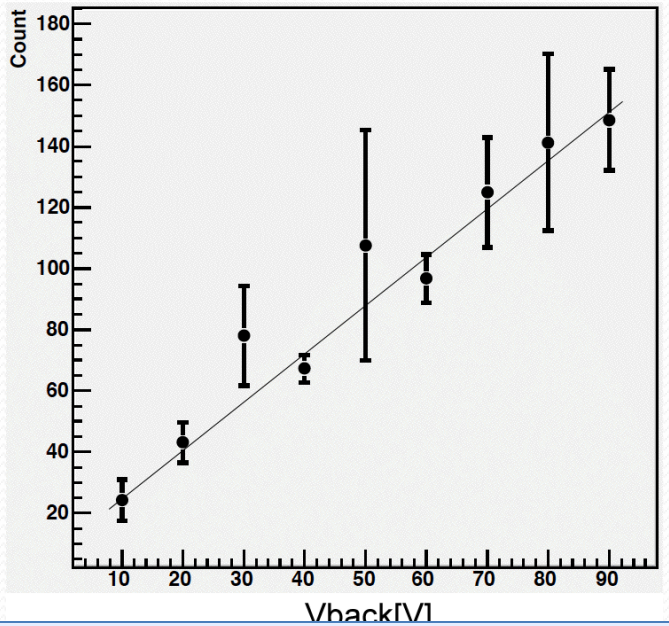
64x64 um²

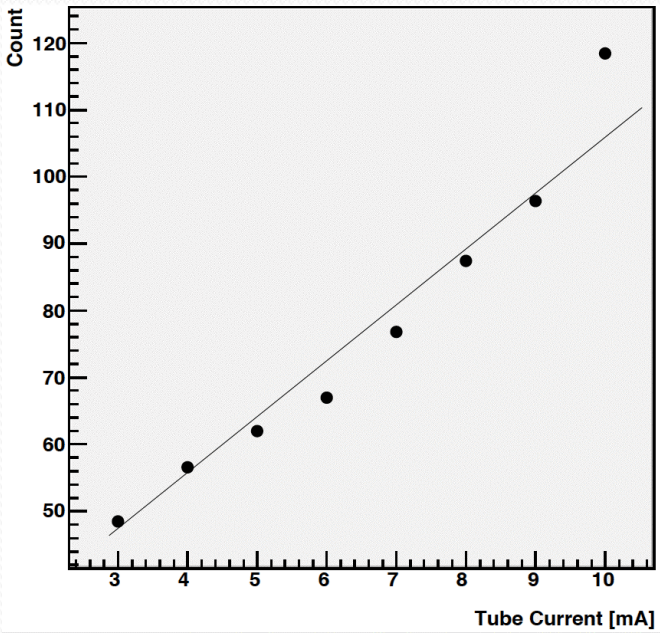
~600 Tr/pix
x 72 x 212
= 10,000,000 Trs

CNTPIX Measurement with X-ray



CNTPIX2





Counting is increased with sensor bias voltage increase, but its behavior is unstable.

Counting is increased with x-ray tube current increase, but insufficient linearity is obtained.

SOI Pixel Issues & Solutions

a. Back Gate Effect : Sensor voltage affect Tr. characteristics
→ Buried P-Well (BPW) layer

b. Wafer Thinning : Thin Sensor
→ TAIKO process

c. Wafer Resistivity: FZ(n, p) wafer and back-side process

d. Cross Talk & Radiation Hardness : Reduce coupling between Sensor and Circuit & control Back gate voltage
→ Nested BNW/BPW, Double SOI Wafer

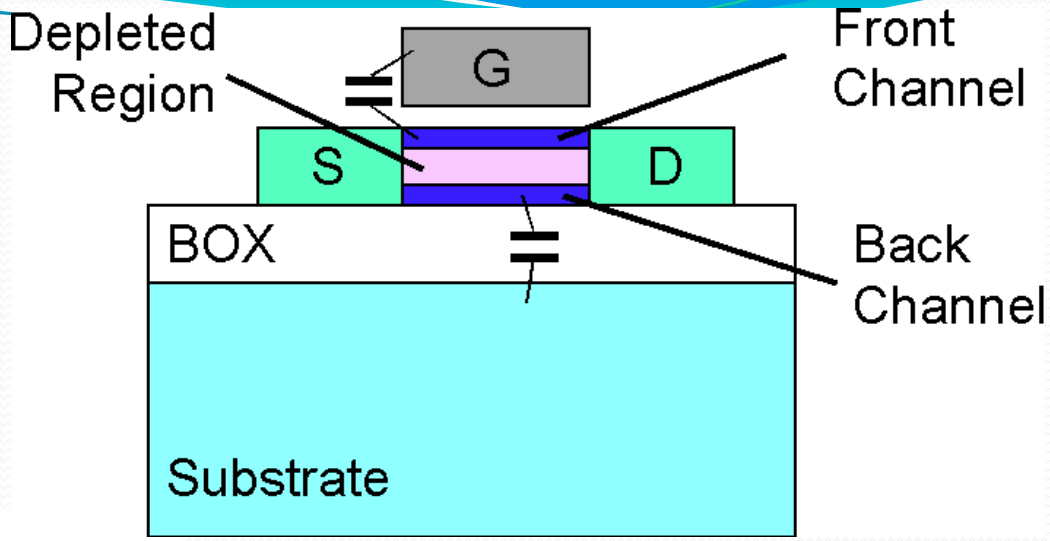
e. Higher Circuit Density : Increase pixel functionality. →
Vertical (3D) Integration

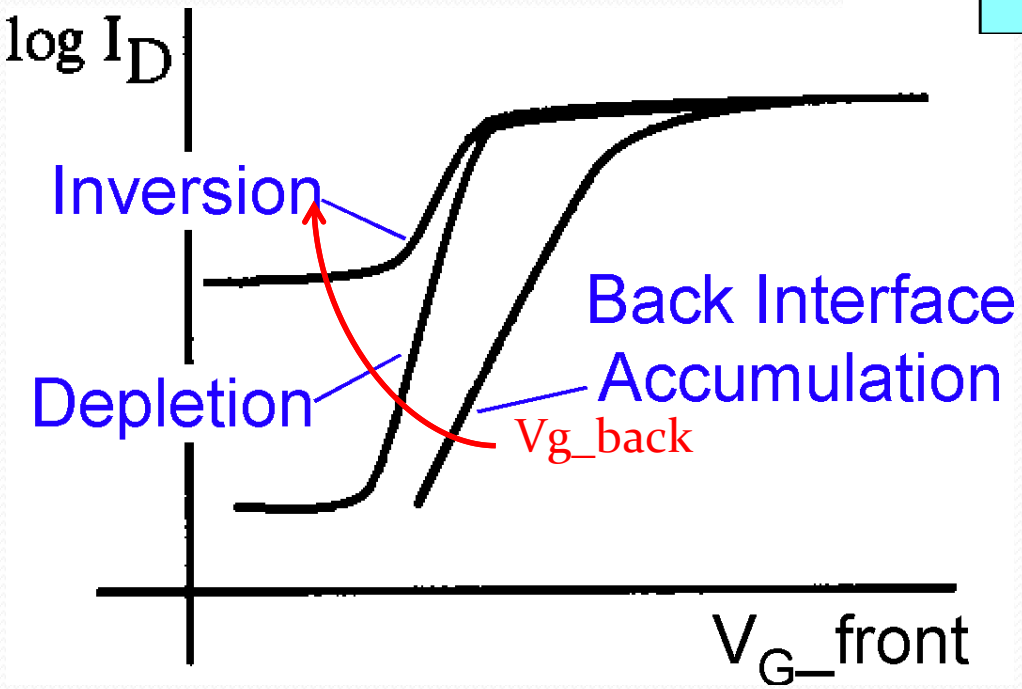
f. Larger Detector: Cover Large area

→ Larger Mask & Stitching

a. Back Gate Effect

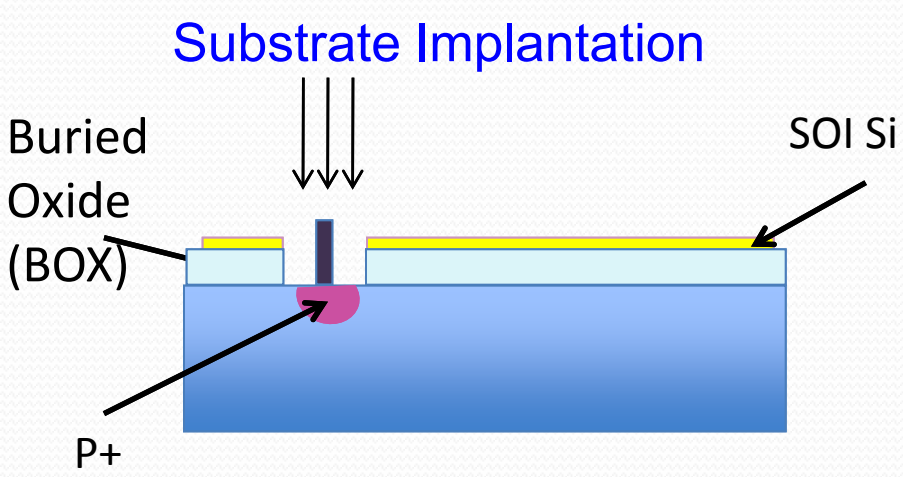
Front Gate and Back Gate are coupled. (Back Gate Effect)

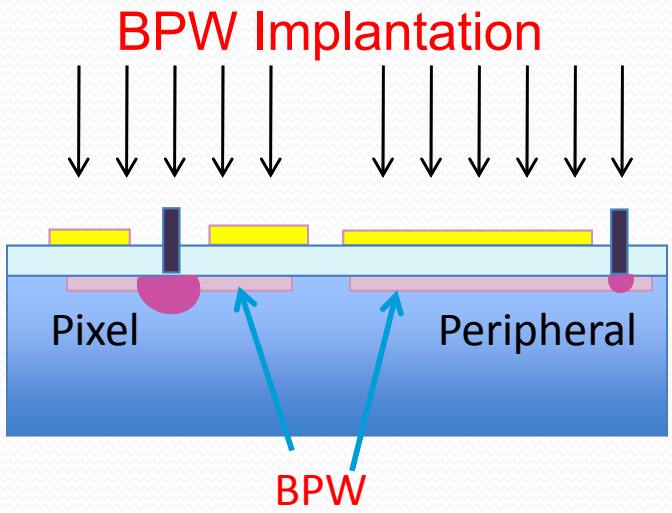




$$\Delta V_{TH\_front} \approx \frac{C_{gate\_oxide}}{C_{BOX}} \Delta V_{G\_back}$$

Buried p-Well (BPW)





- Cut Top Si and BOX
- High Dose

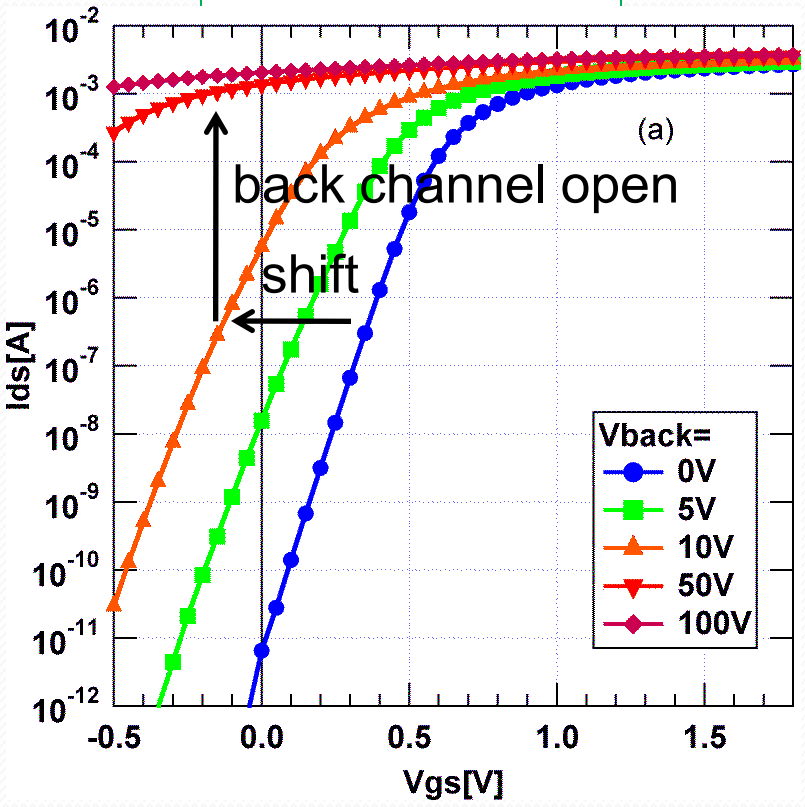
- Keep Top Si not affected
- Low Dose

- Suppress the back gate effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which may improve radiation hardness.

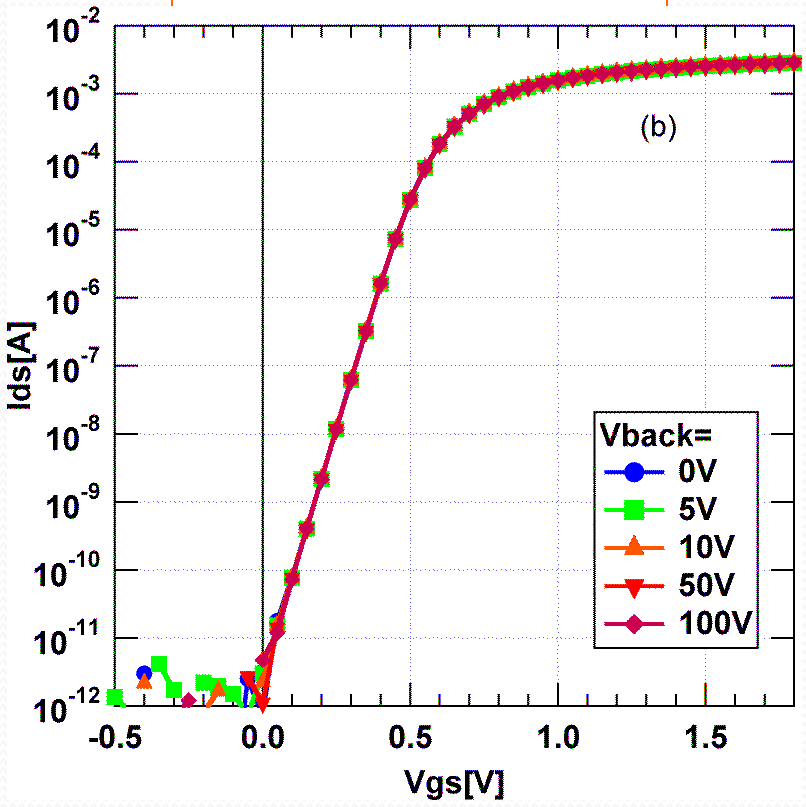
I_d-V_g and BPW

NMOS

w/o BPW



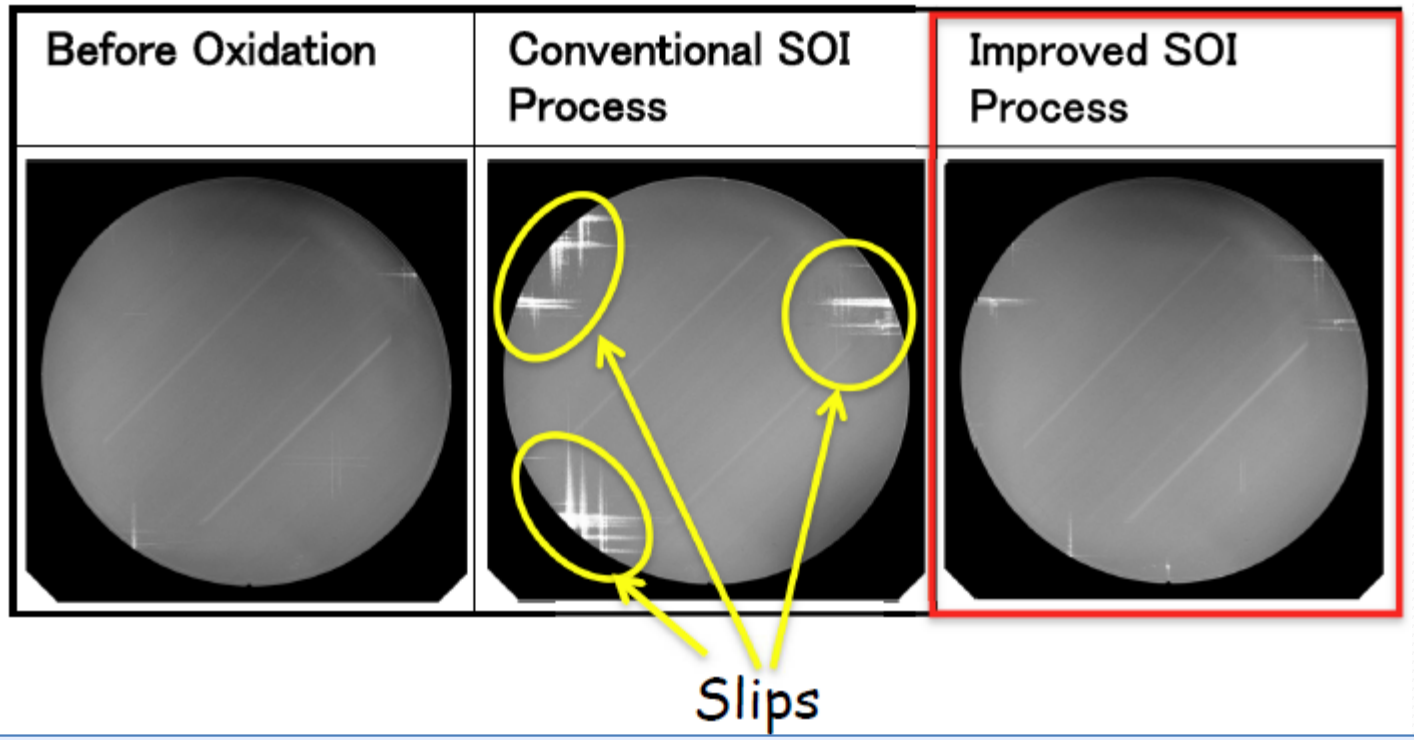
with BPW=0V



Back gate effect is suppressed by the BPW.

c. Thicker depletion layer (FZ SOI wafer)

During the conventional SOI process, many slips were generated in the 8'' FZ-SOI wafer.

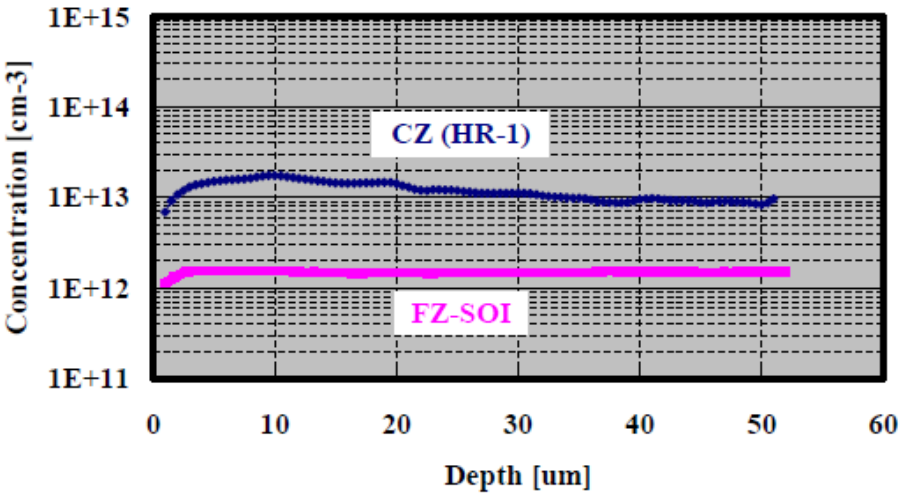


From the effort by an SOI wafer vendor and improvement of thermal process recipes, slip of FZ wafer can be reduced as it can be used for SOIPIX detector.

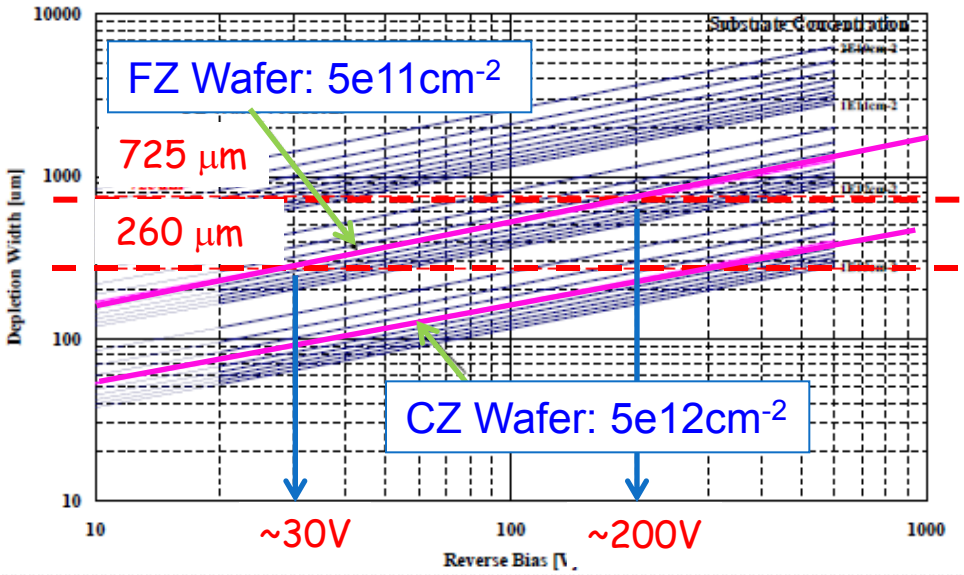
c. Thicker depletion layer (FZ SOI wafer)

- Carrier concentration is determined by C-V method at 10V point.
  - FZ: 5e11cm^{-2}(~10kΩ·cm), CZ: 5e12cm^{-2} (~1kΩ·cm)
- We confirmed them and their flatness in depth with SR method.
- FZ wafer shows one order advantage to gain thicker depletion layer.

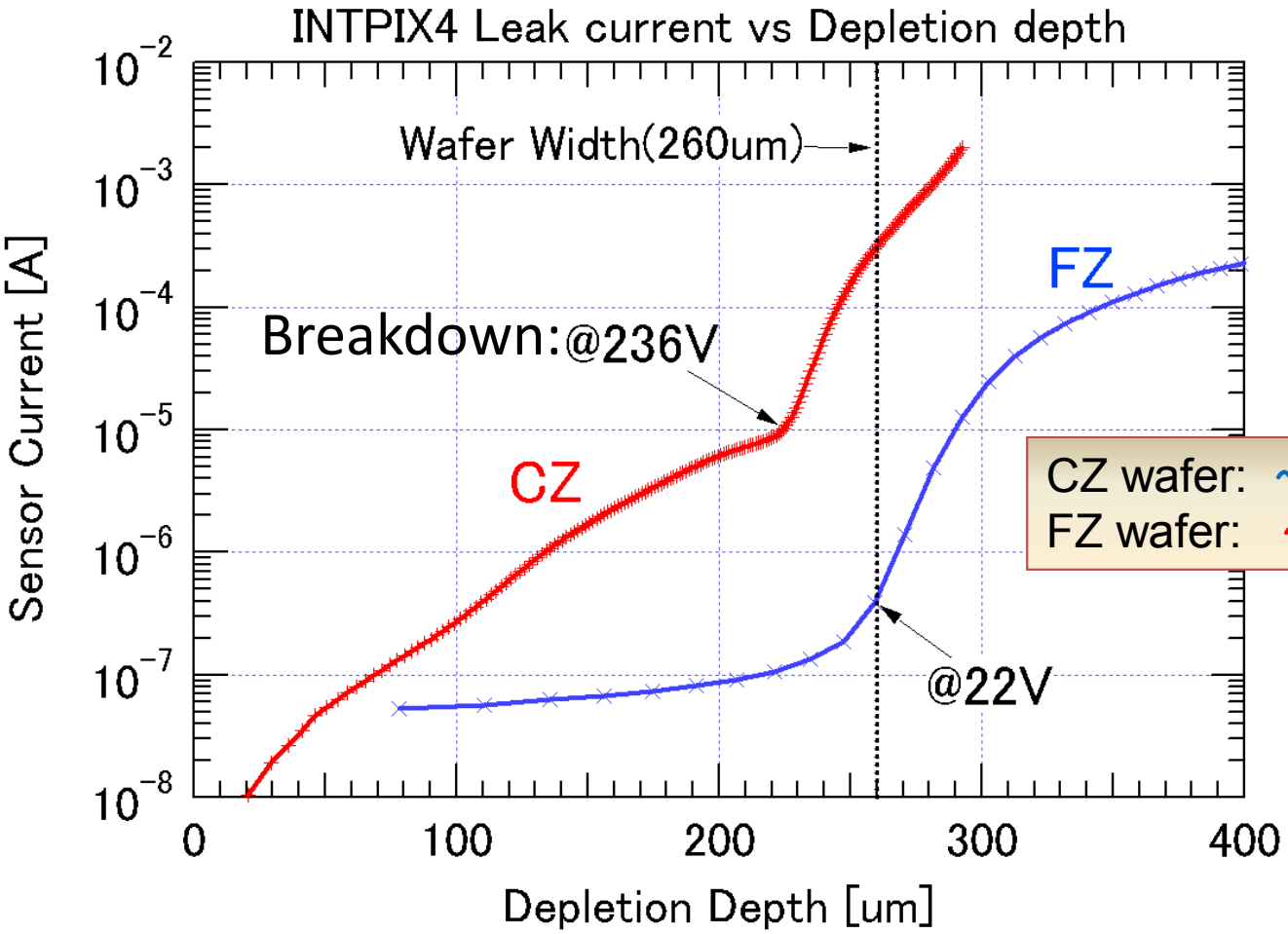
Spreading Resistance (SR) Measurement



Depletion depth vs Bias Voltage



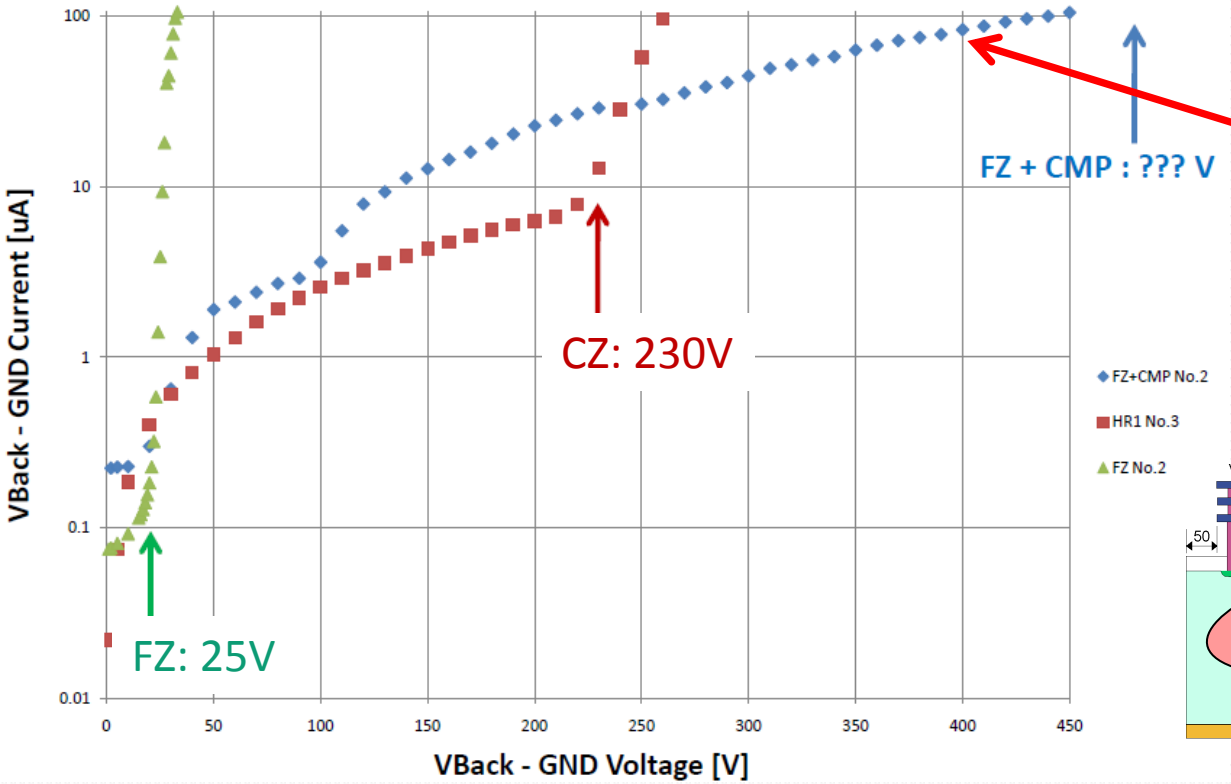
c. Thicker depletion layer (FZ SOI wafer)



CZ wafer: ~1kΩ cm (5e12cm^{-2})
FZ wafer: ~10KΩ cm (5e11cm^{-2})

FZ wafer of 260μm is fully depleted @~22V

c. FZ with backside polishing (CMP)



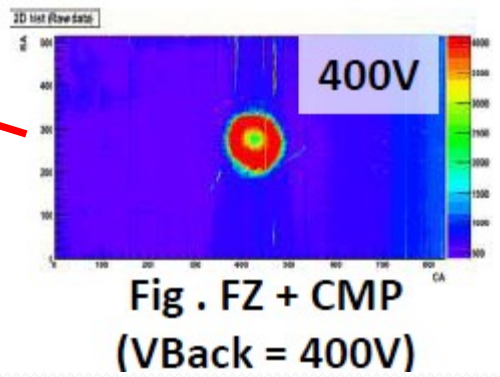
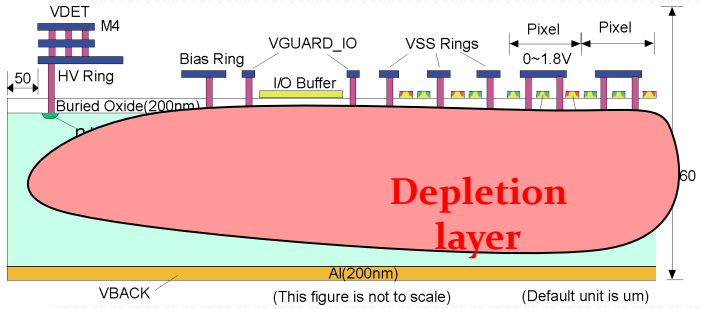


Fig . FZ + CMP
(VBack = 400V)



Backside polished sensor can be operated at V_{det}=400V, without increasing leakage current so much.

Note: Sensor width = 250μm (full deplete @22V); Over-depleted.

Summary

- SOI detectors have become working detectors with 6 years study.
- Although we had several difficulties to maintain the SOI process, we run regular twice MPW runs a year and have very good collaboration with OKI semiconductor.
    - This year: we have only one MPW run; tentatively scheduled on October.
- Main issue to realize the SOI pixel, back-gate effect, has been solved by Buried P-Well.
- Many R&D items are on-going to improve the performance of the SOI pixel detector (FZ, Nested BNW/BPW, 3D, Double SOI, stitching, radiation tolerance,…)
- We recognize that the SOI pixel comes to the stage of practical use, although there are still some items to be improved.
- Although tremendous Earthquake hit Japan, we are OK and we shall continue working on…

Supplement

http://www.shimano.com/publish/content/global_cycle/en/us/index/products/road/105_5700.html

KEK-OKI semiconductor SOI Brief History

'05. 7: Start Collaboration with OKI Semiconductor.

'05.10: First Submission in VDEC 0.15 μm MPW.

'06.12: 1st (and last) 0.15 μm KEK MPW run.

'07.3: 0.15 μm lab. process line was closed.

--> move to 0.2 μm mass production line.

'08.1: 1st KEK SOI-MPW run.

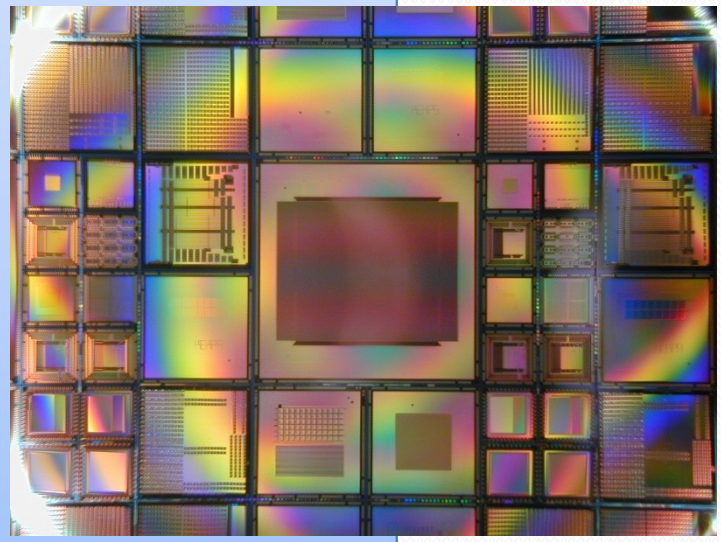
'09.2: 2nd KEK SOI-MPW run.

'09.8: 3rd KEK SOI-MPW run.

'10.1: 4th KEK SOI-MPW run.

'10.8: 5th KEK SOI-MPW run.

'11.1: 6th KEK SOI-MPW run



Readout system for SOIPIX

- We have developed a Ethernet-based (SiTCP) DAQ board for SOIPIX, named SEABAS (SOI EvAluation BoArd with Sitcp).
- Portable DAQ system; same software with Linux, Windows, Apple, etc.