Interconnection technology for ATLAS pixels in the SLID-TSV process

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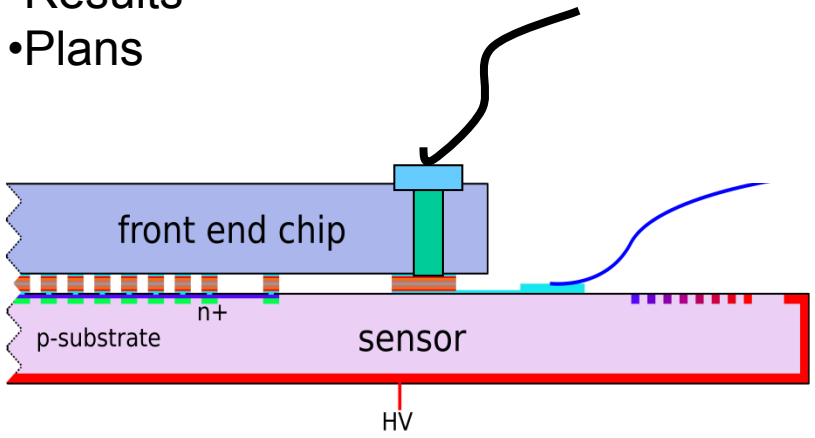
- Motivation
- Production of thin sensors
- SLID and TSV by Fraunhofer EMFT
- Sensor/ASIC assembly
- Results
- Plans



L. Andricek, P. Weigell, R. Nisius, A. Macchiolo, H-G Moser, R. Richter

FEE 2011
Bergamo, Italy
May 24-27, 2011

Motivation

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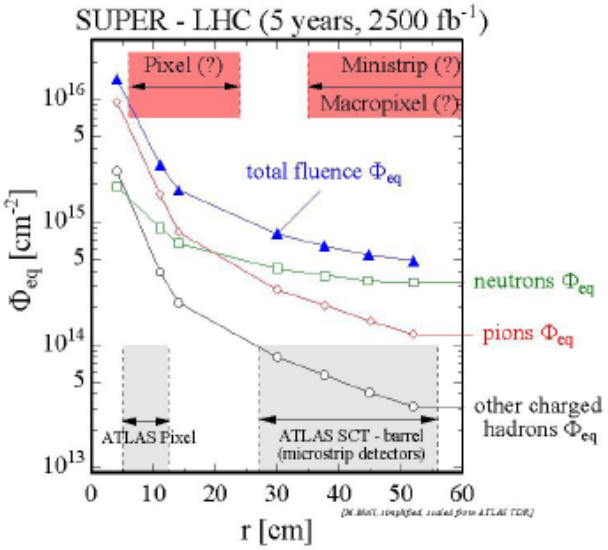
ATLAS pixel detector upgrade for sLHC

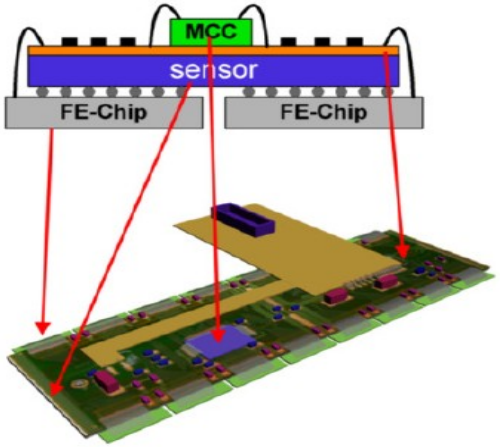
-Radiation hard up to 10^{16} n/cm²
high depletion voltage
high leakage currents
low CCE due to trapping

=> thin detectors



-Optimized module layout
Less material
Lower production costs

=> 3D integration technology



New pixel detector concept based on 3D integration

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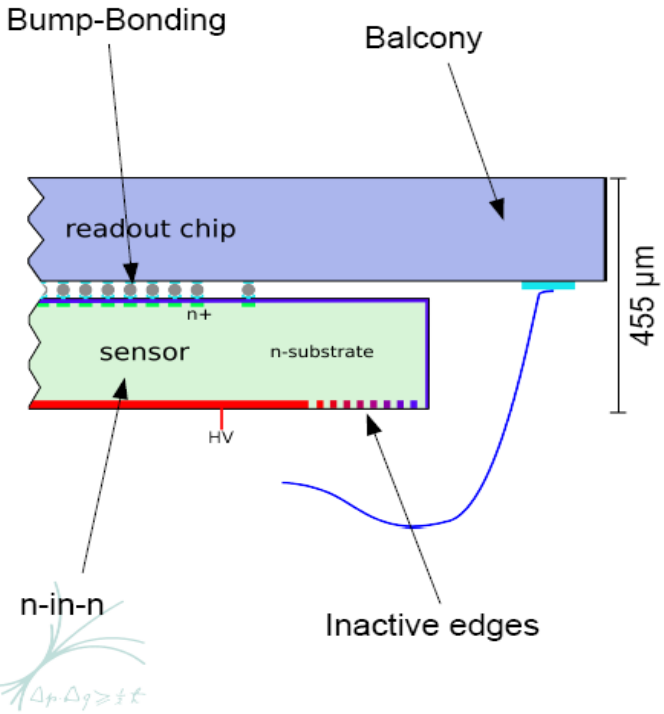
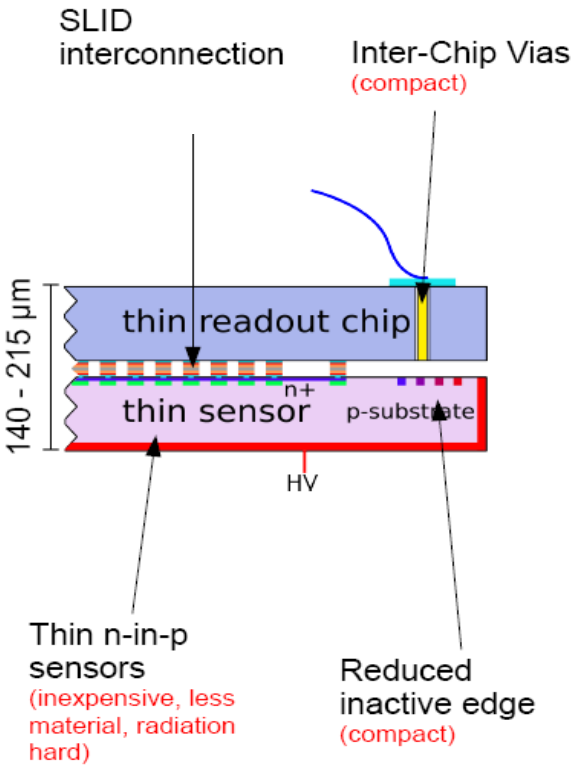
- Thin sensors and ASICs
- Backside connectivity for compact module design (eventually 4 side buttable)
- High density interconnection .

ATLAS standard

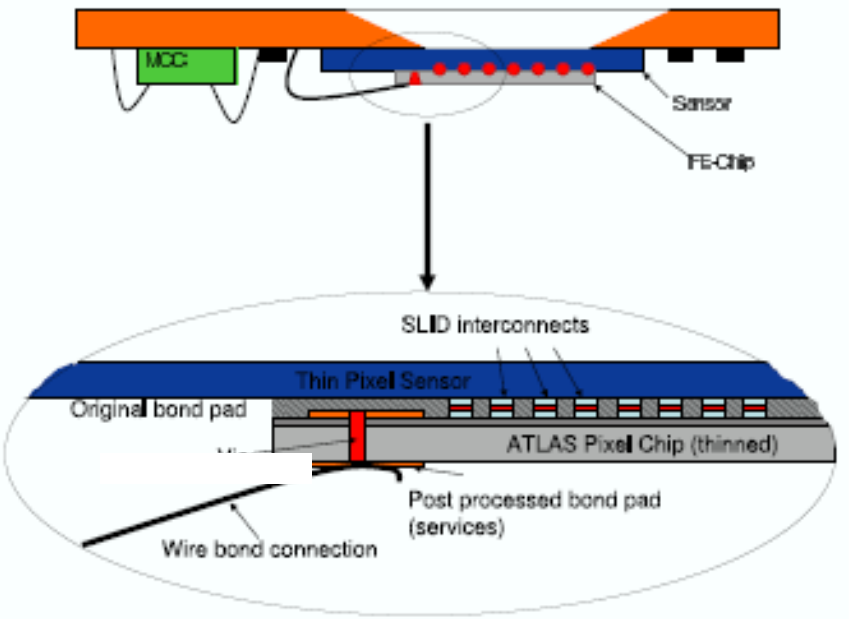


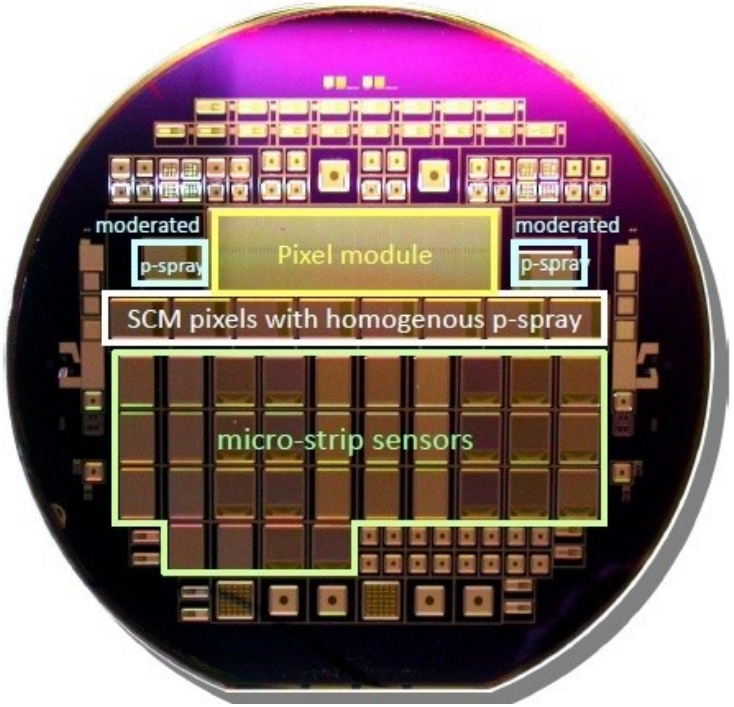
Novel MPP demonstrator



MPI 3D R&D Program

- Build demonstrator using ATLAS pixel chip (FE-I2/3) and thin pixel sensors made by MPI (complete wafers with FEI2, FEI3 chips available!)
- Interconnection with SLID and ICV technology by Fraunhofer EMFT
- Demonstration of postprocessing of standard ASICs with via last





test sensors (strip, pixel)
on 75mm and 150µm SOI wafer

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Advantages of Thin Sensors

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High depletion voltage

$U_{dep} \sim d^2$

High leakage currents

$I_{leak} \sim d$

Trapping:

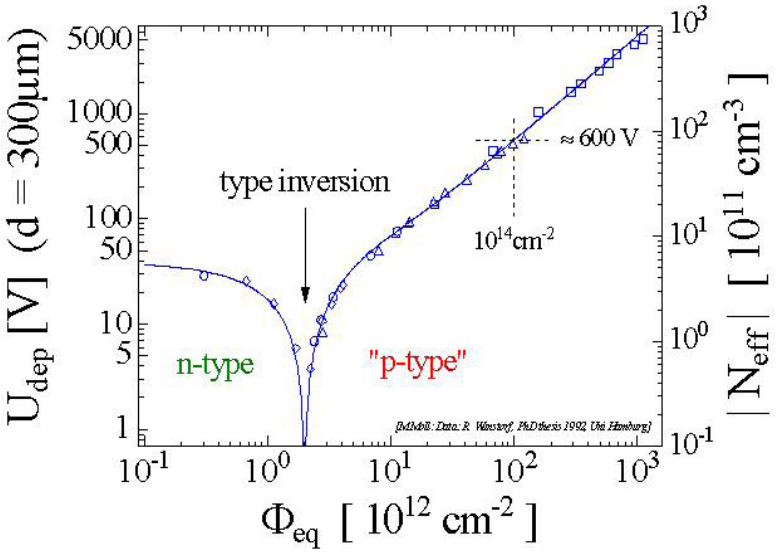
CCE reduced if $l_{trap} < d$

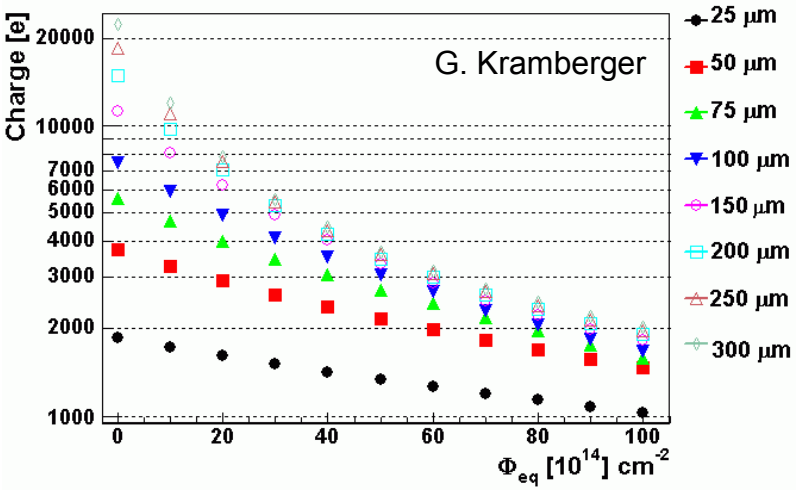
However:

Thin detectors have always a lower signal, even unirradiated

-> need good FEE

Last but not least: less material





Thinning Technology at MPI Semiconductor Laboratory

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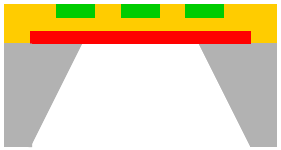
1) Process backside of thick detector wafer. For n-in-n detectors a structured implant is needed.

2) Bond detector wafer on handle wafer (SOI technology)

3) Thin detector wafer to desired thickness (grinding & etching).

4) Process front side of the detector wafer in a standard (single sided) process line.
Perfect backside protection!

5) Etch handle wafer.
If necessary: add Al-contacts
Leave frame for stiffening and handling, if wanted



Sensor Thinning: Examples

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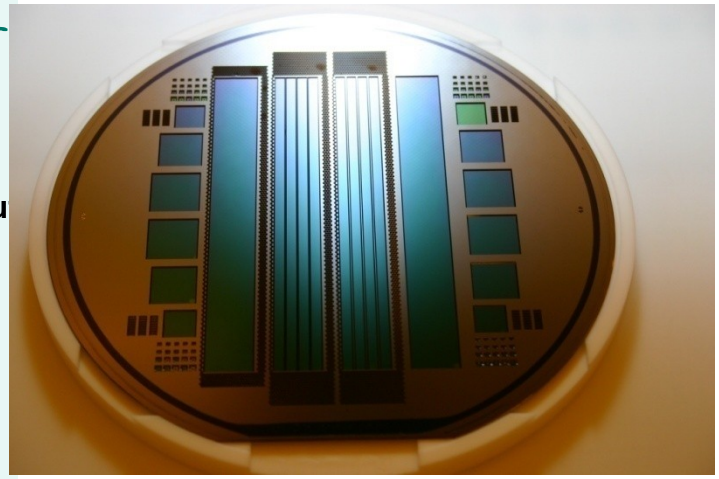
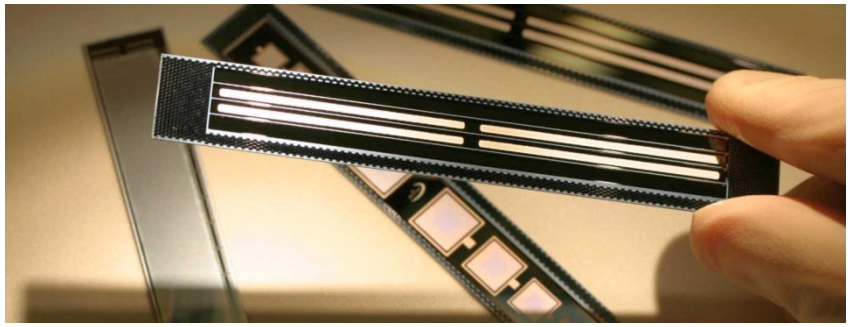
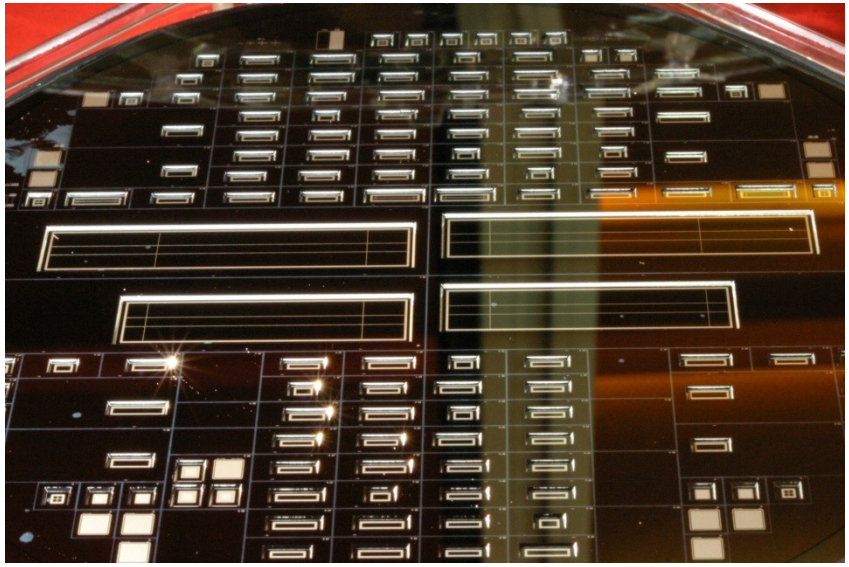


Diodes and large mechanical samples



ILC models (10 cm x 1 cm x 50µm

Belle II samples (50µm)



DEPFET active pixel sensors for Belle II
Wafer before cutting (50 µm thick)

Sensors

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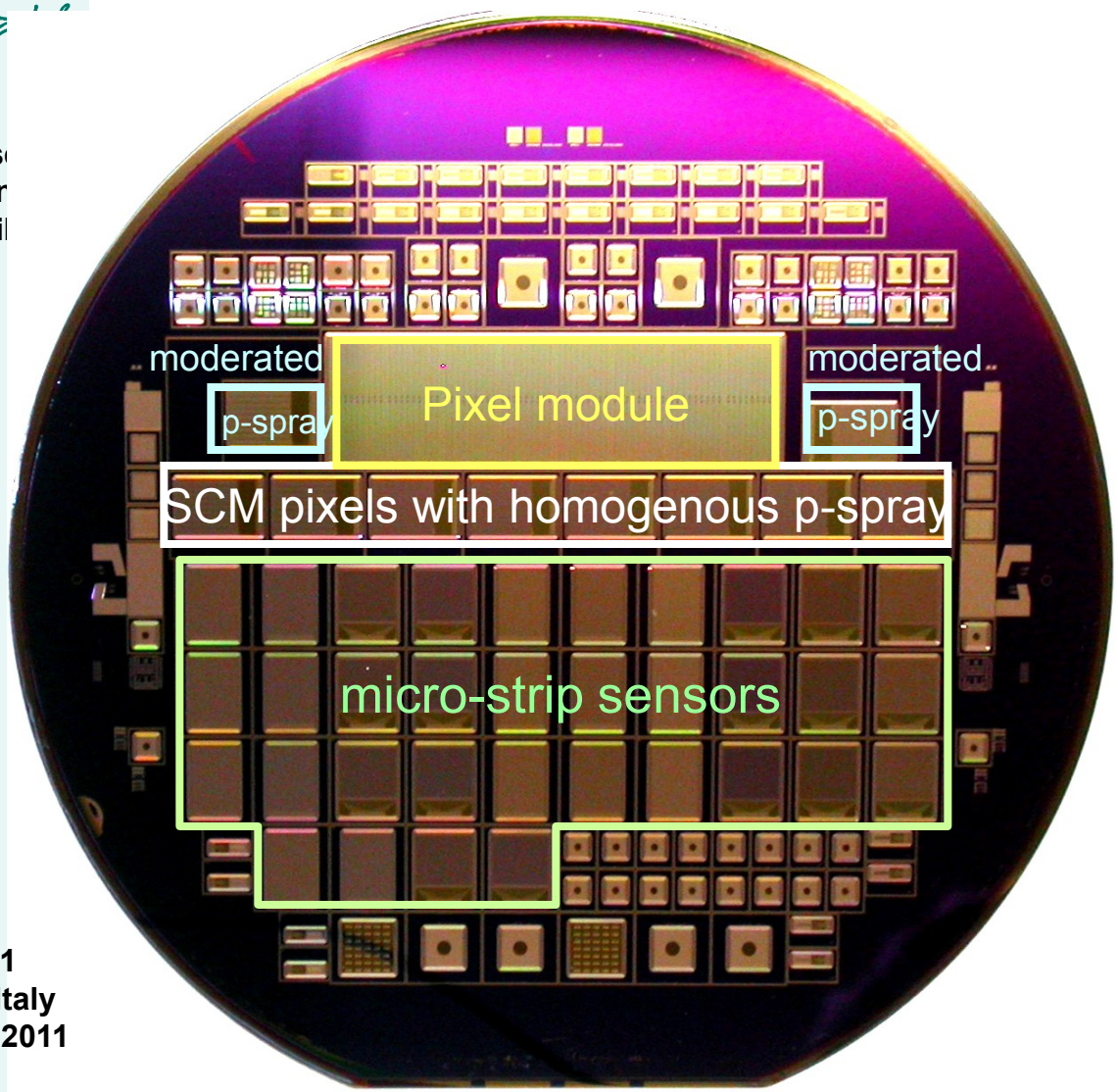
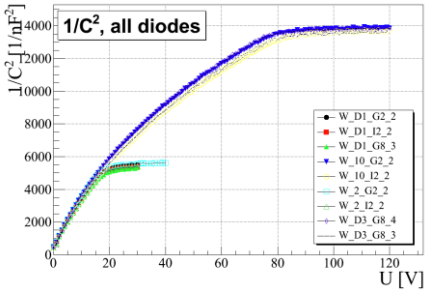


In house production on
6” FZ-SOI material (2 kΩcm)

Top wafer thickness
75 µm and 150 µm

p- and n-type material
p-spray insulation

Footprint for ATLAS FEI3



U_{dep} 20V and 80V

Irradiation Tests

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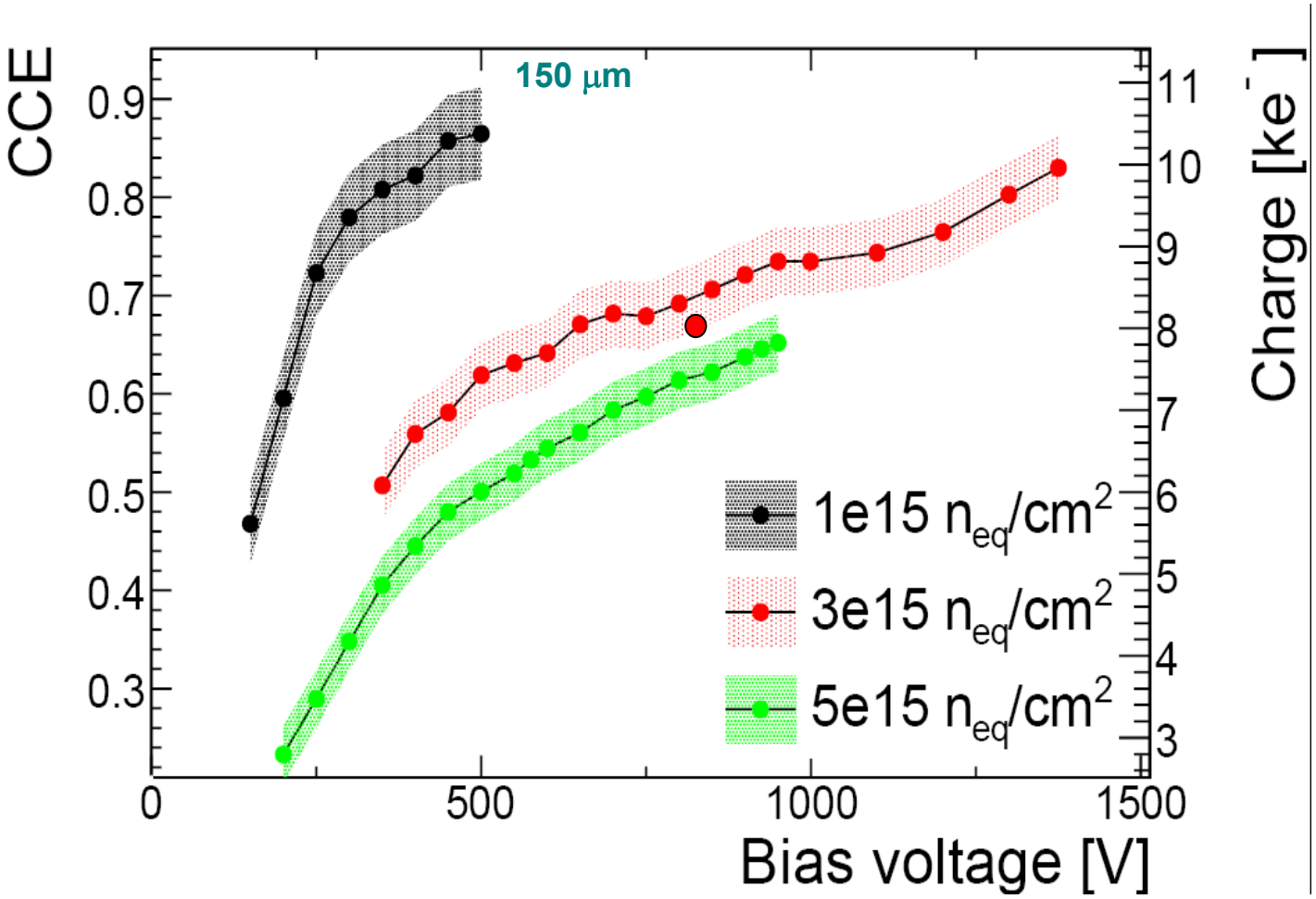
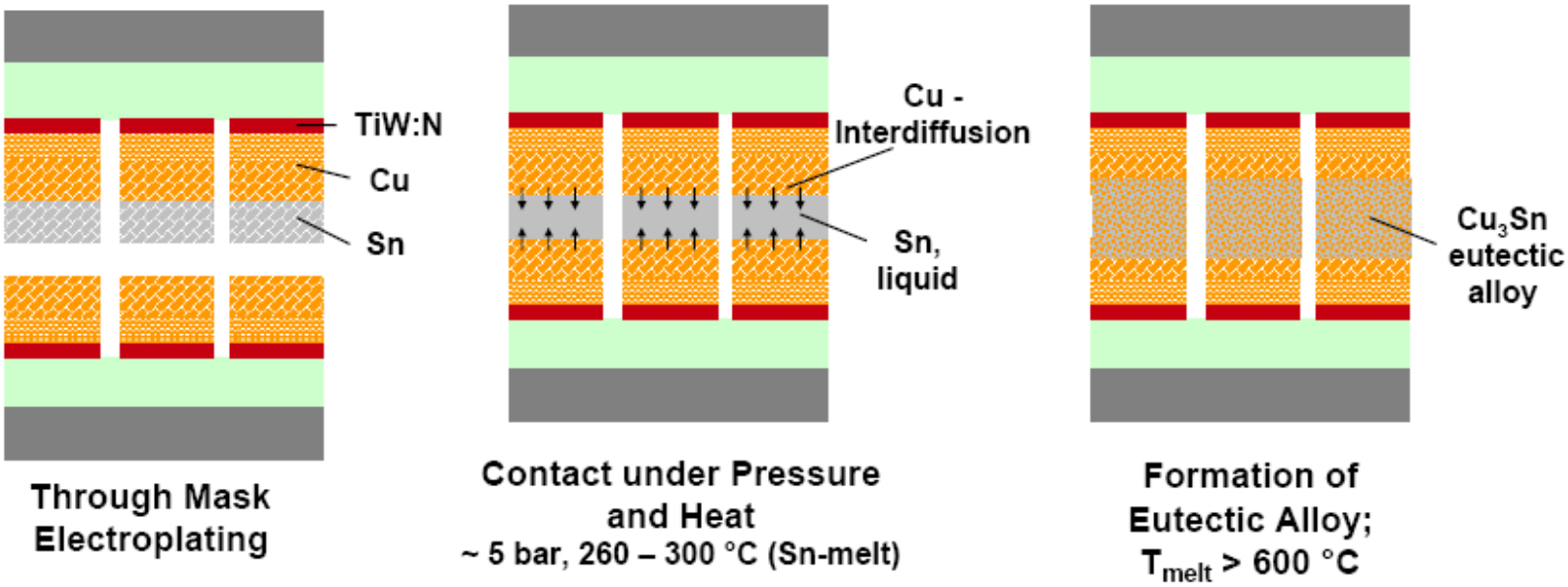


CCE measurements after irradiations

=> Almost complete signal charge can be recovered

IZM SLID Process

Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps “low cost” (EMFT)).
- Small pitch possible (<< 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

- However: no rework!

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Fraunhofer EMFT

Through Silicon Vias

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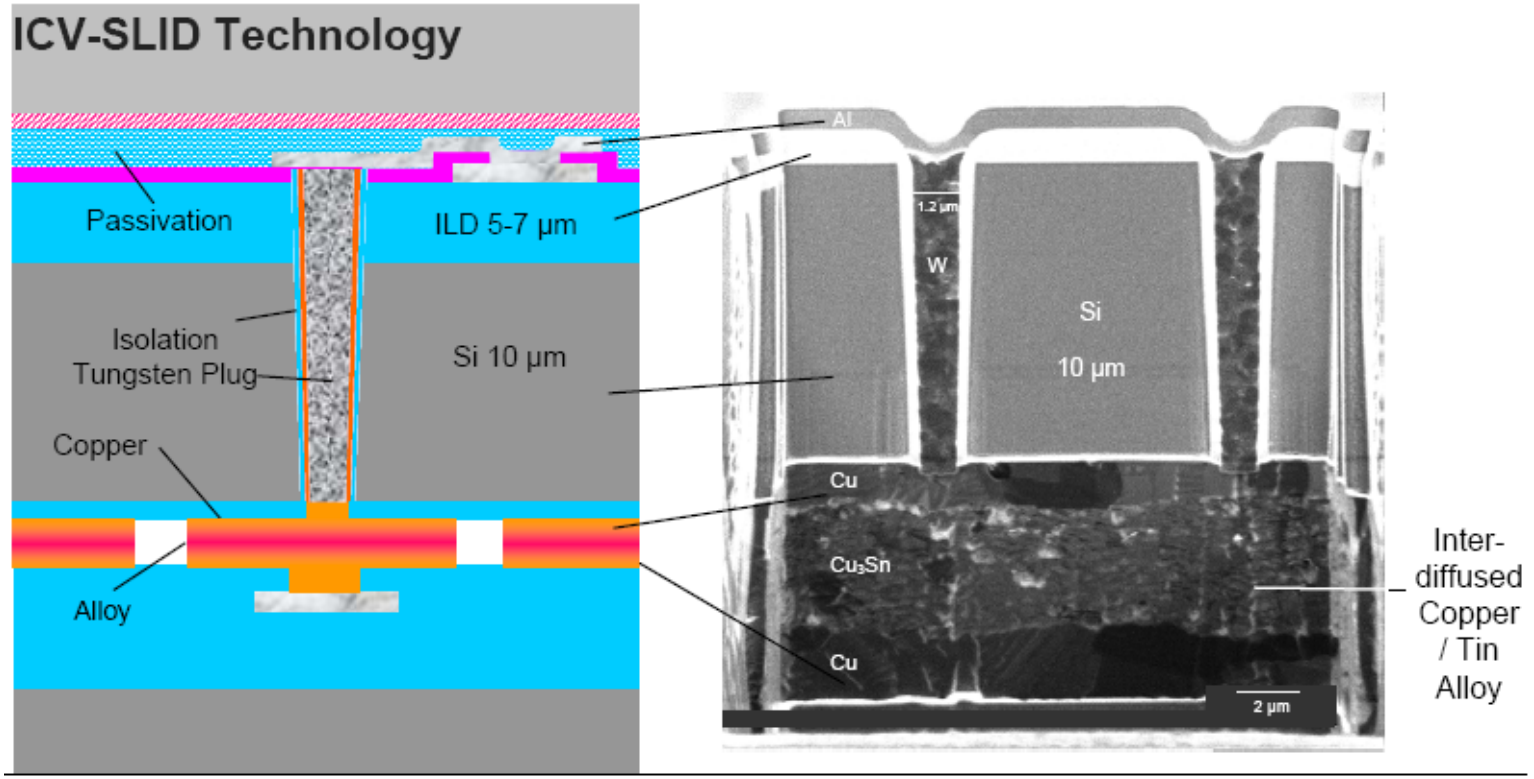

ICV = Inter Chip Vias

- Hole etching and chip thinning
- Via formation with W-plugs.
- Face to face or die up connections.
- 2.5 Ohm/per via (including SLID).
- No significant impact on chip performance (MOS transistors).

Fraunhofer EMFT

Trough Silicon Vias processing

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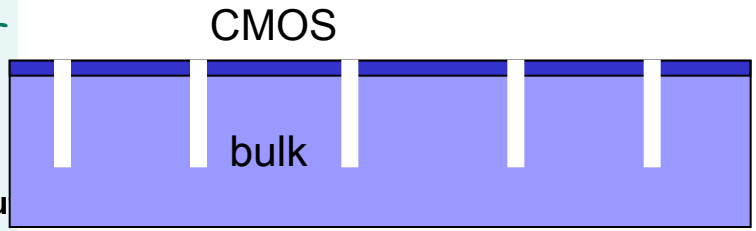
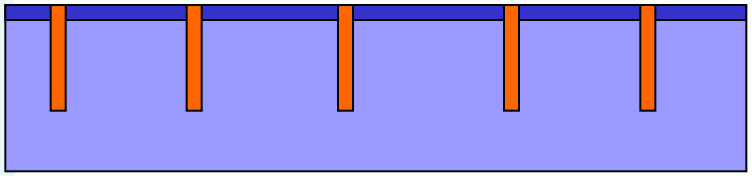
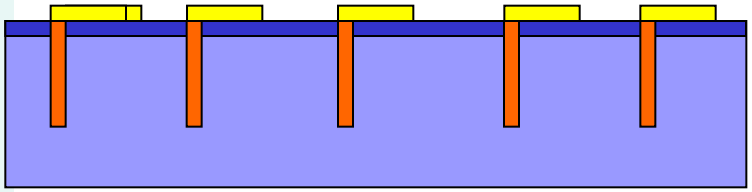


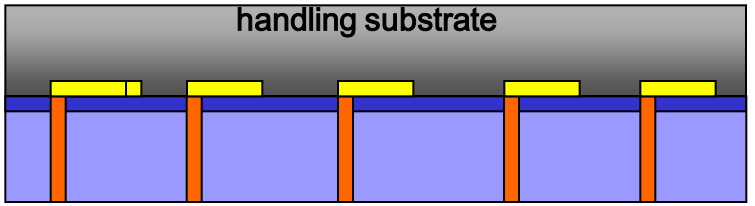
Etching (Bosch process) on FE-I3 8" wafers. 60 µm deep TSVs with lateral dimensions of 3 x 10 µm^2



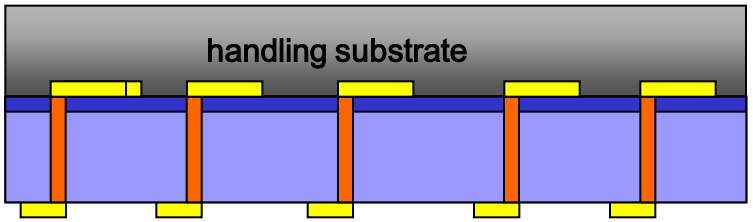
Insulation, filling with tungsten



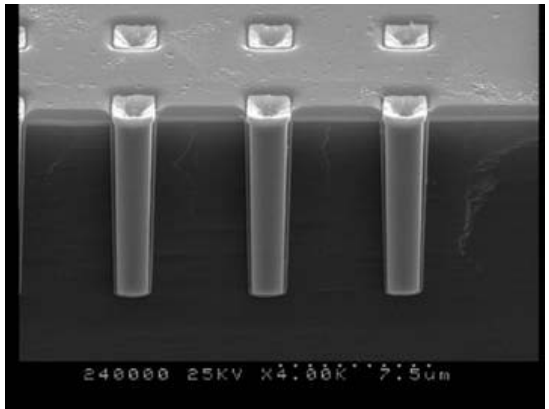
Electroplating, metallization on the ASIC front side



Back thinning to expose the TSV, backside isolation



Electroplating, metallization on the ASIC back side



Fraunhofer EMFT

R&D program

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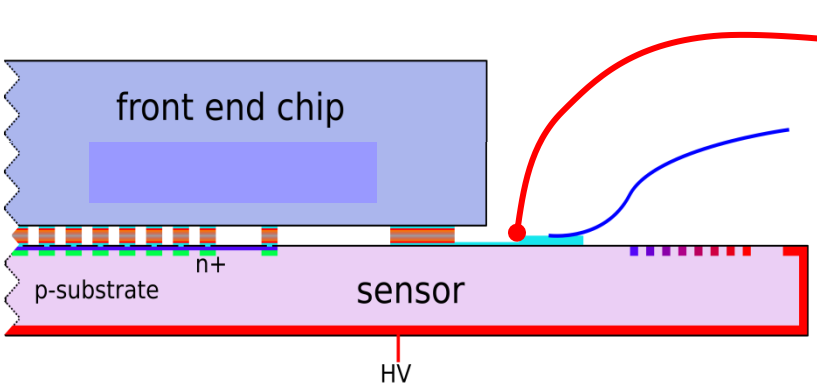
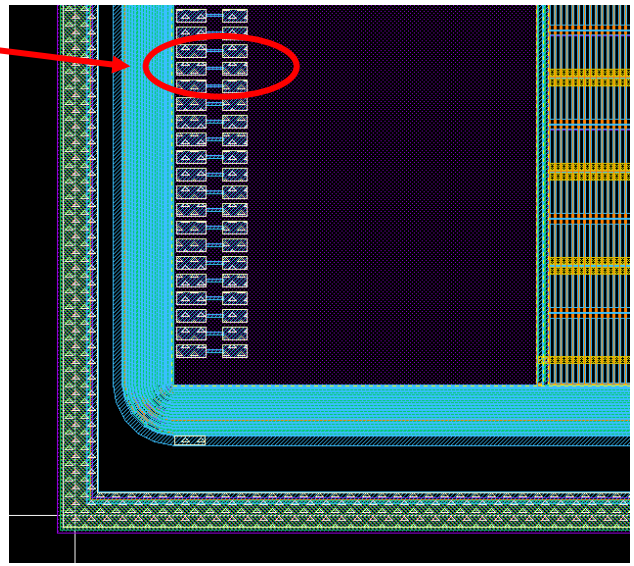
Sensor/ASIC interconnection using SLID
-ASIC thinned to 200 µm
-No vias, integrated fan-out on sensor for service connection

Sensor/ASIC interconnection using SLID
-ASIC thinned to ~50 µm
-vias for service connections (fan-outs for redundancy)

Future: SLID interconnection of sensors/ 3D FEI4





Tests on metal dummies at EMFT

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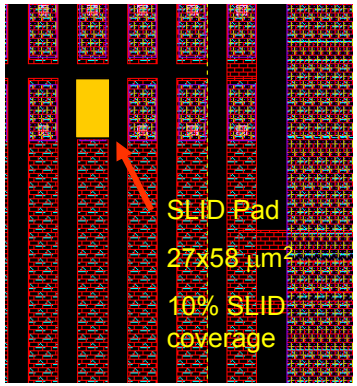
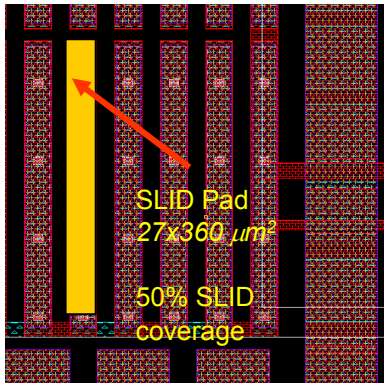
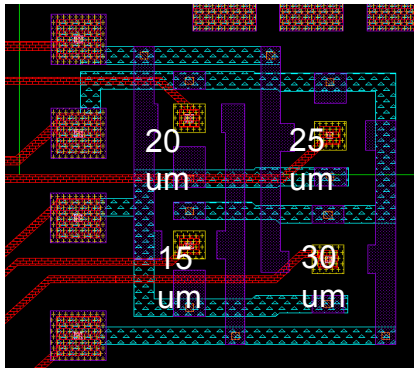
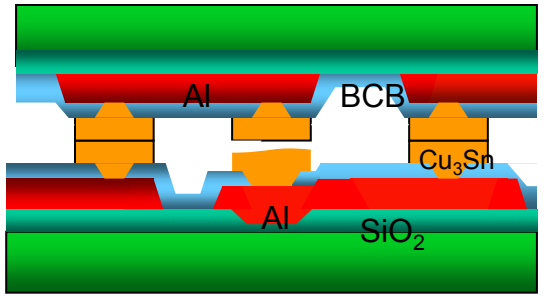
Test of “chip on wafer” SLID interconnection with metal dummies.

- Aim: determine the feasibility of the SLID inter-connection within the parameters we need for the ATLAS pixels.
- Test of the mechanical strength as a function of different area coverage by the SLID pads
- Test the SLID efficiency varying the dimensions of the SLID pads
- Study the SLID efficiency when degrading the planarity of the structure underneath the pads
- Determine the alignment precision between single “chip” and “detector” wafer
- Investigate the BCB isolation capability between the detector and chip surfaces









Test interconnections (SLID)

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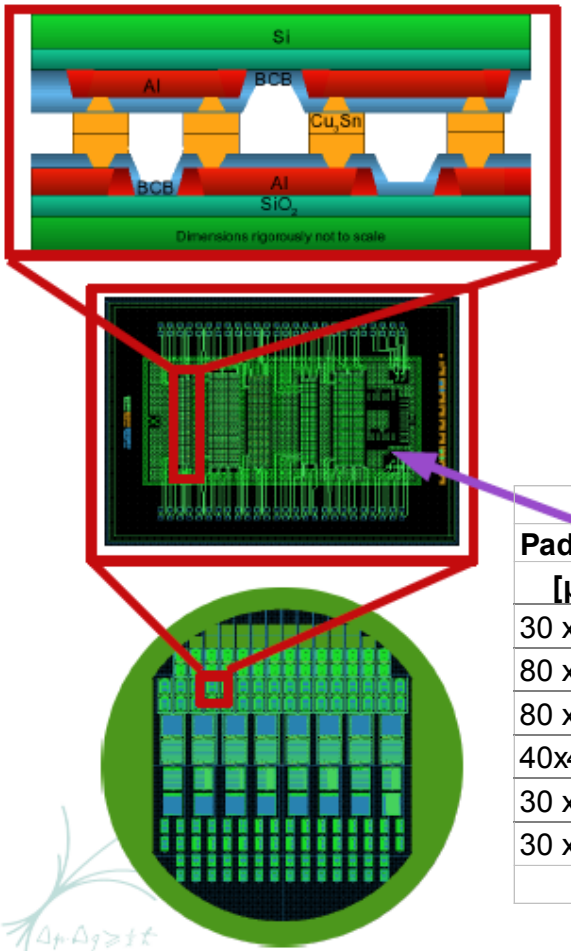
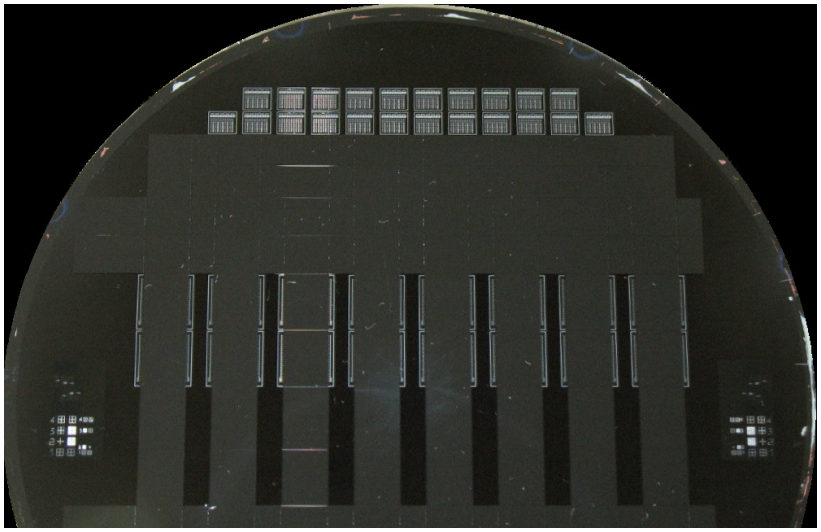
Special test wafers for SLID tests
Chains of SLID connections





Pad width [μm²]	Pitch [μm]	Aplanarity	Number of measured SLID pads	SLID Inefficiency	Resistance per connection [Ω]
30 x 30	60	0	8288	$<4.4\times10^{-4}$	0.73±0.47
80 x 80	115	0	1120	$<3.3\times10^{-3}$	0.29±0.26
80 x 80	100	0	1288	$<2.9\times10^{-3}$	0.25±0.12
40x40	70	0	2016	$<1.5\times10^{-3}$	0.37±0.26
30 x 30	60	100 nm	5400	$(10\pm4)\times10^{-4}$	0.58±0.46
30 x 30	60	1 μm	5400	$(4\pm3)\times10^{-4}$	0.58±0.40

Bonding: chip to wafer

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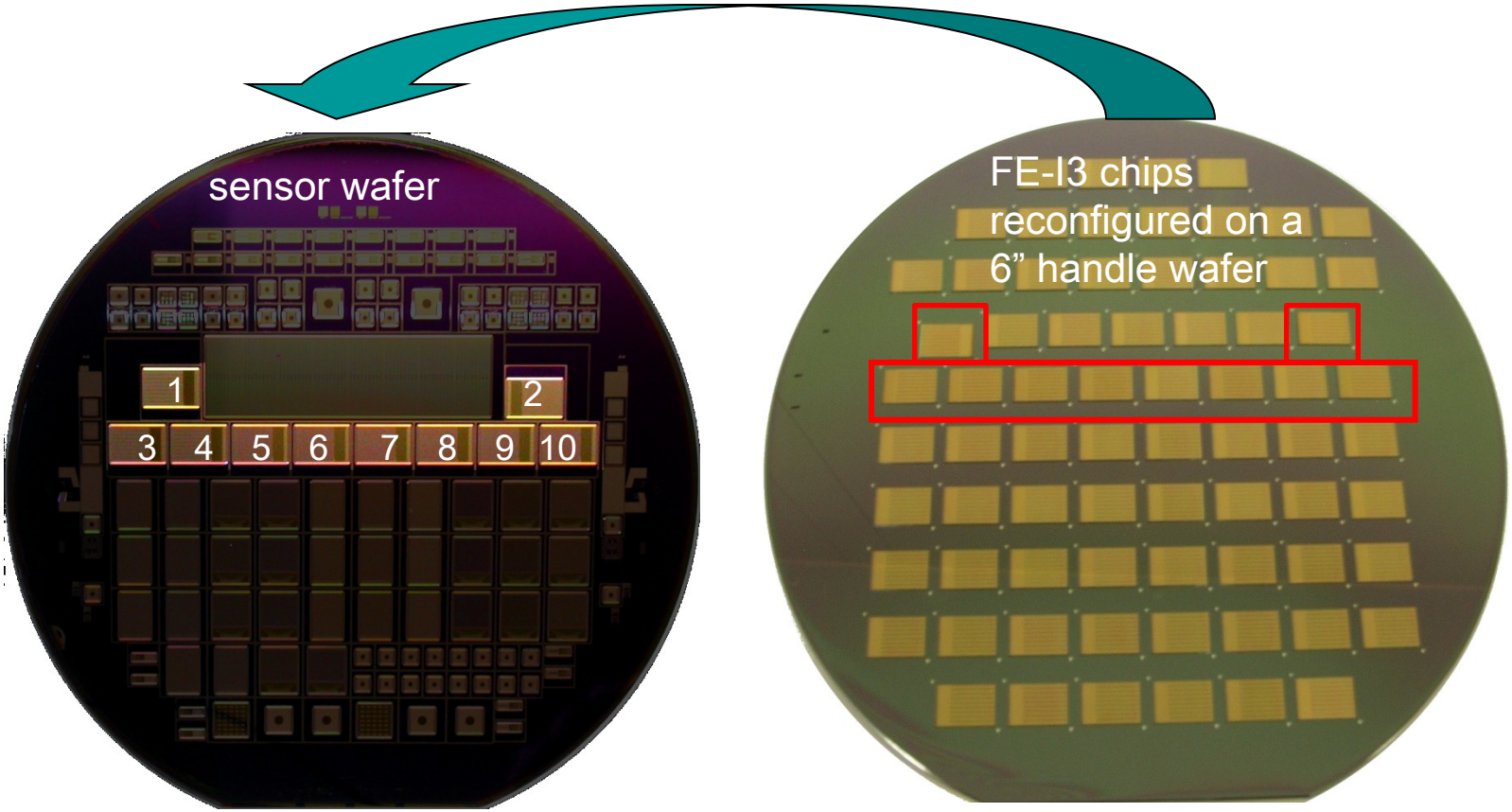


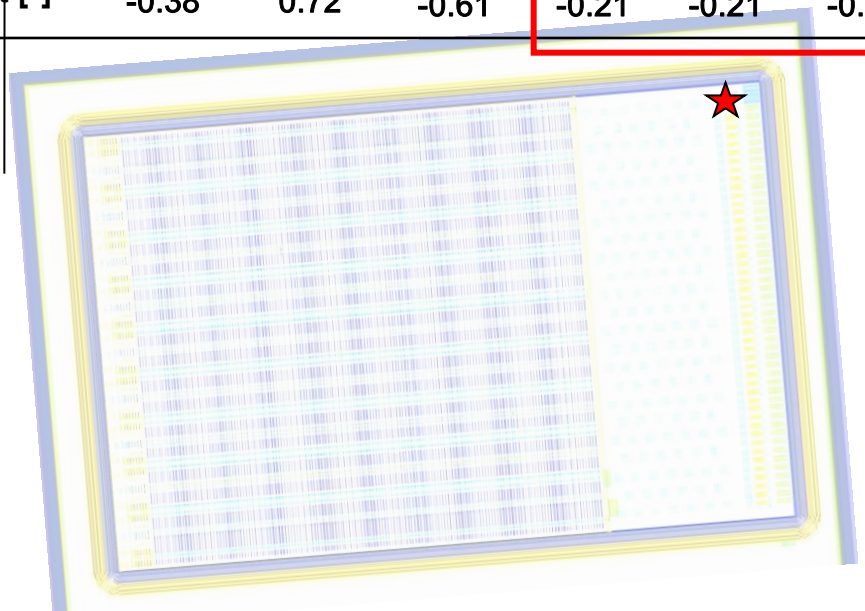
The chips are placed on a handle wafer which is then flipped on the sensor

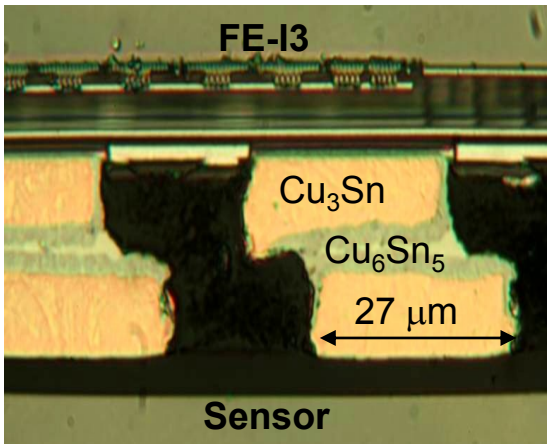
The chips on the handle wafer suffer from misalignment with respect to the nominal positions.

Chip Misalignment

Residual misalignment in ★ after correction for a global offset of the FE-I3 chips

Chip	3	4	5	6	7	8	9	10	Pad size	Distance
Δx [μm]	-23	44	-34	-8	-16	-17	-17	-16	27	23
Δy[μm]	-34	73	-58	-19	-18	-25	-21	-25	60	29
Tilt [°]	-0.38	0.72	-0.61	-0.21	-0.21	-0.23	-0.24	-0.26		





- 5 modules with a misalignment and tilt that does not induce shorts or open, corners included
- Very good alignment for the SLID pads in the central region of the FE-I3 matrix

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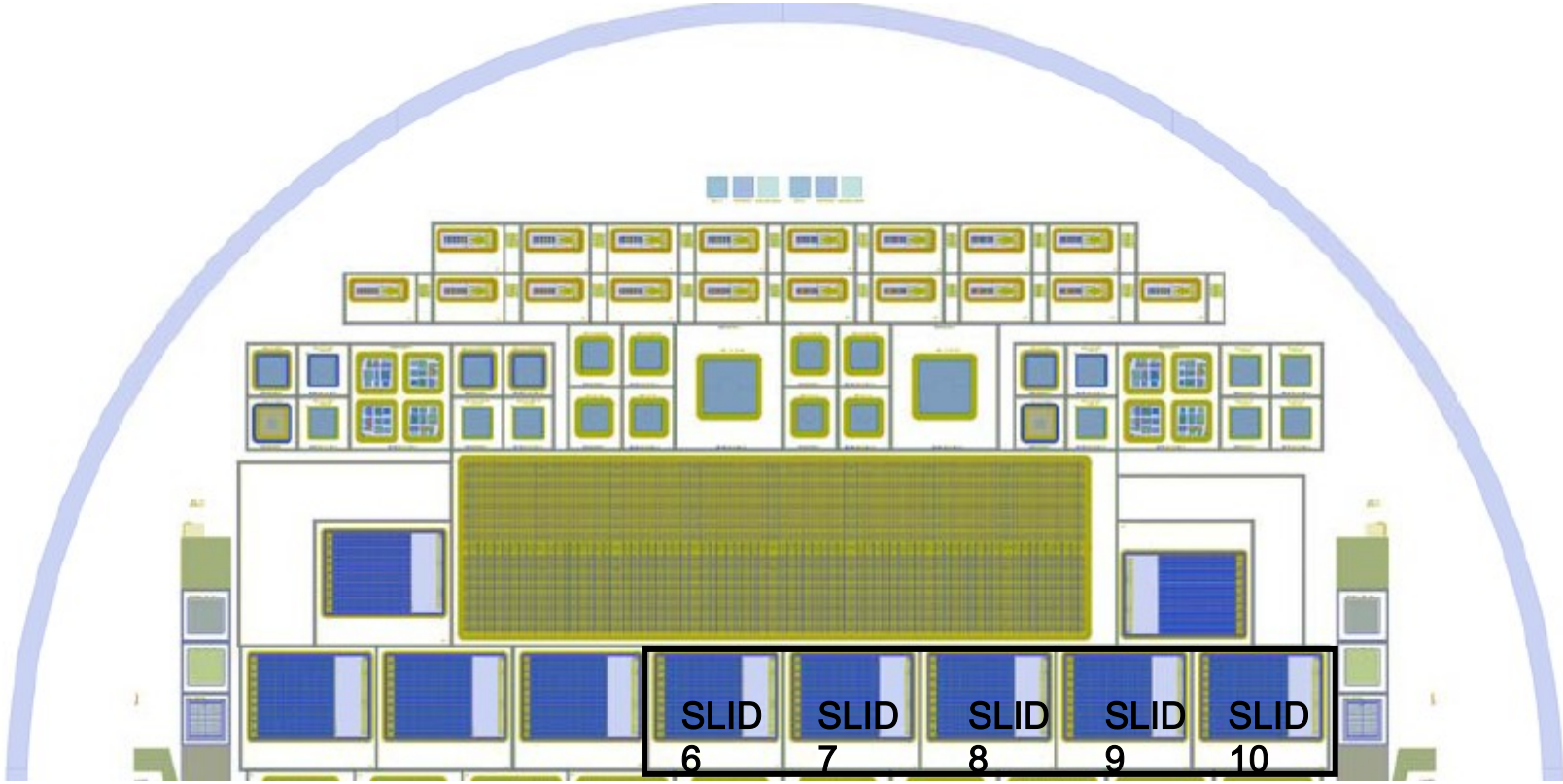
Map of the 5 Modules interconnected

- The five sensors and the chips are all functional
- Chips can be tuned with a small threshold dispersion
- Leakage current at 50 V ~ 25 nA (above Vdepl=40V)
- ^{90}Sr source scan performed for all the modules



Modules tested

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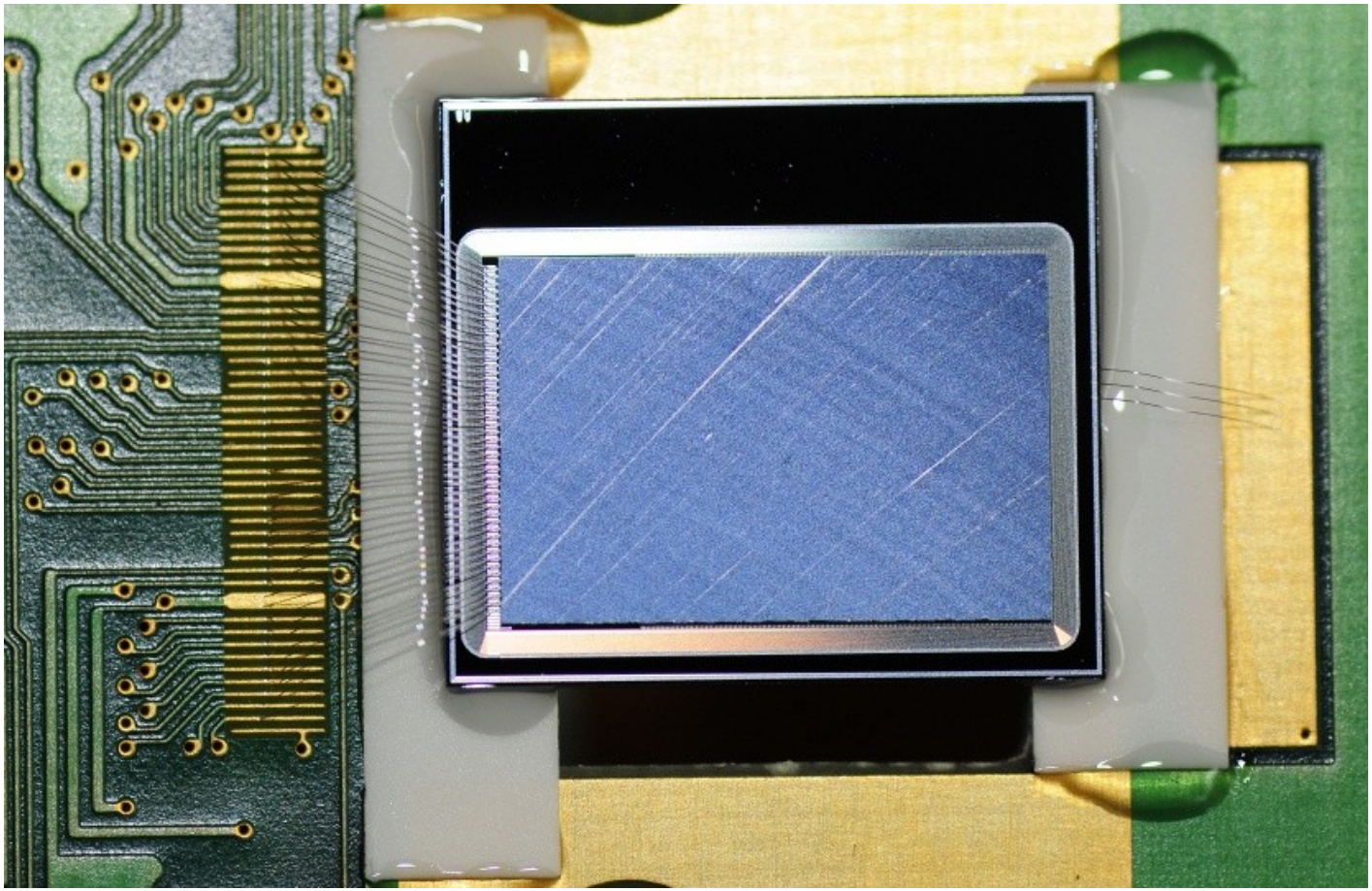
SLID Module

- SLID modules glued and wire-bonded to a modified version of the ATLAS pixel detector board (Bonn University)
- Measurements performed with the ATLAS read-out system USBPix



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Module 10: Results

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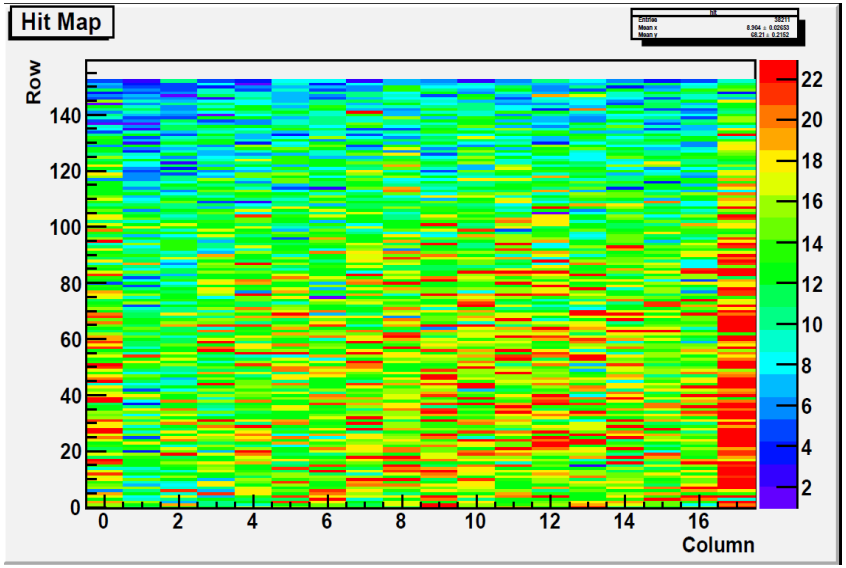
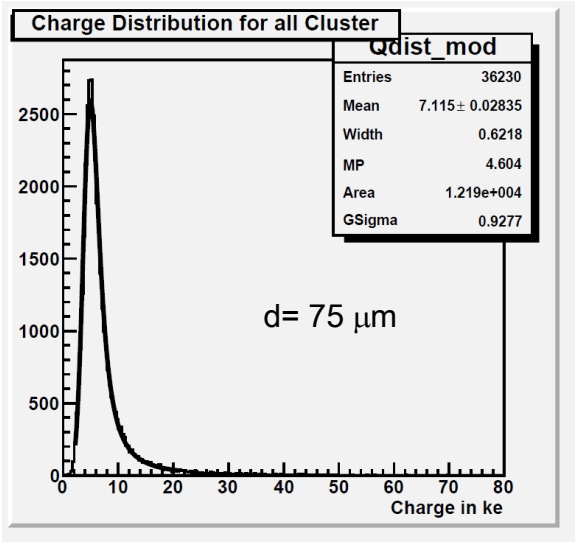
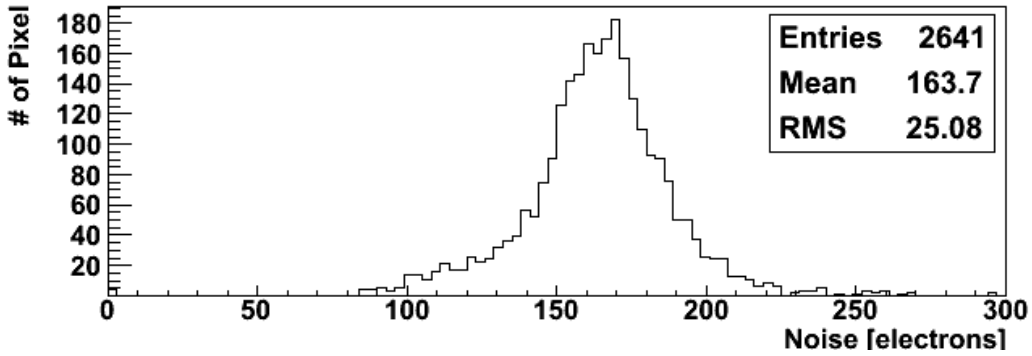


Signal map: all channels connected and functional



- Collected Charge with ^{90}Sr: compatible with CCE of a 75μm thick sensor



Noise excluding threshold dispersion (29e) 164 e

Comparable (even better than!) to bump bonded standard ATLAS sensors (190e)

Module 9: Results

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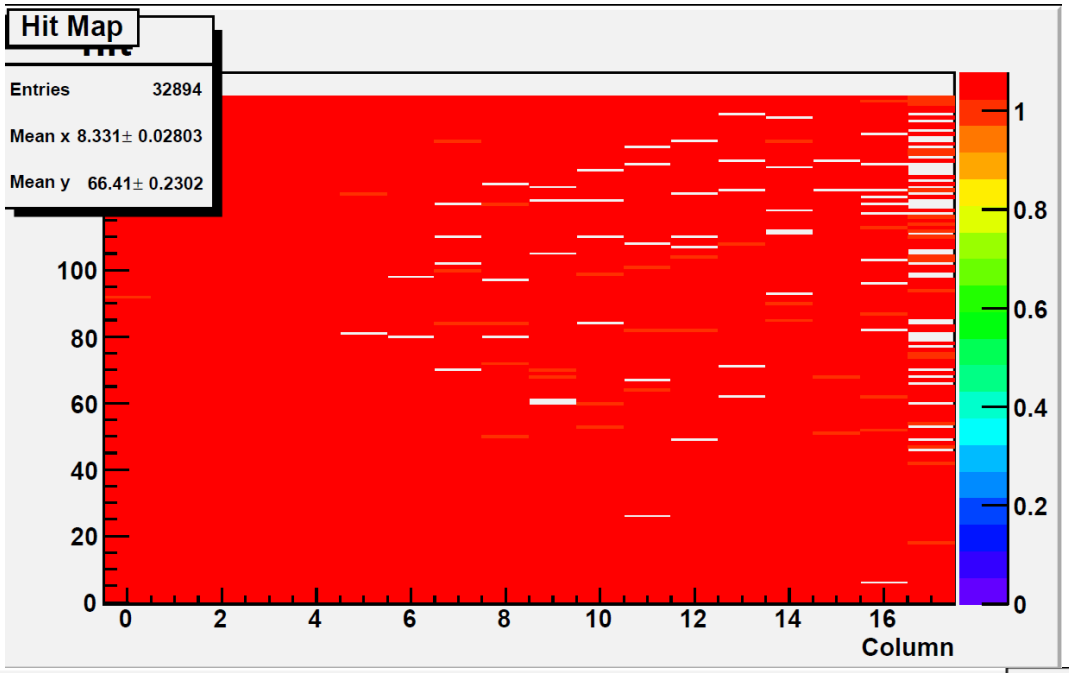
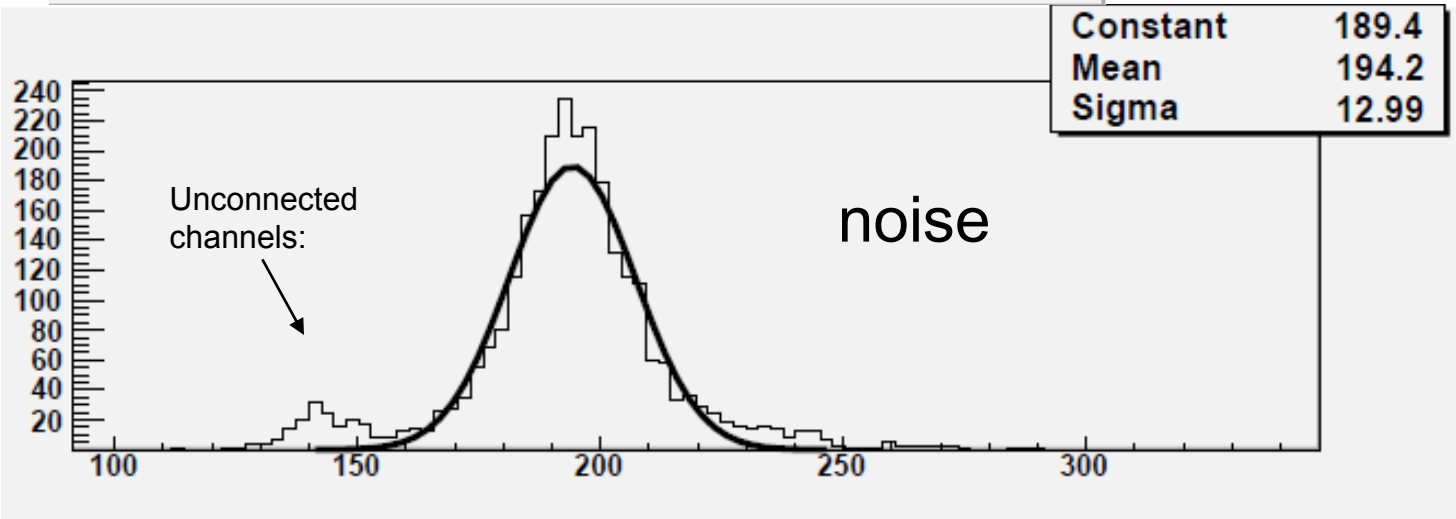


Few unconnected channels

Visible in hit map and noise (low noise due to small capacitance)



Disconnected Channels

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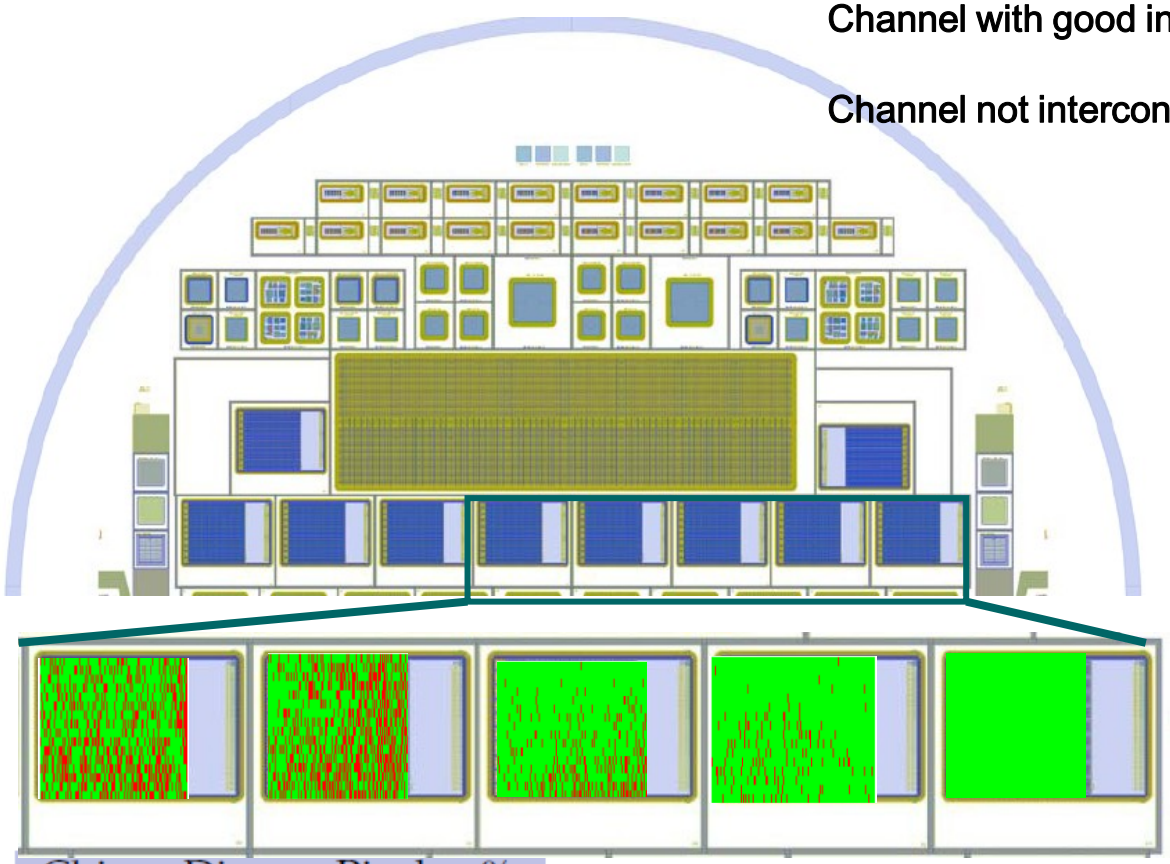
Channel with good interconnection

Channel not interconnected



2880

Chip	Discon. Pixel	%
6	731	30
7	713	29
8	274	11
9	134	6
10	0	

Number of disconnected channel is growing towards the center of the wafer

Pattern of disconnected channels shows that the chip misalignment cannot be the only cause: pressure inhomogeneity? BCB passivation not completely opened?

Connection strength

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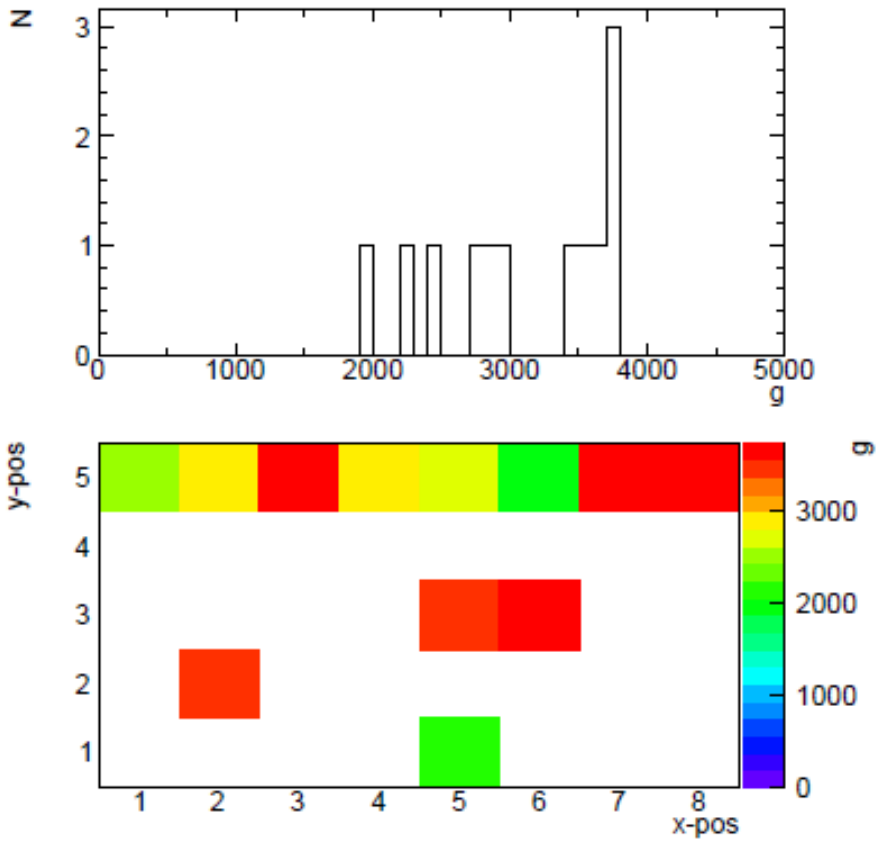

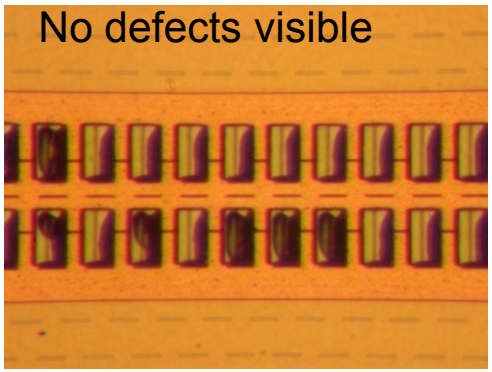

Pull test with dummy connections

Connection strength of the order of 0.01N→

similar to bump-bonding and other pixel interconnection technology

Yield issue still a puzzle

TSV in the FE-I3 chips

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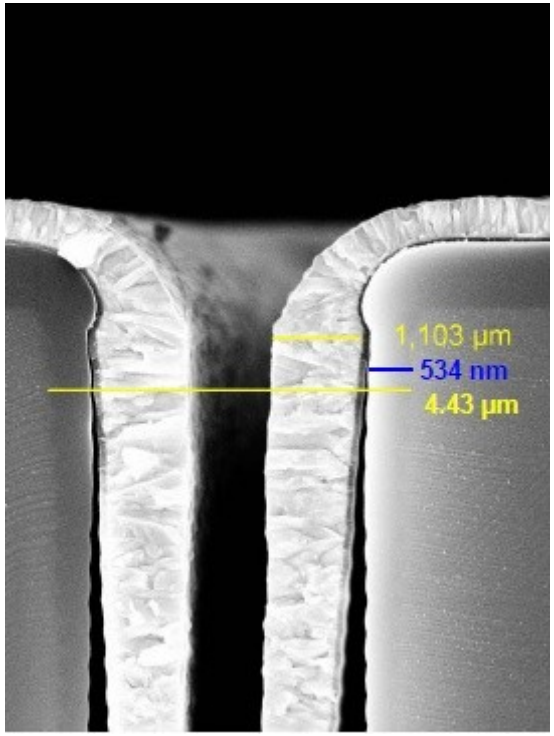
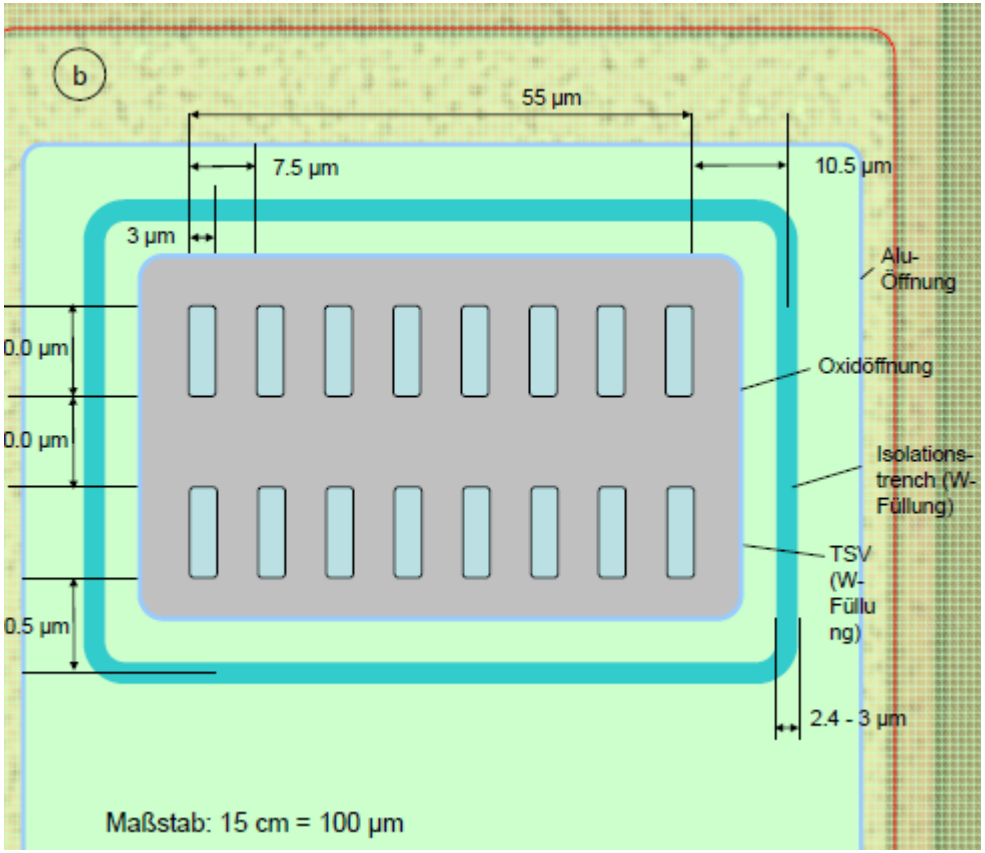
Add insulating trench
around vias
Avoid shorts to silicon bulk





Insulation layer (silicon oxide)
Improve aspect ratio from 10:1 tp 12:1

TSV in the FE-I3 chips

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Fraunhofer EMFT

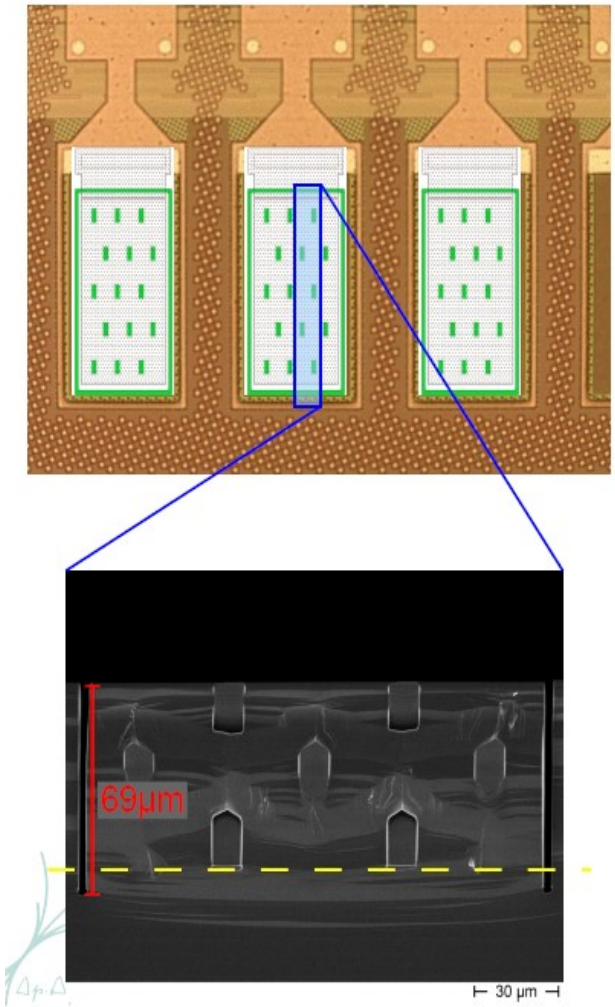
TSV

Etching (Bosch process) applied to FE-I3 8" wafers. 60 µm deep TSVs with lateral dimensions of 3 x 10 µm² on the original wire-bonding pads

- Performed in the un-thinned FE-I3 chips of one designated test-wafer
- Etched to a depth of ~ 69 µm
- Rough cut/break along the long direction of the test structure shows the structure of the vias and of the trench around them
- Local planarisation of the fan-out pads by depositing and etching of SACVD-Oxide

In work:

- Perform via etching and filling in the hot FE-I3 wafer
- Connect the readout chip with SLID to the hot sensor wafers



Advantages even for single layer

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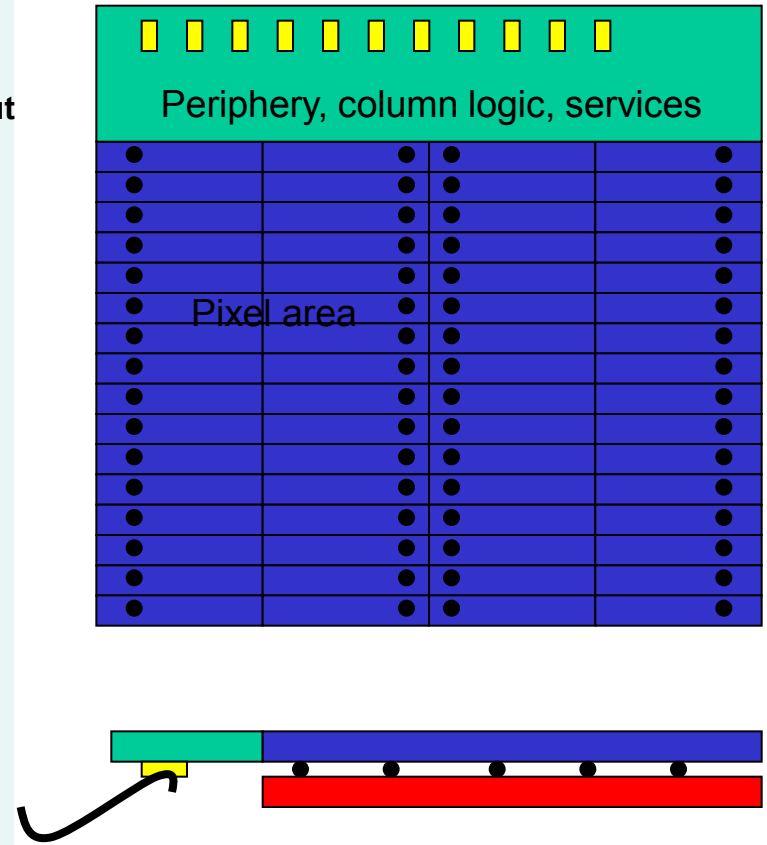
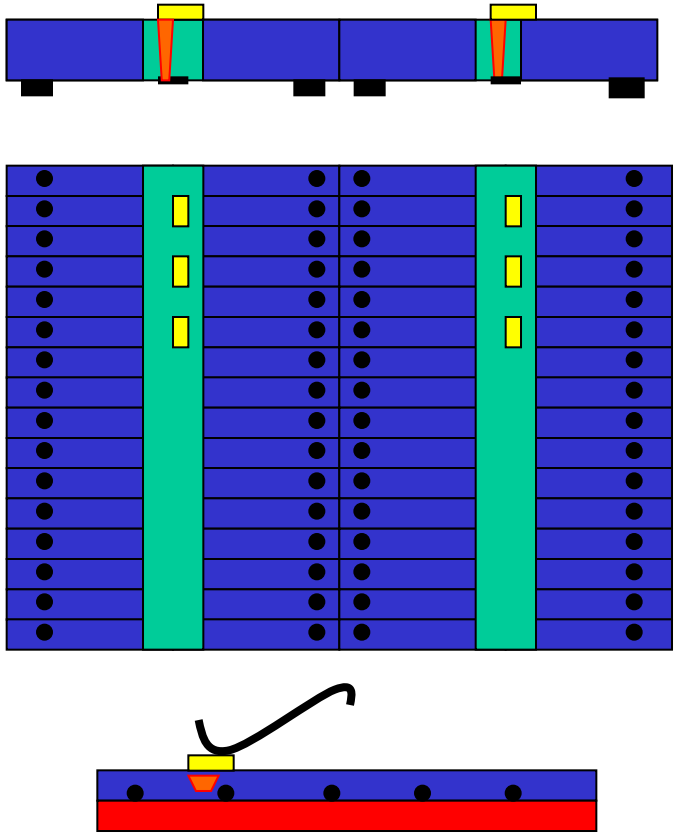
Conventional Layout



3D Layout



Make use of smaller feature size (gain space)
-> move periphery in between pixels (can keep double column logic)
-> backside contacts with vias possible
-> no cantilever needed, 4-side buttable

Summary

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Optimize ATLAS pixel modulev for sLHC: material & rad. hardness

- Thin sensors for rad. harndess (and material reduction)
- SLID interconnection as an alternative to bump bonding
- Thinned ASIC with vias for backside connectivity

Use EMFT SLID and TSV technology
Optimize sensor layout and processing for SLID

First tests successful (SLID only):

- Modules work with good performance
- Problems with chip alignment on handle wafer
- One module with 100% connected channels and excellent electric performance: **big success!**
- Disconnected channels in other modules, seems systematic effect, but reason not yet understood

Next step: full SLID assembly of sensors and ASICs with TCV