CMC-CMP-MOSIS collaboration for a 3D-IC prototyping service

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Agenda

- Introduction & Motivation for 3D-IC
- Process overview
- Partnership for MPW runs service
- 3D-IC Design Platform
- Conclusion

3D-IC Integration : Not a New Story

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure“ IEEE Proceedings of International Electron Devices Meetings, Vo. 32, **1986**, pp. 488-491.

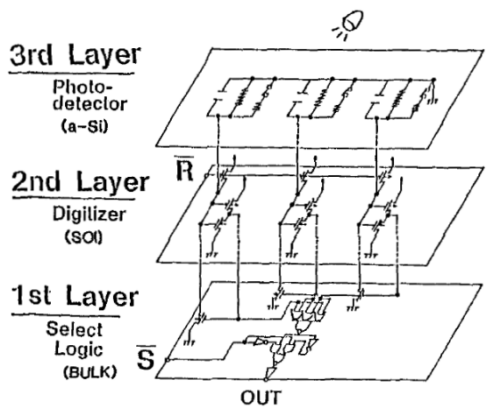


Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

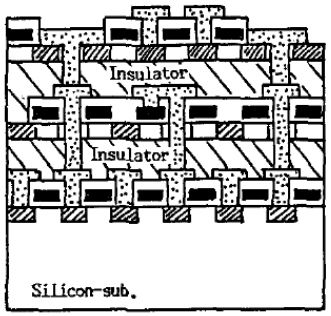


Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

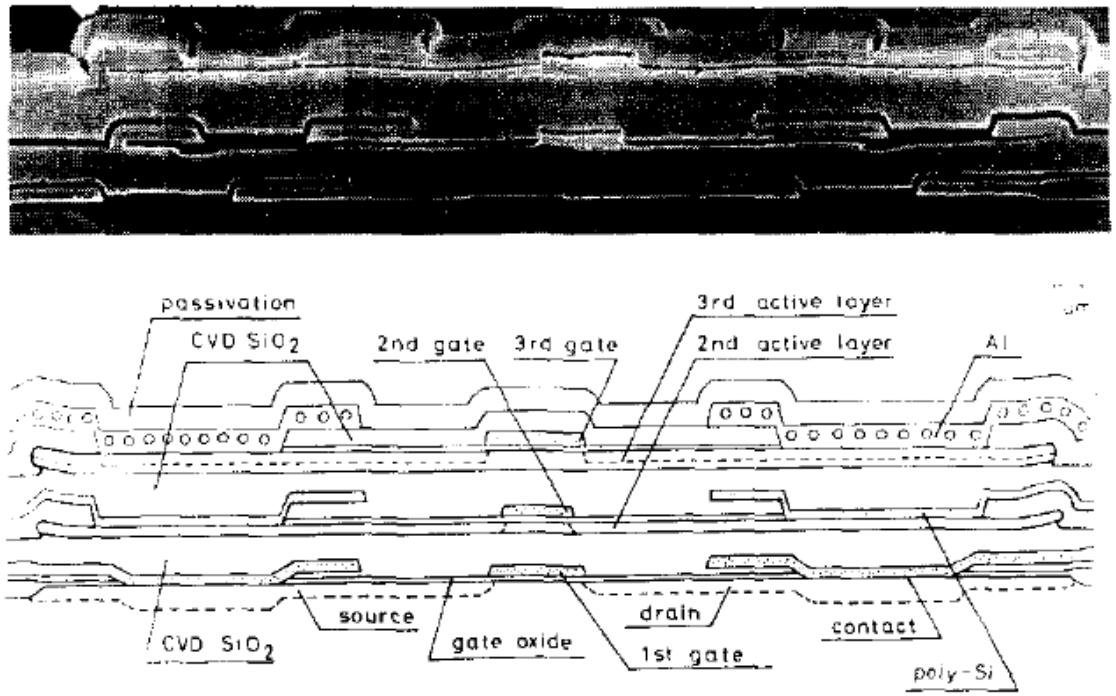
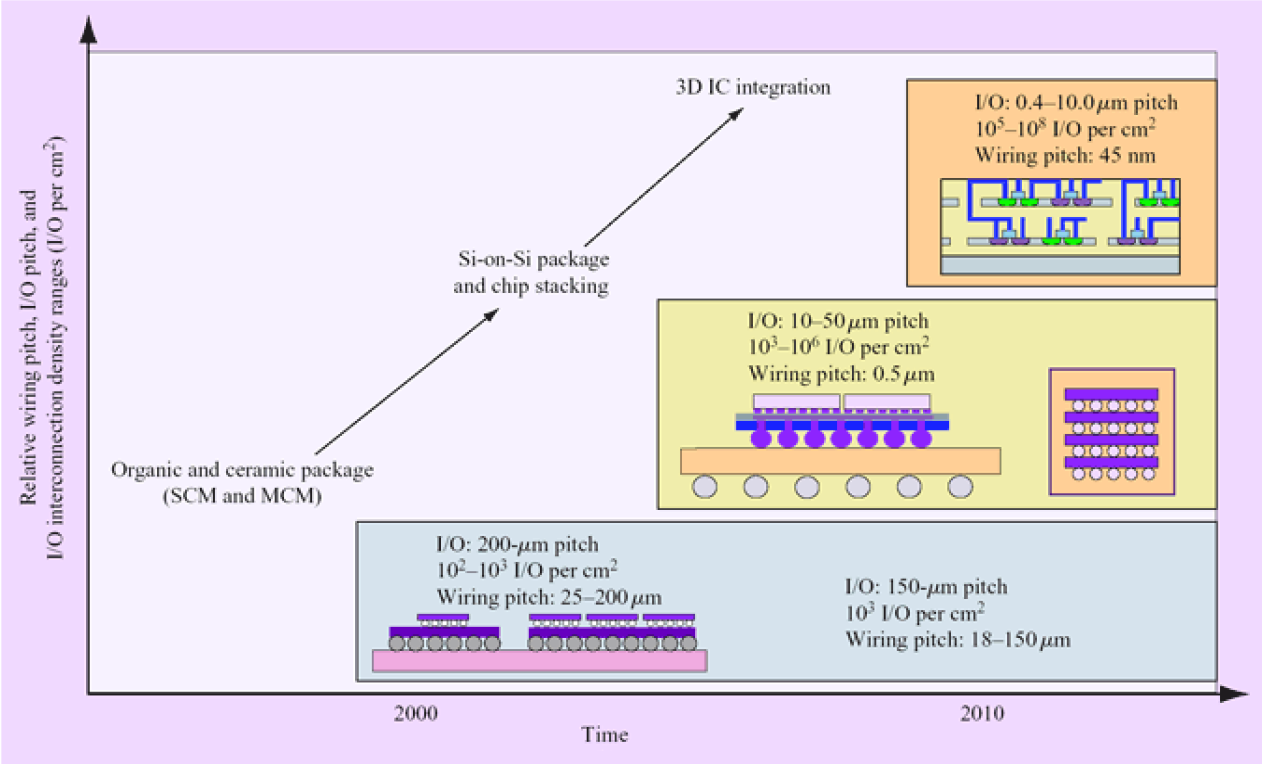


Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.

3D-IC Integration : The Other Path for Scaling



Source IBM http://www.research.ibm.com/journal/rd/526/knickerbocker.html

- Moore's law by scaling conventional CMOS involves huge investments.

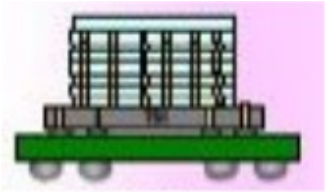
- 3D IC processes : An opportunity for another path towards continuing the scaling, involving less investments.

- Like for conventional CMOS, infrastructures are needed to promote 3D-IC integration, making it available for prototyping at "reasonable" costs.

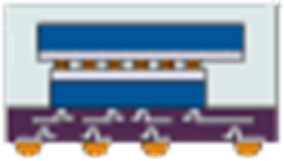
Two Worlds with Different Integration Approaches

"Monolithic"

Distributing a whole system across several tiers

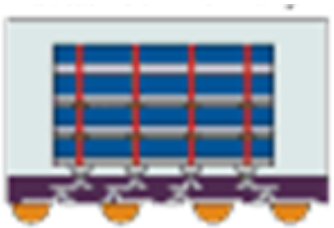


Heterogeneous Multi layer 3D-IC TSV integrated



3D-IC TSV integrated

3D-IC face to face



3D-IC TSV Stacked Memory

Integration

Silicon Interposer to high Integrated MCM

Die to Die Integrated package

Multi-Chip Module

Substrate based Module (PCB)

"Discrete"

Assembly of "Known Good Dies"

Which Design Methodology ?

- Discrete : **3D packaging, stacked dies, …**

  1- Design a whole system.
  2- Split it in subsystems.
  3- Place the subsystems as predefined "Known Good Dies" (IPs).
  4- Determine and place the interfaces in between.
  5- The system is done

- Monolithic : **3D-IC Integration**

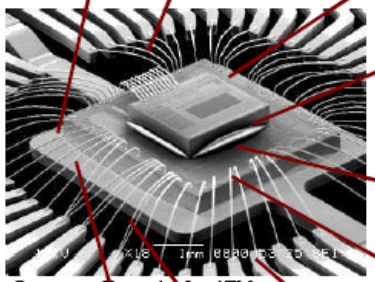
  1- Design a whole system.
  2- Split it in subsystems.
  3- Determine and place the interfaces in between.
  4- Generate and Place the subsystems in between the interfaces.
  5- The system is done

Here comes the difference : The "key" for a true 3D-IC Integration

SiP versus 3D-IC

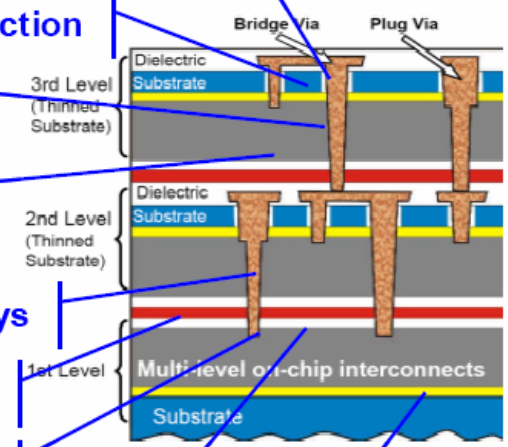
Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



Source : Fraunhofer-IZM

- High Power consumption
- Long Connection
- Low Density
- Poor Heat Dissipation
- RC Delays
- High Impedance
- Large Area
- Challenging Interposers
- I/O Pitch limitations



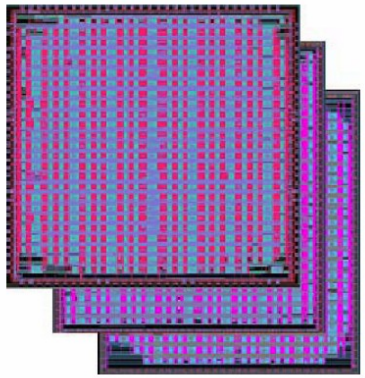
James Lu, RPI, Peaks in Packaging, 2003

- Low Power consumption
- Short Connection
- High Density
- Good Heat Dissipation
- Reduced RC Delays
- Low Impedance
- Smallest Area
- Simple Interposers
- Less I/O Pitch limitations

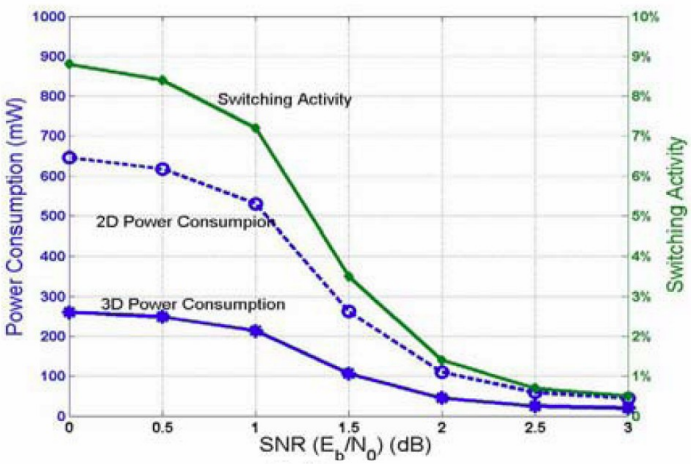
TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Large Systems Benefits from 3D-IC Integration

"Implementing a 2-Gbs 1024-bit ½-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"
Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajarng, Bo Hu, and C.-J. Richard Shi
University of Washington
International Conference on Computer Design, ICCD, Oct. 2007



Final layout view of 3D LDPC structure.



Post-layout power of the LDPC decoder (2D vs 3D).

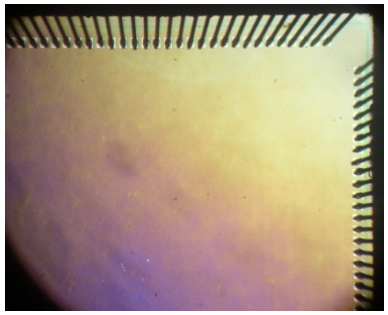
Comparison between 2D and 3D designs

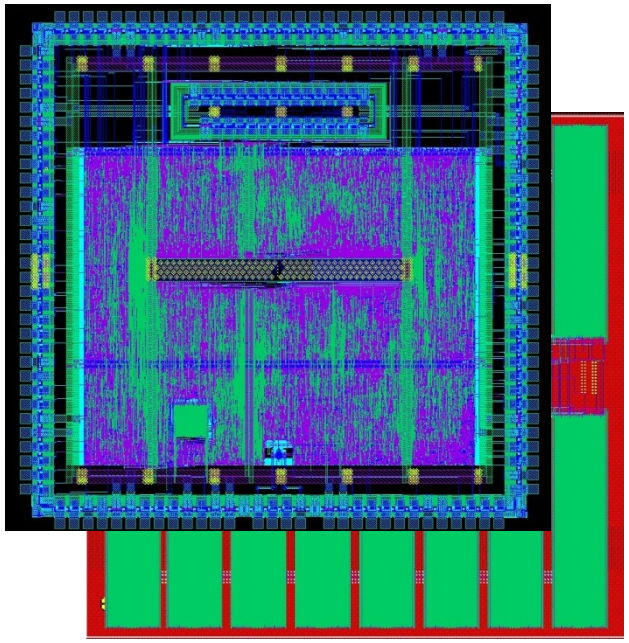
	2D design	3D design
Area (mm*mm)	18.238*15.92 =**290.35**	(6.4*6.227)*3 = **119.56**
Total wire length (m)	**182.42**	22.39+22.57+22.46 =**67.42**
Max WL before buffer insertion (mm)	**13.82**	**8.68**
Max WL after buffer insertion (mm)	**4**	**4**
Buffer used	**32900**	**24636**
Clock skew (ns)	**2.33**	**1**
Power dissipation (mw)	**646.2**	**260.2**

Performance Factor (Area * Timing * Power) = 14

An Illustration: CPU/Memory Stack

- R8051 CPU
  - 80MHz operation; 140MHz Lab test (VDD High)
  - 220MHz Memory interface
- IEEE 754 Floating point coprocessor
- 32 bit Integer coprocessor
- 2 UARTs, Int. Cont., 3 Timers, …
- Crypto functions
- 128KBytes/layer main memory



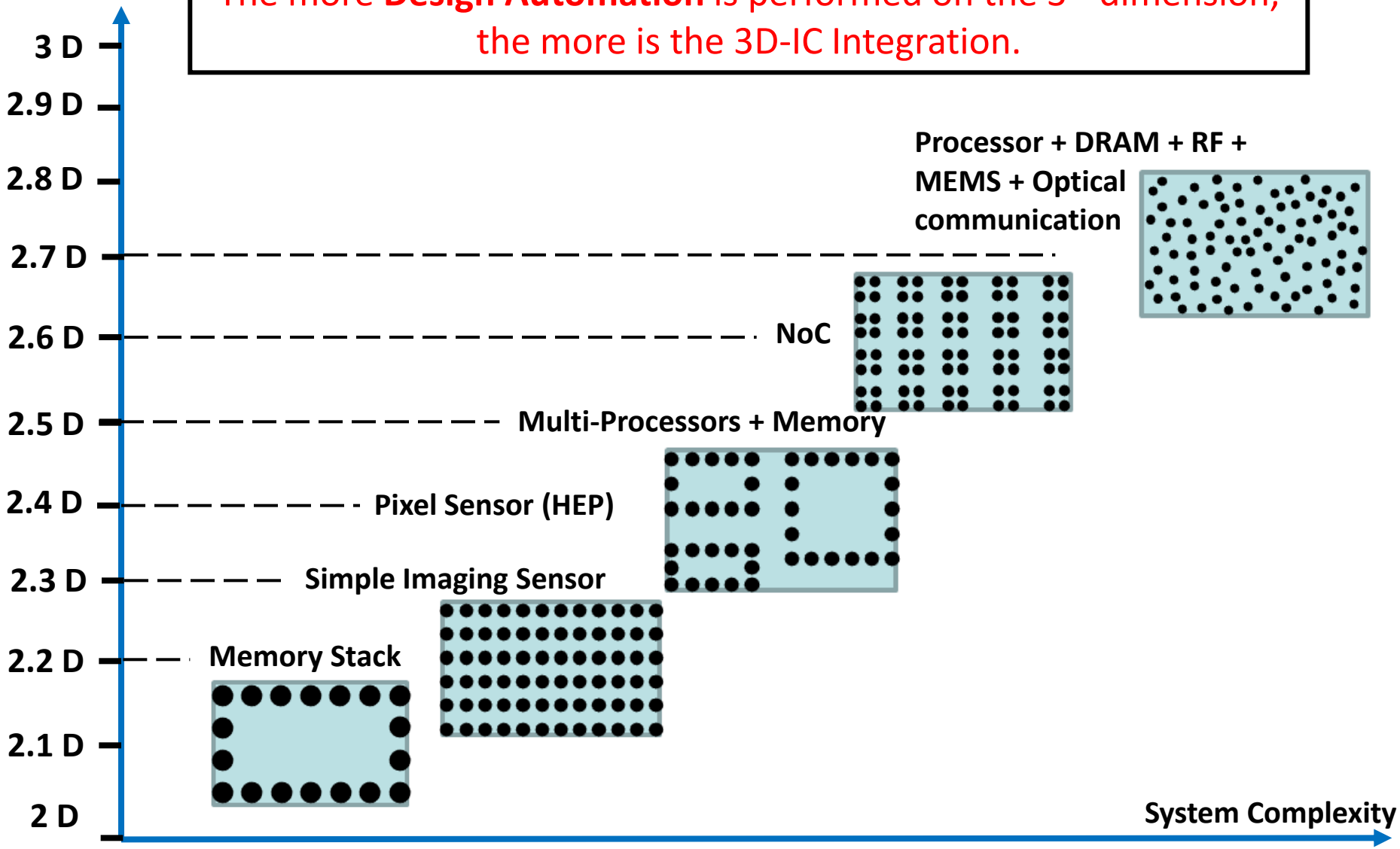


- **5X performance**
- **1/10th Power**

Source Tezzaron (2004)

Design Methodology

The more **Design Automation** is performed on the 3rd dimension, the more is the 3D-IC Integration.



CMC-CMP-MOSIS Collaboration

CMC / CMP / MOSIS partnering for 3D-IC process access

- Stimulate the activity by sharing the expenses for manufacturing.

- Join forces for the technical support, and dedicate roles for each partner.

- Make easier the tech support for local users respectively by each local center.

- Because there is no standard for the 3D-IC integration, it is urgent to setup an infrastructure making possible a broad adoption of 3D-ICs. That will have a beneficial effect on prices, more frequent MPW runs, and more skilled engineers.

CMC-CMP-MOSIS partnering on 3D-IC

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CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

The first MPW run is scheduled to 31 May 2011:

- 2-tier face-to-face bonded wafers
- 130nm CMOS process for both tiers
- Top tier exposing TSV and backside metal pads for wire bonding.

A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

Further MPW runs will be scheduled supporting process flavors (multiple tiers beyond 2, different CMOS flavors for different tiers, ...) driven by user requirements.

Potential users are encouraged to contact **CMP** for details : **cmp@imag.fr**

CMC - CMP - MOSIS Cooperation

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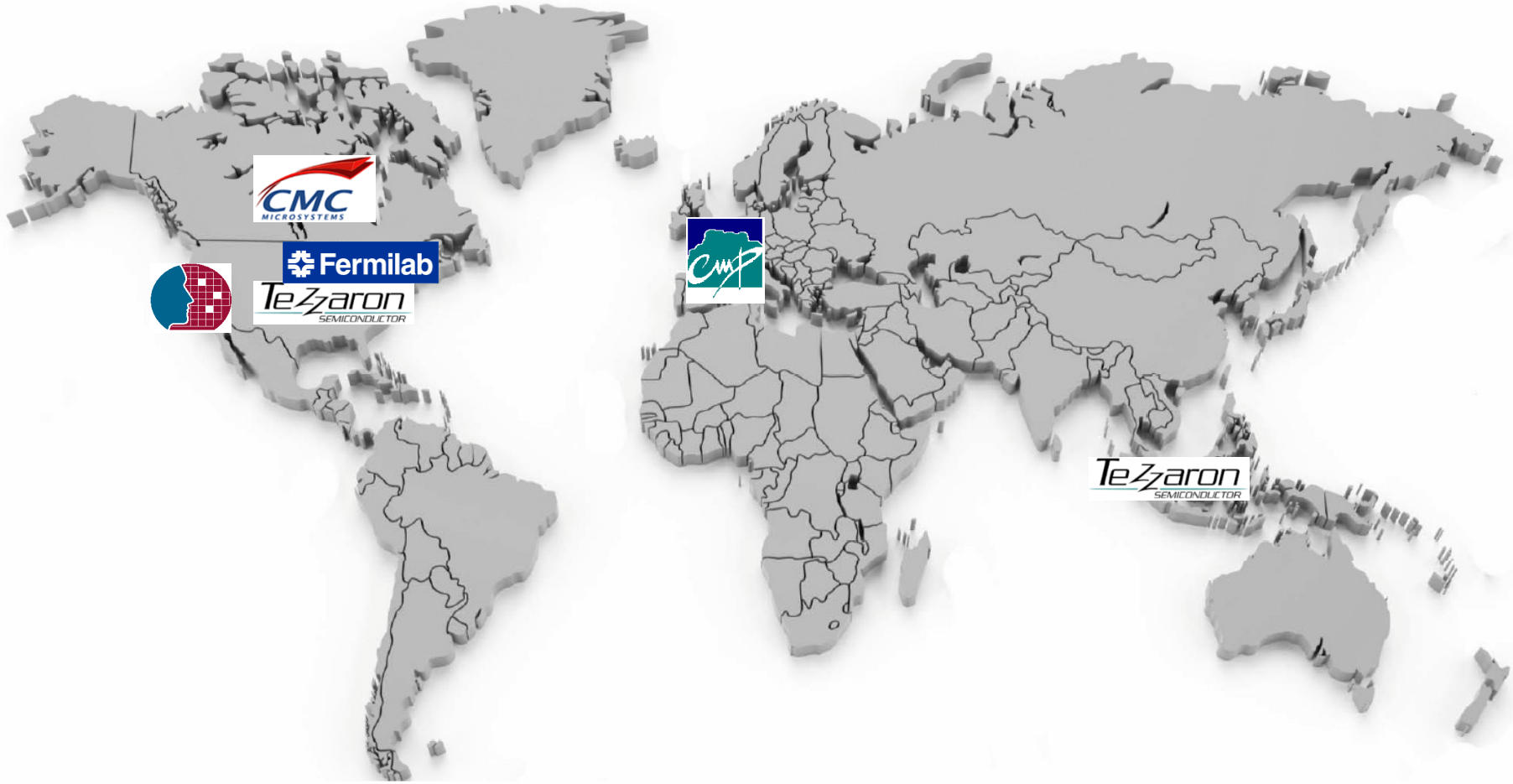
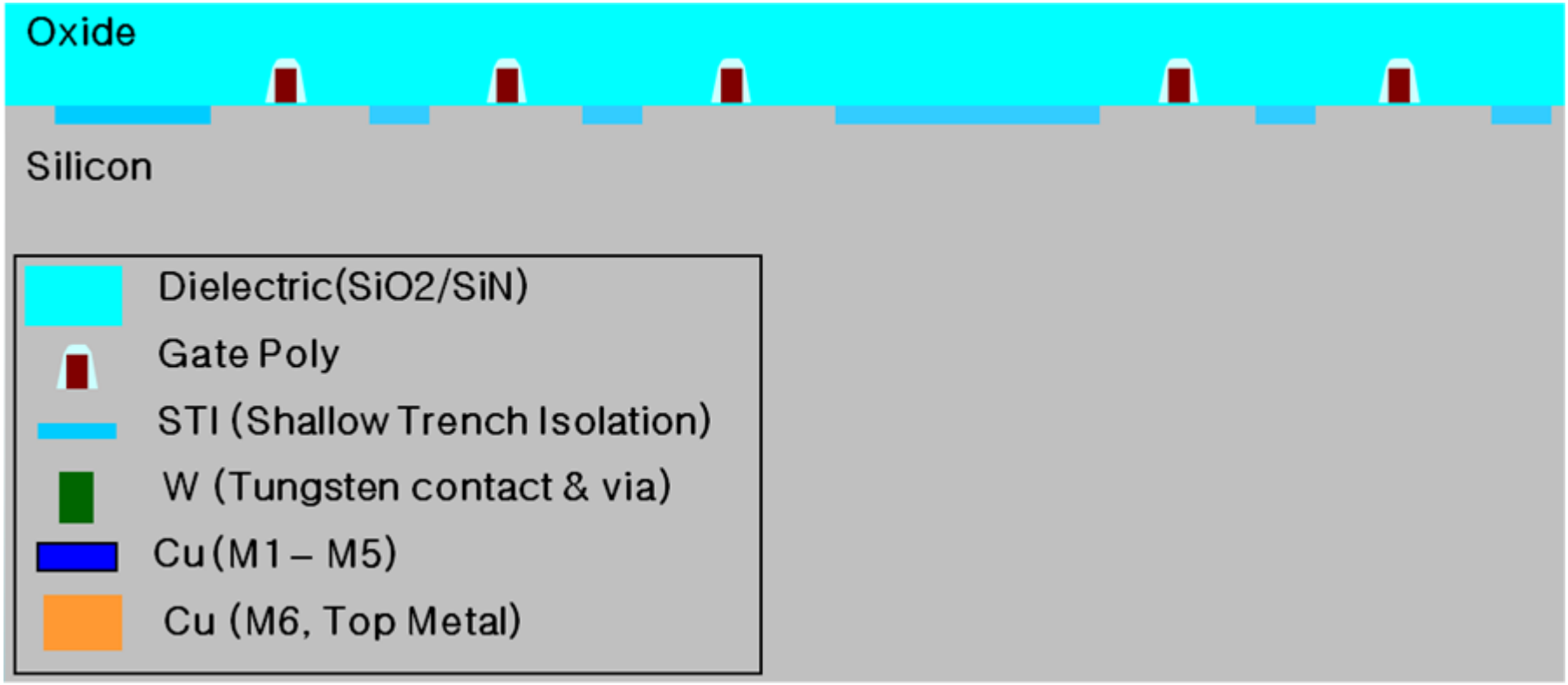
- CMC supporting Canadian Customers
- CMP supporting European Customers
- MOSIS supporting US Customers



Tezzaron 2-Tier Process (130nm CMOS)

Process Overview

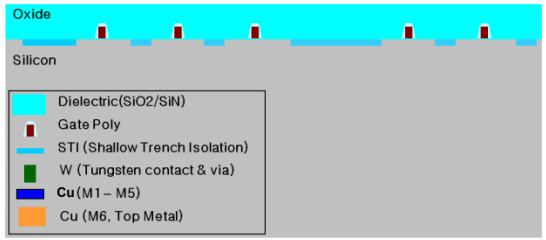
Tezzaron Process Flow for TSV and DBI (using Via Middle process)

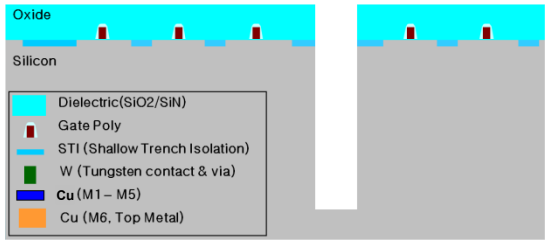


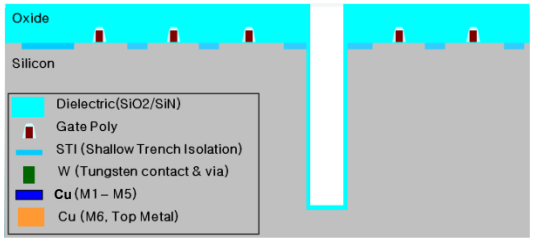
Starting wafer in 130nm (5 Cu metal layers + 6th Cu metal as DBI)

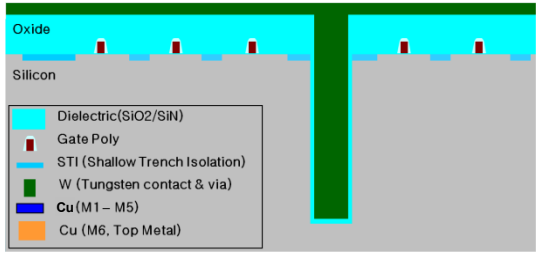
Source Tezzaron

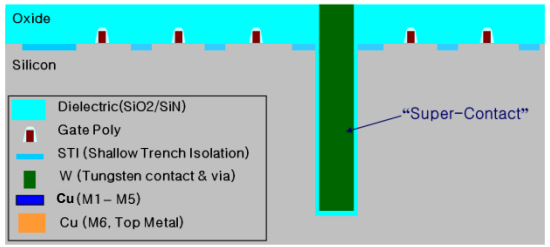
Tezzaron Process Flow for TSV and DBI (using Via Middle process)

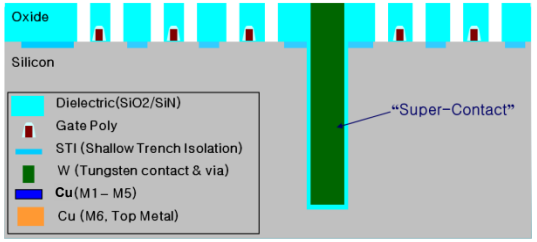


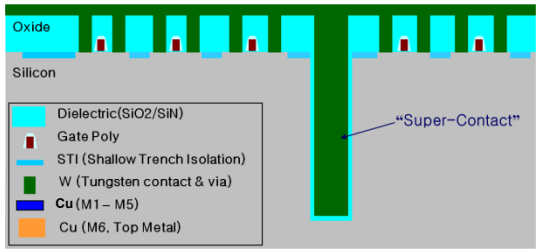


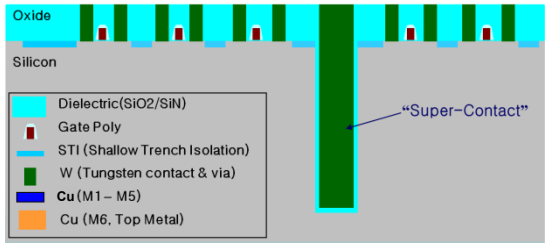


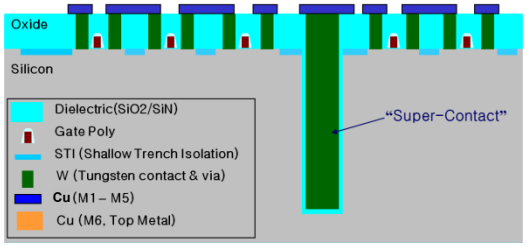


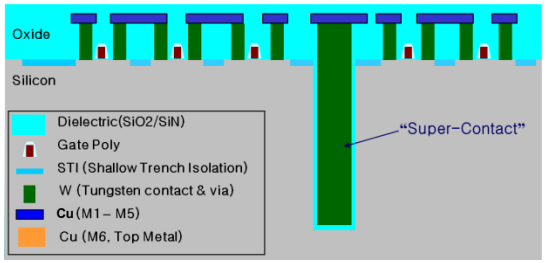


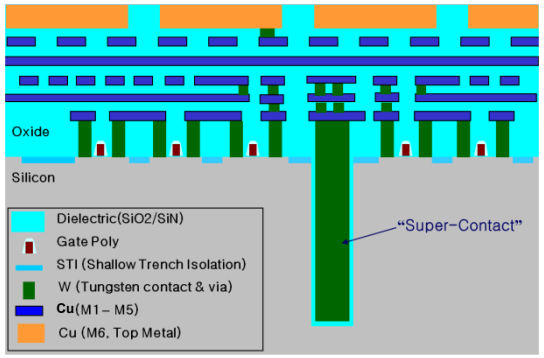












Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)

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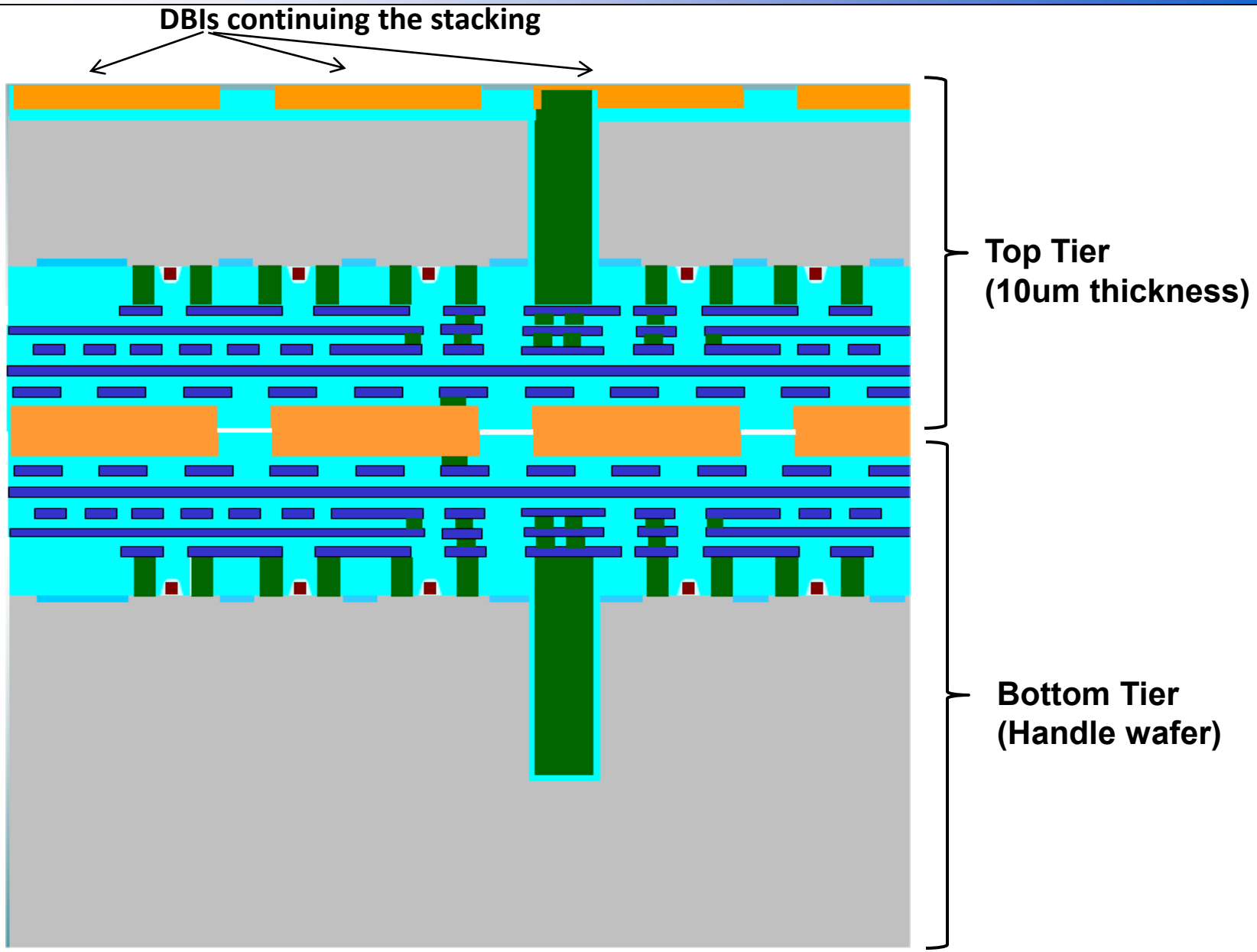
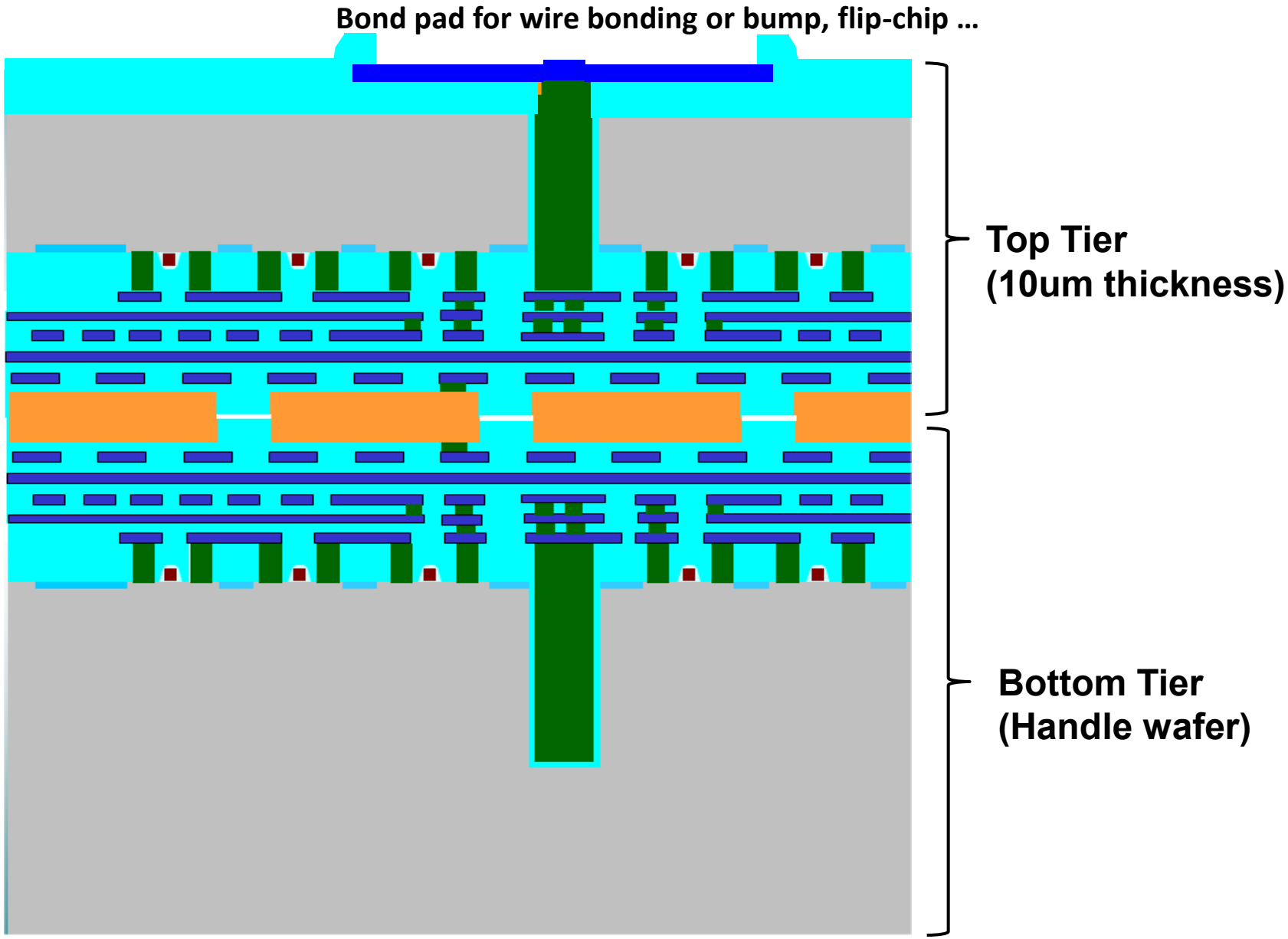


Source Tezzaron

Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)

CNRS – INPG – UJF

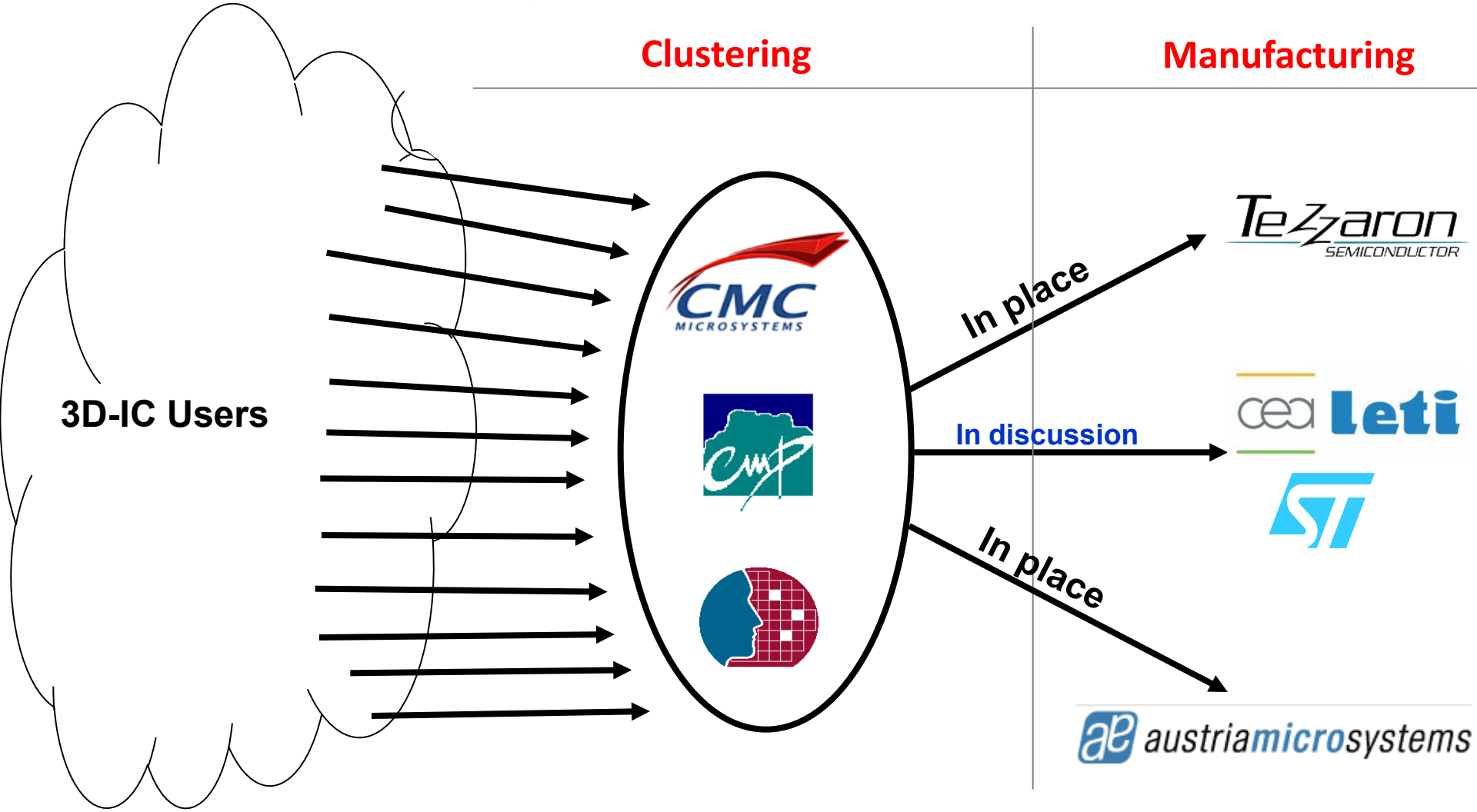


Source Tezzaron

3D-IC MPW runs

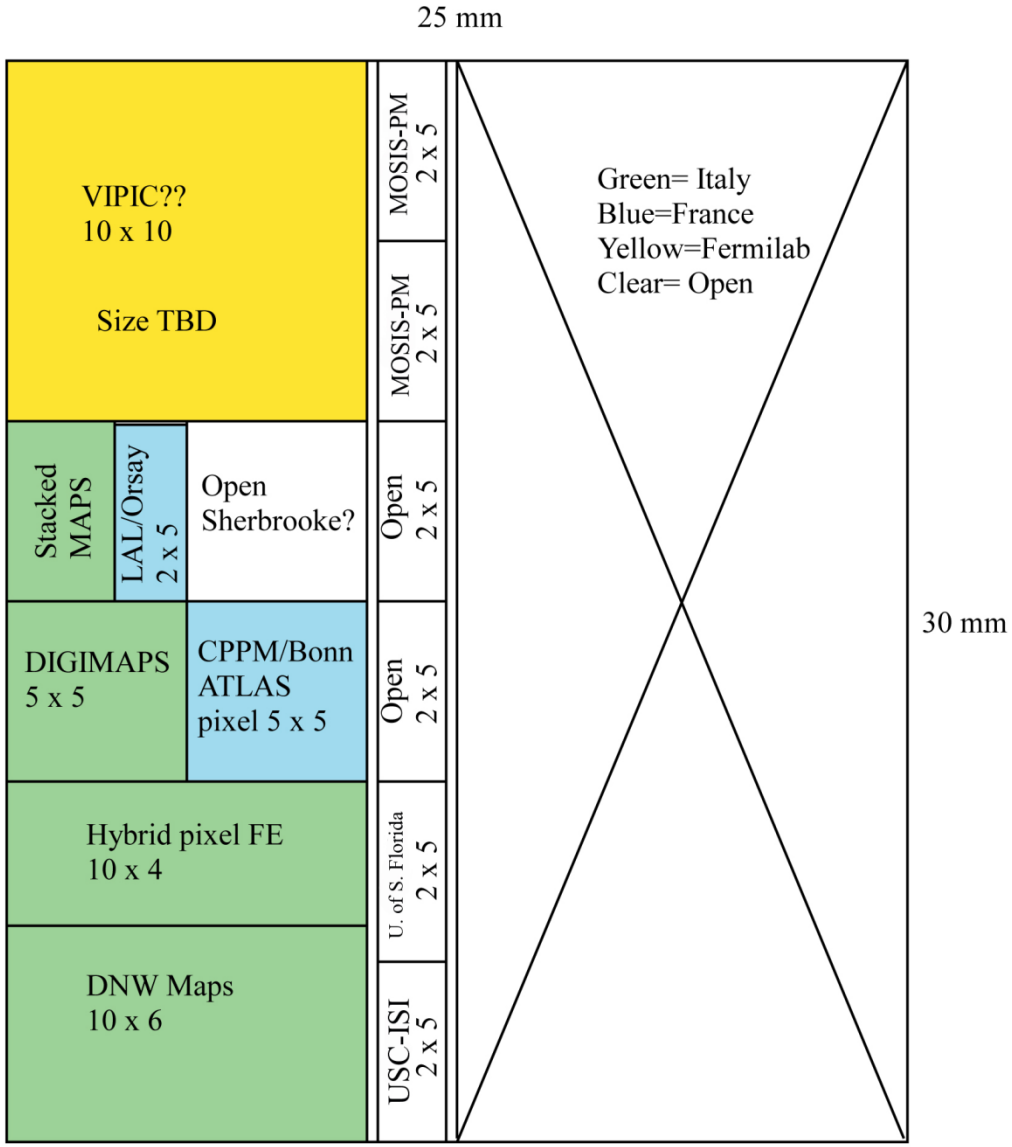
3D-IC MPW Infrastructure

CMC-CMP-MOSIS partnering to offer 3D-IC MPW runs



Critical mass will allow frequent MPW runs and low pricing

CMP/MOSIS/CMC : 1st MPW run



MPW run deadline : May 31st, 2011

3D-IC Design Platform

Tezzaron / GlobalFoundries Design Platform

- The Design Platform is modular. It has all features for full-custom design or semi-custom automatic generation design.
  - **PDK :** ***Original PDK from GF + (TSV / DBI) definition from Tezzaron***
  - **Libraries :** ***CORE and IO standard libraries from ARM***
  - **Memory compilers :** ***SPRAM, DPRAM and ROM from ARM***
  - **3D-IC Utilities :** ***Contributions developments embedded in the platform***
  - **Tutorials, User's setup.**

- All modules inside the platform refer to a unique variable, making it portable to any site. The installation procedure is straightforward.

- Support of CDB and OpenAccess databases.

PDK Tezzaron / GlobalFoundries

chrt13lprf_DK009_Rev_1D (Version issued in Q1 2011)

assura
calibre
cds_cdb
cds_oa
doc
eldo
hercules
hspice
prep3DLVS
skill
spectre
strmMaptables_ARM
strmMaptables_Encounter

assura:
FILLDRC
LVS
QRC

calibre:
3DDRC
3DLVS
DRC
FILLDRC
calibreSwitchDef

hercules:
DRC
LVS
STAR_RCXT

Collaborative Work on the Design Platform

HEP labs contributing with Programs, Libraries, and Utilities. All included in the Design Platform

- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)

Virtuoso Layout Editor with 3D layers and verification

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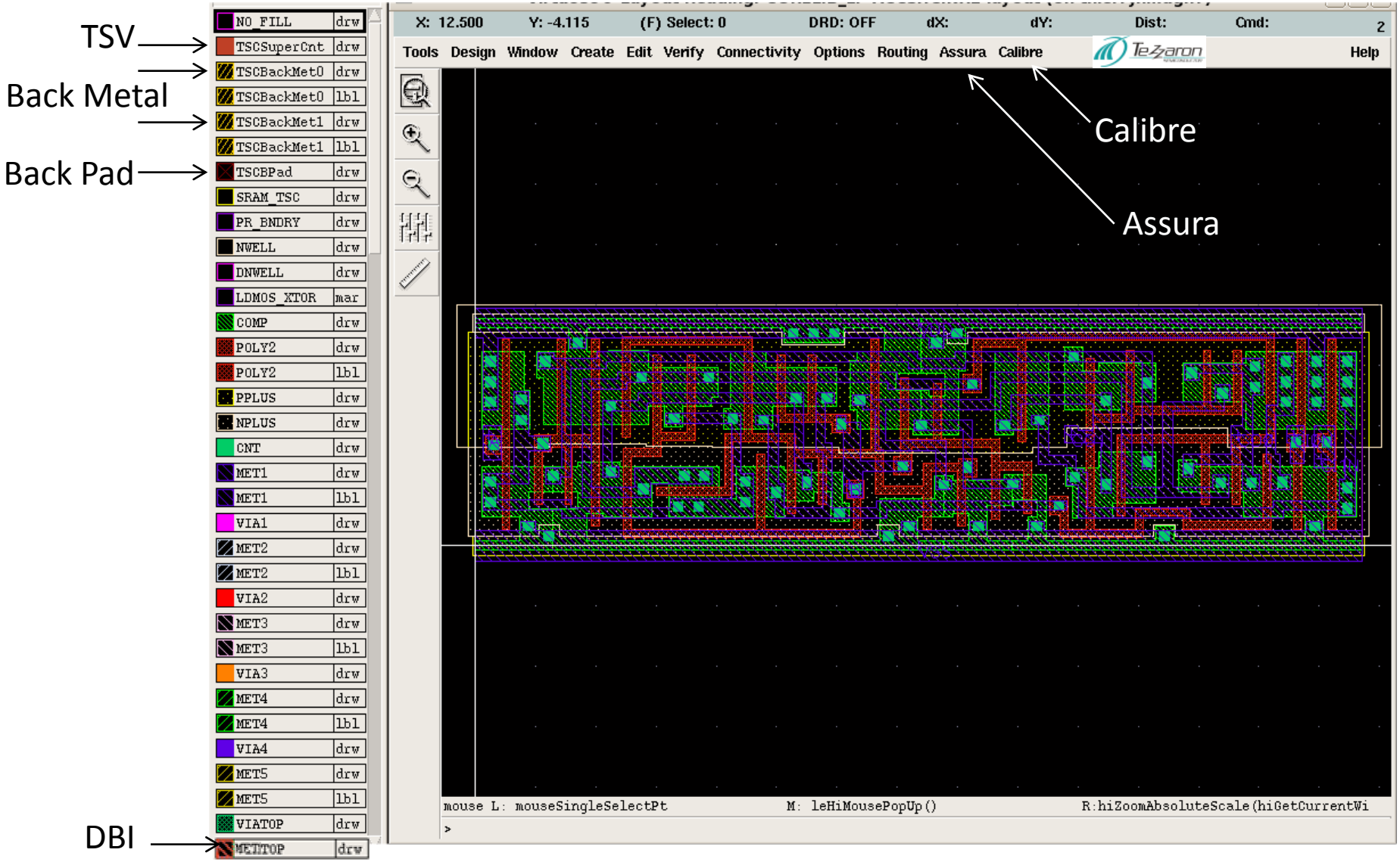
Virtuoso from Cadence IC 5.1.41



Customized Menu with some utilities

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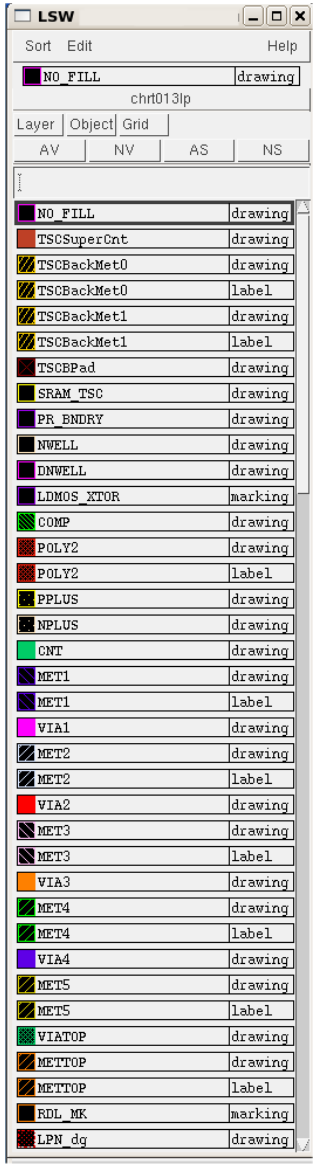
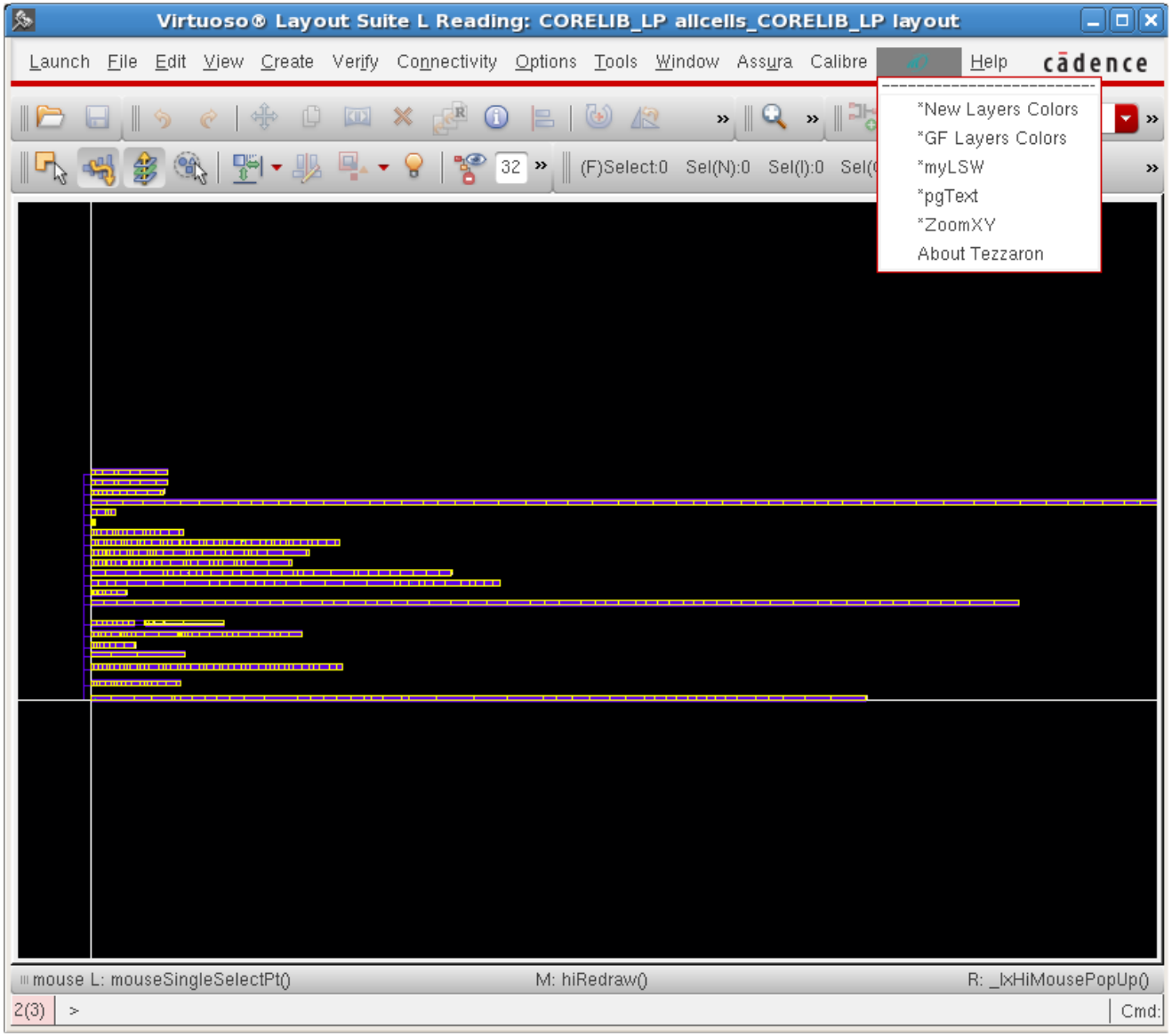
Virtuoso from Cadence IC 6.1.4





Libraries from Providers and Users

Univ. Bonn

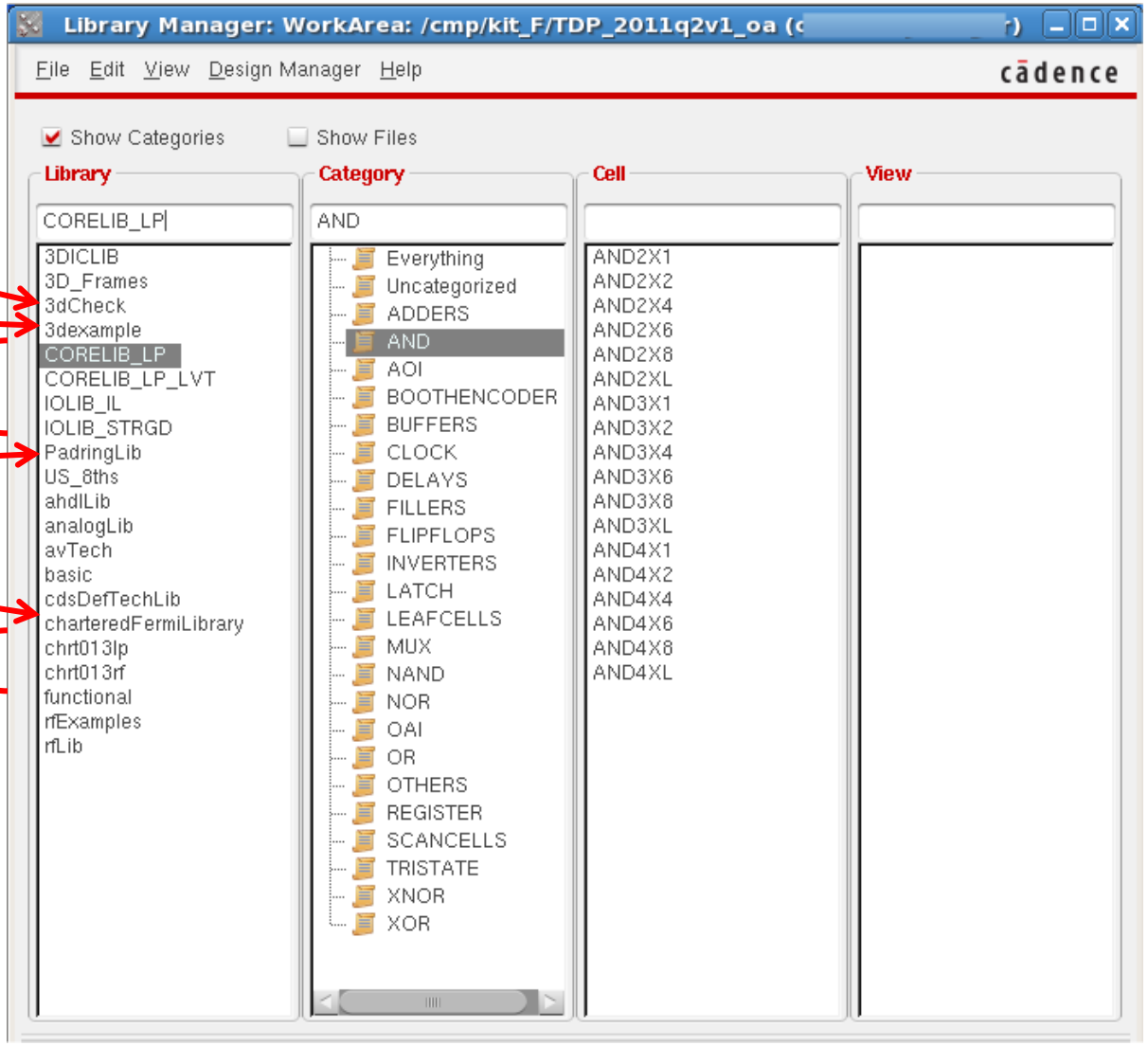
NCSU

ARM

IPHC

FermiLab

GF/TSC



Virtuoso / Calibre DRC Interactive Menu

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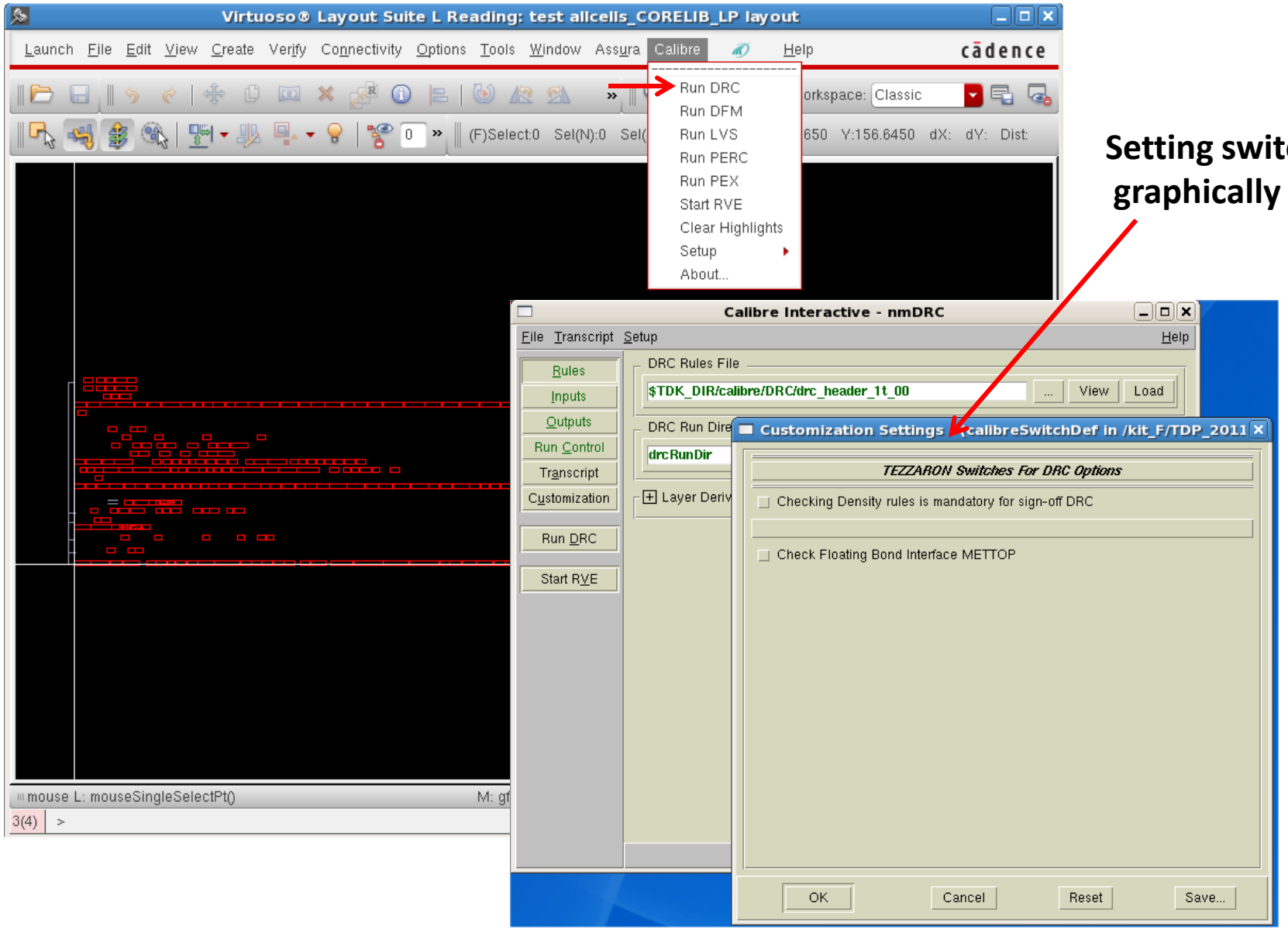
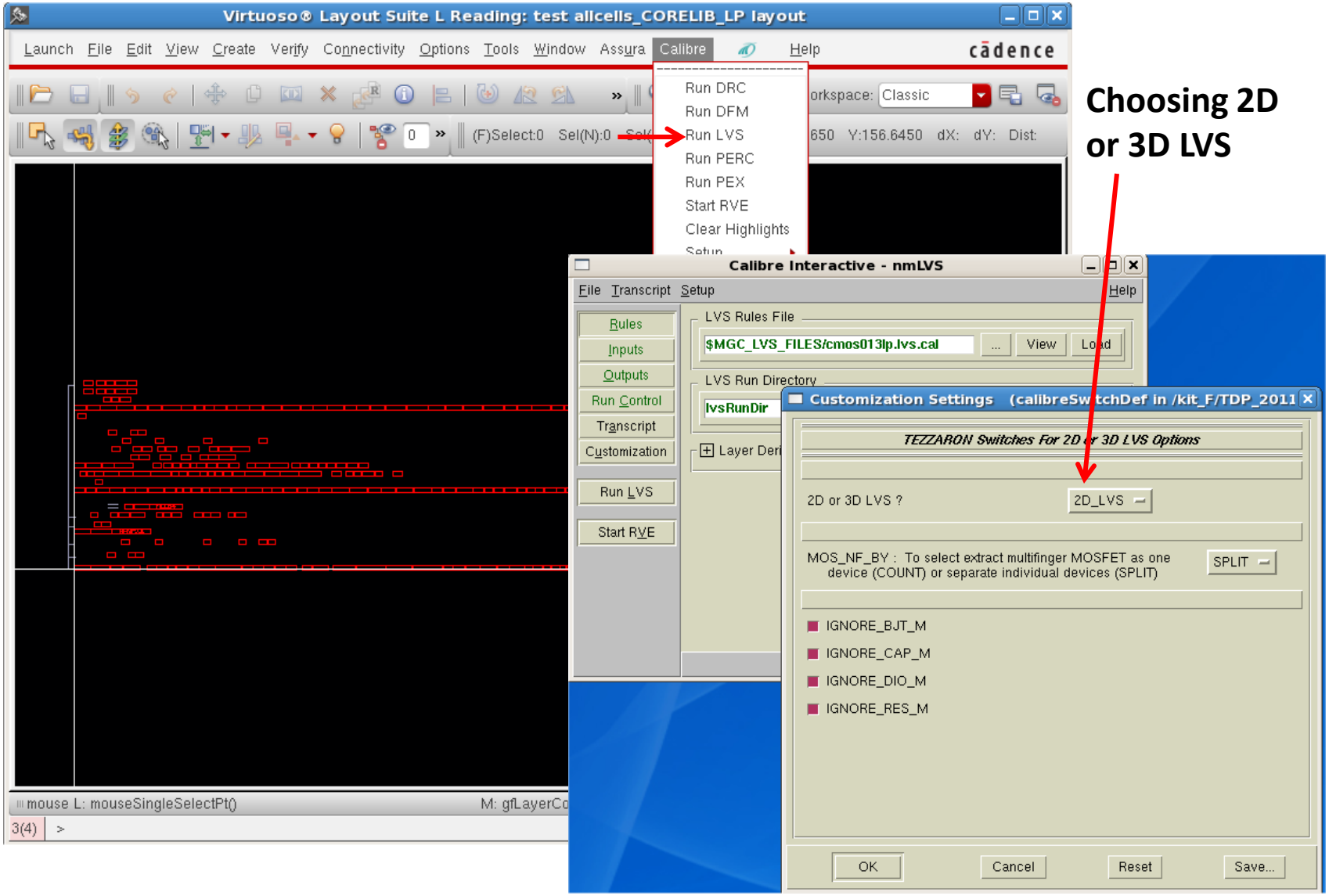


Setting switches graphically

Virtuoso / Calibre LVS Interactive Menu

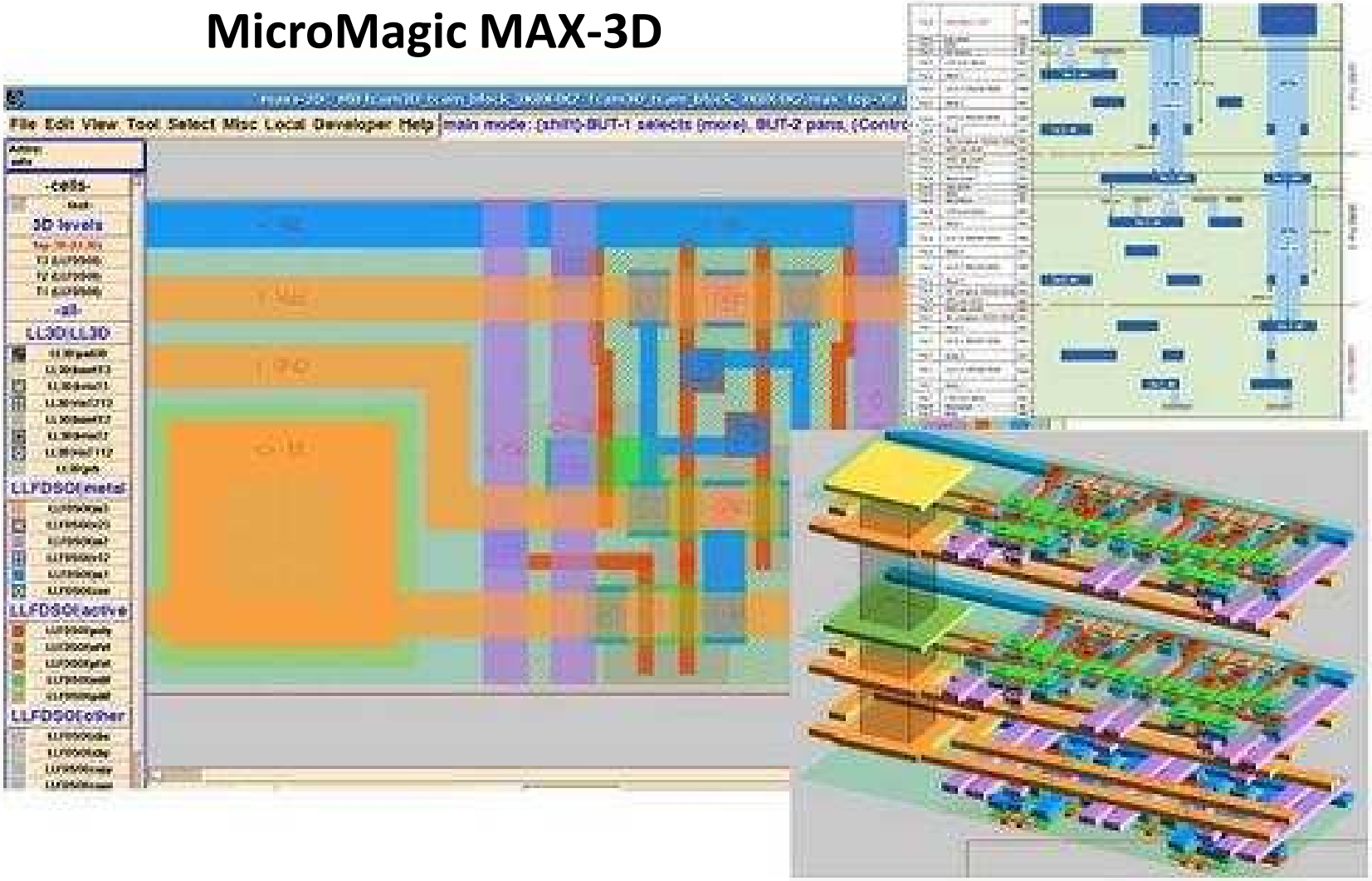


Choosing 2D or 3D LVS

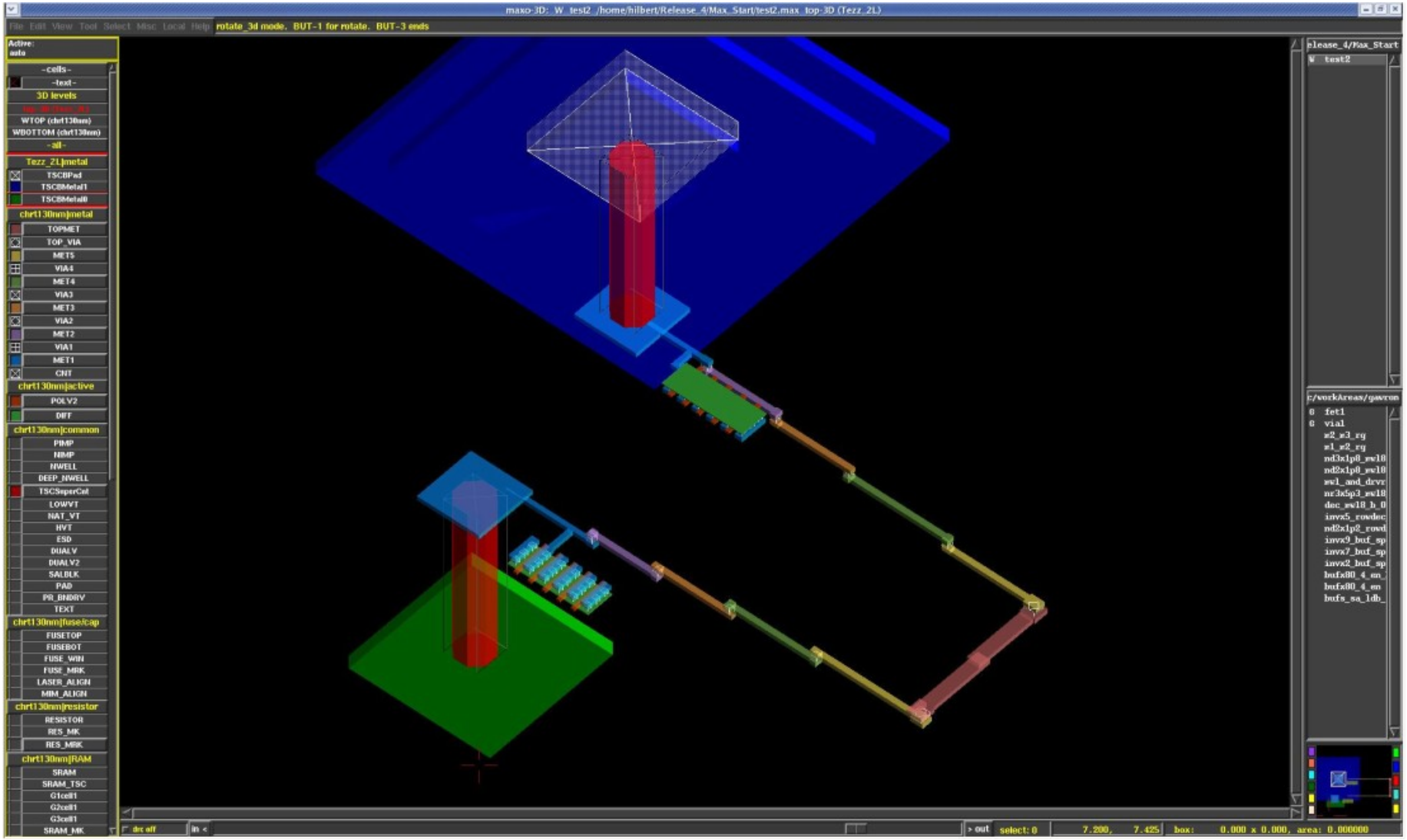
True 3D Mask Layout Editor

Technology Files fully supported by Tezzaron

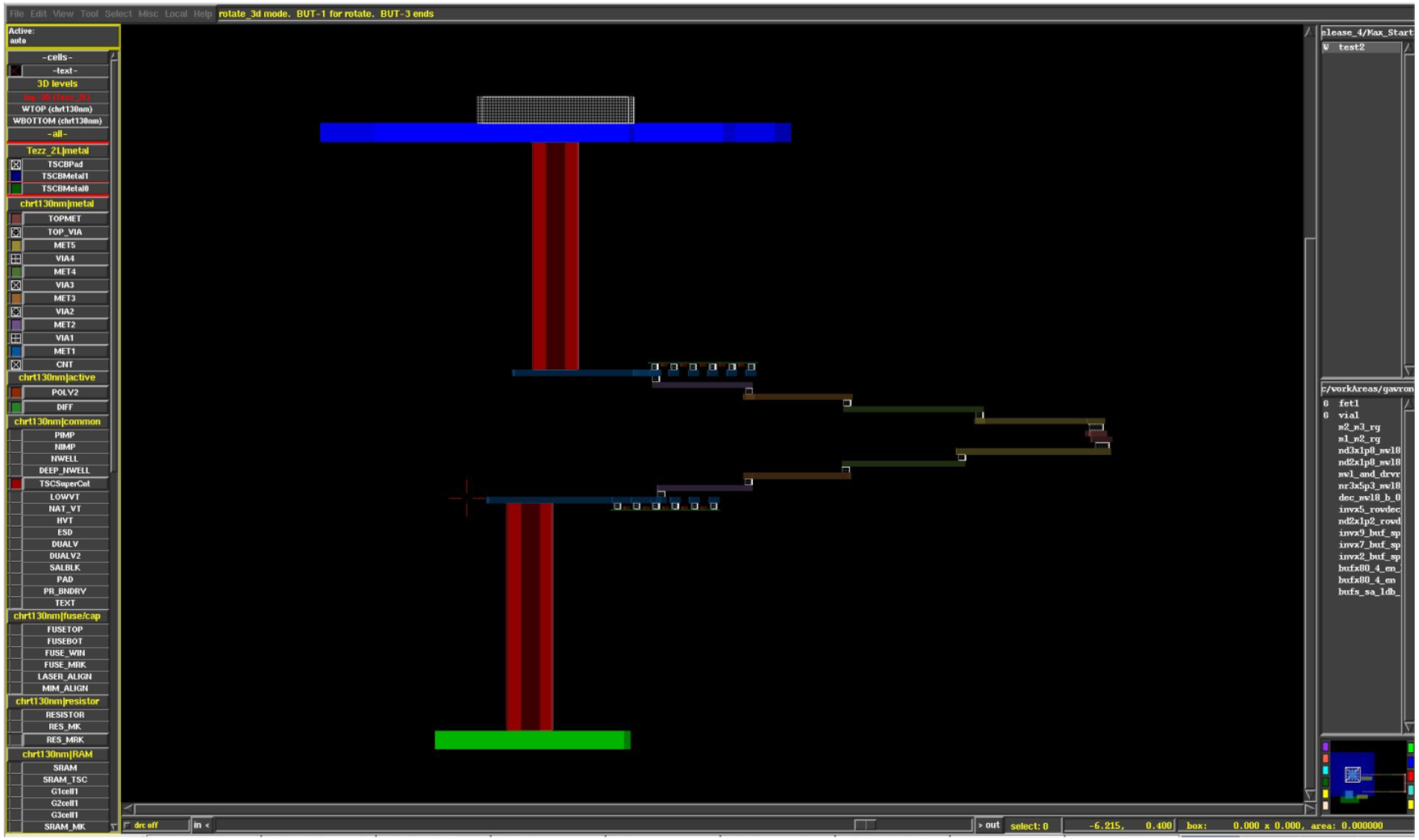
MicroMagic MAX-3D



MicroMagic 3D viewer



MicroMagic 3D crossection

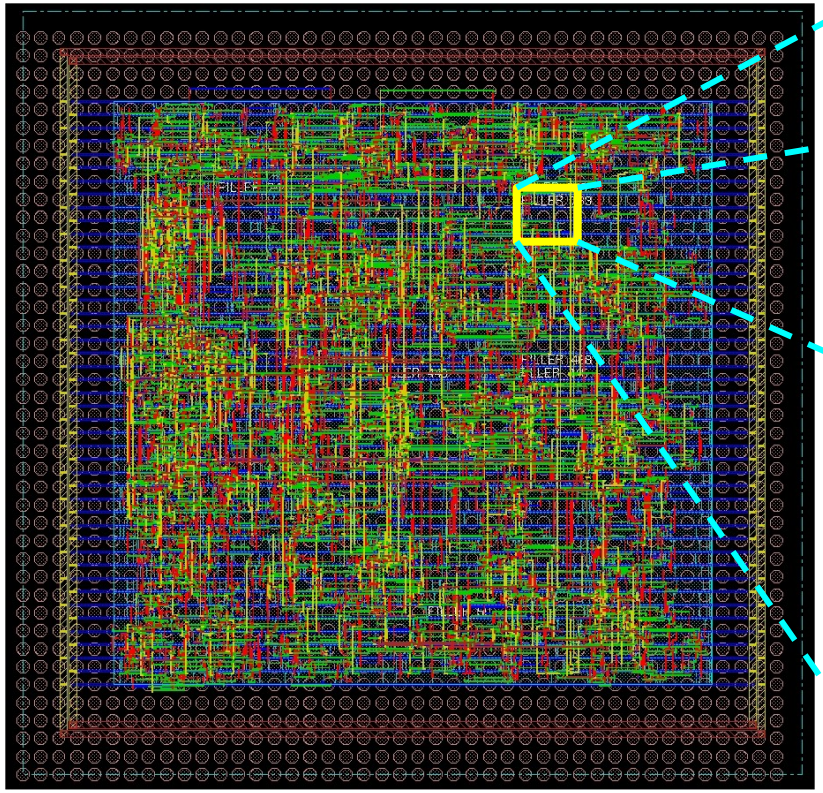


3D-IC Automatic P&R using DBI and TSV

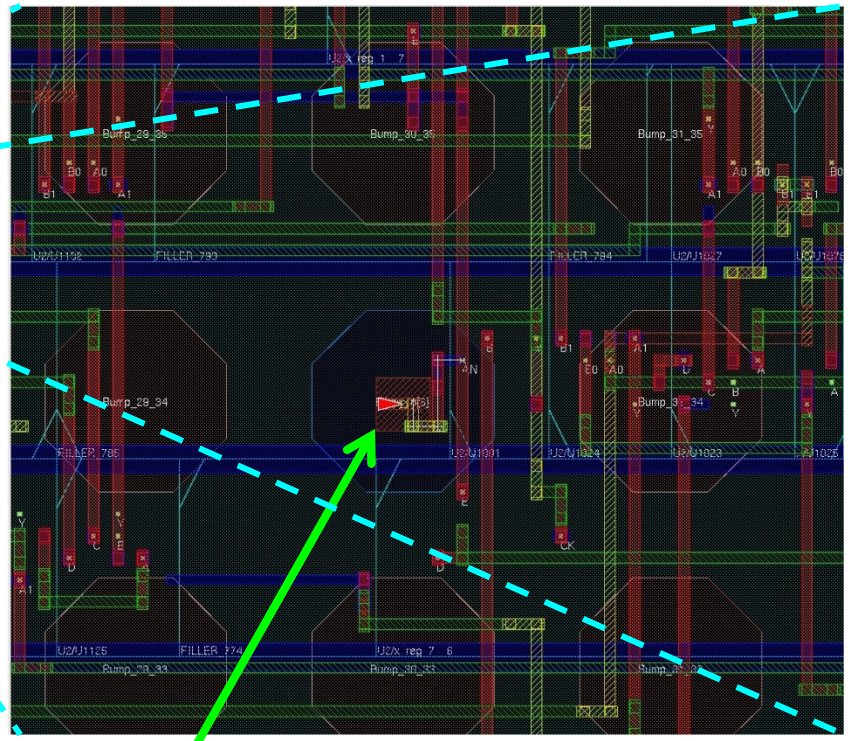
System Level Partitioning	Design exploration at system level
3D Floor-Planning DBI, TSV, IO placement	Design exploration at the physical level DBI, TSV, and IO placement & optimization
Automatic Place & Route	Cells and blocks place & route can be done tier by tier
Extraction, Timing Analysis	To be done for each tier, then combined for back-annotation to the 3D top level system
Physical verification 3D DRC, 3D LVS	Similar to the full-custom design flow
Dummies Filling	
Final 3D DRC	

Automatic P&R with Direct Bond Interface

- Encounter natively refuses to make the routing for pins on DBIs.
- Custom scripts solve the problem.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc …



DBI array generation + P&R

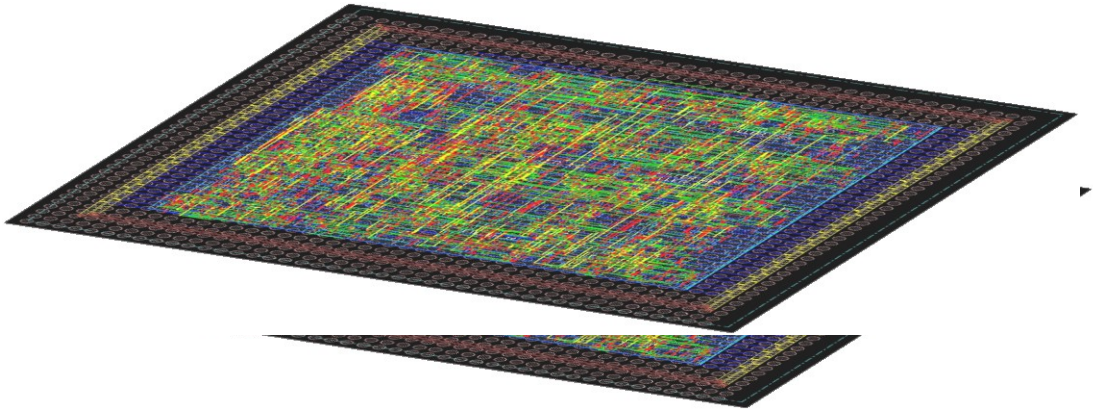


DBI completely routed down to the lower metal layers

Automatic P&R with Direct Bond Interface

Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

The place & route for both tiers is optimal for timing, buffer sizing and power performance.



This results in a "correct-by-construction" design.

Access to the Design-Rules and the Design Platform

http://cmp.imag.fr

Customer Request → **NDA Edition** → NDA → **Signed NDA reception**

Request to access from CMP Web page or by E-mail to :

cmp@imag.fr

The user receive by E-mail the NDA + ARM lirary Addendum.

The user sign and return by post 2 original signed copies

CMP forward to Tezzaron the NDAs.

When Tezzaron is OK, they counter-sign and return one copy to CMP.

CMP return the copy to the user and give the access to the DRM and Design-Platform.

Foundry's Agreement

Yes

Design kit
&
Design Rules access

Users having access to the Design Platform

CNRS – INPG – UJF

CPPM, Marseille, France
IPHC, Strasbourg, France
LAL, Orsay, France
LPNHE, Paris, France
IRFU, CEA Saclay, France
LAPP, Annecy-Le-Vieux, France
ENSTA PARISTECH, Paris, France
ISEA, Toulouse, France
ENSSAT – Universite Rennes, France
CEA-DIF, France

University of Bergamo, Italy
University of Bologna, Italy
University of Perugia, Italy
INFN, Roma, Italy
INFN, Pavia, Italy
INFN, Pisa, Italy

University of Bonn, Germany
University of Barcelona, Spain
IMSE-CNM-CSIC, Sevilla, Spain
TuDelft, The Netherlands
University of Turku, Finland
Norwegian University, Trondheim, Norway

22 Users in Europe

Tezzaron Semiconductor, USA

FermiLab, USA

North Carolina State University, USA

MOSIS, USA
CMC Microsystems, Canada

University of Sherbrooke, Canada

+ Other centers supported by MOSIS and CMC
Not listed here.

Conclusion

- CMC-CMP-MOSIS collaborating to offer services for 3D-IC prototyping and low volume production.
- Continuous enhancements on the Design Platform offering updates, features, and design methodologies.
- First MPW run deadline : May 31st, 2011