



8th International Meeting on Front-End Electronics
Bergamo, May 24-27, 2011



CMC-CMP-MOSIS collaboration for a 3D-IC prototyping service

Khouldoun TORKI

Khouldoun.Torki@imag.fr

CMP

46, Avenue Félix Viallet,

38031 Grenoble, France

<http://cmp.imag.fr>

Agenda

- **Introduction & Motivation for 3D-IC**
- **Process overview**
- **Partnership for MPW runs service**
- **3D-IC Design Platform**
- **Conclusion**

3D-IC Integration : Not a New Story

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure"
 IEEE Proceedings of International Electron Devices Meetings, Vo. 32, **1986**, pp. 488-491.

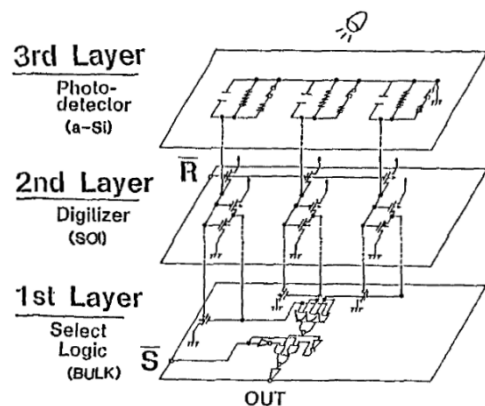


Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

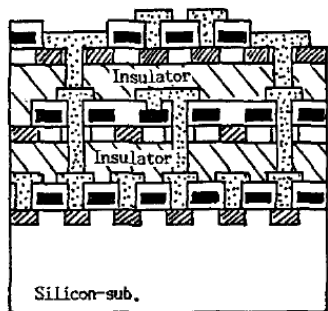


Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

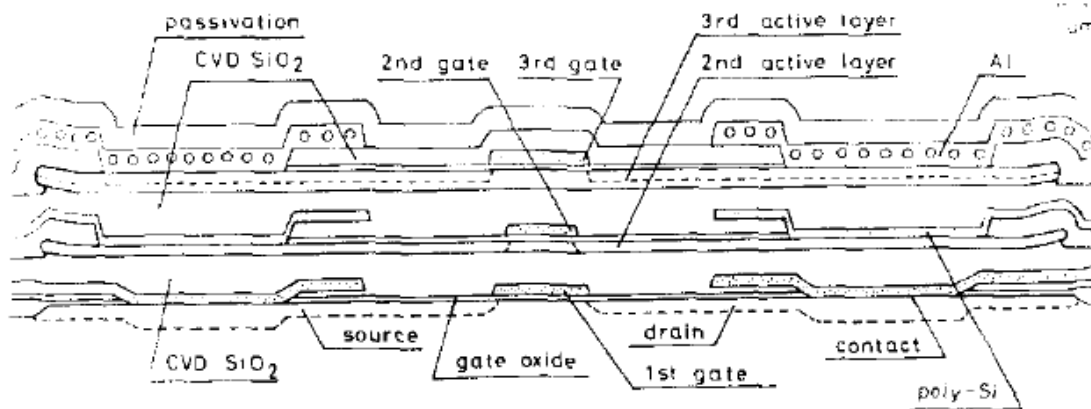
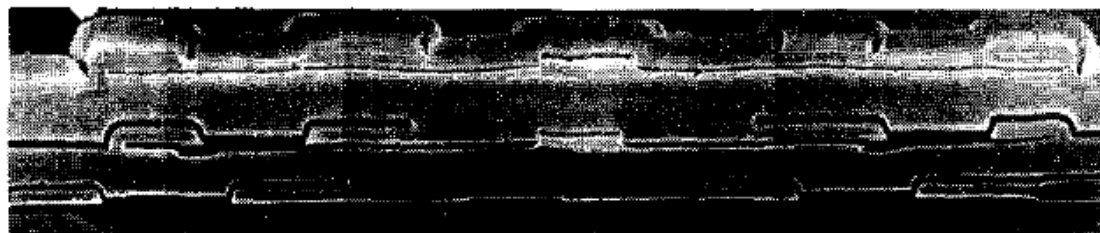
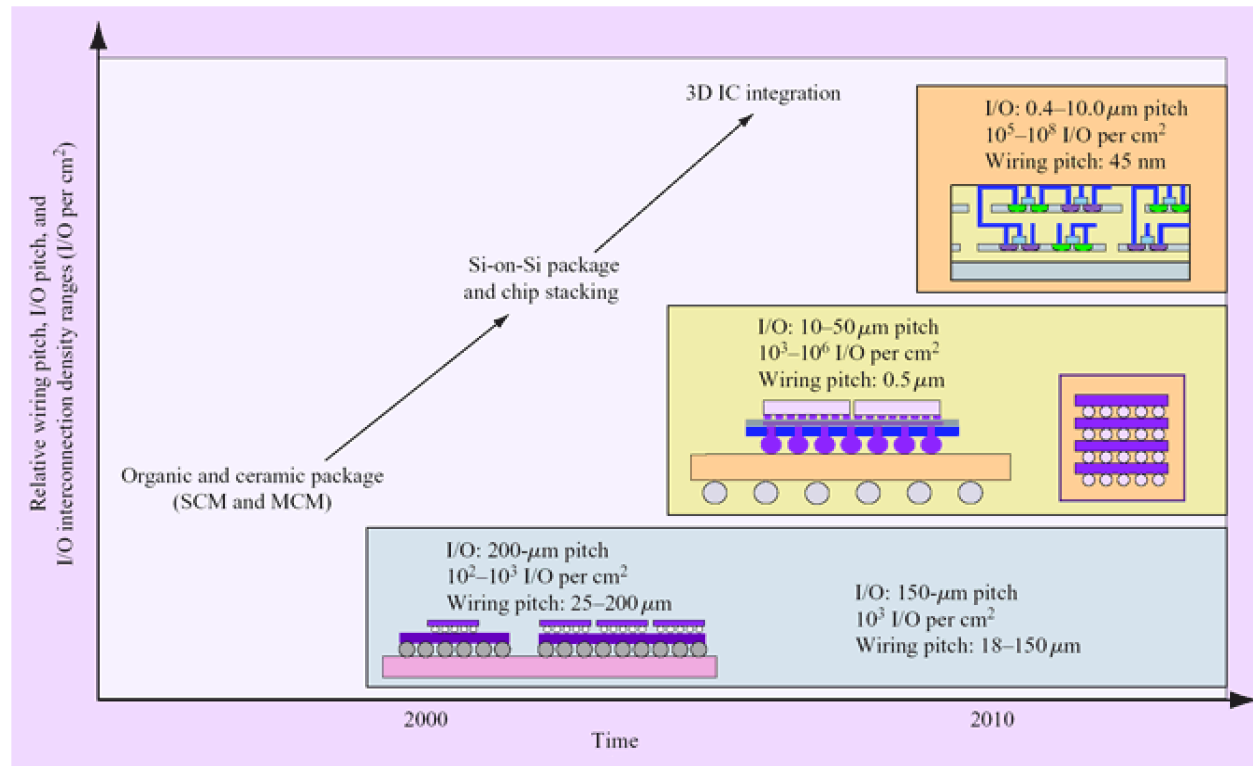


Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.

3D-IC Integration : The Other Path for Scaling



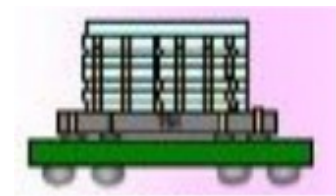
Source IBM <http://www.research.ibm.com/journal/rd/526/knickerbocker.html>

- Moore's law by scaling conventional CMOS involves huge investments.
- 3D IC processes : An opportunity for another path towards continuing the scaling, involving less investments.
- Like for conventional CMOS, infrastructures are needed to promote 3D-IC integration, making it available for prototyping at "reasonable" costs.

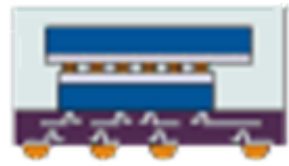
Two Worlds with Different Integration Approaches

“Monolithic”

Distributing a whole system across several tiers



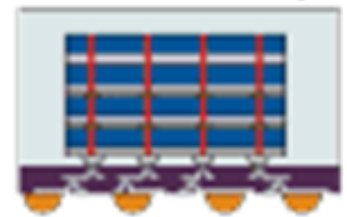
Heterogeneous Multi layer 3D-IC TSV integrated



3D-IC TSV integrated



3D-IC face to face



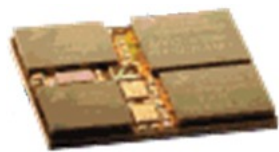
3D-IC TSV Stacked Memory



Silicon Interposer to high Integrated MCM



Die to Die Integrated package



Multi-Chip Module



Substrate based Module (PCB)

Integration

“Discrete”

Assembly of “Known Good Dies”

Which Design Methodology ?

- Discrete : **3D packaging, stacked dies, ...**

- 1- Design a whole system.

- 2- Split it in subsystems.

- 3- Place the subsystems as predefined “Known Good Dies” (IPs).

- 4- Determine and place the interfaces in between.

- 5- The system is done

- Monolithic : **3D-IC Integration**

- 1- Design a whole system.

- 2- Split it in subsystems.

- 3- Determine and place the interfaces in between.

- 4- Generate and Place the subsystems in between the interfaces.

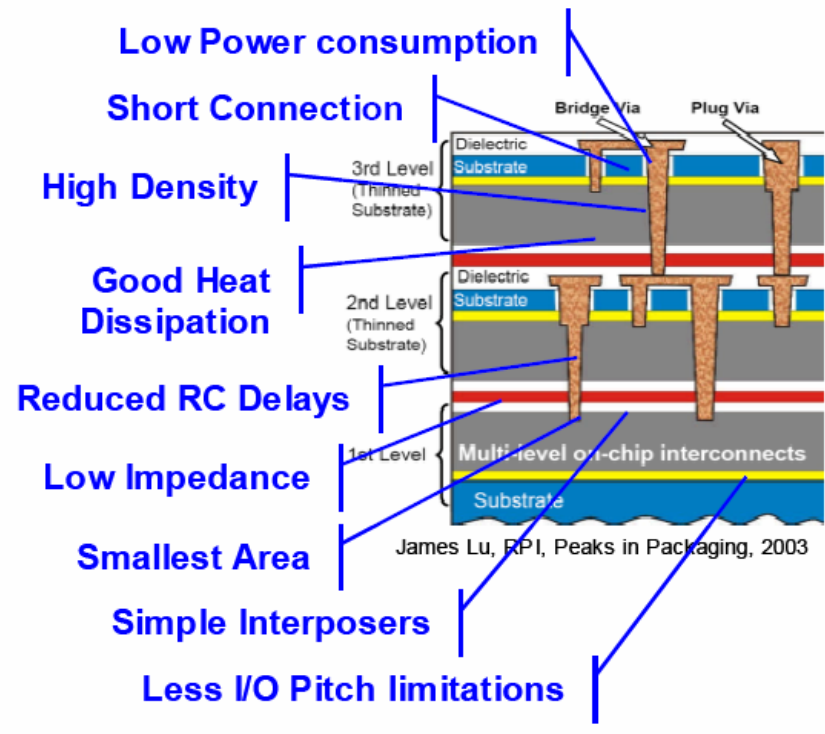
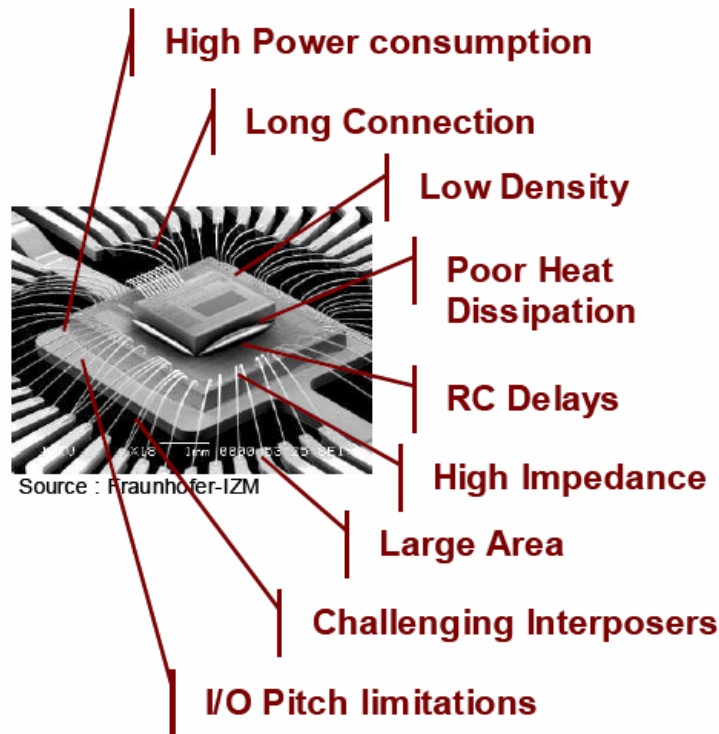
- 5- The system is done

Here comes the difference : The “key” for a true 3D-IC Integration

SiP versus 3D-IC

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



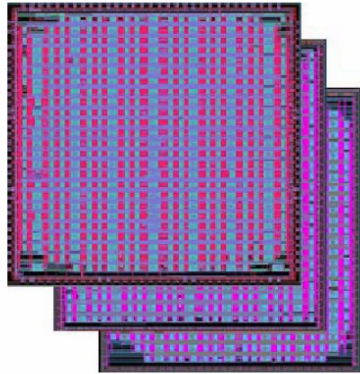
TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Large Systems Benefits from 3D-IC Integration

"Implementing a 2-Gbs 1024-bit ½-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"

Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrarng, Bo Hu, and C.-J. Richard Shi
University of Washington

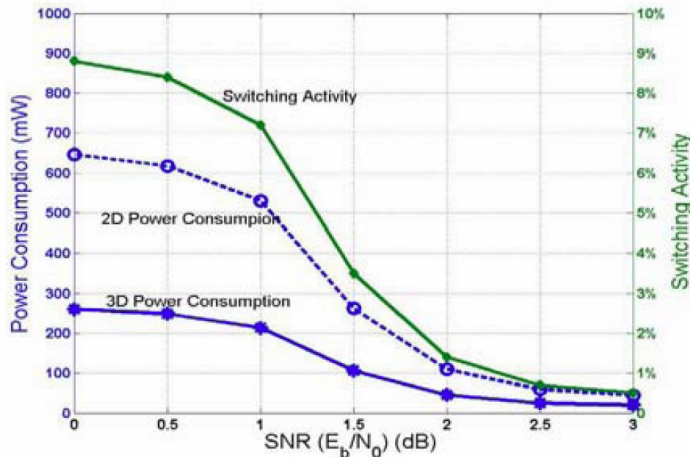
International Conference on Computer Design, ICCD, Oct. 2007



Final layout view of 3D LDPC structure.

Comparison between 2D and 3D designs

	2D design	3D design
Area (mm*mm)	18.238*15.92 = 290.35	(6.4*6.227)*3 = 119.56
Total wire length (m)	182.42	22.39+22.57+22.46 = 67.42
Max WL before buffer insertion (mm)	13.82	8.68
Max WL after buffer insertion (mm)	4	4
Buffer used	32900	24636
Clock skew (ns)	2.33	1
Power dissipation (mw)	646.2	260.2

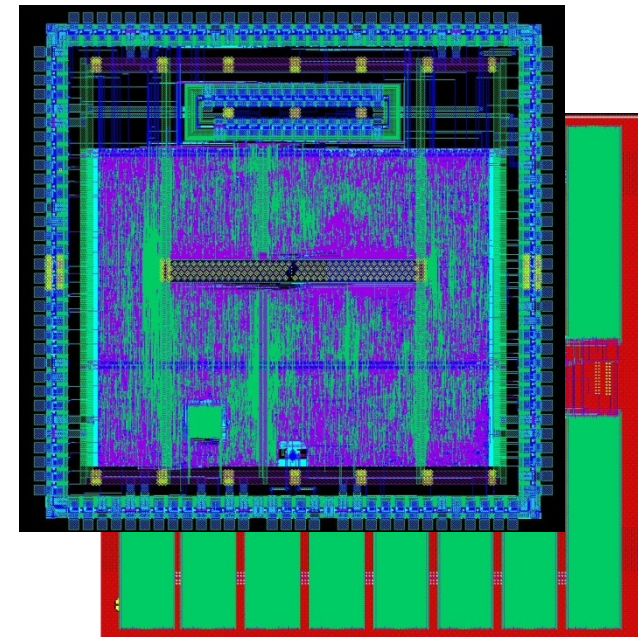
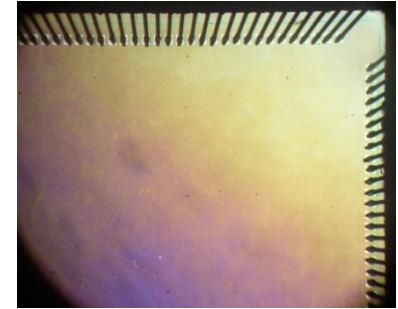


Post-layout power of the LDPC decoder (2D vs 3D).

Performance Factor (Area * Timing * Power) = 14

- R8051 CPU
 - 80MHz operation; 140MHz Lab test (VDD High)
 - 220MHz Memory interface
- IEEE 754 Floating point coprocessor
- 32 bit Integer coprocessor
- 2 UARTs, Int. Cont., 3 Timers, ...
- Crypto functions
- 128KBytes/layer main memory

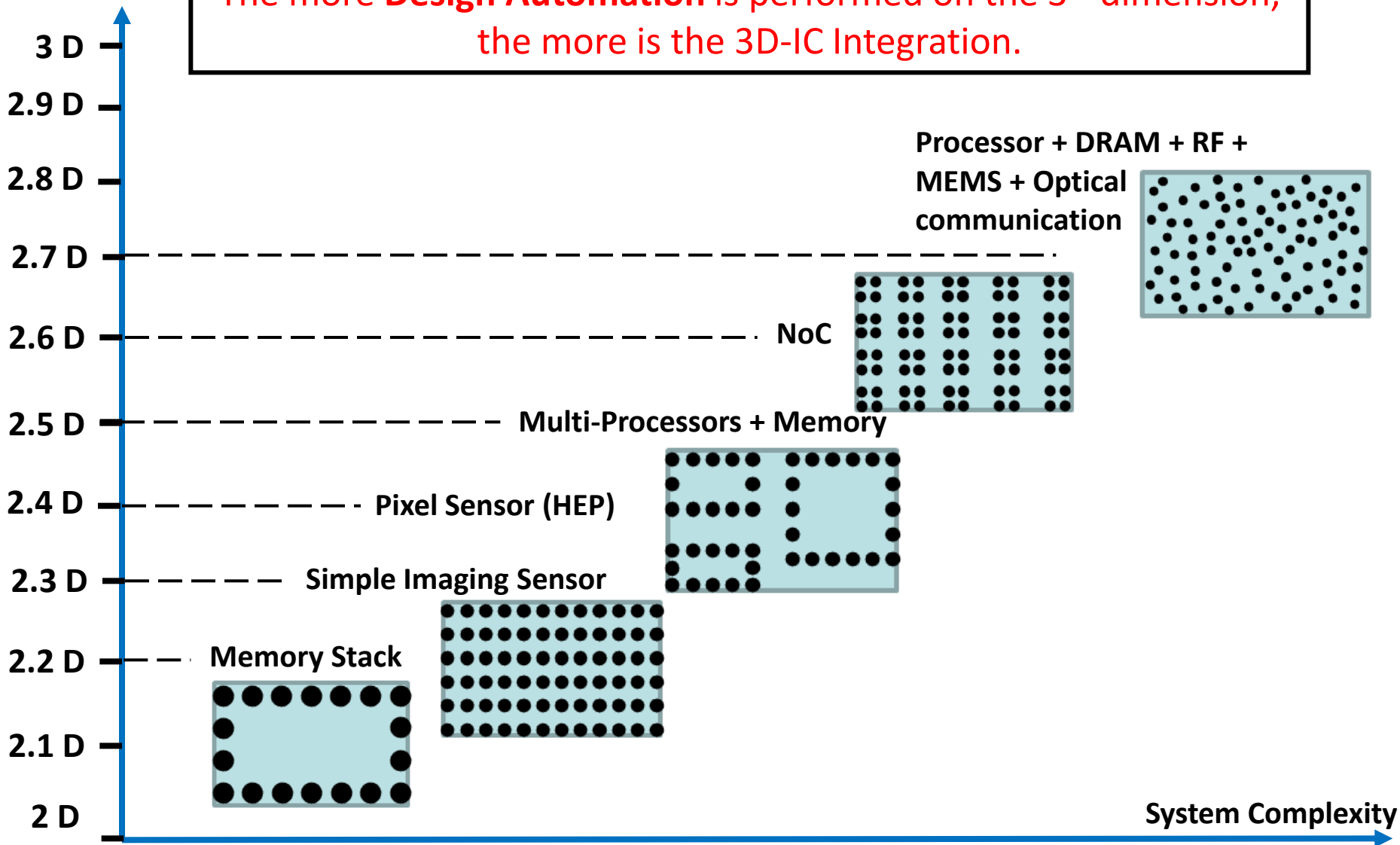
- **5X performance**
- **1/10th Power**



Source Tezzaron (2004)

Design Methodology

The more **Design Automation** is performed on the 3rd dimension, the more is the 3D-IC Integration.



CMC-CMP-MOSIS Collaboration

CMC / CMP / MOSIS partnering for 3D-IC process access

- **Stimulate the activity by sharing the expenses for manufacturing.**
- **Join forces for the technical support, and dedicate roles for each partner.**
- **Make easier the tech support for local users respectively by each local center.**
- **Because there is no standard for the 3D-IC integration, it is urgent to setup an infrastructure making possible a broad adoption of 3D-ICs. That will have a beneficial effect on prices, more frequent MPW runs, and more skilled engineers.**



CNRS - INPG - UJF

CMC-CMP-MOSIS partnering on 3D-IC



CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC

MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

The first MPW run is scheduled to 31 May 2011:

- 2-tier face-to-face bonded wafers
- 130nm CMOS process for both tiers
- Top tier exposing TSV and backside metal pads for wire bonding.

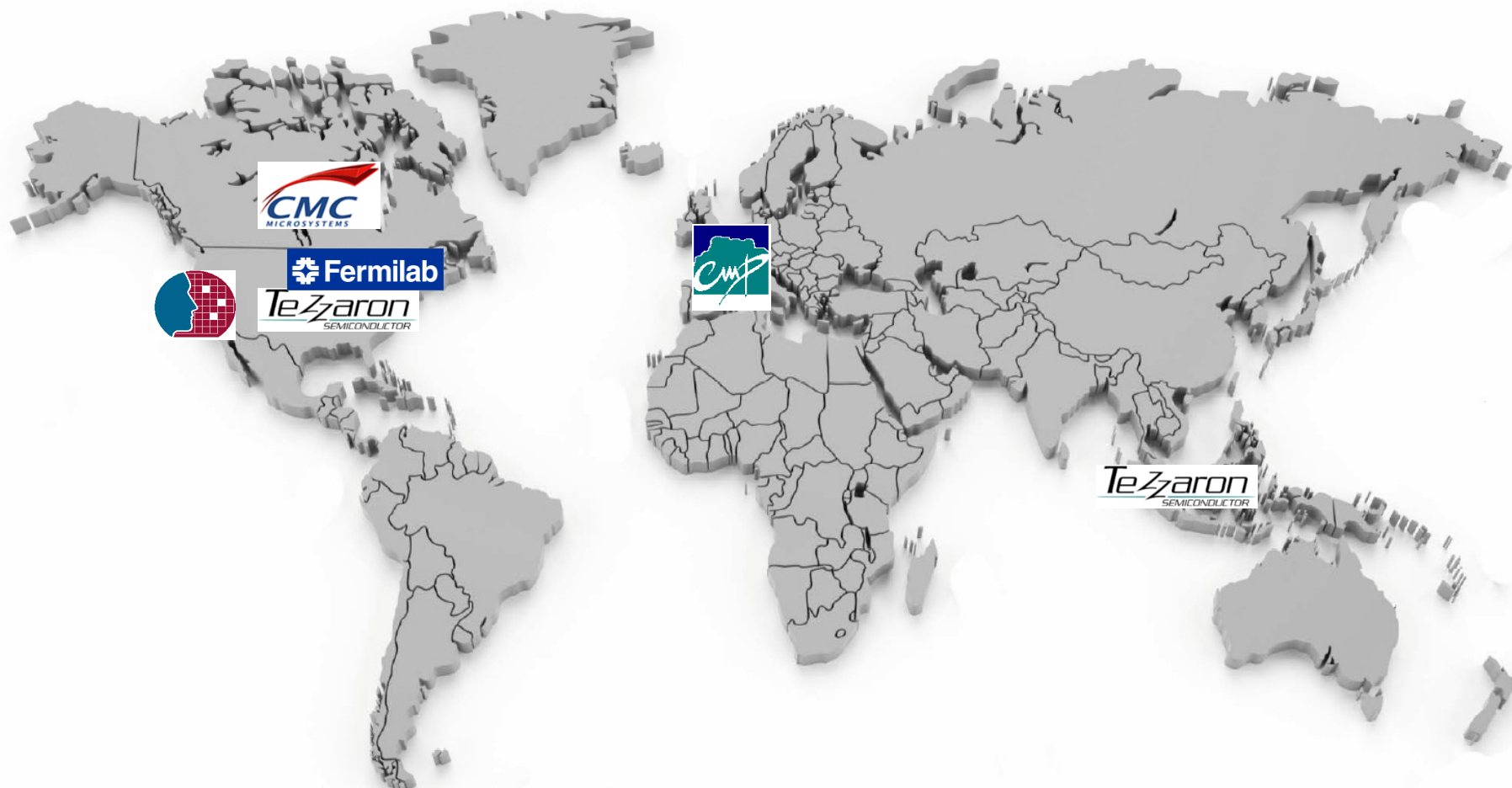
A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

Further MPW runs will be scheduled supporting process flavors (multiple tiers beyond 2, different CMOS flavors for different tiers, ...) driven by user requirements.

Potential users are encouraged to contact **CMP** for details : cmp@imag.fr

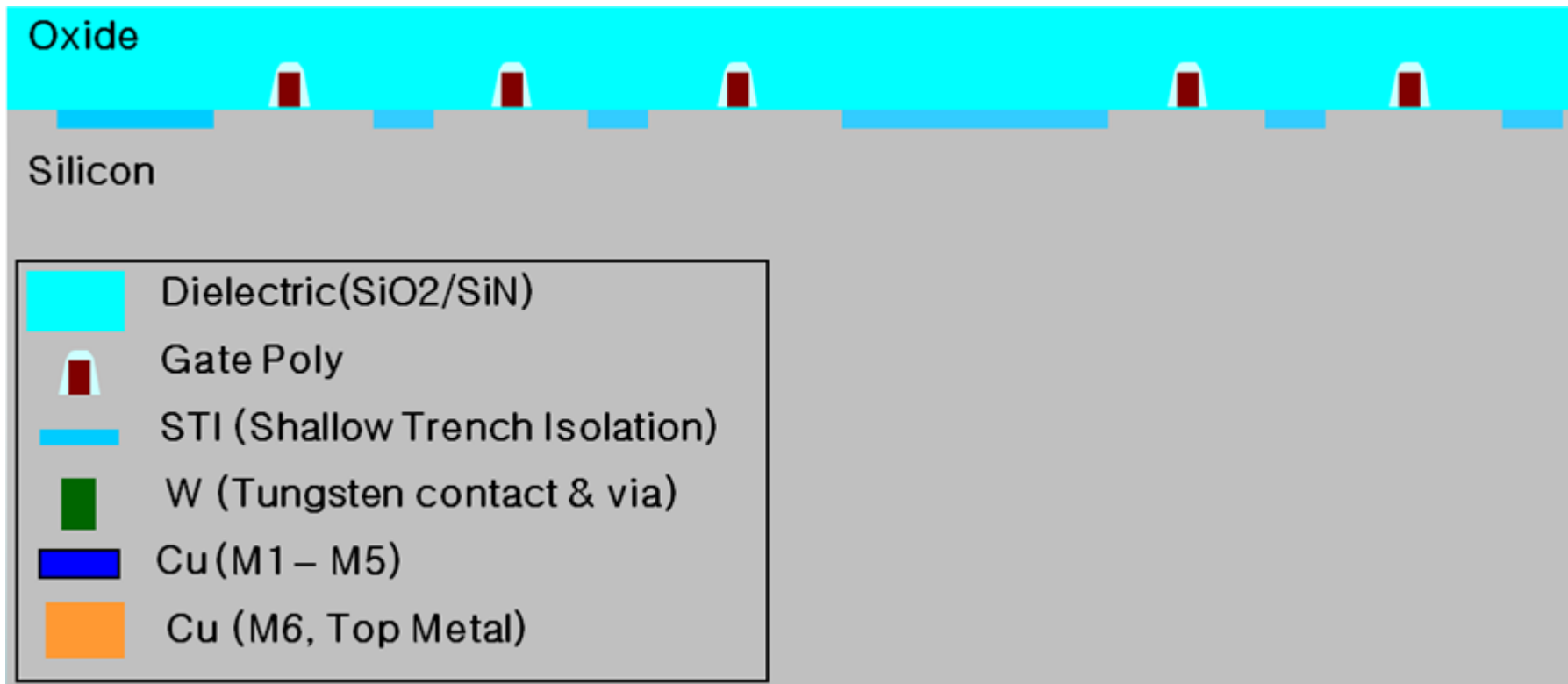
CMC - CMP - MOSIS Cooperation

- CMC supporting Canadian Customers
- CMP supporting European Customers
- MOSIS supporting US Customers



Tezzaron 2-Tier Process (130nm CMOS)

Process Overview



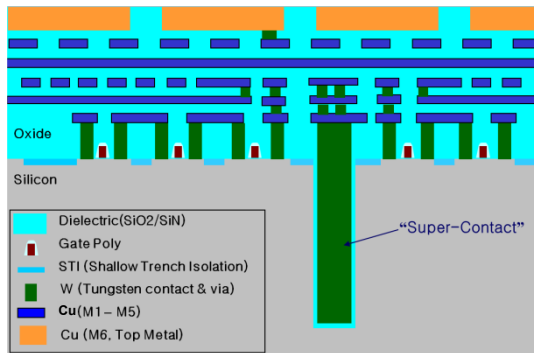
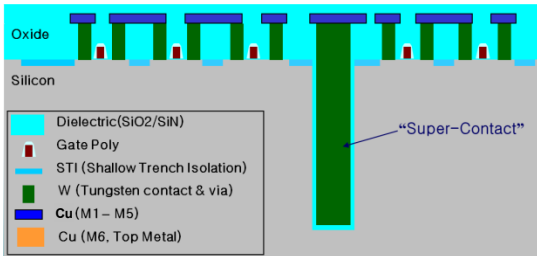
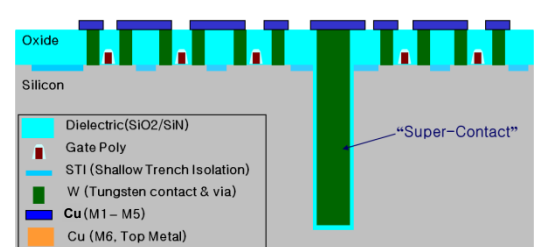
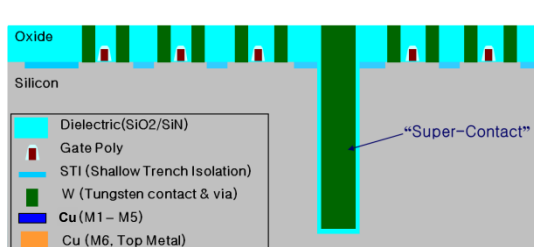
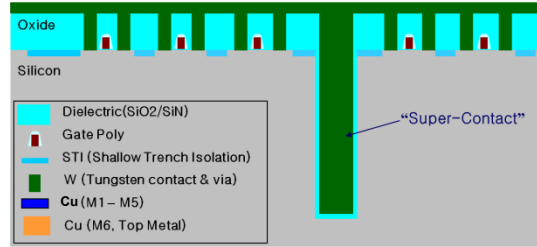
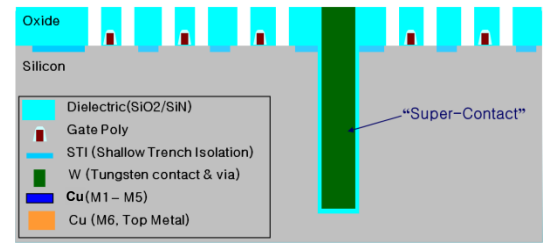
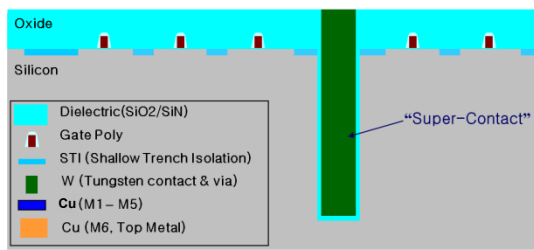
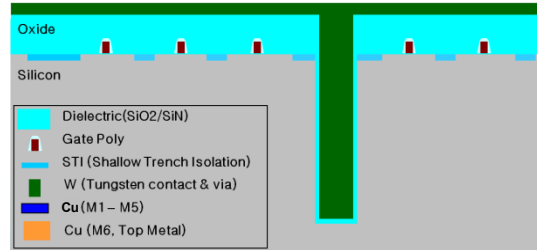
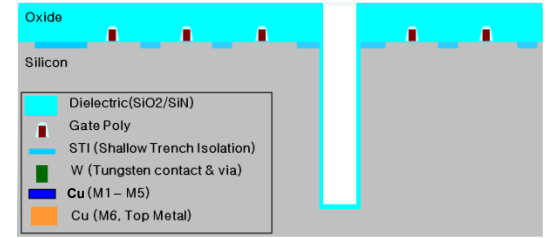
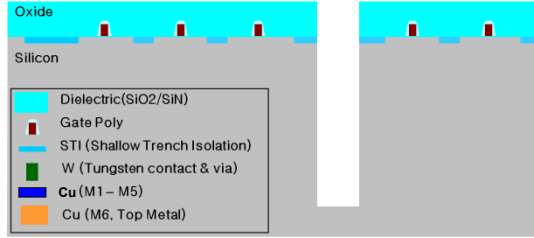
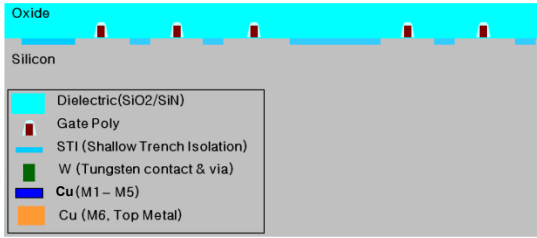
Starting wafer in 130nm (5 Cu metal layers + 6th Cu metal as DBI)

Source Tezzaron



Tezzaron Process Flow for TSV and DBI (using Via Middle process)

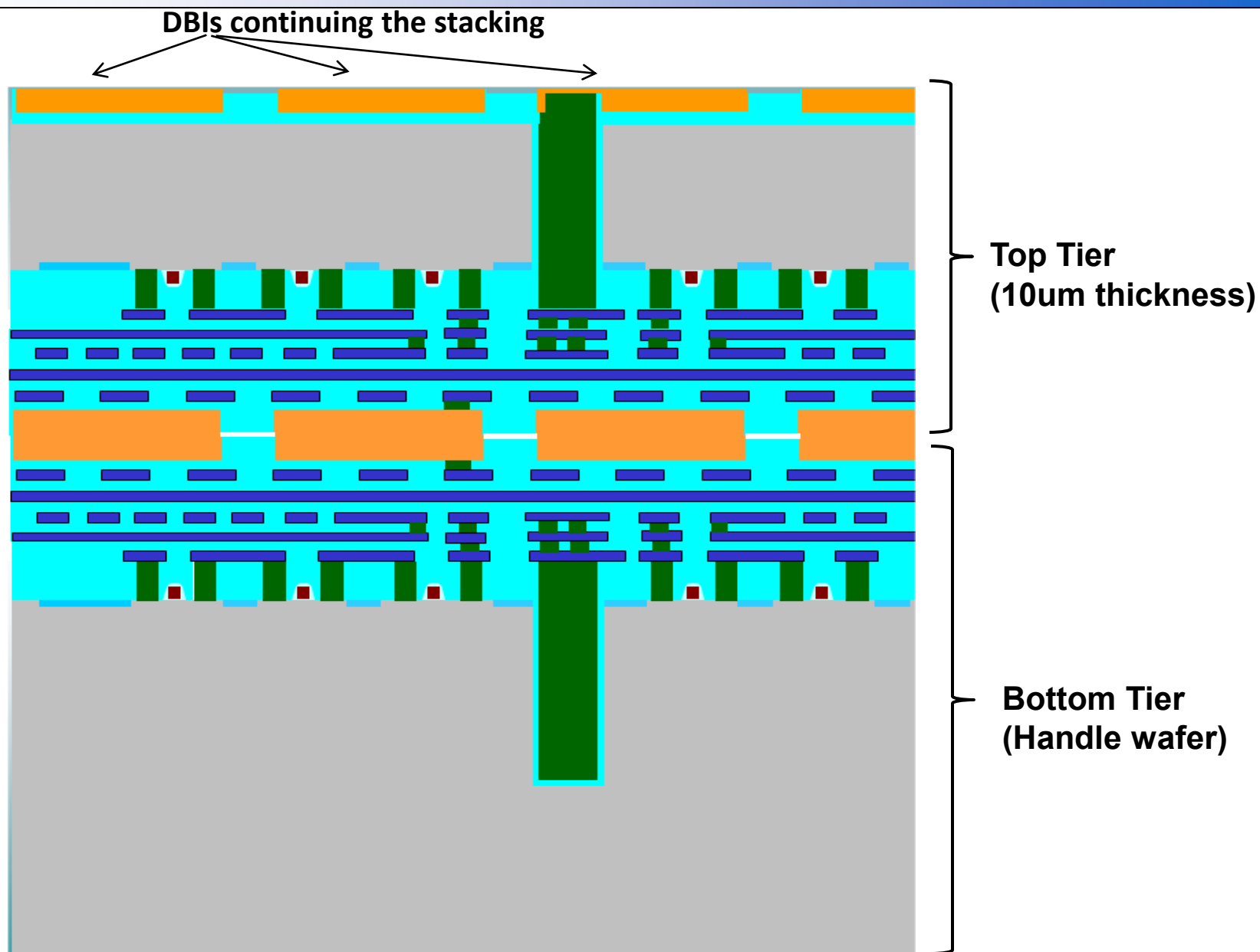
CNRS - INPG - UJF





Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)

CNRS - INPG - UJF

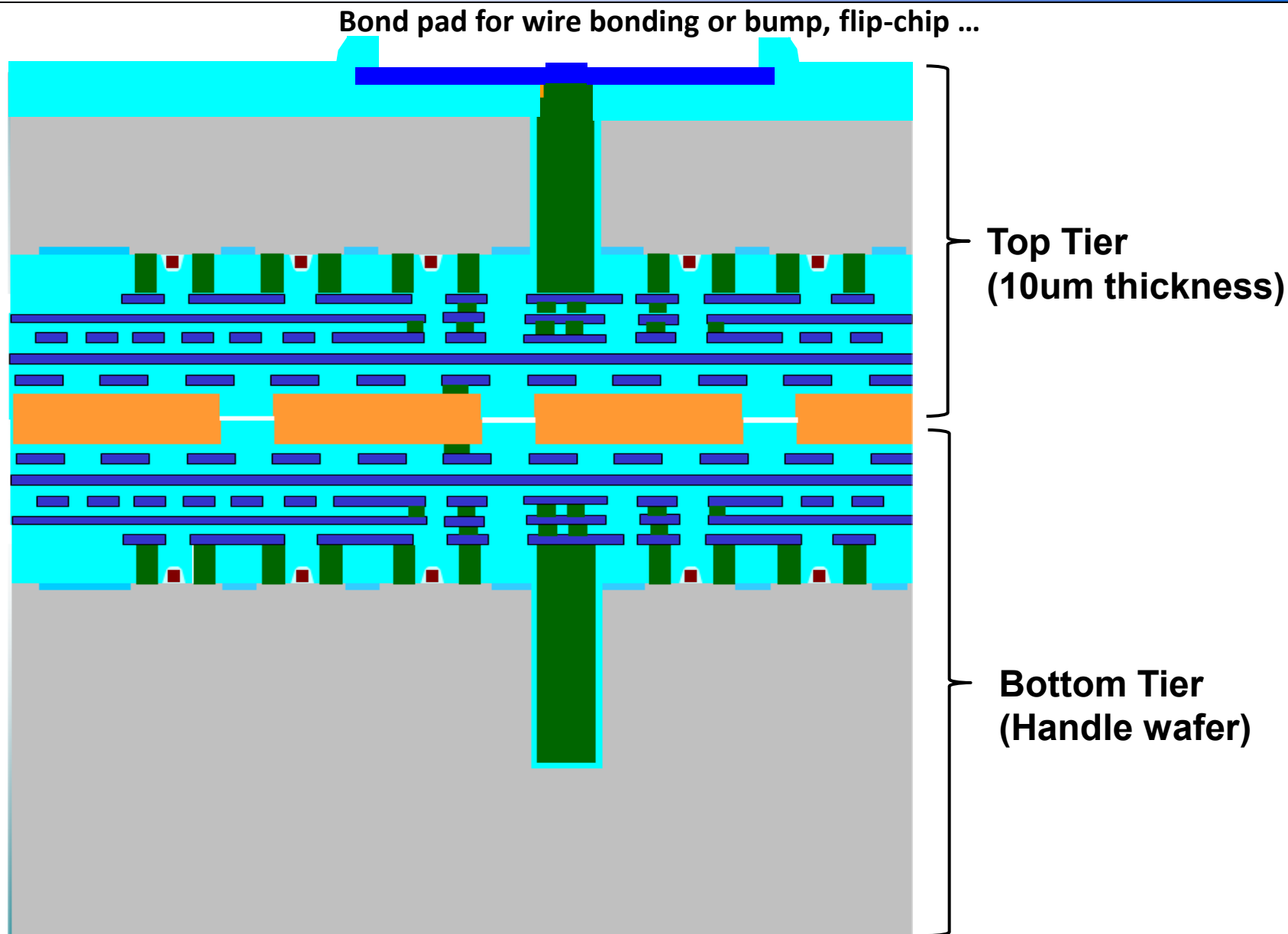


Source Tezzaron



CNRS - INPG - UJF

Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)

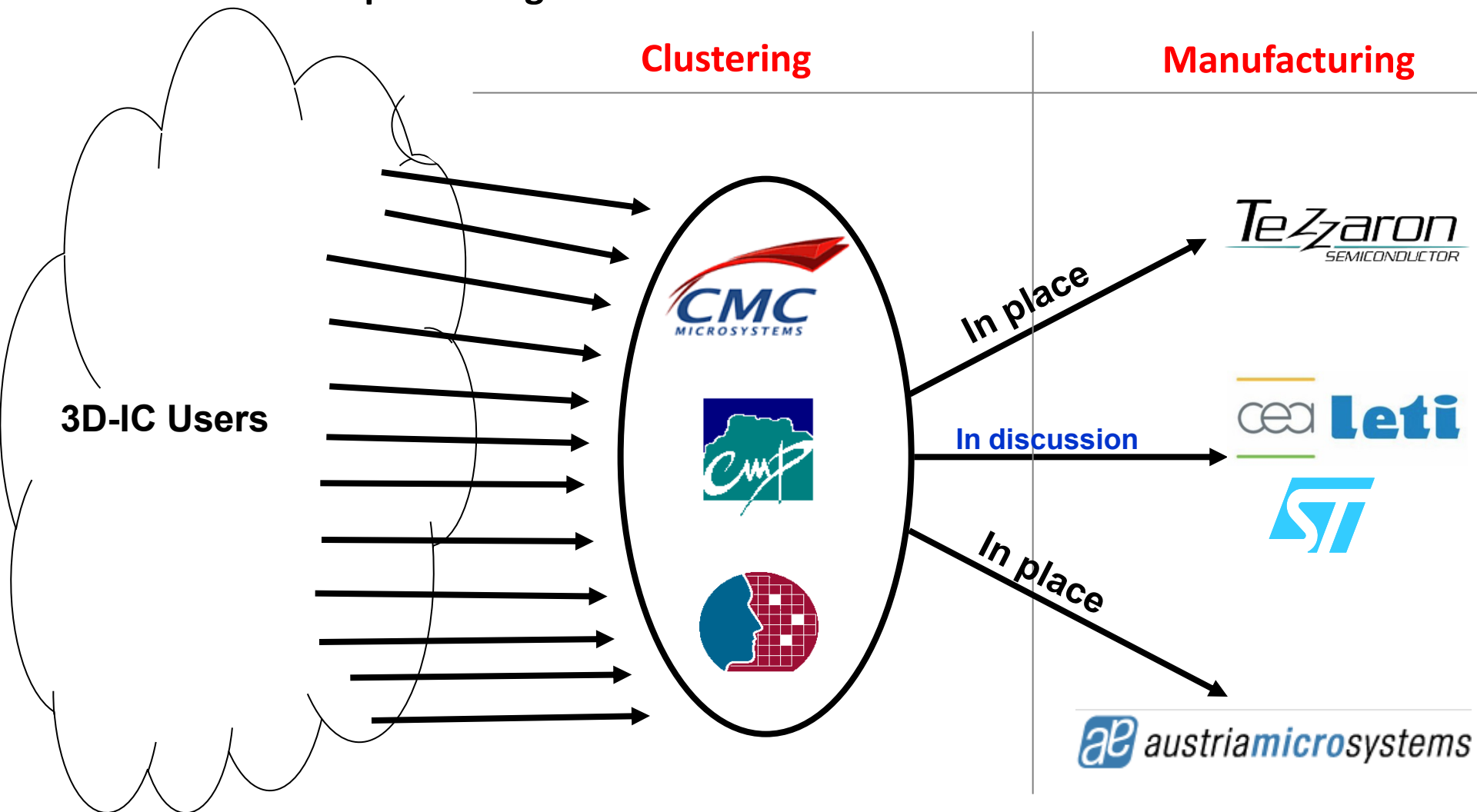


Source Tezzaron

3D-IC MPW runs

3D-IC MPW Infrastructure

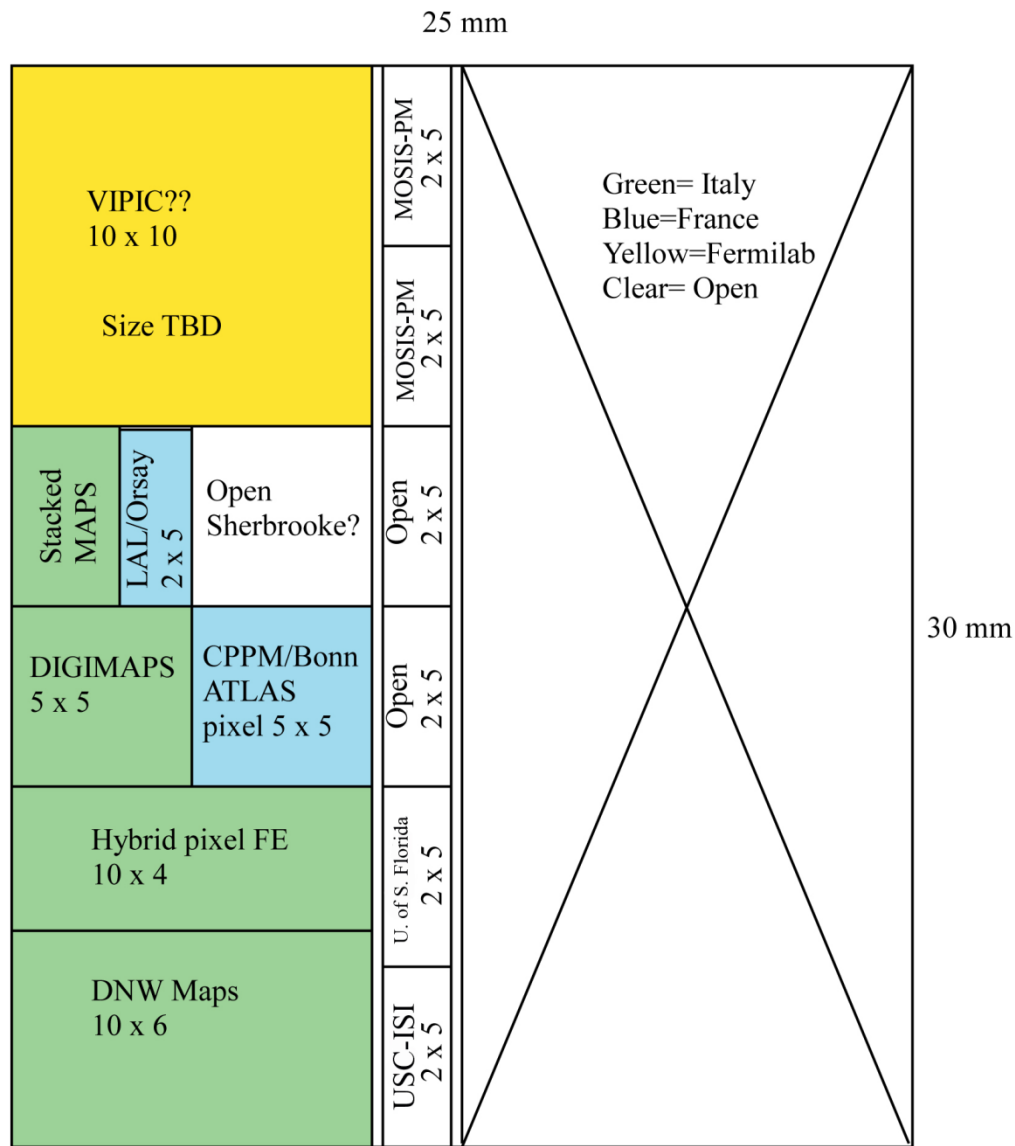
CMC-CMP-MOSIS partnering to offer 3D-IC MPW runs



Critical mass will allow frequent MPW runs and low pricing



CMP/MOSIS/CMC : 1st MPW run



MPW run deadline : May 31st, 2011

3D-IC Design Platform

- The Design Platform is modular. It has all features for full-custom design or semi-custom automatic generation design.
 - **PDK** : *Original PDK from GF + (TSV / DBI) definition from Tezzaron*
 - **Libraries** : *CORE and IO standard libraries from ARM*
 - **Memory compilers** : *SPRAM, DPRAM and ROM from ARM*
 - **3D-IC Utilities** : *Contributions developments embedded in the platform*
 - **Tutorials, User's setup.**
- All modules inside the platform refer to a unique variable, making it portable to any site. The installation procedure is straightforward.
- Support of CDB and OpenAccess databases.



chrt13lprf_DK009_Rev_1D (Version issued in Q1 2011)

assura

calibre

cds_cdb

cds_oa

doc

eldo

hercules

hspice

prep3DLVS

skill

spectre

strmMaptables_ARM

strmMaptables_Encounter

assura:

FILLDRC

LVS

QRC

calibre:

3DDRC

3DLVS

DRC

FILLDRC

calibreSwitchDef

hercules:

DRC

LVS

STAR_RCXT

Collaborative Work on the Design Platform

HEP labs contributing with Programs, Libraries, and Utilities. All included in the Design Platform

- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)



Virtuoso Layout Editor with 3D layers and verification

Virtuoso from Cadence IC 5.1.41

TSV	NO_FILL	drw
	TSCSuperCnt	drw
	TSCBackMet0	drw
Back Metal	TSCBackMet0	lbl
	TSCBackMet1	drw
	TSCBackMet1	lbl
Back Pad	TSCBPad	drw
	SRAM_TSC	drw
	PR_BNDRY	drw
	NWELL	drw
	DNWELL	drw
	LD MOS_XTOR	mar
	COMP	drw
	POLY2	drw
	POLY2	lbl
	PPLUS	drw
	NPLUS	drw
	CNT	drw
	MET1	drw
	MET1	lbl
	VIA1	drw
	MET2	drw
	MET2	lbl
	VIA2	drw
	MET3	drw
	MET3	lbl
	VIA3	drw
	MET4	drw
	MET4	lbl
	VIA4	drw
	MET5	drw
	MET5	lbl
	VIATOP	drw
DBI	METTOP	drw

X: 12.500 Y: -4.115 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 2

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Calibre Tezaron Help

Calibre
Assura

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: hiZoomAbsoluteScale (hiGetCurrentWi



Customized Menu with some utilities

Virtuoso from Cadence IC 6.1.4

Layer	Object	Grid
AV	NV	AS NS
NO_FILL	drawing	
TSCSuperCnt	drawing	
TSCBackMet0	drawing	
TSCBackMet0	label	
TSCBackMet1	drawing	
TSCBackMet1	label	
TSCBPad	drawing	
SRAM_TSC	drawing	
PR_BNDRY	drawing	
NWELL	drawing	
DNWELL	drawing	
LDMOS_XTOR	marking	
COMP	drawing	
POLY2	drawing	
POLY2	label	
PPLUS	drawing	
NPLUS	drawing	
GNT	drawing	
MET1	drawing	
MET1	label	
VIA1	drawing	
MET2	drawing	
MET2	label	
VIA2	drawing	
MET3	drawing	
MET3	label	
VIA3	drawing	
MET4	drawing	
MET4	label	
VIA4	drawing	
MET5	drawing	
MET5	label	
VIATOP	drawing	
METTTOP	drawing	
METTTOP	label	
RDL_MK	marking	
LPN_dg	drawing	

Virtuoso® Layout Suite L Reading: CORELIB_LP allcells_CORELIB_LP layout

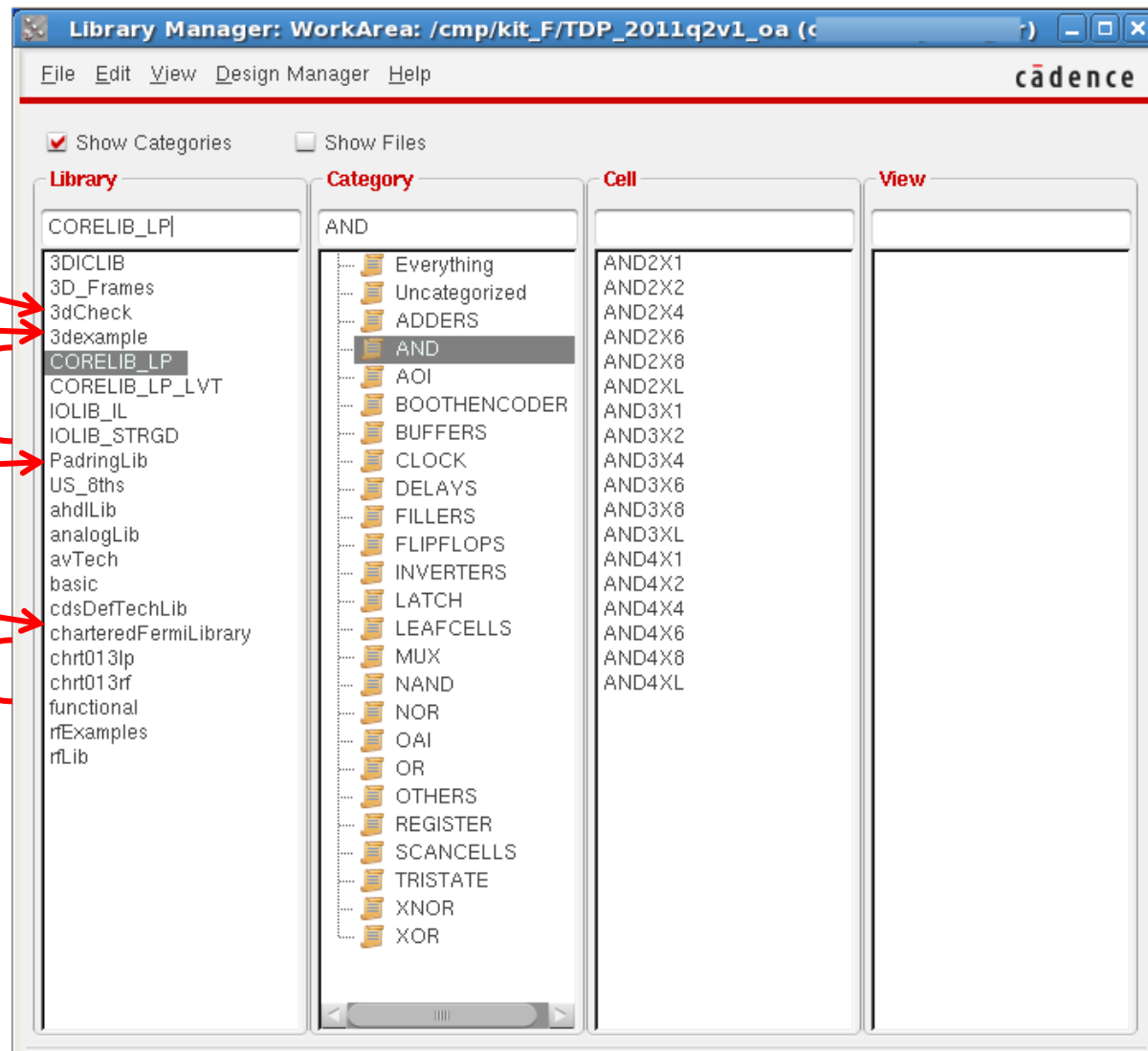
Launch File Edit View Create Verify Connectivity Options Tools Window Assura Calibre Help cadence

- *New Layers Colors
- *GF Layers Colors
- *myLSW
- *pgText
- *ZoomXY
- About Tezzaron

mouse L: mouseSingleSelectPt() M: hiRedraw() R: _IxHiMousePopUp()

2(3) > Cmd:

Libraries from Providers and Users





Virtuoso / Calibre DRC Interactive Menu

CNRS - INPG - UJF

The image shows a screenshot of the Virtuoso Layout Suite L Reading interface. The main window title is "Virtuoso® Layout Suite L Reading: test allcells_CORELIB_LP layout". The menu bar includes "Launch", "File", "Edit", "View", "Create", "Verify", "Connectivity", "Options", "Tools", "Window", "Assura", "Calibre", and "Help". The Calibre menu is open, showing options: "Run DRC", "Run DFM", "Run LVS", "Run PERC", "Run PEX", "Start RVE", "Clear Highlights", "Setup", and "About...". A red arrow points from the text "Setting switches graphically" to the "Setup" option in the Calibre menu. Below the main window, the "Calibre Interactive - nmDRC" dialog box is open. It has a sidebar with "Rules", "Inputs", "Outputs", "Run Control", "Transcript", and "Customization". The "Customization" section is selected, showing "Run DRC" and "Start RVE" buttons. A sub-dialog box titled "Customization Settings" is also open, showing "TEZZARON Switches For DRC Options" with two unchecked checkboxes: "Checking Density rules is mandatory for sign-off DRC" and "Check Floating Bond Interface METTOP". A red arrow points from the text "Setting switches graphically" to the "Customization Settings" dialog box.

Setting switches graphically

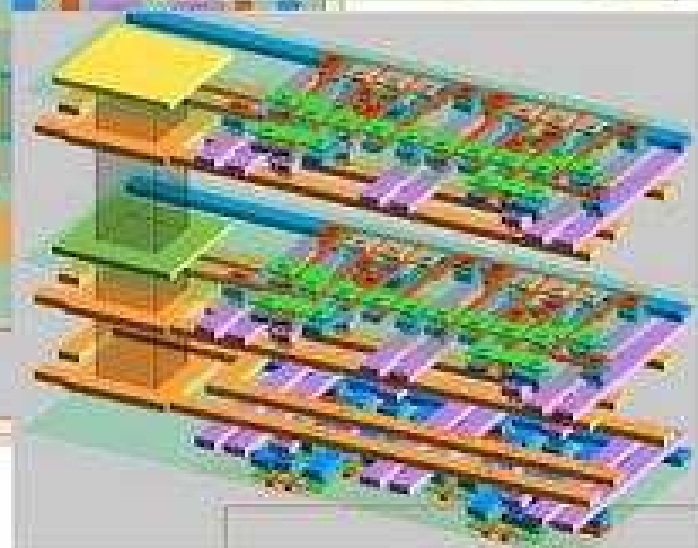
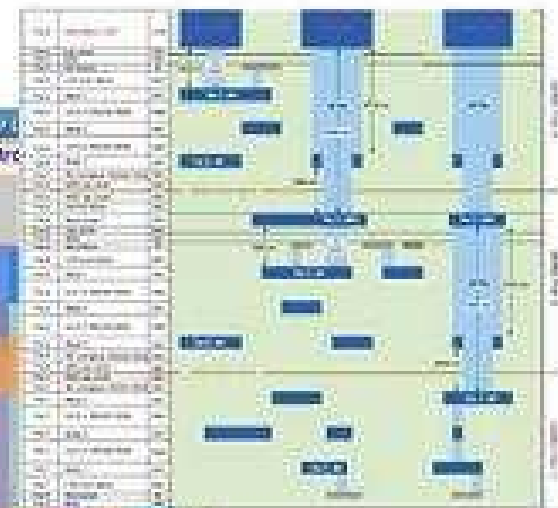
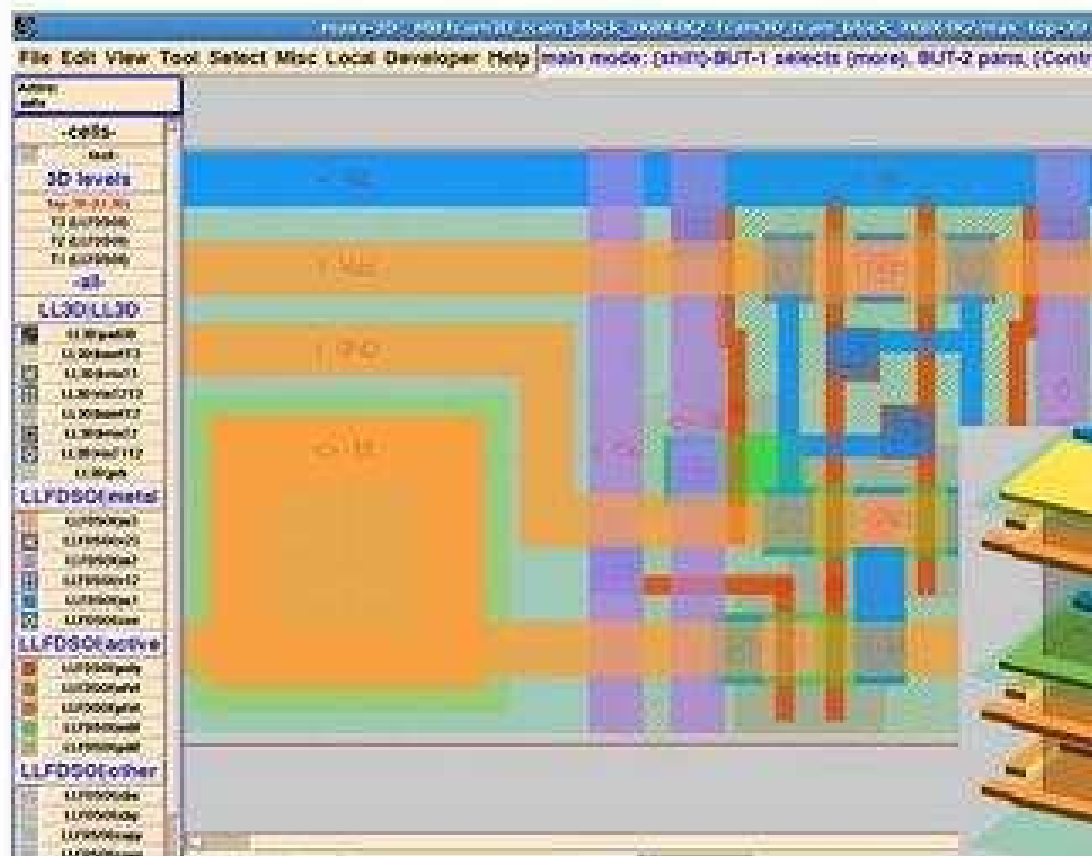
Virtuoso / Calibre LVS Interactive Menu

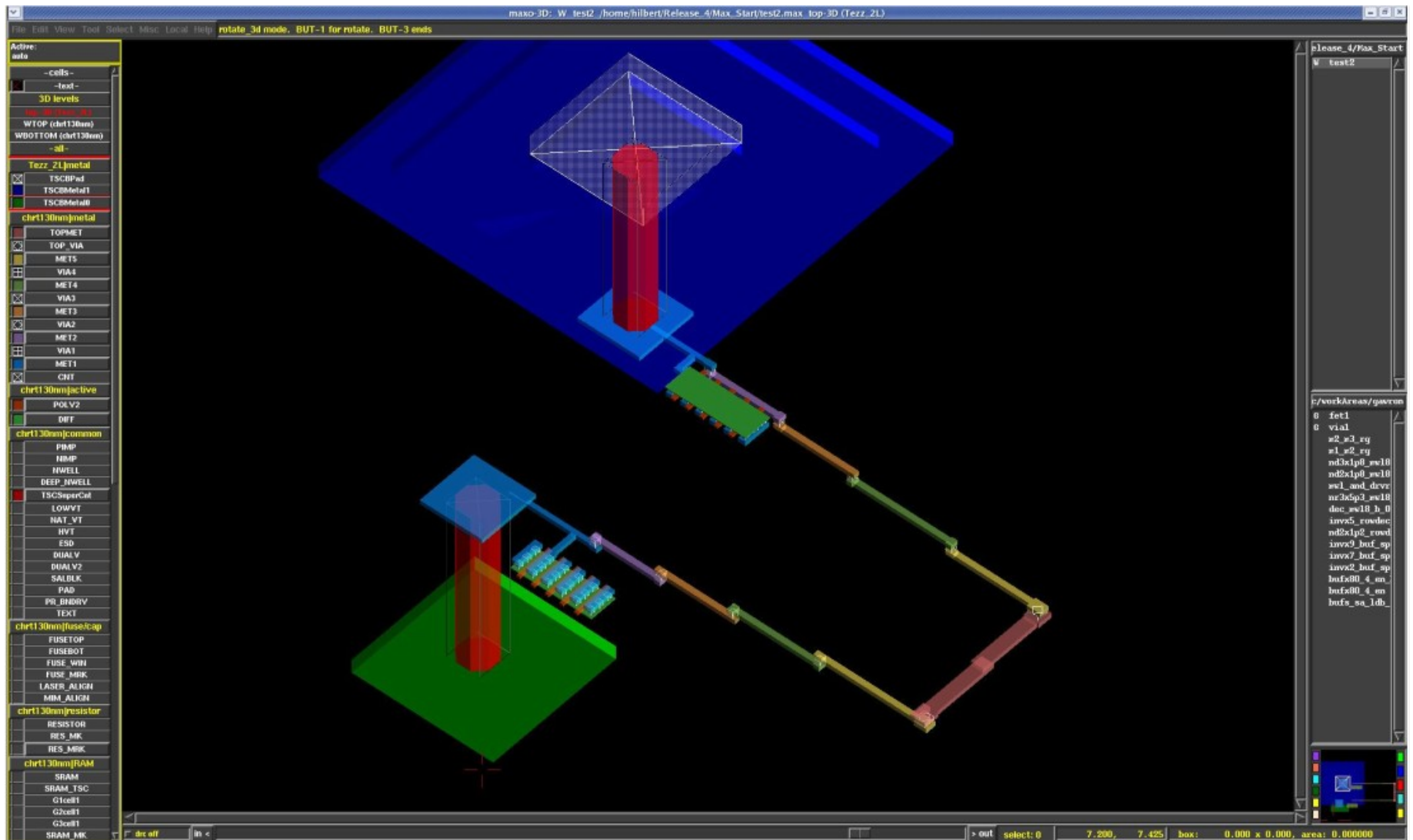
The image shows the Virtuoso Layout Suite L Reading interface for a test allcells_CORELIB_LP layout. The Calibre menu is open, showing options like Run DRC, Run DFM, Run LVS, Run PERC, Run PEX, Start RVE, Clear Highlights, and Setup. A red arrow points to the 'Run LVS' option. Below the main window, the 'Calibre Interactive - nmLVS' dialog is open, showing the LVS Rules File path as '\$MGC_LVS_FILES/cmos013lp.lvs.cal' and the LVS Run Directory as 'lvsRunDir'. A 'Customization Settings' dialog is also open, titled 'TEZZARON Switches For 2D or 3D LVS Options'. This dialog has a dropdown menu for '2D or 3D LVS ?' set to '2D_LVS'. Other options include 'MOS_NF_BY' set to 'SPLIT' and several 'IGNORE_*' checkboxes (IGNORE_BJT_M, IGNORE_CAP_M, IGNORE_DIO_M, IGNORE_RES_M). A red arrow points from the text 'Choosing 2D or 3D LVS' to the '2D_LVS' dropdown.

Choosing 2D or 3D LVS

Technology Files fully supported by Tezzaron

MicroMagic MAX-3D







MicroMagic 3D crosssection

CNRS - INPG - UJF

File Edit View Tool Select Misc Local Help rotate_3d mode. BUT-1 for rotate. BUT-3 ends

Active: auto

- cells-
- text-
- 3D levels
- WTOP (chr130nm)
- WBOTTOM (chr130nm)
- all-
- Tezz_21|metal
 - TSCBPad
 - TSCBMetal1
 - TSCBMetal0
- chr130nm|metal
 - TOPMET
 - TOP_VIA
 - MET5
 - VIA4
 - MET4
 - VIA3
 - MET3
 - VIA2
 - MET2
 - VIA1
 - MET1
 - CNT
- chr130nm|active
 - POLV2
 - DIFF
- chr130nm|common
 - PIMP
 - MBMP
 - NRWELL
 - DEEP_HWELL
 - TSCSmearCut
 - LOWVT
 - NAT_VT
 - HVT
 - ESD
 - DUALV
 - DUALV2
 - SALBLK
 - PAD
 - PR_BNDRY
 - TEXT
- chr130nm|fuse/cap
 - FUSETOP
 - FUSEROT
 - FUSE_WRN
 - FUSE_MRK
 - LASER_ALIGN
 - MIN_ALIGN
- chr130nm|resistor
 - RESISTOR
 - RES_MK
 - RES_MRK
- chr130nm|RAM
 - SRAM
 - SRAM_TSC
 - G1cell1
 - G2cell1
 - G3cell1
 - SRAM_MK

File: test2

```
6 fet1
6 via1
  n2_n3_rg
  n1_n2_rg
  nd2xlp0_nwl0
  nd2xlp0_nwl0
  nwl_and_drvr
  nr3xsp2_nwl0
  dec_nwl0_b_0
  invx5_rowdec
  nd2xlp2_rowd
  invx9_buf_sp
  invx7_buf_sp
  invx2_buf_sp
  bufx00_4_en_
  bufx00_4_en_
  bufx_sa_ldb_
```

File: /workAreas/gawron

in < > out Select: 0 -6.215, 0.400 box: 0.000 x 0.000, area: 0.000000

System Level Partitioning

Design exploration at system level

3D Floor-Planning
DBI, TSV, IO placement

Design exploration at the physical level
DBI, TSV, and IO placement & optimization

Automatic Place & Route

Cells and blocks place & route can be
done tier by tier

Extraction, Timing Analysis

To be done for each tier, then combined for
back-annotation to the 3D top level system

Physical verification
3D DRC, 3D LVS

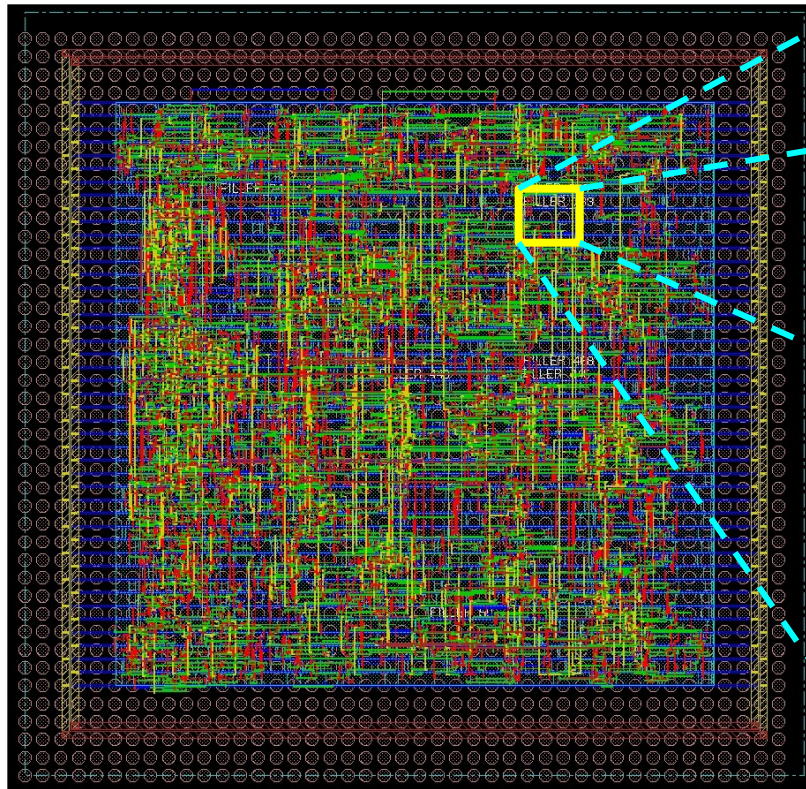
Dummies Filling

Final 3D DRC

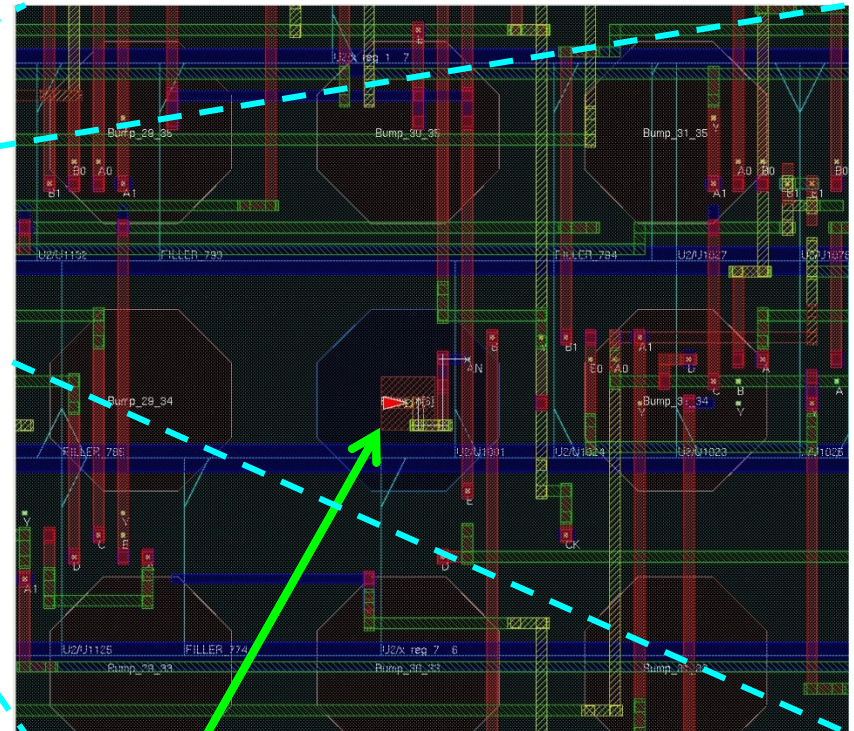
Similar to the full-custom design flow

Automatic P&R with Direct Bond Interface

- Encounter natively refuses to make the routing for pins on DBIs.
- Custom scripts solve the problem.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc ...



DBI array generation + P&R

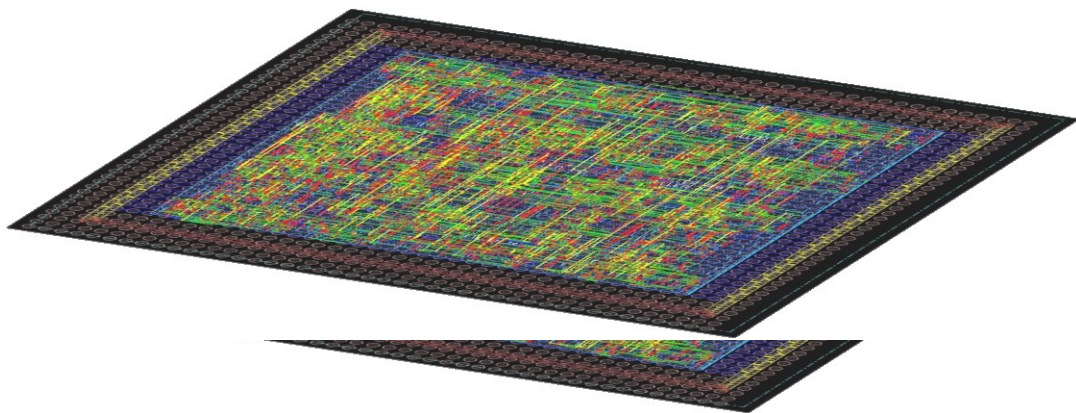


DBI completely routed down to the lower metal layers

Automatic P&R with Direct Bond Interface

Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

The place & route for both tiers is optimal for timing, buffer sizing and power performance.



This results in a **“correct-by-construction”** design.

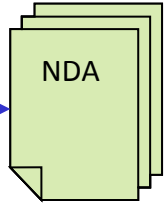
Access to the Design-Rules and the Design Platform



Customer Request



NDA Edition



Signed NDA reception



Foundry's Agreement

Yes



Design kit & Design Rules access

<http://cmp.imag.fr>

Request to access from CMP Web page or by E-mail to : **cmp@imag.fr**

The user receive by E-mail the NDA + ARM linary Addendum.

The user sign and return by post 2 original signed copies

CMP forward to Tezzaron the NDAs.

When Tezzaron is OK, they counter-sign and return one copy to CMP.

CMP return the copy to the user and give the access to the DRM and Design-Platform.



Users having access to the Design Platform

CPPM, Marseille, [France](#)
IPHC, Strasbourg, [France](#)
LAL, Orsay, [France](#)
LPNHE, Paris, [France](#)
IRFU, CEA Saclay, [France](#)
LAPP, Annecy-Le-Vieux, [France](#)
ENSTA PARISTECH, Paris, [France](#)
ISEA, Toulouse, [France](#)
ENSSAT – Université Rennes, [France](#)
CEA-DIF, [France](#)

University of Bergamo, [Italy](#)
University of Bologna, [Italy](#)
University of Perugia, [Italy](#)
INFN, Roma, [Italy](#)
INFN, Pavia, [Italy](#)
INFN, Pisa, [Italy](#)

University of Bonn, [Germany](#)
University of Barcelona, [Spain](#)
IMSE-CNM-CSIC, Sevilla, [Spain](#)
TuDelft, [The Netherlands](#)
University of Turku, [Finland](#)
Norwegian University, Trondheim, [Norway](#)

Tezzaron Semiconductor, [USA](#)

FermiLab, [USA](#)

North Carolina State University, [USA](#)

MOSIS, [USA](#)

CMC Microsystems, [Canada](#)

University of Sherbrooke, [Canada](#)

**+ Other centers supported by MOSIS and CMC
Not listed here.**

22 Users in Europe

Conclusion

- ❑ CMC-CMP-MOSIS collaborating to offer services for 3D-IC prototyping and low volume production.
- ❑ Continuous enhancements on the Design Platform offering updates, features, and design methodologies.
- ❑ First MPW run deadline : May 31st, 2011