The First Multiproject Wafer Run With Chartered/Tezzaron

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On behalf of the 3D Consortium

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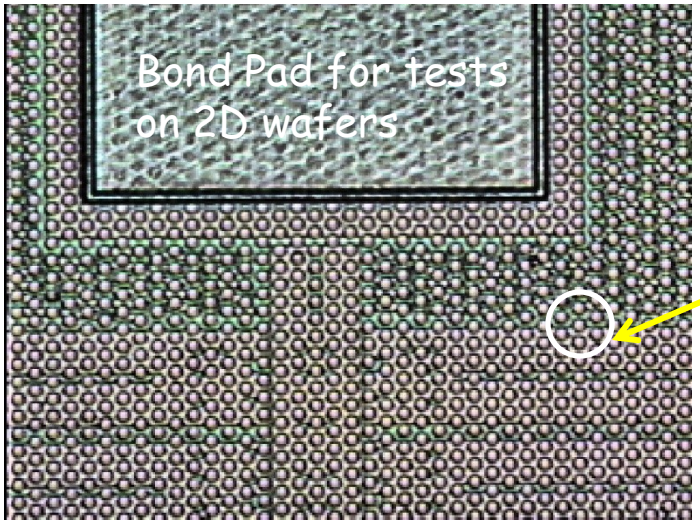
Outline

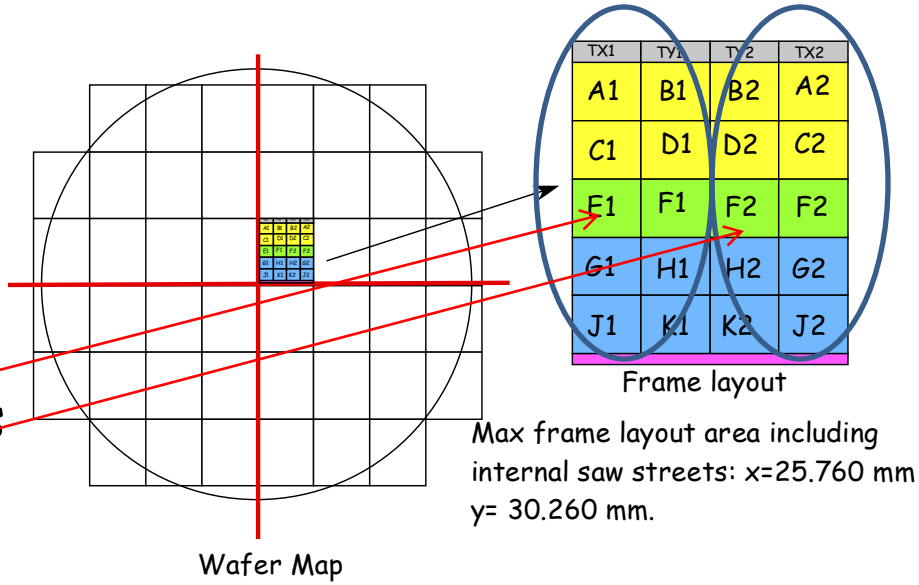
- Tezzaron/Chartered/Global Foundry MPW overview
- Brief summary of submission problems
- Overview of production problems
- Bonding sensors to 3D chips
- Test results from 2D wafers
- Next MPW run using commercial silicon brokers
- Future
- Summary

First HEP Multi-Project Run

- HEP consortium for 3D circuit design formed in late 2008
  - 17 member groups from 6 countries (France, Italy, Germany, Poland, Canada, USA)
- Tezzaron Process
  - Two tiers, 6 um TSVs
  - Single set of masks to reduce cost
  - Cu/Cu thermo compression face to face bonding between identical wafers. One wafer thinned to 12 um.
- More than 25 two tier designs (circuits and test devices)
  - ATLAS pixels
  - CMS strip ROIC for track trigger
  - X-ray imaging
  - B-factory and Linear Collider pixels
  - Test circuits
- Frame divided into 24 subreticules
  - 12 for top tier
  - 12 for bottom tier
  - ***Frame must be placed symmetrically on wafer for proper bonding!!***



Copper hex bond interface pattern at 4 um pitch



Max frame layout area including internal saw streets: x=25.760 mm y= 30.260 mm.

Some Design Problems

- All designers did not use the same design kit provided by Tezzaron leading to
  - Stream layer map inconsistencies – big problem
  - Misuse of top metal
  - Incorrect MiM cap rules

  Lesson - Use the same design kit
- Some design rules were interpreted incorrectly leading to various TSV design problems.

  Lesson-Clarify 3D design rules
  - Dishing of wafers where a third layer was to be added
  - Metal 1 over lap on TSV which could cause contamination problems
- Initially some designs did not use a fill program resulting in fill problems later on

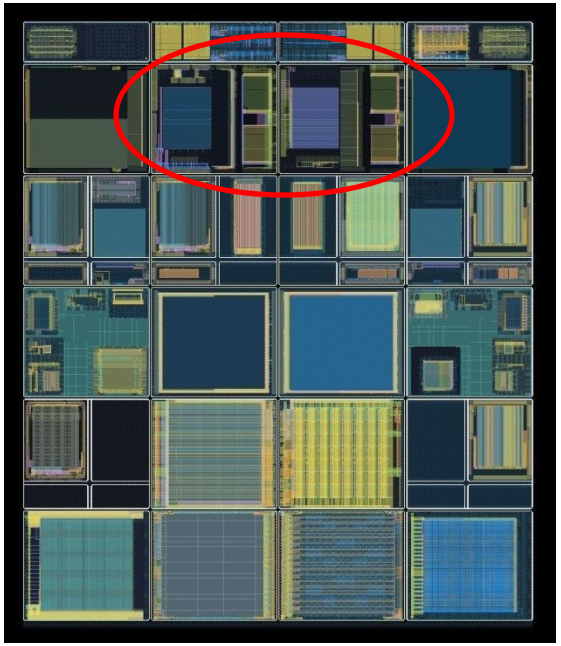
  Lesson – use automated fill program
- Custom SRAM cells raised numerous questions.

  Lesson – custom SRAM cells should only be used after close discussion with Tezzaron and Chartered since some cells may be rejected by Chartered even if they pass the design rules
- Bugs found in MicroMagic software used assemble the frame for 3D submissions.
  - In the course of receiving designs, two separate software problems were found due to the nature of our designs
    - A rounding error caused off grid placement of bond interface pads only in some designs leading to unnecessary errors.
    - An ARM cell was used that had off grid vertices that created unnecessary errors
  - The problems have been fixed

    Lesson- You can't avoid Murphy's Law

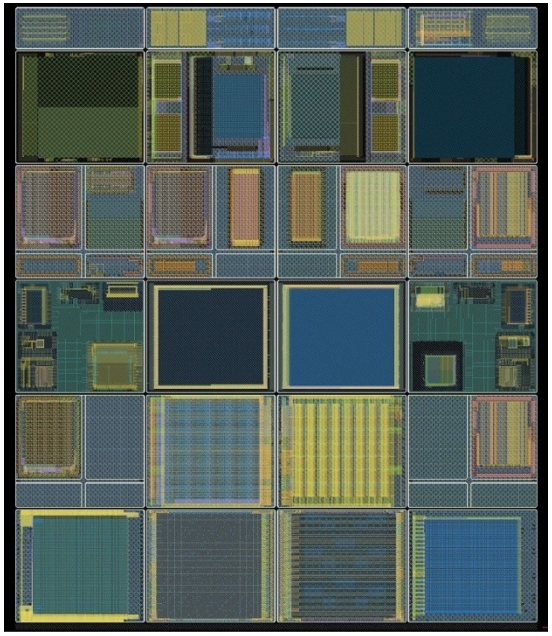
Some Submission Problems

- Chartered provided initial size of design area in the frame. After all designs were completed and used all the design space, Chartered requested additional street space. It took three submission revisions before Chartered would finally accept the frame.
- Some designs had labels outside the design area causing Chartered to reject submission and much rework.
- After designs received by mask house, individual blocks were incorrectly mirrored by the mask house which fortunately was caught by Tezzaron before the masks were made.
- Chartered considers every design is for high volume and thus they would not accept some error waivers we thought were acceptable.
- Some designs were submitted with incorrect mirroring



MPW run frame

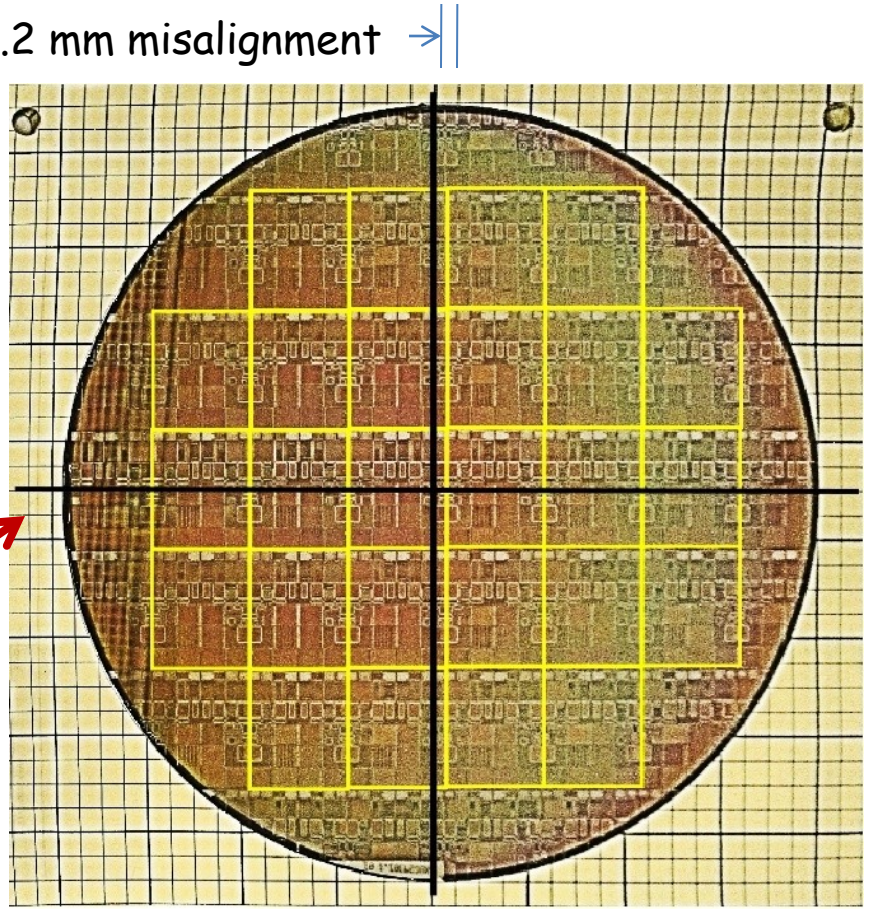
One layout Incorrectly mirrored



All layouts correctly mirrored

Fabrication Issues

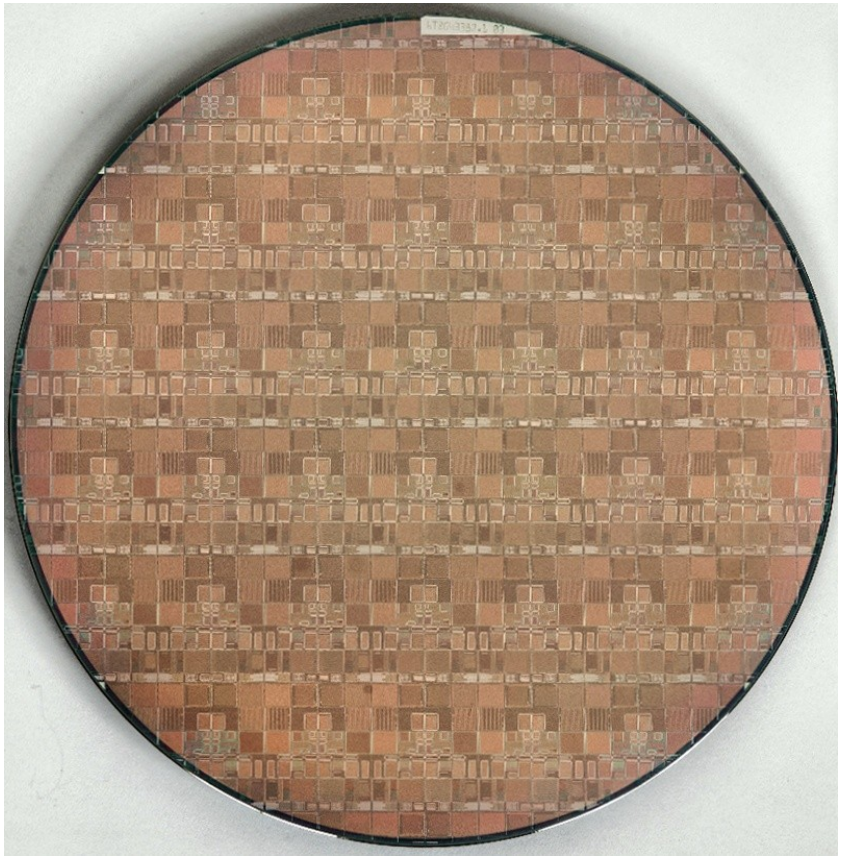
- 3D wafer fabrication done in Chartered prototype line
- Chartered was bought by Global Foundries which slowed our wafer fabrication process
  - Personnel knowledgeable in 3D fab issues were moved
  - Some equipment use for 3D fab moved to higher profit production line
- Global/Chartered did not properly place frames on wafers for 4 different lots of wafers being processed for Tezzaron. The wafers could not be aligned properly for 3D bonding.
  - Never happened before
- These wafers however have been used for some 2D IC testing as discussed later.



Frames are not placed symmetrically about the wafer center lines

Fabrication Issues

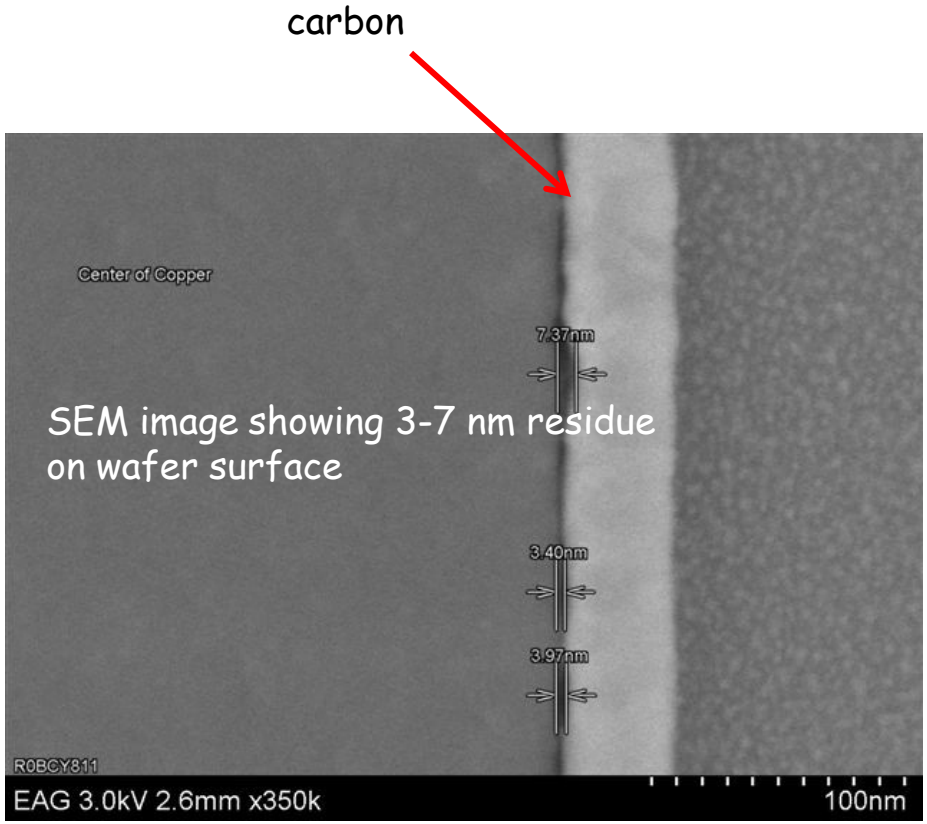
- A new lot of 31 wafers was fabricated at no cost to Tezzaron or us except for time (3 months)
- Due to delays in fabrication, the 3D wafer bonding facilities were not available when the second batch of wafers were ready.
- New wafers had 400 nm of protective nitride removed from surface and then were sent to EVG in Tempe for bonding at about 240 lb/in2 and 400 degrees C.



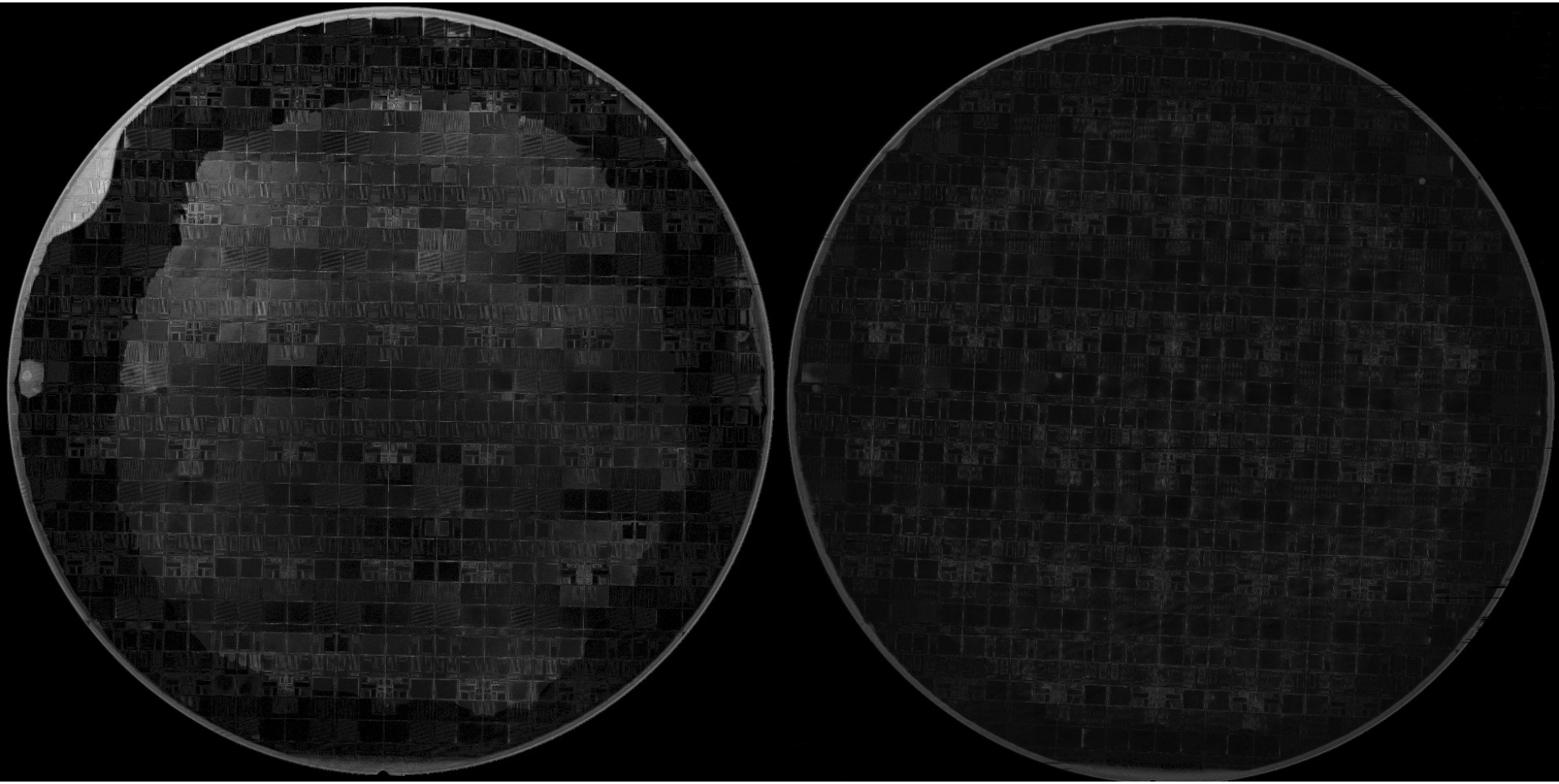
Newly fabricated wafer with proper frame placement on the wafer

Fabrication Issues

- After the nitride removal, three wafer pairs were bonded and all three had large unbonded areas in the center of the wafer pairs.
- There was not sufficient bond strength to continue with grinding one of the bonded wafers to 12 um because the wafers would break.
- The problem was thought to be either a small amount of nitride which was not removed or problems with the bonding machine.
- The unbonded wafers were sent to another EVG facility while the bonded pairs were sent to Ziptronix for analysis.
- One wafer pair was broken to expose the center and using a SEM a 3-7 nm thick layer was found on the wafer surface.
- At first the layer was thought to be nitride but an Auger electron microscope chemical analysis showed that the layer was carbon.
- All the unbonded wafers were then returned to Ziptronix where the carbon layer has been removed.
- After removing the residue the unbonded wafers were sent back to EVG in Tempe for bonding.
- By May 17 two new wafers pairs were bonded by EVG with better bonding results. Thinning is the next step, followed by back metal deposition



Acoustic Microscope Image of 3D bonded Wafers

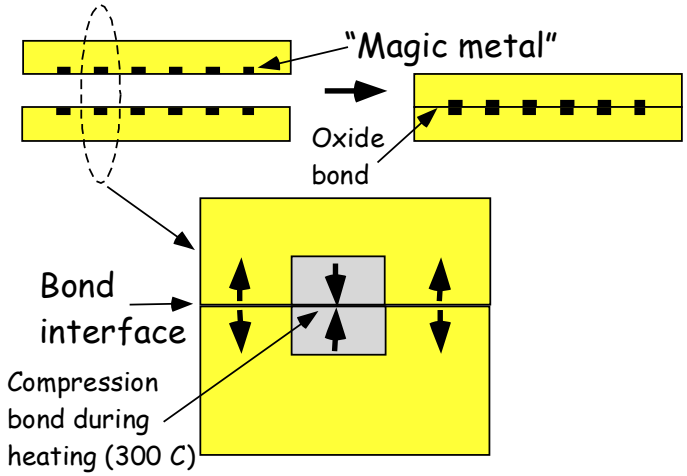


Poorly bonded wafer pair

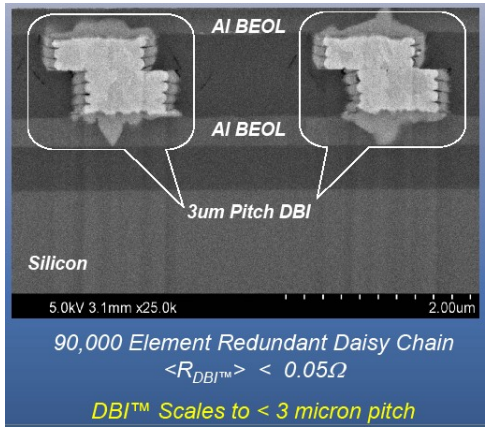
Good bonded wafer pair

Wafer Recovery

- The normal DBI (Direct Bond Interconnect) at Ziptronix uses a low temperature oxide bond followed by a heating cycle that forms a compression bond between micron sized nickel ("magic metal") pads.
- Fermilab has used this process before to bond sensors to a ROIC wafer.
- Our two poorly bonded 3D wafer pairs with large voids were useless to us
- Ziptronix has been evaluating a copper DBI process instead of nickel and will attempt to recover some parts for us using this process.
- A "razor blade test" was performed at Ziptronix and it was found that the wafer pairs separated easily confirming non-suitability for thinning.
- There was a small amount of copper delamination that occurred.
- They will resurface our wafers and attempt to bond our wafers using an oxide bond followed by a copper thermo-compression bond.
- There is no guarantee and no date has been promised.



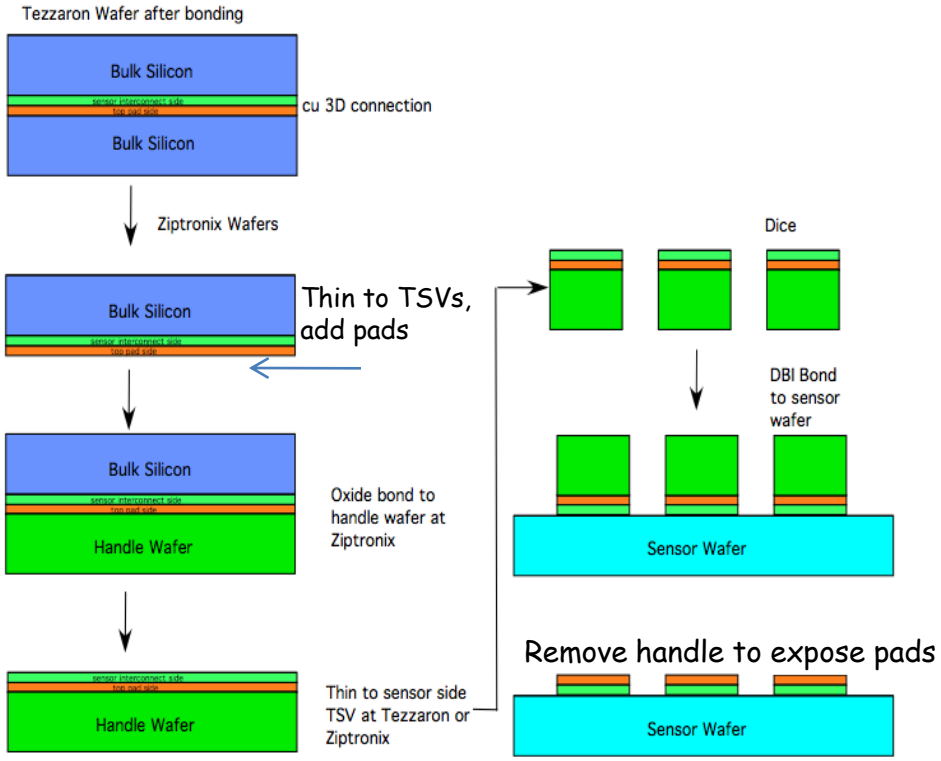
Direct Bond Interconnect



3 um DBI bonds using nickel

Fermilab's Efforts to Bond Sensors to Tezzaron 3D Chips

- Fermilab designed 3 chips to be bonded to Brookhaven sensors at Ziptronix
  - VIP2a - linear collider pixel chip based on MIT LL chip
  - VICTR – track trigger chip for CMS
  - VIPIC – X-ray imaging chip for light sources
- Other groups were also interested in using Ziptonix DBI process
- Initially we did not know enough about the DBI process but quickly learned that the requirements were more involved and there was a significant risk.
- Decided to use Fermilab chips as a test case and save high cost of extra masks .
- The most aggressive bonding approach is shown on the right.

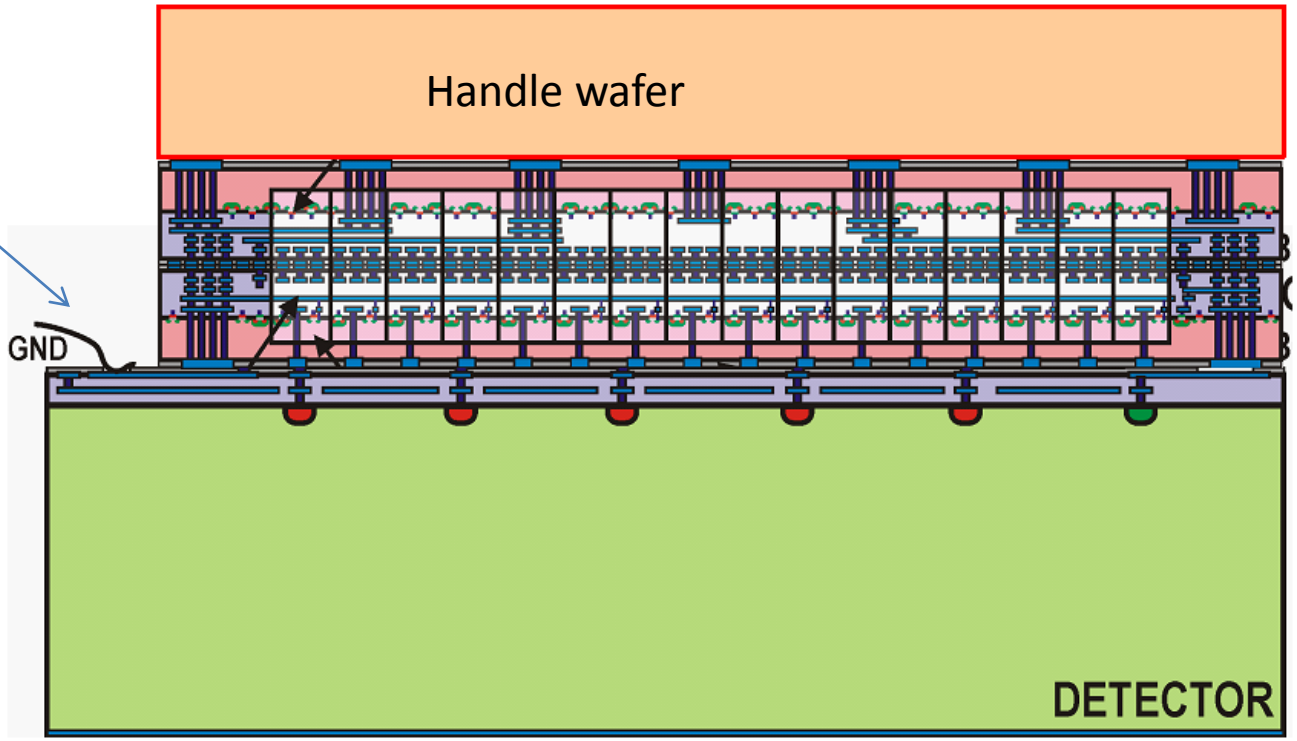


Process used to bond 3D ICs to sensor wafer

(More aggressive approach)

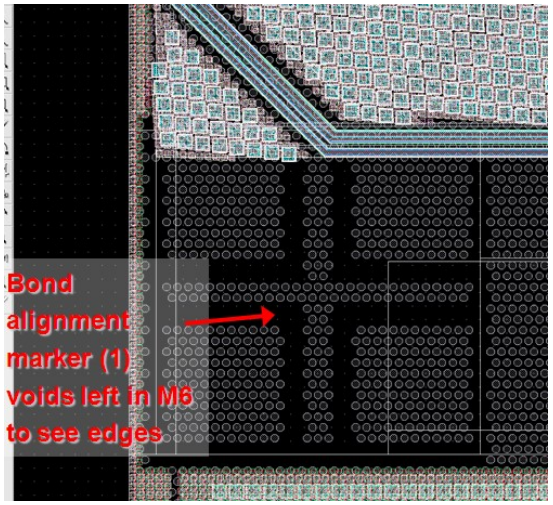
Less Aggressive Approach

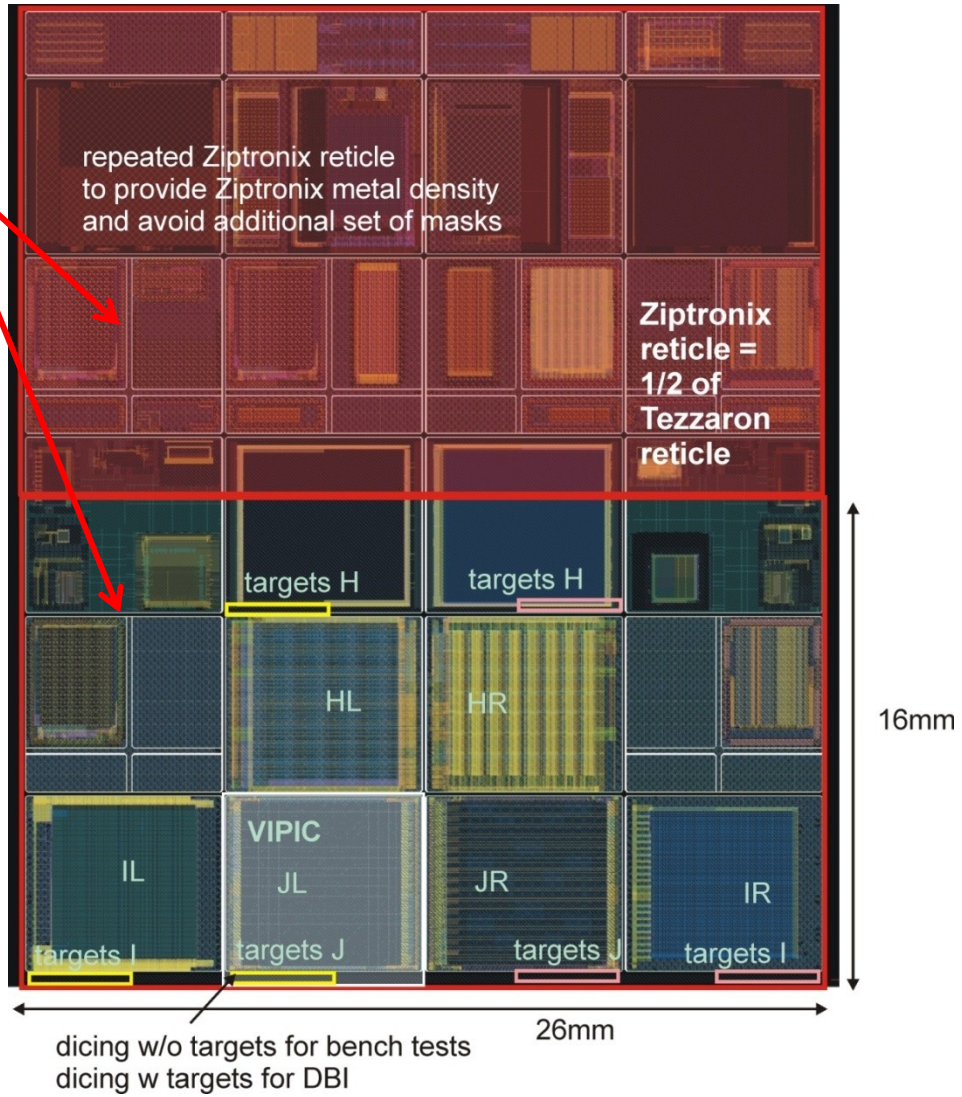
Handle wafer is not removed and connections are made to dual set of pads placed on the sensor wafer



Some ROIC Wafer Issues

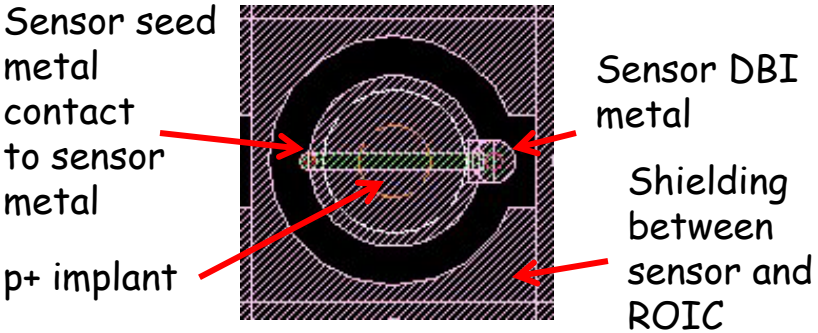
- Frame size for adding Ziptronix DBI bonding pads was smaller than Chartered frame – repeat bond pad mask twice on 3D frame to avoid extra mask cost.
- Space was limited for different alignment targets needed for deposition of seed/DBI post metal and DBI bonding.
- IR transparent bond alignment targets are needed on each ROIC and sensor (conflicts with M6 density requirement)

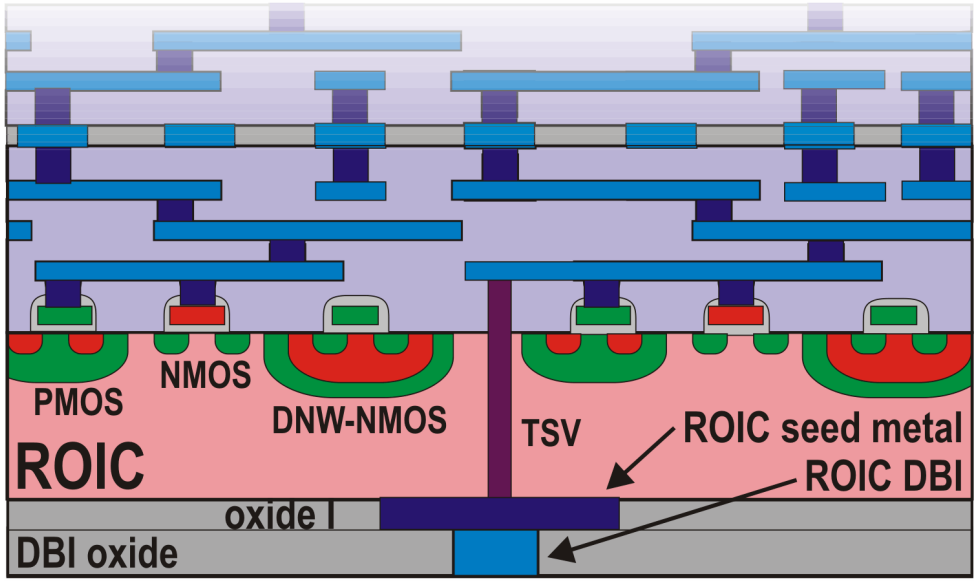


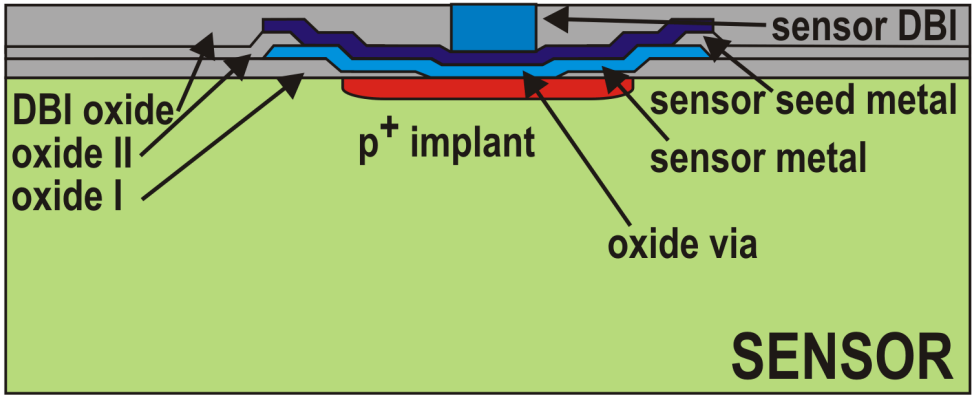


Some Sensor Issues

- Brookhaven sensor process does not have CMP resulting in uneven surface which is OK for bump bonding but not DBI.
- Thickness of layers for fabrication of sensors had to be carefully chosen to obtain desired surface topology
- Final sensor layout had to have sensor DBI metal offset from p+ implant as shown below to avoid planarity problems with pads.



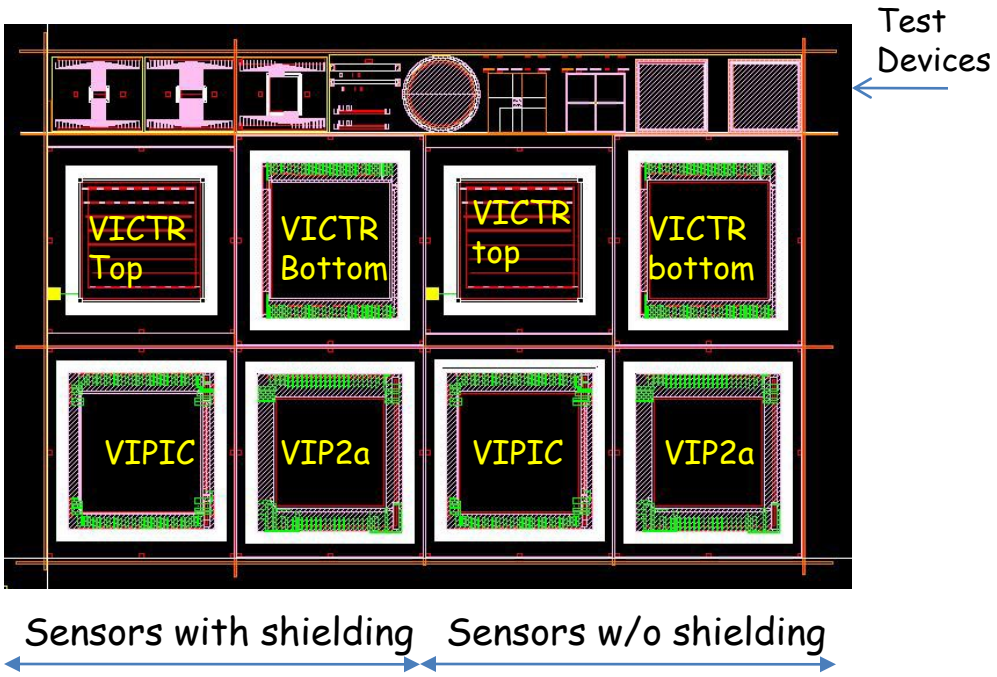




BNL completes oxide 1, sensor metal, oxide 2.
Ziptronix completes sensor seed metal and DBI.

Sensor Frame

- Sensors have been made on four inch wafers at Brookhaven
  - Top and bottom sensors for VICTR
  - Sensors for VIPIC
  - Sensors for VIP2a
  - Sensors and test structures for other applications
- Sensors with and without shielding between sensors and 3D ROICs were fabricated to study coupling.
- 3D ROICs are bonded to sensor wafer.
  - Some parts are to be diced with pad connections on the sensors
  - If above is successful, on another wafer 3D ROIC will be thinned and connections made to back side of ROICs.

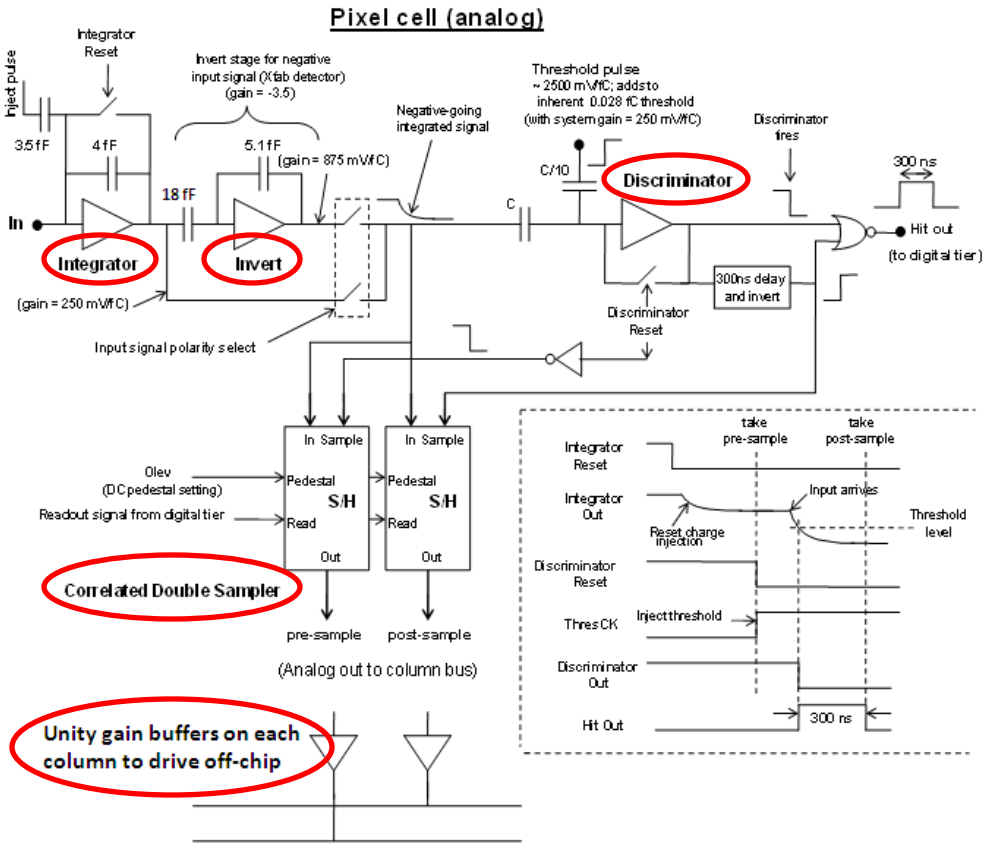


Tests on Chartered Parts

- Unfortunately 3D circuits and test structures are still not available.
- Fortunately some circuits were fabricated in 2D for testing and some 3D wafers had pads added so testing could be done of individual tiers (our misaligned 2D wafers).
- All circuits tested by various collaborators in 2D have been found to performed as expected.

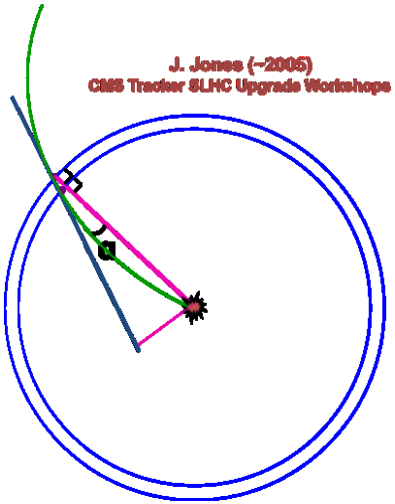
Tests on Fermilab Circuits

- VIP2a design for ILC pixels is separated into separate digital and analog tiers.
- Circuits on analog tier could be tested independently.
- Functionality of each block of analog circuit was verified.
- Good linearity and range
- Process findings
  - NMOS thresholds ~ 100 mv lower than simulations
  - NMOS gm a few % lower than simulations
  - PMOS gm 10-15% lower than simulations
  - MiM caps ~4% lower than expected
  - Noise @ 75 ns time constant is equal to 8e + 0.5e/fF* Cin

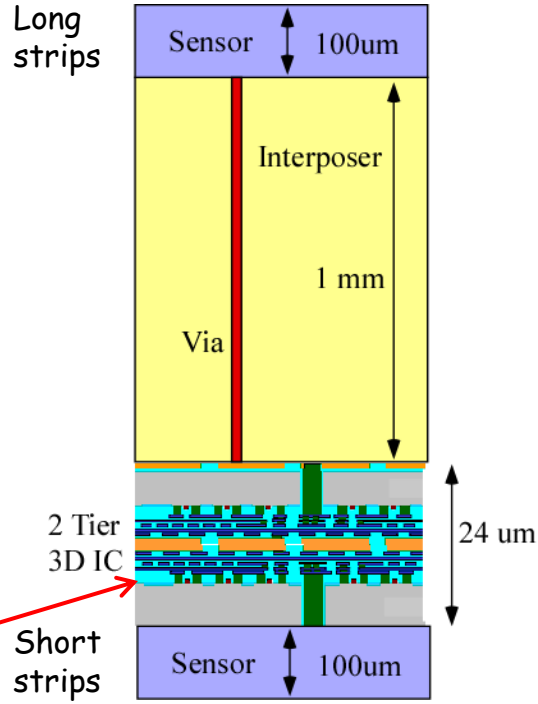


Tests on VIPIC for CMS Track Trigger

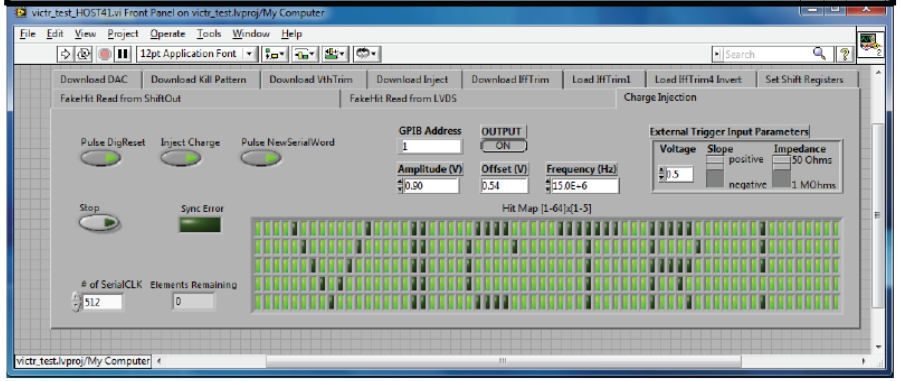
- Idea for track trigger is to discriminate on tracks with high pt
- Compare hits locally on two closely spaced strip sensors.
- Very aggressive use of 3D technologies.
- One tier processes signals from top tier
- Other tier processes hits from bottom tier, accepts hit information from top tier, performs comparison and transmits data off detector.
- Functionality of short strip tier has been proven on 2D chip
  - Downloading of registers
  - Control of front end bias
  - Front end response
  - Backend readout
  - DAQ system
  - Strip Vth sigma = 197e
  - Noise mean= 75e, sigma= 13e



Two rings of strip sensors shown with bent track

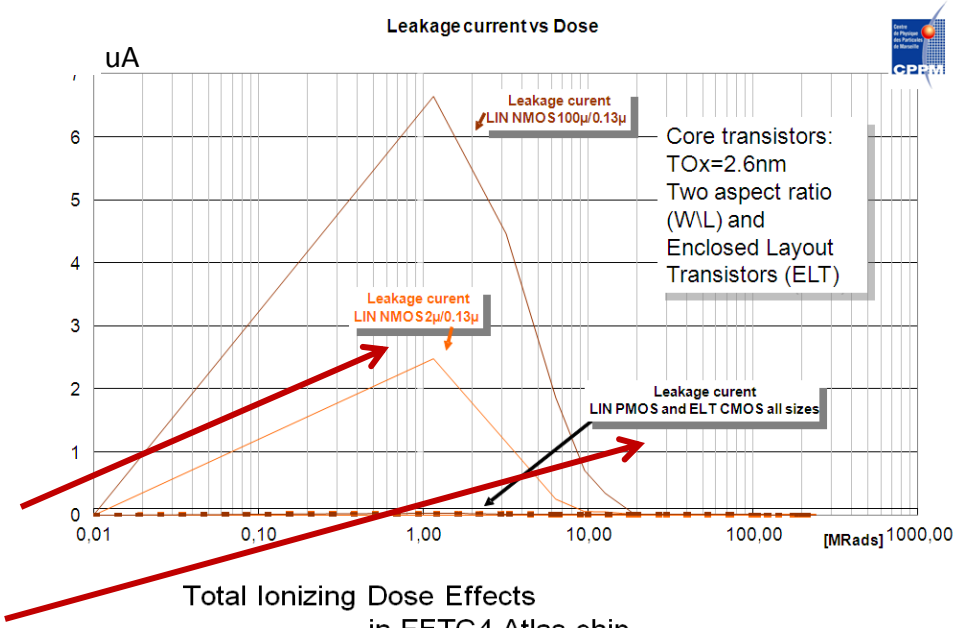


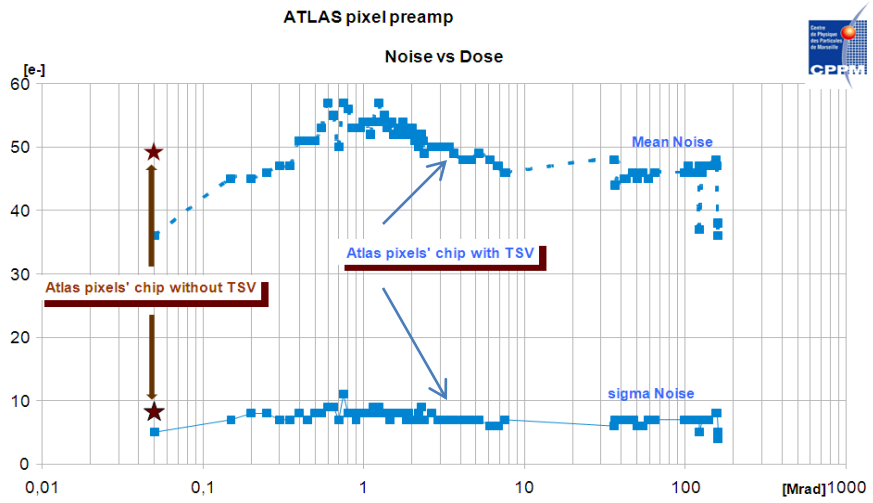
Hit Map from Charge Injection (consistent with kill map)



Early Chartered Radiation Test Results by CPPM

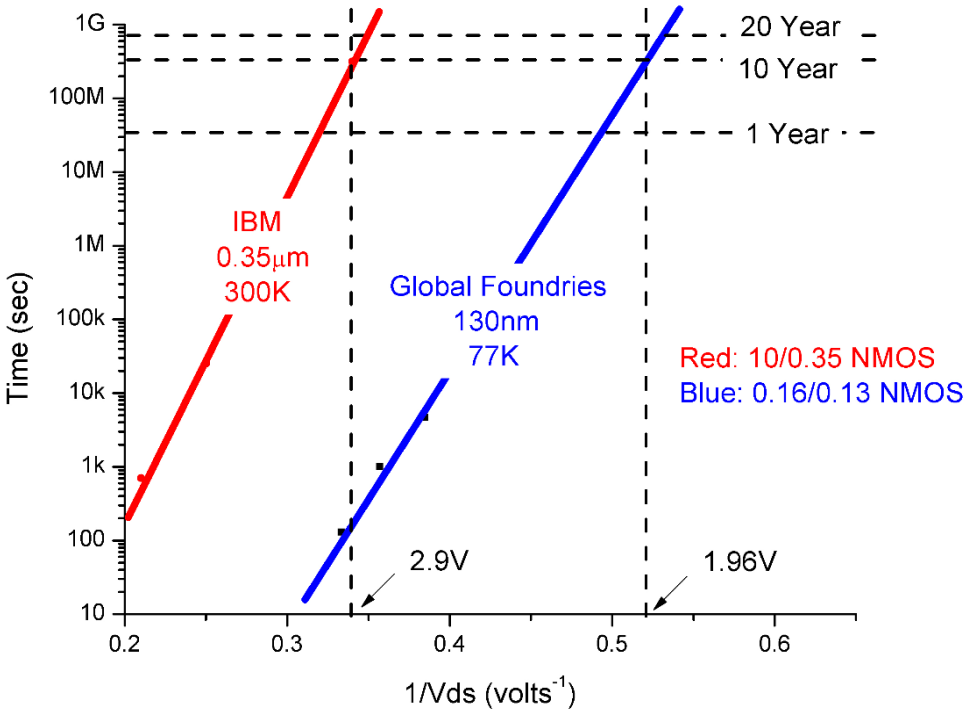
- In 2009, rad tests done on the ATLAS upgrade pixel chip were done in a proton beam
  - No design optimization done for the Chartered process
  - Circuit fully operational up to 160 Mrads
  - Suspect a dose induced problem in digital section ~ 160 Mrads (not confirmed)
- Testing of core linear and ELT transistors and ATLAS pixel circuits on 2D parts with TSVs in CERN's X-ray test lab at 3.2 Mrads/hour (Preliminary results)
- 2D test results (compare transistor results to CERN 130 nm results)
  - NMOS leakage current shows peak around 1 Mrad – similar to other CERN results
    - Linear NMOS leakage may be a concern
  - Linear PMOS and ELT NMOS and PMOS are good
  - NMOS and PMOS Vt shifts are similar to CERN tests on other 130 nm processes, however Chartered NMOS Vt shift is positive instead of negative.
  - Tests on ATLAS pixel preamp show only a small change in noise up to 160 Mrads
- Radiation tests thus far suggest that the Chartered 130 nm process is similar to other 130 nm processes tested at CERN
- Rad tests thus far validate move to commercial CMOS for high radiation tolerance.





Preliminary Cryo Transistor Tests

- Fermilab is involved with developing electronics which need to operate at cryogenic temperatures.
- The main problem of CMOS devices operating at cryogenic temperatures is that they have reliability issues du to hot carrier effects (HCE).
- One way to measure reliability is to bias devices at maximum substrate current and measure time at which a 10% change is gm takes place for different Vds.
- A straight line projection provides maximum Vds for 10 year lifetime under maximum stress.
- Processes thus far reported in the literature all required a Vds derating from specification to achieve 10 year life time.
- Preliminary results for the Global/Chartered low power process indicate that no derating whatsoever is necessary at cryogenic temperatures showing that the Chartered process could be very robust at low temperatures.



Note:
The IBM process is a 3.3 volt process
The Global process is a 1.5 volt process

3D Moves to Commercial Silicon Brokers

ANNOUNCEMENT

CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

* CMP will provide and maintain the design kit
* CMC and CMP will accept designs and send them to MOSIS for interfacing with Tezzaron
* Tezzaron will handle NDAs and submission of designs to Global/Chartered
* Parts will be distributed by MOSIS after 3D assembly

Design Kit Features

- A comprehensive design kit has been assembled by CMP.
- Tools included for
  - Cadence
    - Cadence data base
    - Open access
    - Encounter for 3D
  - Calibre
  - Hercules
  - Mentor (Eldo, HSPICE)
  - Micromagic
  - ARM libraries (physicals?)
- Numerous programs and libraries provided by HEP Consortium
- Monte Carlo models
- Automatic fill program
- User set up files
- Two packages are available
  - Design kit with ARM libraries
  - Design kit without ARM libraries
- The next talk by Kholdoun Torki will provide more detailed information

Summary of 3D Design Kit Packages

- **Package 1 : TDK (Tezzaron Design-kit) without the ARM libraries :**

  TDP_2011q2v2 directory contains following directories :

  chrt13lprf_DK009_Rev_1D (full-custom PDK : all techfiles are here)
  - assura (FILLDRC, LVS, QRC)
  - calibre (FILLDRC, 3DLVS, DRC, 3DDR, calibreSwitchDef)
  - prep3DLVS
  - hercules (DRC, LVS, STAR_RCXT)
  - eldo (BSIM4 model for Devices)
  - hspice (BSIM4 model for Devices)
  - spectre (BSIM4 model for Devices)
  - cds_cdb (Cadence cdb library)
  - cds_oa (Cadence oa library)
  - skill (skill code bindkey, color,....)
  - strmMaptables_ARM (for ARM)
  - strmMaptables_Encounter (for Encounter)

  MMI_PDK_I (MicroMagic PDK part I)
  MMI_PDK_II (MicroMagic PDK part II)

  UTILITIES_2011q2v1 (contributions from the HEP users)

  install_fullcustom (a variation of the original "install" without the definition of the ARM libs)

- **Package 2 : TDP (Tezzaron Design-Platform) with all products :**

  TDP_2011q2v2 directory contains following directories :

  Package 1

  PLUS

  - CSM013LP_LVT_SC_2007q2v1 (ARM core lib LP/LVT)
  - CSM013LP_SC_2005q1v1 (ARM core lib LP)
  - CSM013_IO_GP_IL_2005q3v2 (ARM IO lib in-line pads)
  - CSM013_IO_GP_ST_2005q2v1 (ARM IO lib staggered pads)

  Note: physicals are included in libraries

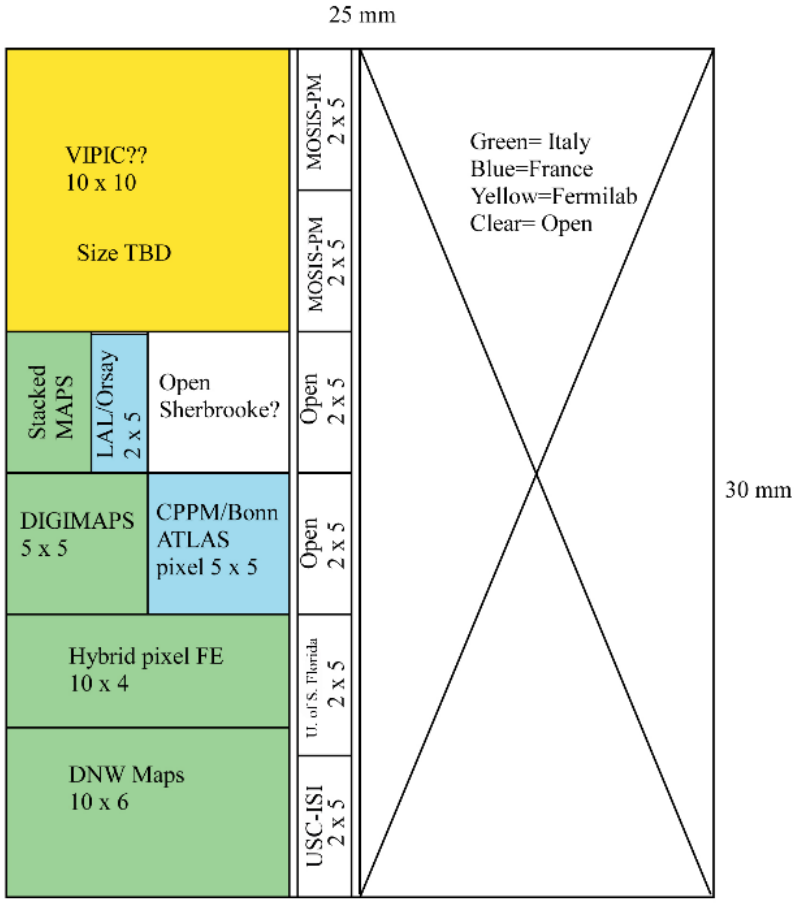
  - CSM013_MEM_COMPILERS (ARM memory compilers)

  tutorials (presently only the Encounter tutorial including Bond Interface place&route)

  install (User's setup files)

Future

- Tezzaron working to improve process flow by moving all steps except TSVs to NC
- Tezzaron moving toward using wafers from other foundries and inserting TSVs at SVTC
- Tezzaron TSV process has been installed at Honeywell on SOI process
- Tezzaron and IBM are having discussions about running 65 nm with TSVs at IBM
- MOSIS is hoping to have two 3D runs this year. One for HEP consortium and one for other customers.
  - Enough non-HEP customers have express interest for a separate MPW run.
  - Tentative HEP frame layout for next run shown at the right



Chip size in mm	Sold area	Chip cost for 350K run	Chip cost for 400K run	Chip cost for 450K run	Chip cost for 500K run
100	300	116	132.6	149.1	165.7
60	300	70	80	90	100
40	300	46.6	53.3	59.9	66.6
25	300	29.1	33.2	37.4	41.6
15	300	17.5	20	22.5	25
10	300	11.6	13.2	14.9	16.6

Summary

- Progress on Tezzaron 3D run has been frustratingly slow. However, it is noted our other 3D chips have experienced similar fabrication delays. (e.g. MIT LL 1-2 years, Zcube/T-micro 1.5+ years, Tezzaron 1.2+ years. Good news is that all tested 2D Chartered circuits are working, suggesting that 3D bonded chips should work. The HEP effort has led to commercial silicon brokers providing 3D service in the future. A much more comprehensive and better design kit is now available which should reduce or eliminate most of the submission problems that were encountered. We are looking forward to improvements being made by Tezzaron to centralize facilities and improve fabrication turn around time.