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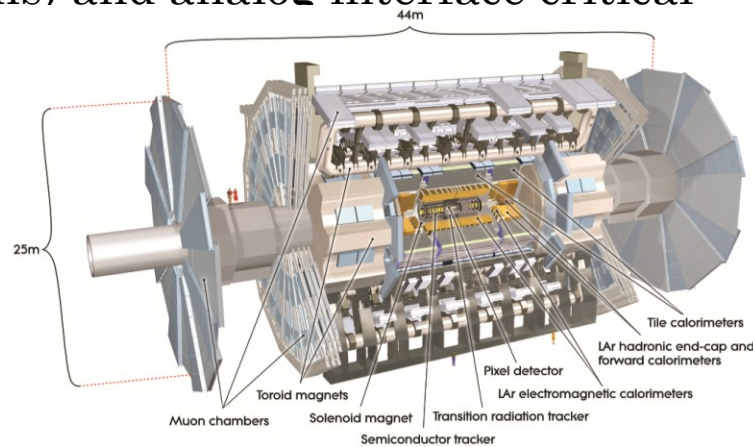
TDC ARCHITECTURES IN ASIC'S

Jorgen Christiansen

CERN/PH-ESE

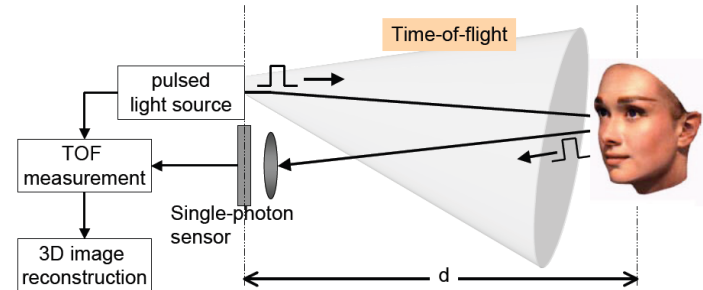
TIME TO DIGITAL CONVERTERS IN HEP

- Large HEP systems with many (100k or more) channels
 - Time resolution, precision and stability required across whole system.
 - Time correlations to be made across “all” channels
 - Use and distribution of common time reference to all channels
 - Large dynamic range
 - Single shot measurements (with some exceptions, e.g. RICH)
 - Short dead time
 - No reason to aim at much better TDC time resolution than detector and system can effectively use (TDC contribution to total system time resolution should though not be significant)
 - Detector (e.g. MCP, SIPM, MGRP, etc. for high resolution applications) and analog interface critical

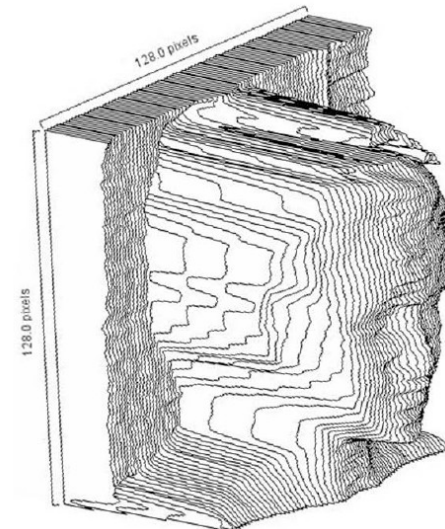


OTHER TDC APPLICATIONS

- Laser ranging,
- PLL's,
- 3D imaging
- Etc.
- General differences to HEP systems
 - Small local systems
 - Few channels
 - Limited dynamic range
 - Averaging can often be used to improve effective RMS resolution



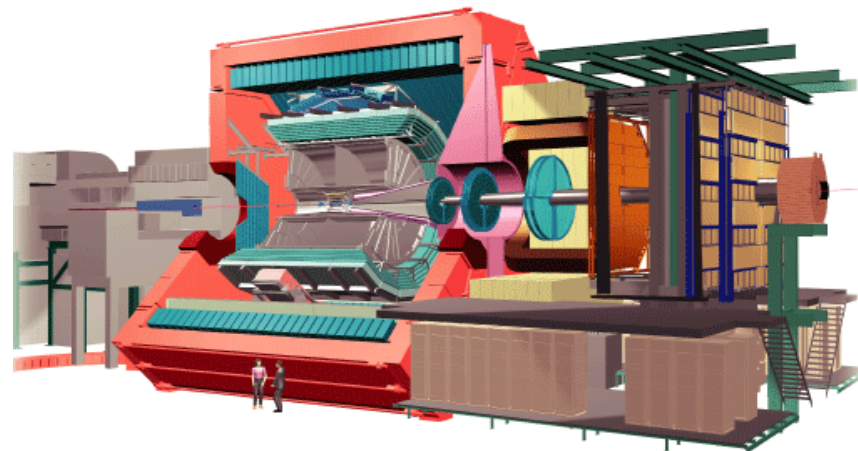
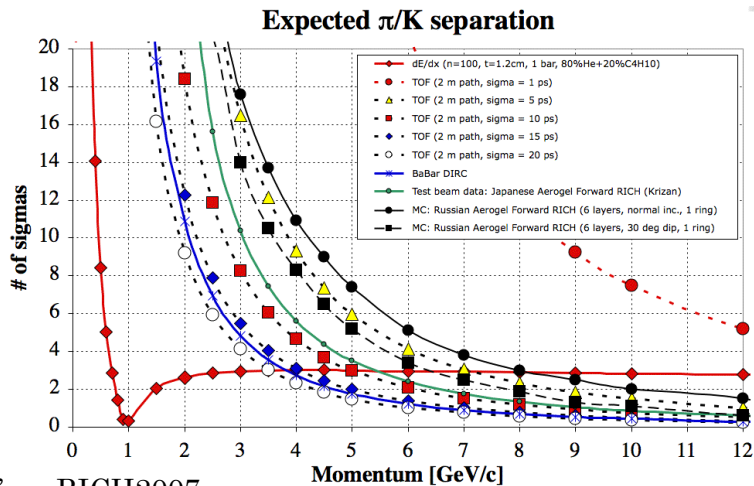
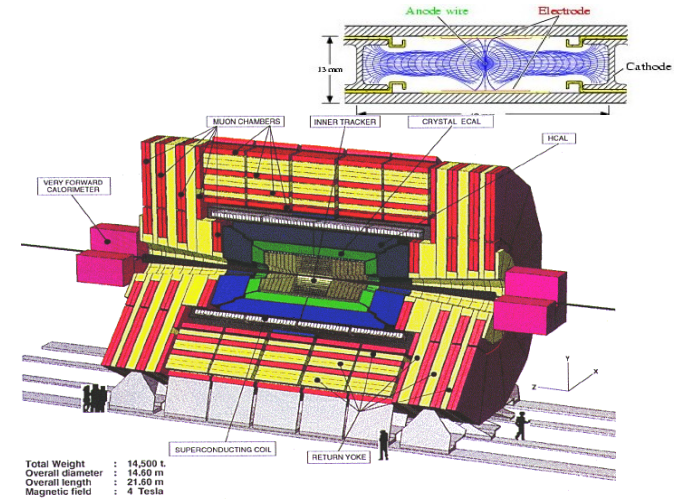
$$d = (c/2) \text{ TOF}$$



E. Charbon, DELFT

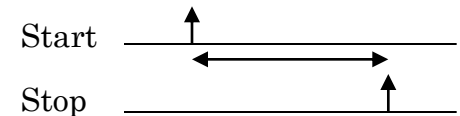
TDC APPLICATIONS IN HEP

- Drift time in gas based tracking detectors
 - Low resolution: $\sim 1\text{ns}$
 - Examples: CMS and ATLAS muon detectors
- TOF, RICH TOP
 - **High resolution: 10ps – 100ps**
 - Example: ALICE TOF
- Background reduction
- Signal amplitude measurement: TOT



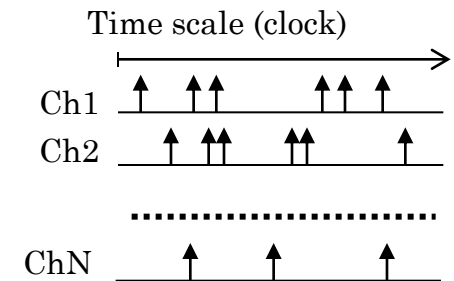
○ Start – stop measurement

- Measurement of time interval between two local events:
 Start signal – Stop signal
- Used to measure relatively short time intervals with high precision
- For small systems (1 channel)
- Like a stop watch for a local event



○ Time tagging

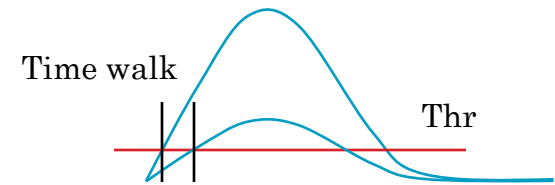
- Measure time of occurrence of events in relation to a given time reference
 Time reference (Clock)
 Events to be measured (Hit)
- Used to measure relative occurrence of many events on many channels on a defined time scale
- Such a time scale will have limited range but can be circular (e.g. LHC machine orbit time)
- For large scale HEP systems
- Like a normal watch with a common 24h scale



INTERFACE TO FRONT-END AND TIME WALK COMPENSATION SCHEMES

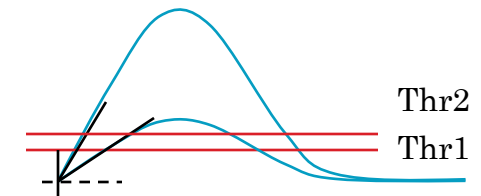
○ Basic discriminator

- Significant time walk (depending on signal slew rate)



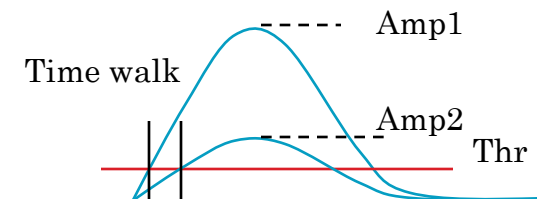
○ Double threshold

- Interpolate to “0” volt amplitude
- Needs two discriminators and two TDC channels, Limited efficiency reported in practice.



○ TDC plus pulse amplitude (peak or charge) measurement with ADC

- ADC measurement expensive and slow (may be needed anyway)

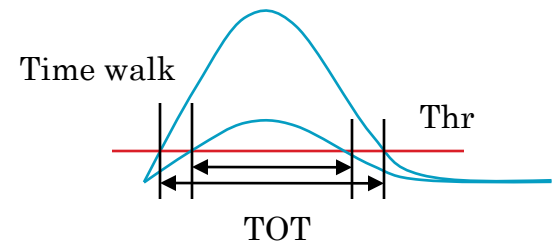
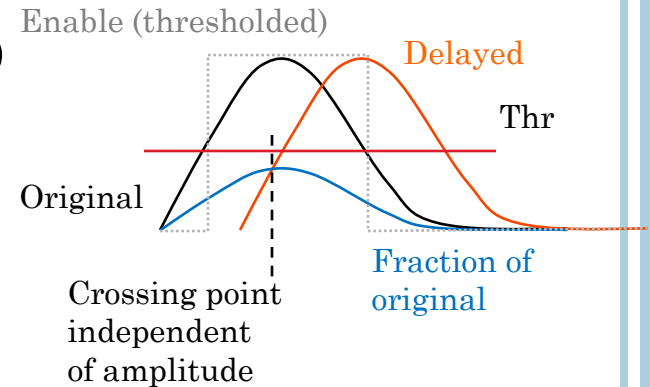


- Constant Fraction Discriminator: CFD

- Compensate directly in discriminator
- Works very well for fixed pulse shape with varying amplitude.
 - Needs delay: Made as distributed RC within ASIC's (but also works as filter)
- If signal shape not constant then ?.

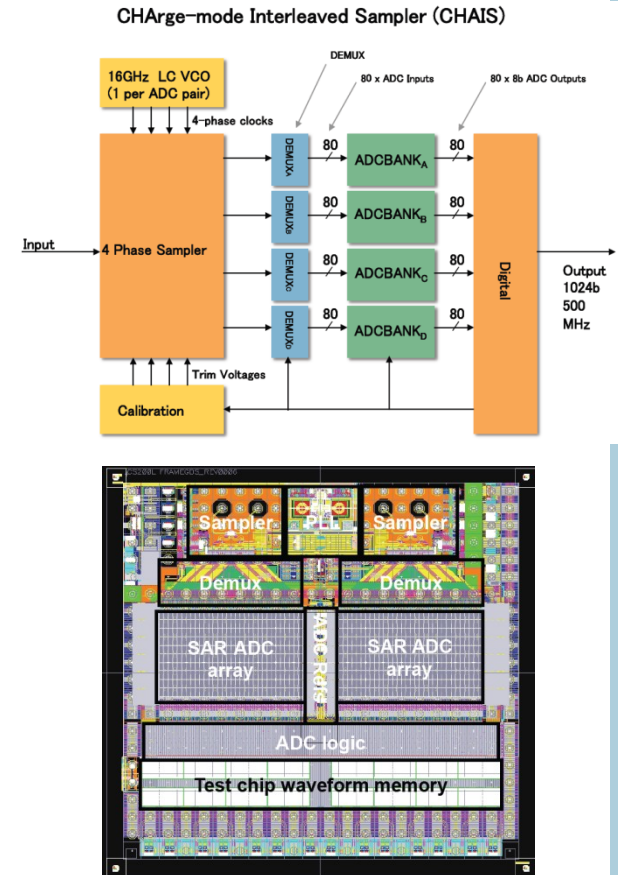
- Leading edge + Time Over Threshold (poor mans ADC)

- Minimal extra hardware (also measure falling edge time)
- Has been seen to work quite well in several applications.
- If signal shape not constant then ?.
- TOT now very often seen in HEP for indirect amplitude measurement with moderate resolution



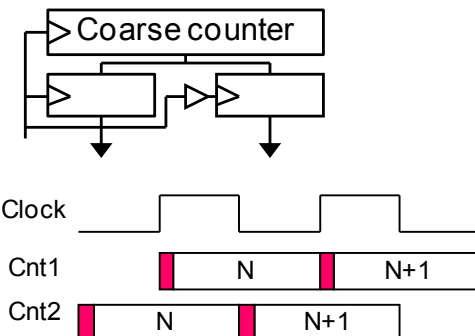
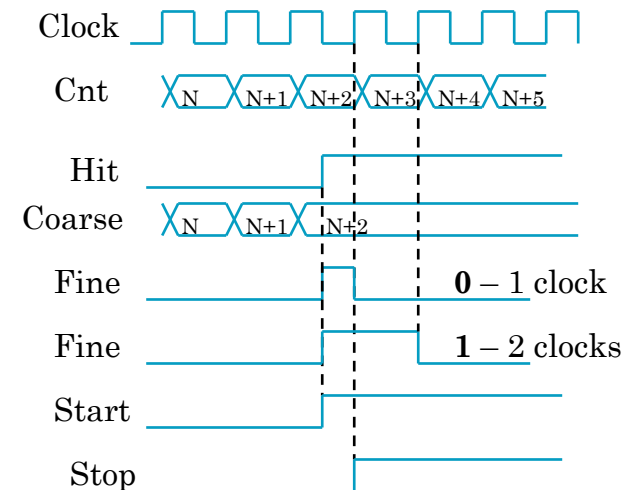
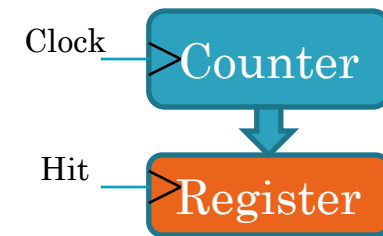
- Alternative: Very fast analog sampling

- Pulse matching – highest possible flexibility and performance
- High power – low channel density
- 64GHz 8b ADC's now feasible, 2W
 - 100GbE optical
- Large amount of data to read out and process (unless done on chip).
- Multiple sampling capacitor array chips made in HEP community
 - Sampling rate: 1 – 5Gs/s
 - Analog bandwidth: Few hundred MHz - GHz
 - Resolution: 8 – 12 bits
 - Memory size
 - Channel count
 - Triggering - Buffering
 - ADC
 - Readout



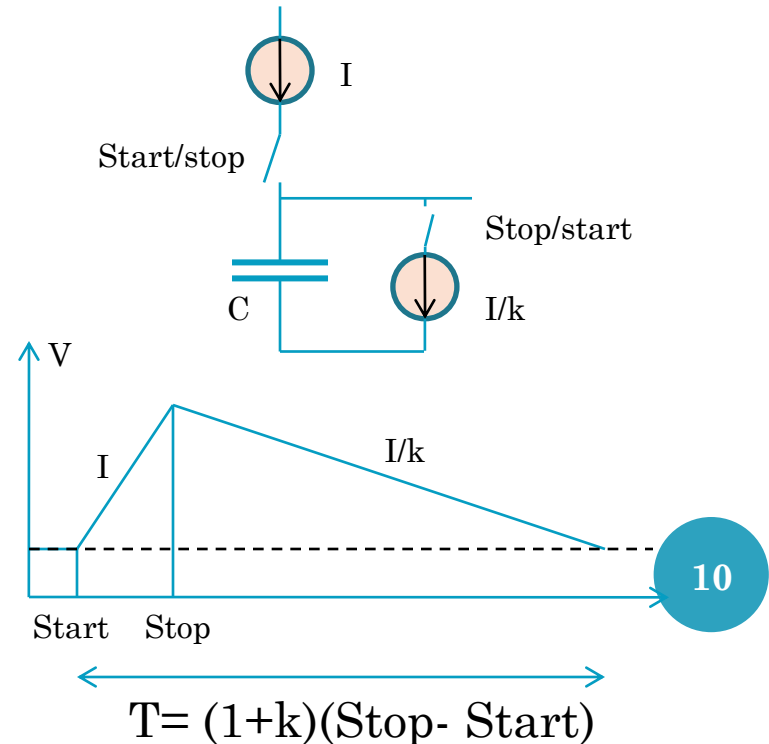
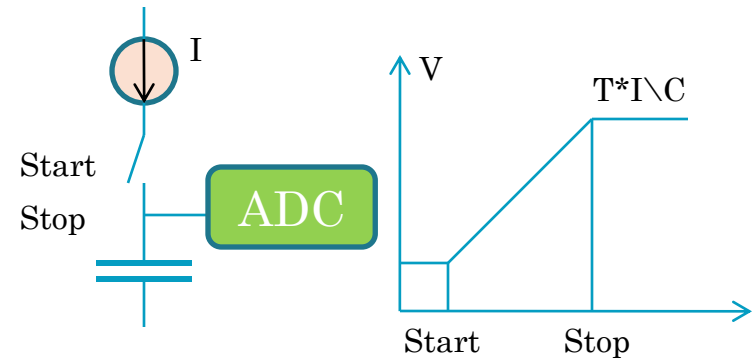
TIME MEASUREMENT

- Coarse count: $\sim 1\text{ns}$
 - Multi GHz counters can be made in modern ASIC's.
 - Gray code
 - Only one bit changing
 - Dynamic range: Large
- 1st. Level fine interpolation:
 - Extract timing difference between signal and reference (clock)
 - Dynamic range: 1 (2) clock cycle
 - A: Use same interpolation reference as counter (Clock).
 - B: Use Different "reference"
- Alignment between coarse and fine needs special care.
 - Must be done with precision of full resolution
 - If badly done then large error (coarse count) in small time window around coarse time change.
 - Example: Use of two phase shifted binary counters and selecting one based on fine interpolation.



TIME TO AMPLITUDE

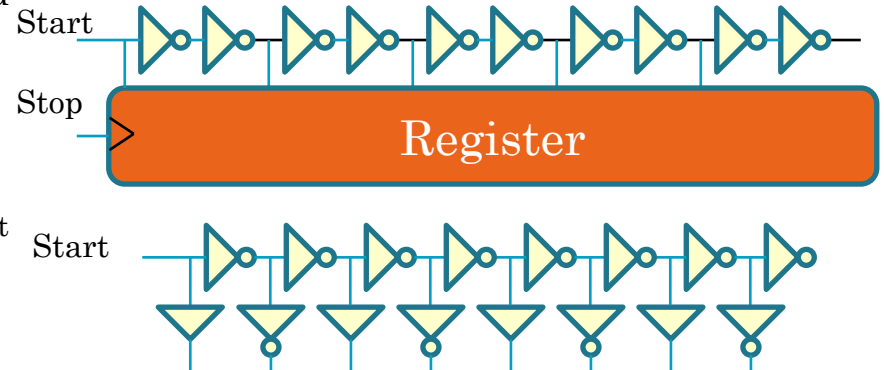
- Time to Amplitude Conversion: TAC
 - Classical type high resolution TDC implemented with discrete components
 - Delicate analog design
 - Requires ADC
 - Slow conversion time \rightarrow dead time
 - Not using same reference as coarse time
- Dual slope Wilkinson ADC/TDC
 - Time stretcher
 - Measure stretched time with counter
 - Slow: Analog de-randomizer
 - Example: NA62 GTK in-pixel design



DELAY LINE BASED

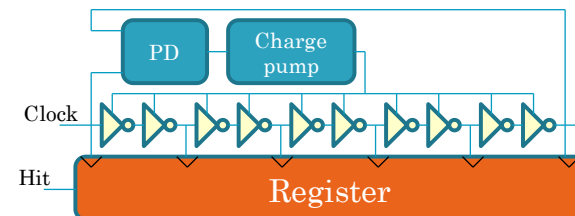
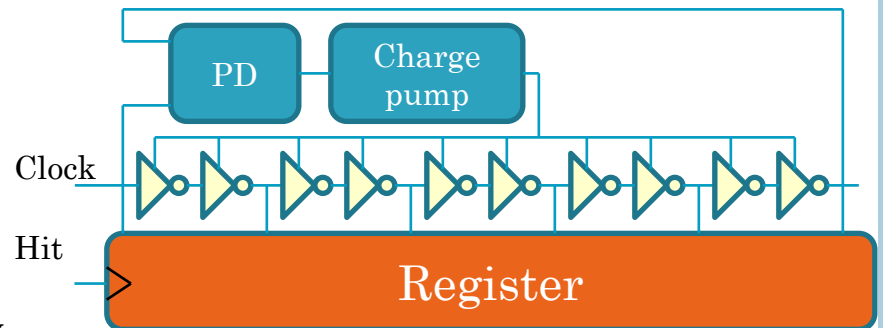
Basic principle

- Use “gate” (inverter) delays
 - Normally two inverters
- Gate delays have large process, voltage and temperature dependency
- Using inverting cell
 - Rise and fall time (N and P transistors) does not match well over process, voltage and temperature.
 - Different tricks can be used to make inverting and non inverting buffer have “same” delay but remains problematic.
- Fully “digital”
- Capture:
 - Use hit as clock to capture state of delay chain
 - Use delay signals to capture state of hit signal (high speed sampler)



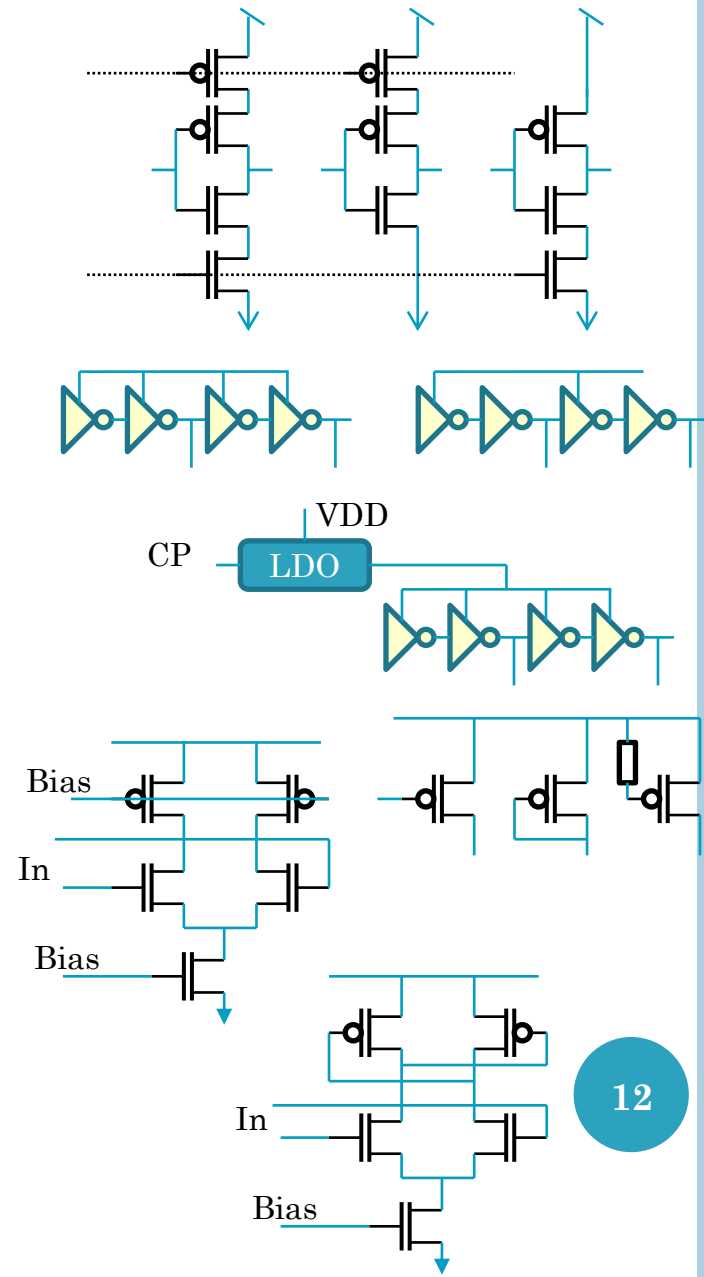
Delay Locked Loop

- Control delay chain to cover exactly one clock cycle.
 - Compensates for Process, Voltage and Temperature effects (but not miss-match)
 - Uses same timing reference as course count and self calibrates to this.
- Begin-end effects, Phase error, Jitter, Delay cell matching
- Such a delay locked loop is a very quite circuit as all transitions are perfectly distributed over clock period (not the case for the Hit signal)
- Half digital / half analog



DELAY ELEMENTS

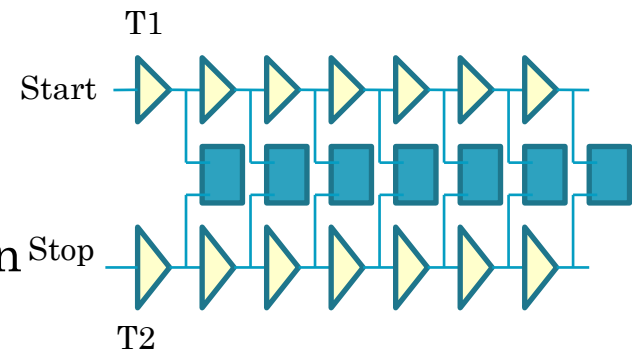
- Current starved inverters/buffers
 - N-side, P-side, Both
 - Only one of the two current starved
- Regulate delay chain power supply with local LDO
 - Careful interfacing to other circuits
- Differential delay cell
 - Consumes DC power -> More power
 - Only needs one cell per delay (better resolution)
 - (Less sensitive to power supply noise)
 - (Generates less noise)
 - Different types of loads can be used
 - Inductive peaking can gain ~20%
 - ~25ps possible in 130nm, worst case
- Pseudo differential and many more



SUB-GATE DELAY. 2ND. INTERPOLATION

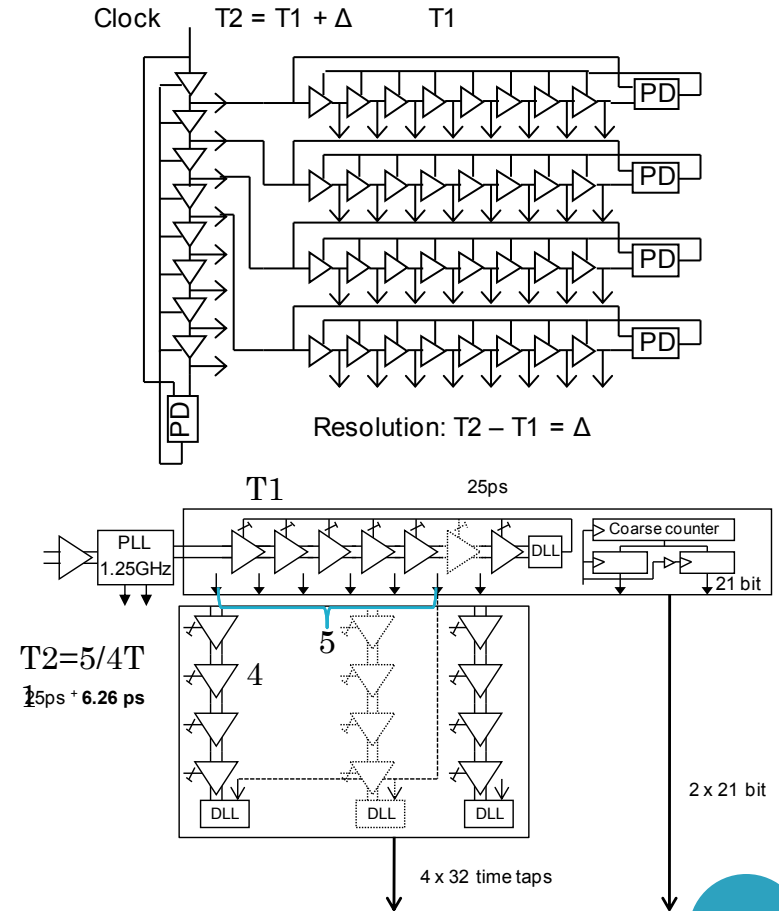
- Vernier principle

- Difference in delays can be made much smaller than delay in cell $R=T_2-T_1$
- Basic Vernier chain gets impractical long
- Performance gets miss-match dominated
- Delay difference can be implemented in many ways:
 - Capacitance loading
 - Transistor sizing
 - Different current starving
 - etc.,
- How to lock to reference ?
 - DLL's locked to different references
 - DLL's with different number of delay cells locked to same reference.



○ DLL arrays

- An array of DLL's can use the Vernier principle
 - DLL's auto lock to common timing reference
- Example: Improve binning from 25ps to 6.25ps
 - 4 equal DLL's driven by fifth DLL with slightly larger delay
 - Potentially very miss-match sensitive
- 1 DLL driving many small DLL's
 - Less miss-match sensitive (miss-match correction still advantageous)
 - Non trivial layout to assure matching routing capacitances and R-C delays



- Passive delays

- In modern IC technologies wiring delays already the dominating source of delays.
- No easy way to “lock” to global reference
 - Some kind of adjustment required

- R-C delay

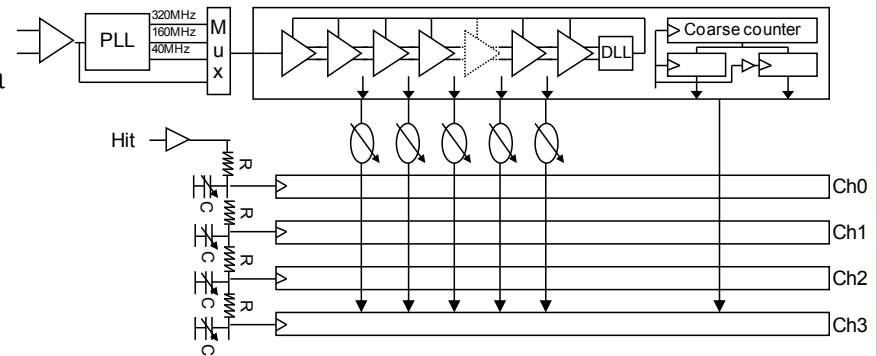
- The adjustment of any tap affects all the other taps
 - Used in HPTDC. In practice a bit of a pain (but works)

- Transmission line

- Short delays can be made with on-chip transmission lines
- Predefined and characterized transmission lines exists in may chip design kits.
- Lossy so signal shape changes down the line.

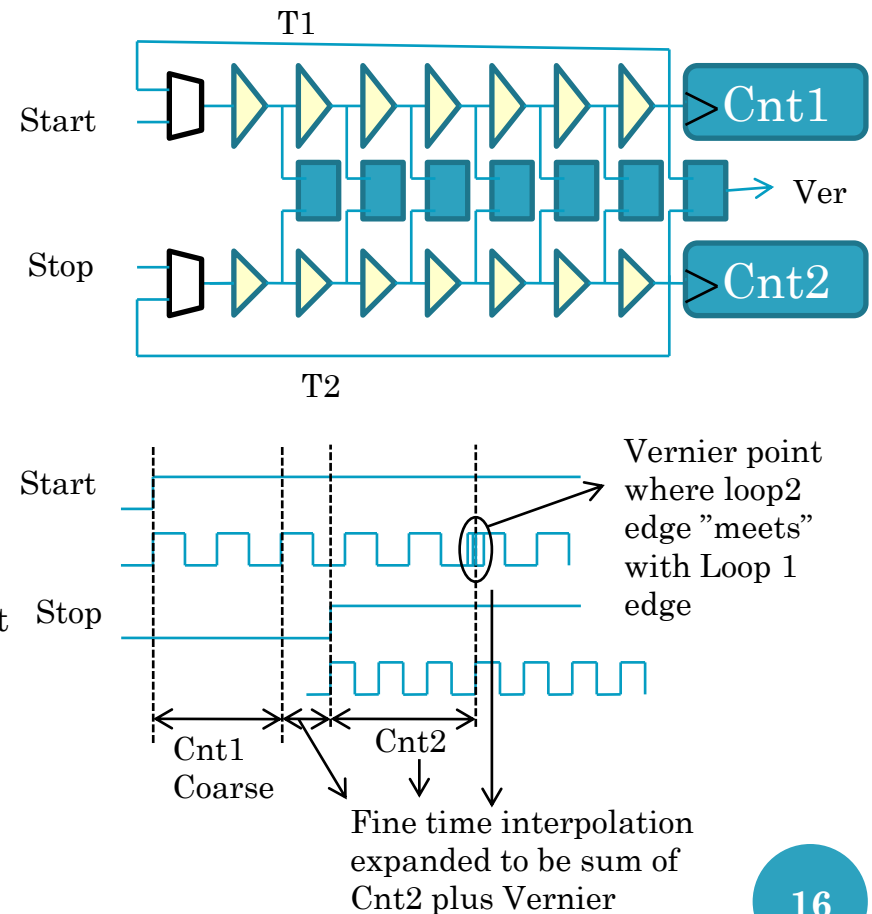
- Can be used on hit signals instead of on DLL signals

- Flexibility on channel count versus resolution (used in HPTDC)
- This scheme can be used with many approaches



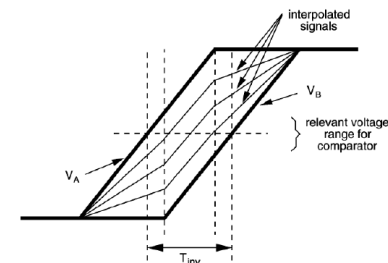
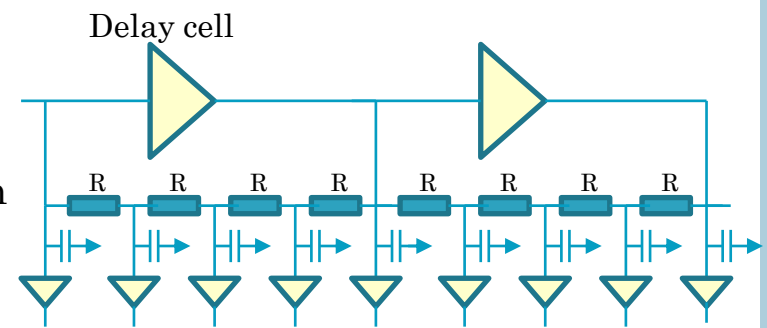
- Looped Vernier (beating oscillators)

- Two delay chains/loops propagates timing signals with slightly different delay.
 - Start – Stop type
- Start oscillators with start and stop signals
 - Latch loop1 count (start) when stop occurs
 - Latch loop2 count (stop) when edge in loop2 catches up with edge in loop1.
 - Store in which vernier cell the two edges meet.
- Appears elegant but hard to implement:
 - Loop feedback time and re-coupling must be “zero” delay
 - Circular layouts tried (but not so good for matching)
 - All this per channel
 - No direct lock to a reference
 - Long conversion time -> Dead-time
 - Some errors accumulate during recirculation

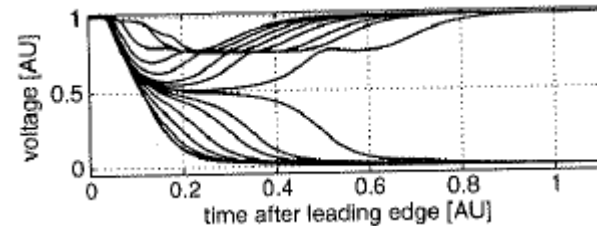
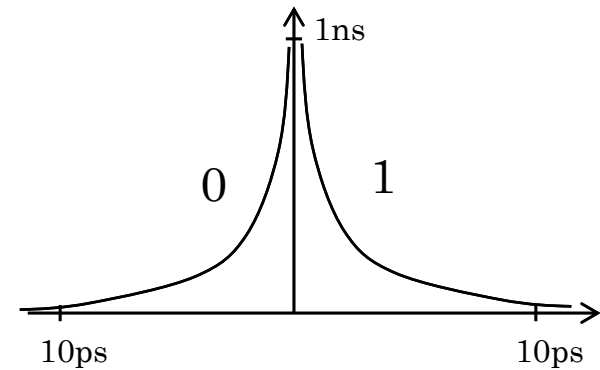


- Analog interpolation between delay cells

- Resistive voltage division across neighbor delay cells.
 - Rise times in delay chain longer than delay of cell.
 - Purely resistive division “autoscales” with delay of delay cell
 - Only carries current during transitions.
- Parasitic capacitance makes this resistive division a mixture of resistive division and R-C delays
 - Relatively low resistor values required to prevent being R-C dominated.
 - With equal resistances the bins are not evenly spaced -> re-optimize individual resistors
 - Does not any more fully “autoscale” to delay of delay cell.
- Can be done on single ended and differential delay cells

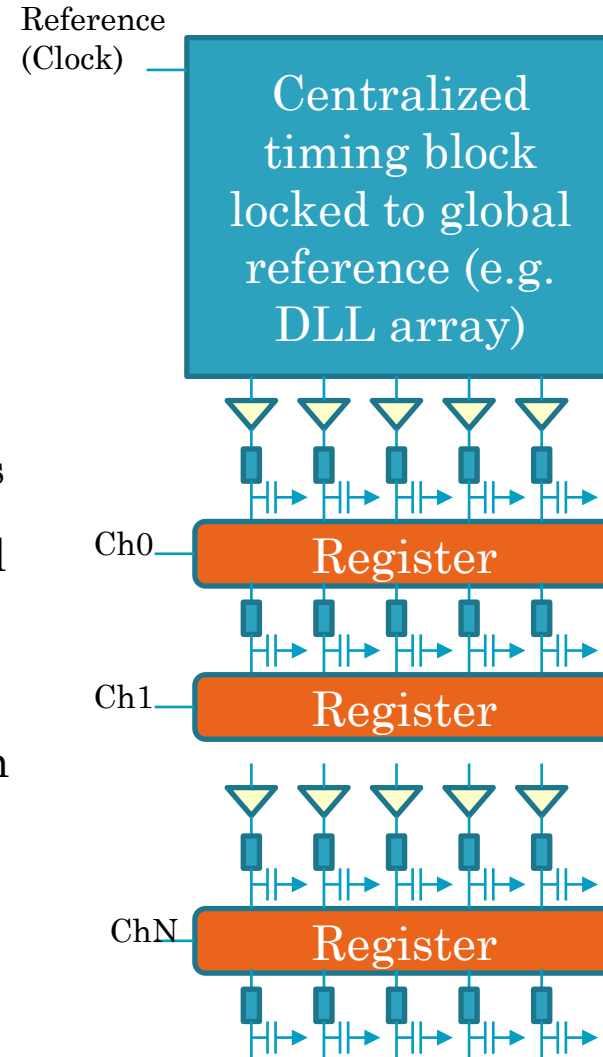


- Time amplifier in “metastable window” of latch (with internal feedback).
 - Any type of latch have a small time window where it enters a metastable region and it takes some time to resolve this
 - A small change of timing on the input gives a “large” change of timing on the output: Time Amplifier
 - For very high time resolution cases.
 - Only small window where time amplification occurs
 - Non linear, Very sensitive to power supply, etc.
 - Hard to use in practice
 - For 3rd level interpolation
- Plus other “exotic” schemes.
 - (implementation nightmare)



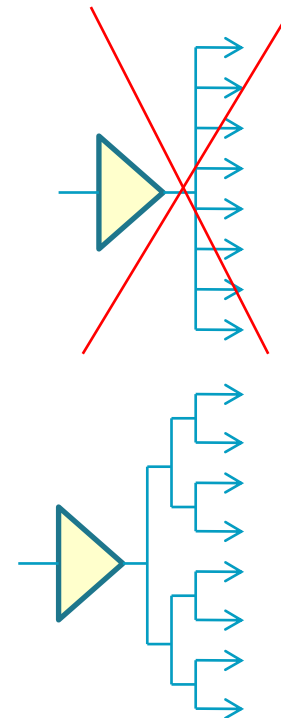
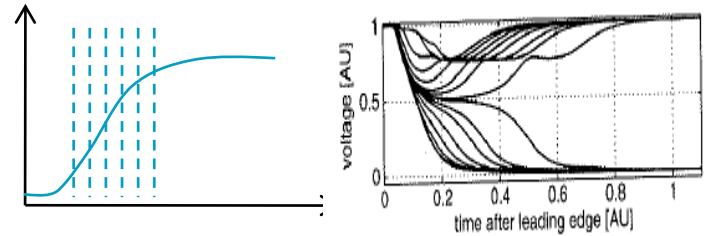
CENTRAL TIMING BLOCK

- For multi channel TDC's it is attractive to have a central timing block used to drive array of individual channels
 - Minimal complexity per channel.
 - Only one block to calibrate.
 - Power consumed in timing block less critical (but timing distribution to channels gets significant)
- For very high resolution TDC's this gets increasing difficult as required signal propagation delays larger than required resolution (miss-match !).
- Buffer delays large than resolution: miss-match sensitive
- For highly distributed TDC functions on large chips (e.g. pixel chips) it gets routing and power prohibitive even for low time resolution.
 - Alternative: Centralized DLL locked to reference generates control voltage to distributed delay loops (miss-match !)

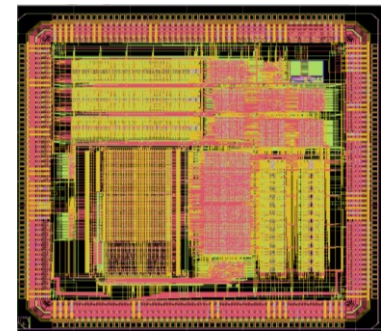


TIME CAPTURE REGISTERS

- The latches/registers used to capture the timing event gets critical in the ps range
- Fast capture/regeneration registers required
 - Timing signals have large rise/fall times compared to required resolution.
 - Small and well defined metastability window with good resolving capability.
 - Single ended (e.g. classical master slave FF) or differential (sense amplifier for fast SRAM's)
- Mismatch between registers
 - Assuming multiple registers must latch at same instance
- Routing of hit signal to registers must be done with care

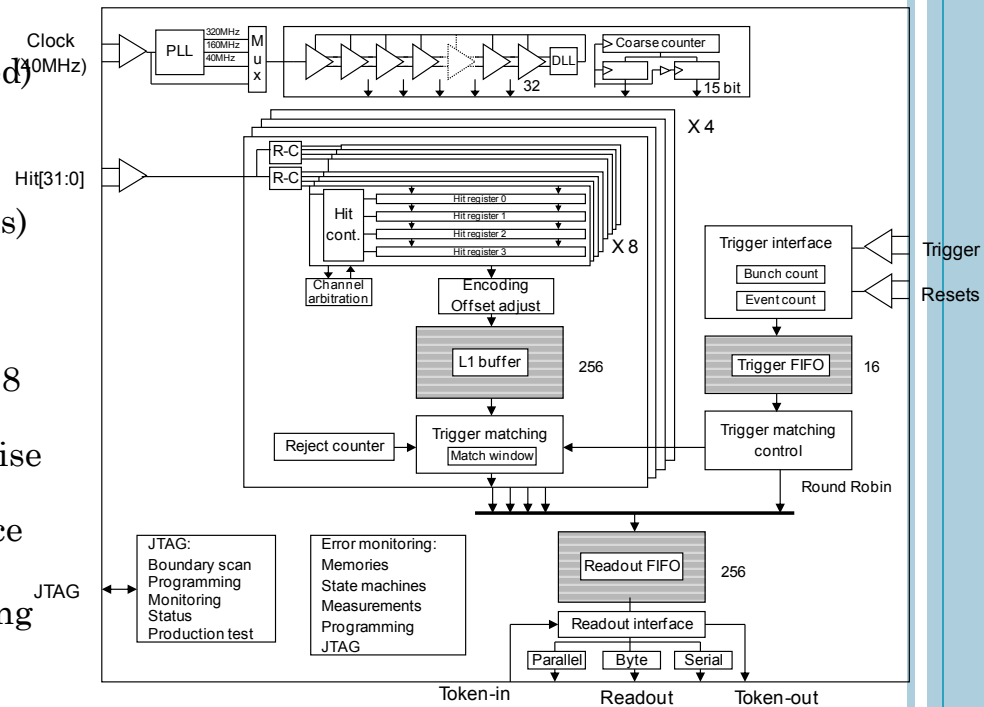


EXAMPLE HPTDC

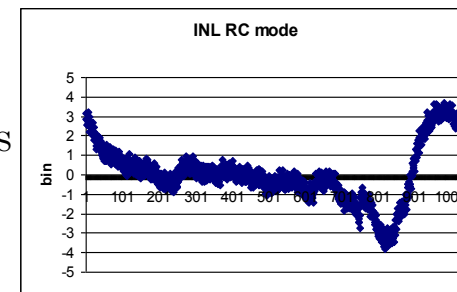


Features

- 32 channels(100ps binning),
8 channels (25ps binning)
 - LVDS (differential) or LVTTTL (single ended) inputs
 - 40MHz time reference (LHC clock)
 - Leading, trailing edge and time over threshold (for leading edge time corrections)
 - Non triggered
 - Triggerred with programmable latency, window and overlapping triggers
 - Buffering: 4 per channel, 256 per group of 8 channels, 256 readout fifo
 - Token based readout with parallel, byte-wise or serial interface
 - JTAG control, monitoring and test interface
 - SEU error detection.
 - Power consumption: 0.5W – 1.5W depending on operating mode.
- Used in large number (>20) of HEP applications:
- ALICE TOF, CMS muon, STAR, BES, KABES, , ,
 - Commercial modules from 3 companies
 - ~50k chips produced
- 250nm technology (designed ~10 years ago for LHC experiments)

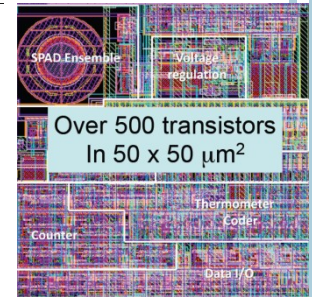
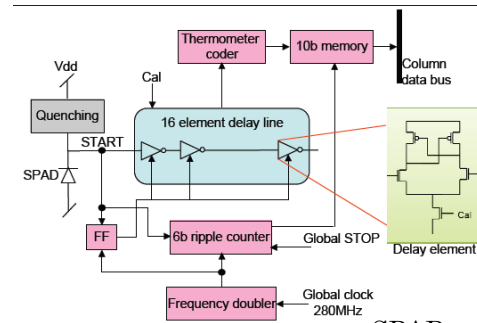


On-chip clock crosstalk corrected
Offline:
40ps → 17ps RMS



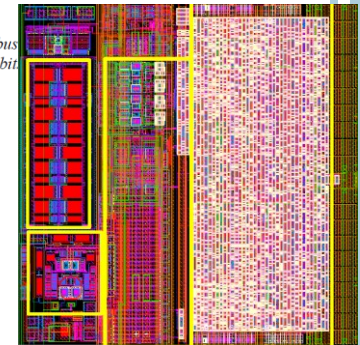
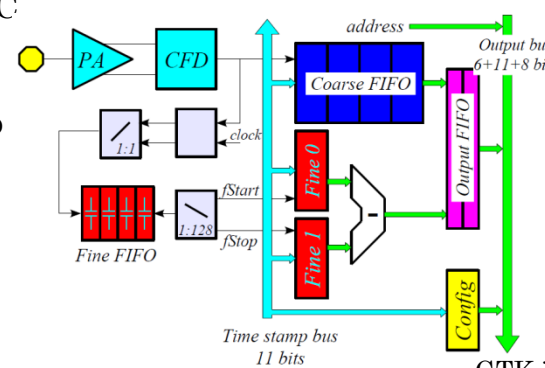
TDC'S FOR PIXEL APPLICATIONS

- For large pixel array chips with TDC function the routing and power to distribute required TDC signals to whole array may get power/routing prohibitive
 - Local TDC in each pixel or shared among neighbor pixels (super-pixel)
 - Local TAC with dual slope Wilkinson ADC
 - Local delay loop (oscillator) only running when hit has been seen.
 - Controlled from central DLL locked to timing reference
 - Route hit signals (e.g. or'ing of pixels if rate allows) to centralized TDC block
- SPAD with TDC: ~100ps binning
- NA62 GTK: 100ps binning
 - A: TAC per pixel with CFD and analog de-randomizer
 - B: DLL for leading and TOT per column
- Timepix3: ~1ns binning
 - Local oscillator only running when hit occurs. Controlled from central DLL

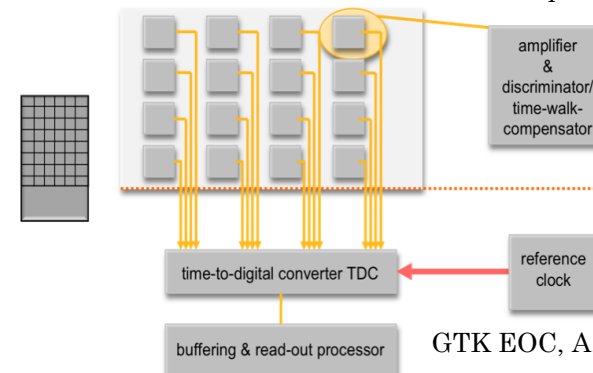


Over 500 transistors In $50 \times 50 \mu\text{m}^2$

SPAD array, E. Charbon, Delft



GTK in-pixel, G. Mazza, Turin



GTK EOC, A. Kluge, CERN

DIFFICULTIES IN THE PS RANGE

- Calibration is a must, but at what rate
 - We therefore tend to prefer auto calibrating architectures based on DLL's (basic offset calibration still required)
- Slew rate of signals much slower than resolution aimed at (digital signals do not exist in the ps domain)
- Matching gets critical and mis-match compensation becomes a must if aiming at ~ps resolution.
 - Automated on chip (for commercial applications)
 - With help from “outside” (OK in HEP). We can even work with imperfect TDC's if it can be appropriately corrected in software.
- Distribution of timing signals gets critical (R-C delays in Al, Cu wires, via's, contacts, etc.)
- Metastability in timing capturing circuit gets significant/critical.
- Interpolation to high ratios gets increasingly sensitive to power supply noise (even for the digital approaches), substrate coupled noise, etc.
- Routing delays are significant and difficult to balance (especially for loop feedbacks and parallel load of many registers)
- Phase error across DLL (phase error in PD and end-begin effect)
- Testing a TDC with ps resolution is far from trivial
 - Stochastic testing for linearity (Code Density Test).
 - Fixed delays for jitter and stability.
 - Time sweep if you can find the appropriate instrument (resolution and jitter) and can afford it
- **System level performance is what counts in HEP !**
 - Detector, analog front-end, discriminator, time walk compensation, board design, power decoupling, connectors, cables, stability (jitter) across full system, timing distribution across full system, calibration, , ,

CONCLUSIONS

- Many different schemes and variants to get \sim ps resolution in ASIC's.
- Combination of several to get dynamic range and resolution
 - Fast (Gray) counters +
 - DLL's +
 - Vernier - delay difference +
 - R-interpolation +
 - Time amplifier
 - Etc.
- Stability, jitter and miss-match critical at this level of timing resolution.
- Global system timing resolution is what counts in HEP



BACK UP SLIDES



25



WARNINGS WHEN IT COMES TO COMPARE TDC PERFORMANCE

- If only obtained on simple test circuit
 - No additional circuitry introducing noise (substrate, ground, Vdd, crosstalk)
- If only demonstrated over small dynamic range
- If not clearly demonstrating correct alignment between coarse and fine interpolation(s).
- If results shown with averaging over many hits.
- If only showing jitter/effective resolution at some fixed measured intervals
- Temperature, voltage, process variations
- Mismatch not analyzed and only show measurements from one single chip.
- Why make a 1ps “resolution” TDC if effective RMS resolution is much worse than this ?
 - Reminder for perfect TDC: $RMS = bin/\sqrt{12} = bin/3.5$
 - Global aim: $RMS \leq Bin \text{ size}$.
 - (Exception if averaging of multiple measurements can be made)

TDC ASIC'S FOR PHYSICS

- Only very few flexible TDC ASIC's are available for HEP (e.g. HPTDC).
 - Resolution
 - Number of channels
 - Data buffering, triggering and readout
 - Radiation tolerance
- Flexibility can be obtained by FPGA based TDC's but
 - Limited resolution (but many experimental circuits tried: Gate delays, fast carry chains, Vernier principle using different loading)
 - Channel count
 - Radiation tolerance
 - Cost, power and integration for large scale system

NEW HEP VERSATILE TDC ?

- 64 or 128 channels
- 5 – 10 ps bin, RMS: 2 – 5 ps, Delay Locked Loop based
 - Option A: R(-C) interpolation
 - Option B: Array of delay locked loops on same reference
 - Option C: Single DLL on clock + DLL on hits
 - Adjustment features to allow compensation of miss-match effects.
 - RMS to be better than bin size (resolution)
- Global time reference compatible with major experiments (e.g. 40MHz for LHC)
 - Internal PLL for clock multiplication (jitter critical)
- Flexible data buffering, triggering and readout
 - Use general scheme as used in HPTDC
- Max 10mW per channel
- Timing part of such TDC currently under study
 - 130nm CMOS
- Finalization depending on actual needs (and funding and manpower)
- Versatile front-end/discriminator more delicate

