The Road Ahead

August 30, 2023

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630-561-6813

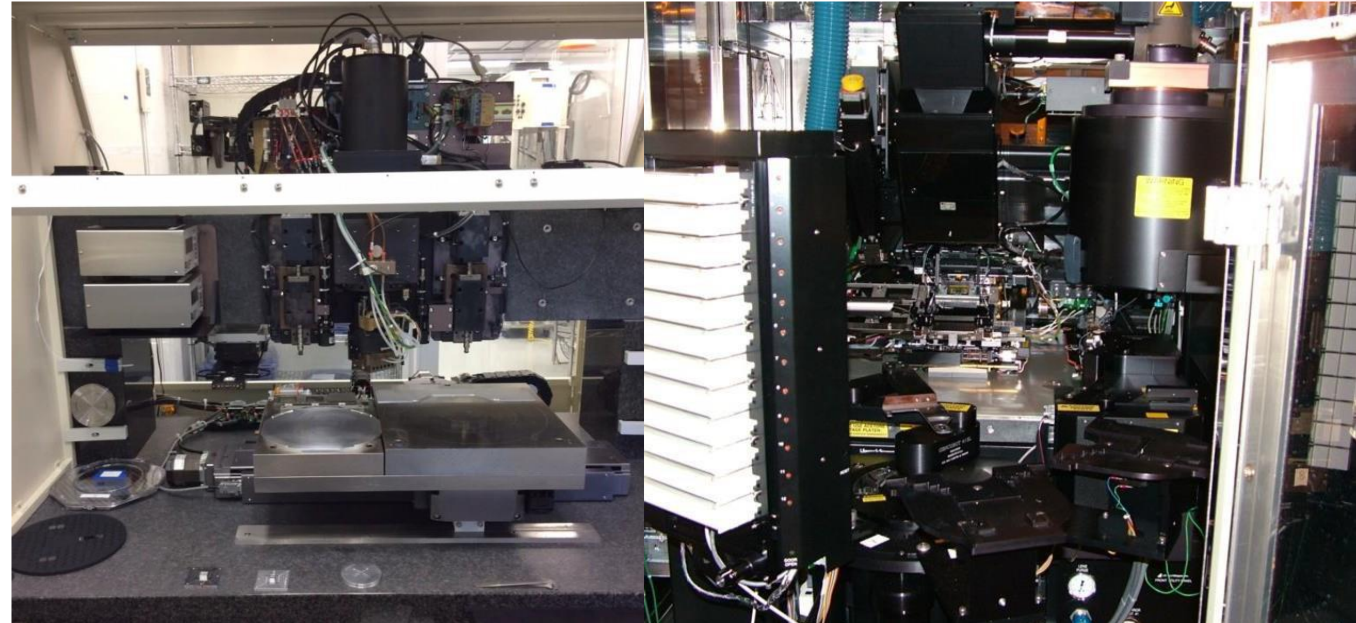
Wall Street Journal - July 11, 2023

Page 1 of Financial Section

"To Drive AI, Chip Makers Stack ‘Chiplets’ Like Lego Blocks"

NHanced Semiconductors

- Batavia, IL: Design and Test
  - Complete front end and backend design down to 12nm
  - Supports AI and HPC systems development
- Morrisville, NC: Foundry
  - 3”-200mm
  - Copper, Al, Ni BEoL
  - Interposers
  - 2.5/3D Integration
- Odon, IN: Packaging
  - Packaging
  - RadHard Microelectronics
- New Fab: L/MVM
  - 55,000 sqft cleanroom
  - ~5,000 wafers/month
  - 3”-200mm + 300mm
  - Copper, Al, Ni BEoL
  - Interposers
  - 2.5/3D Integration



NHANCED SEMICONDUCTORS

Effective End of Moore’s Law

Moore’s Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

– This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
– Today we can indeed shrink transistors further, but the cost per transistor no longer declines.

We can get something a little more compact

- Perhaps a little less power
- But we pay more for these features now.

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What Does This Mean?

The semiconductor industry is about to undergo a sea change.

- New ways of accomplishing Moore’s law economics and performance are needed.
  - The industry is now looking to use advanced packaging to drive future semiconductors.
    - Better Cost
    - Better Performance
    - Better SWaP

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Foundry 1.0 – Todays Model

- Current semiconductor business has been focused on driving smaller transistors.
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk
- Twilight of Moore's Law

Vision of the Future

A new semiconductor industry paradigm is evolving…

Foundry 2.0 –

A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

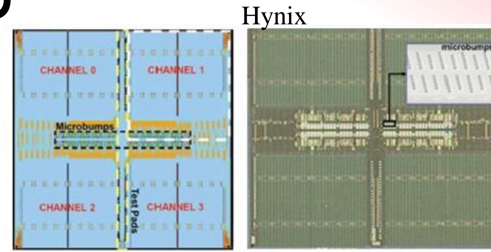
Foundry 2.0 – New Model

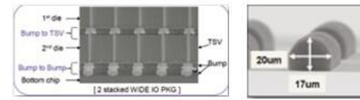
- System solution focus
  - Best of class components
  - Additive Semiconductor Processing
- Relies on Advanced Packaging (AP) and Chiplets
  - Heterogenous integration
  - Photonics
  - MEMS
  - RF
- Advantages
  - Low development cost
  - Low capital cost
  - Short development times
  - Inexpensive design tools
  - Low risk

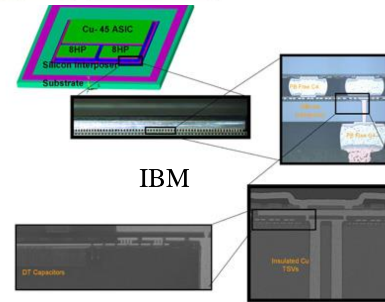
What Is Advanced Packaging?

- Sensors (Cameras)
  - Sony 10+ years ago, - now mainstream
  - Virtually every new USG IR sensor is an AP
  - Driven by size/form factor
  - System cost reduction
- GPUs
  - Dawn of both interposers and chiplets
- Micro-Displays
  - Driven by materials (GaN) and pitch requirements
- Compute Devices
  - leading edge risk takers
  - AMD and Xilinx early and now Intel
  - Driven by
    - Memory BW/Latency
    - Heterogenous targeted compute
    - Photonics coming on scene for I/O and compute
  - Lower power per bit-op
  - Effective Larger die with much better yield/cost

Hynix

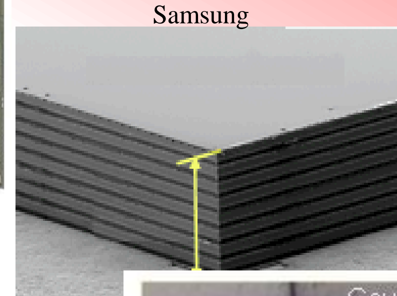


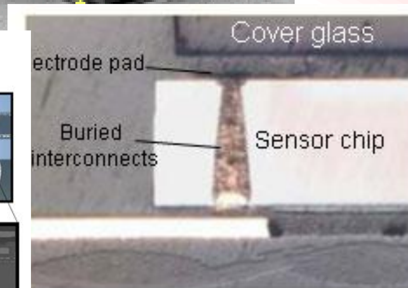




IBM

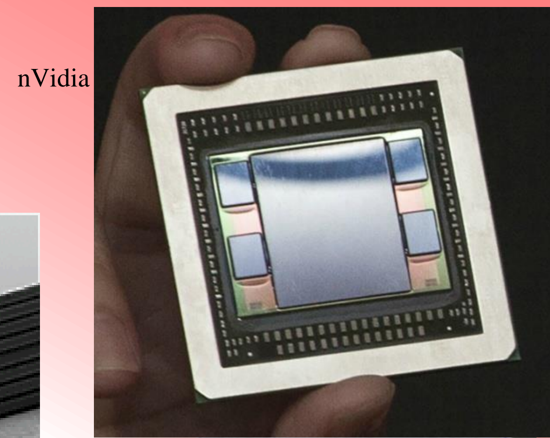
Samsung

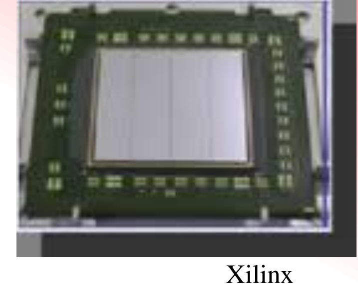




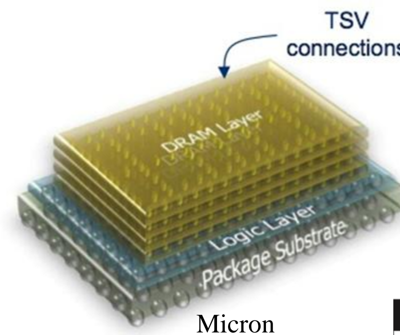
Sony

nVidia

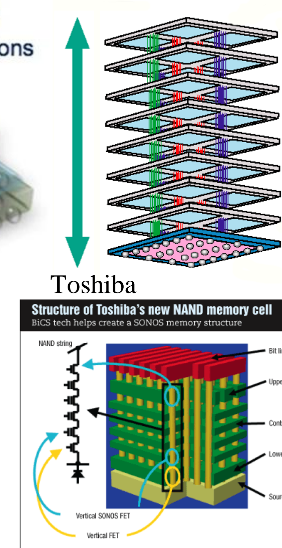




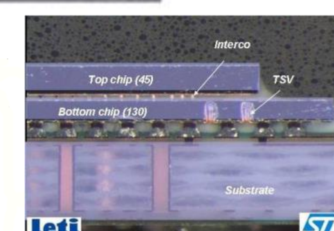
Xilinx



Micron



Toshiba



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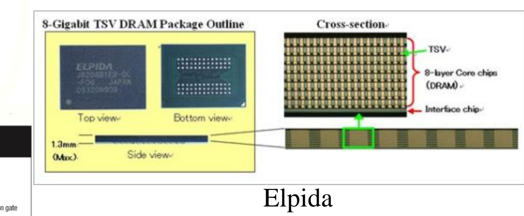


Elpida

NHANCED SEMICONDUCTORS

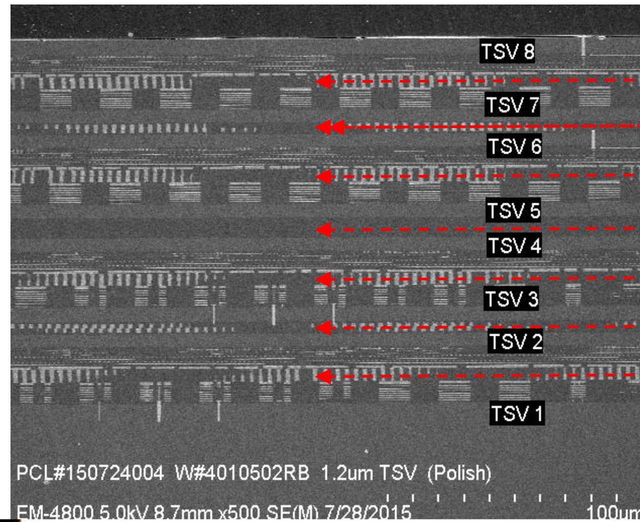
AP Elements: Bonding

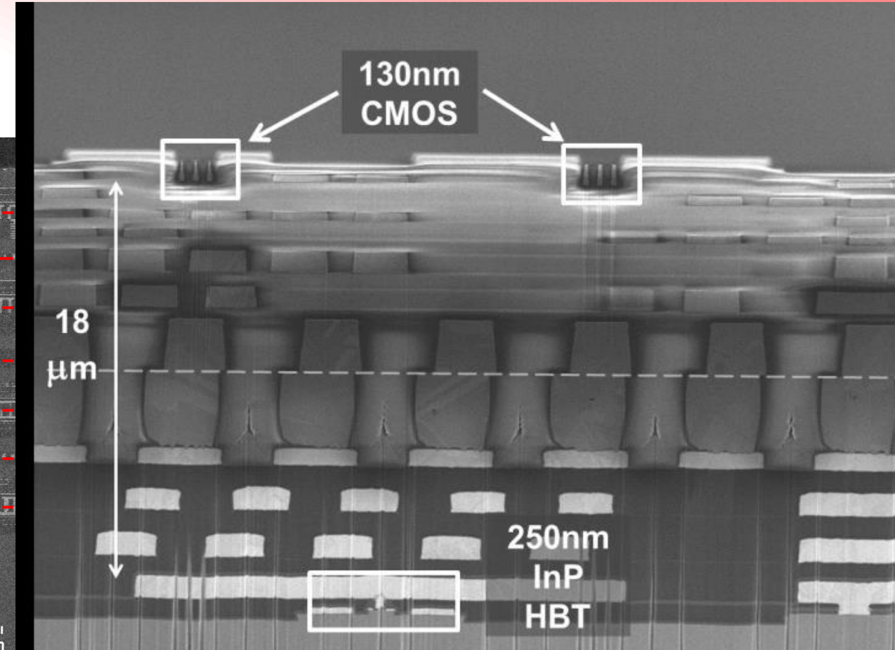
Millimeters ⇨ Microns

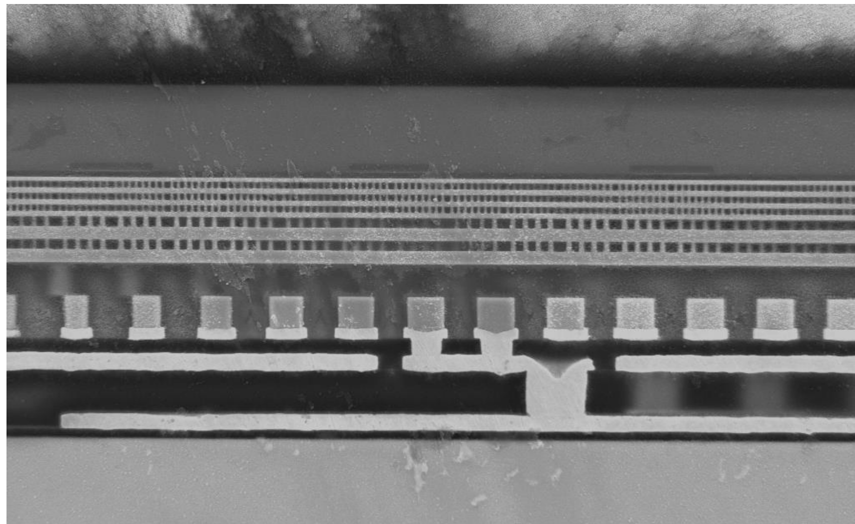
Kilograms ⇨ Grams

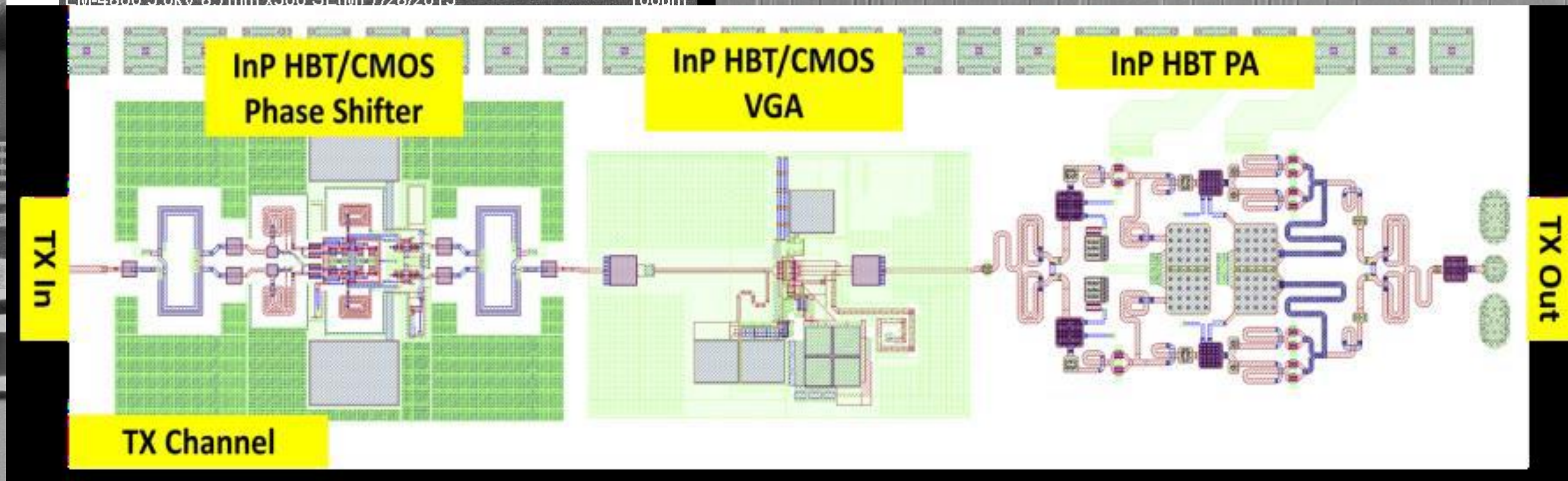
Mixed Materials

Best of Class



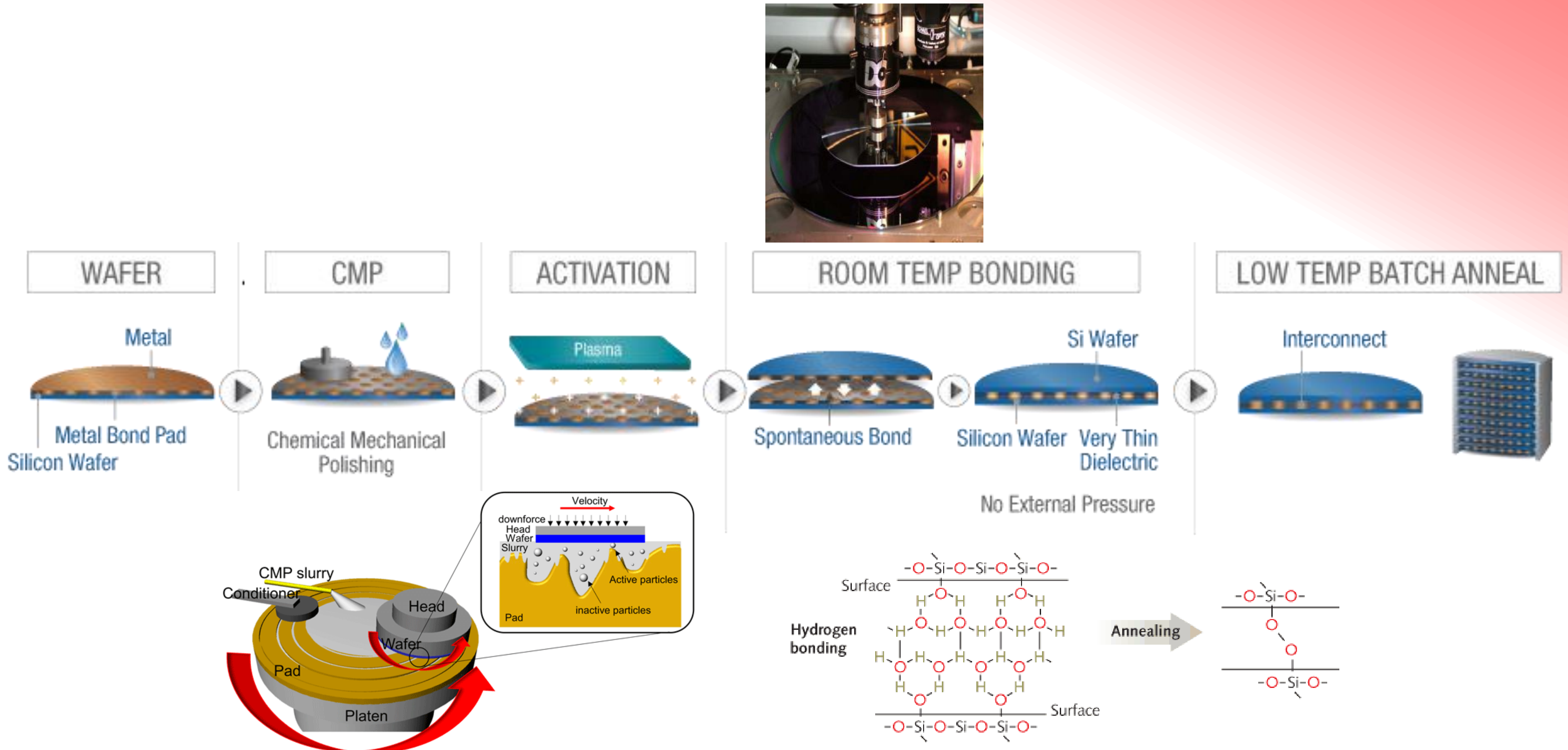






NHANCED SEMICONDUCTORS

DBI®: Low Temperature Hybrid Bonding Process



Jihoon Seo / Materials Research Society

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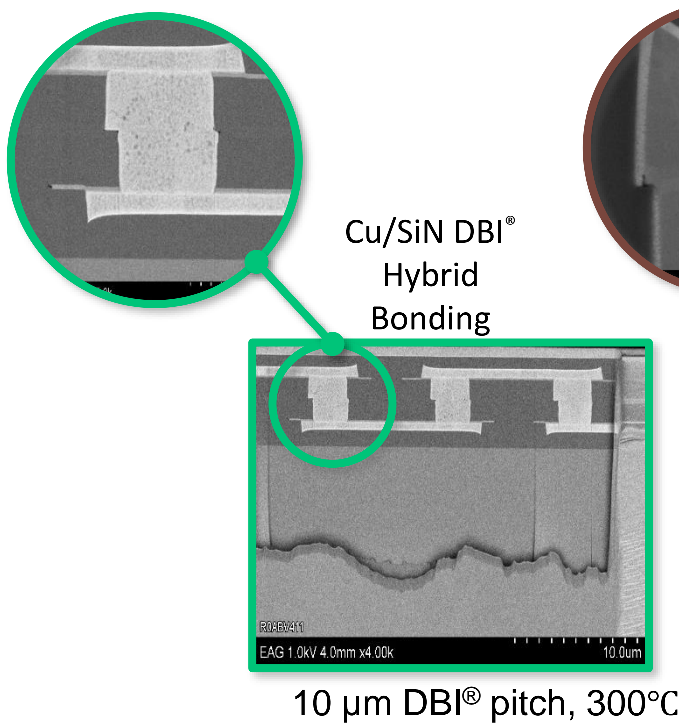
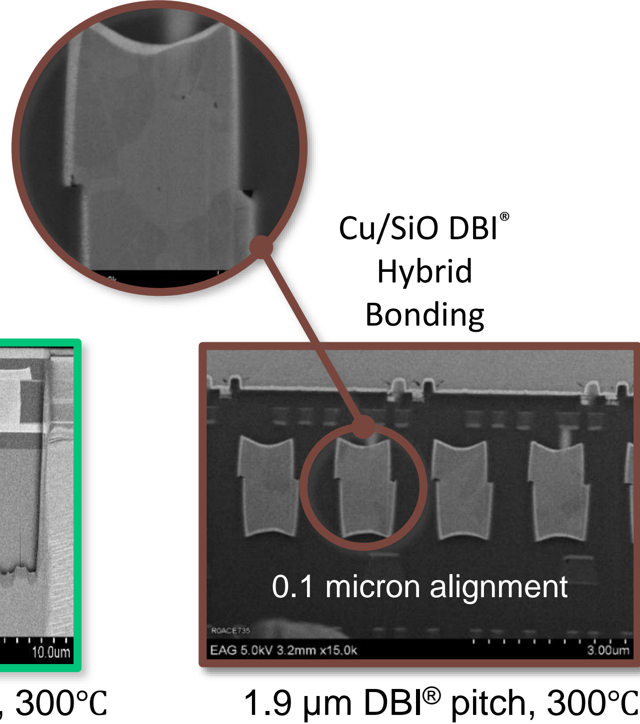
Bonding in Action

Hybrid Bonding Interconnect Pitch Scaling

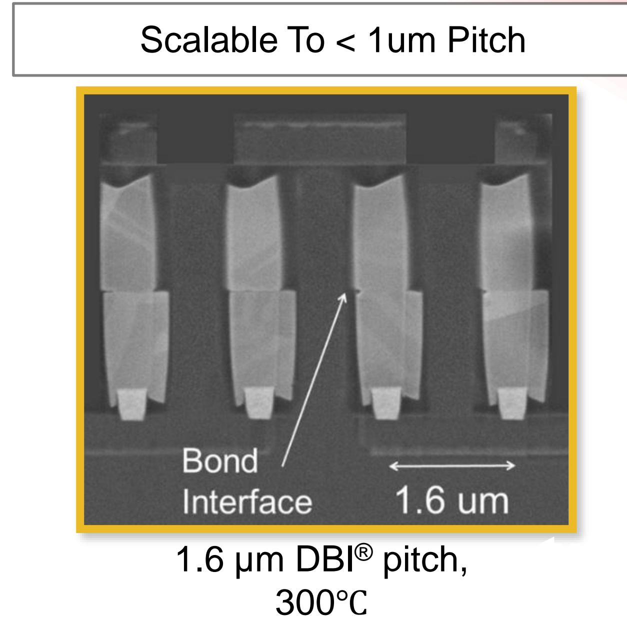


10 µm DBI® pitch, 300℃



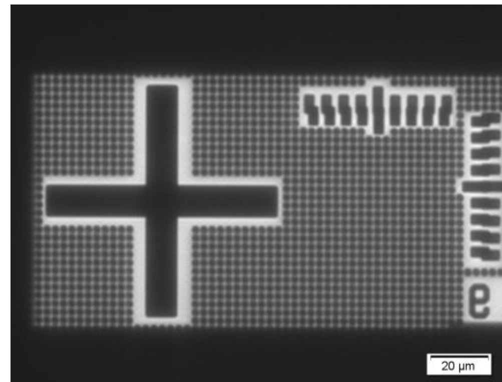
1.9 µm DBI® pitch, 300℃

Scalable To < 1um Pitch

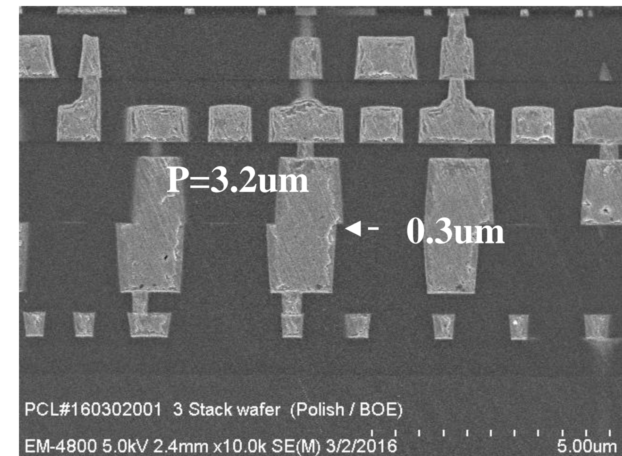


1.6 µm DBI® pitch, 300℃

- 3sigma < +/- 1um misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding



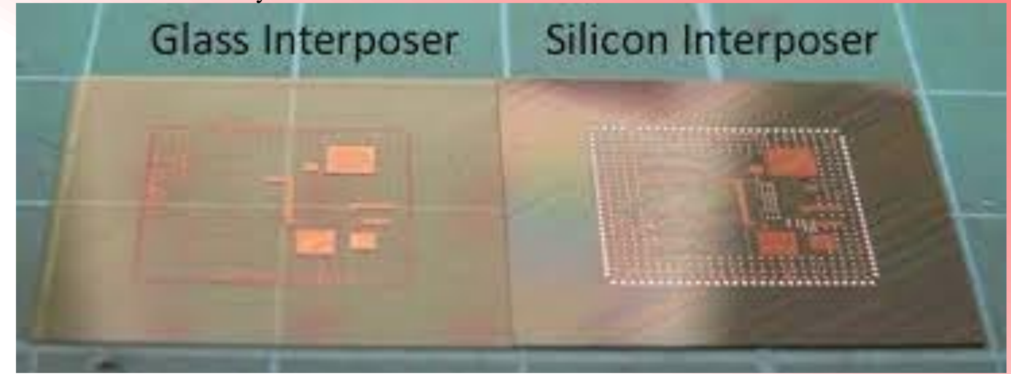
NHANCED SEMICONDUCTORS

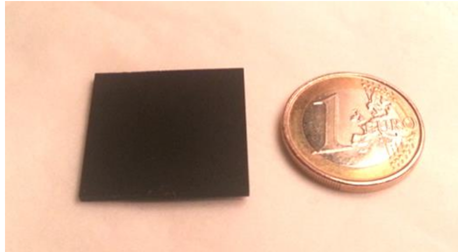


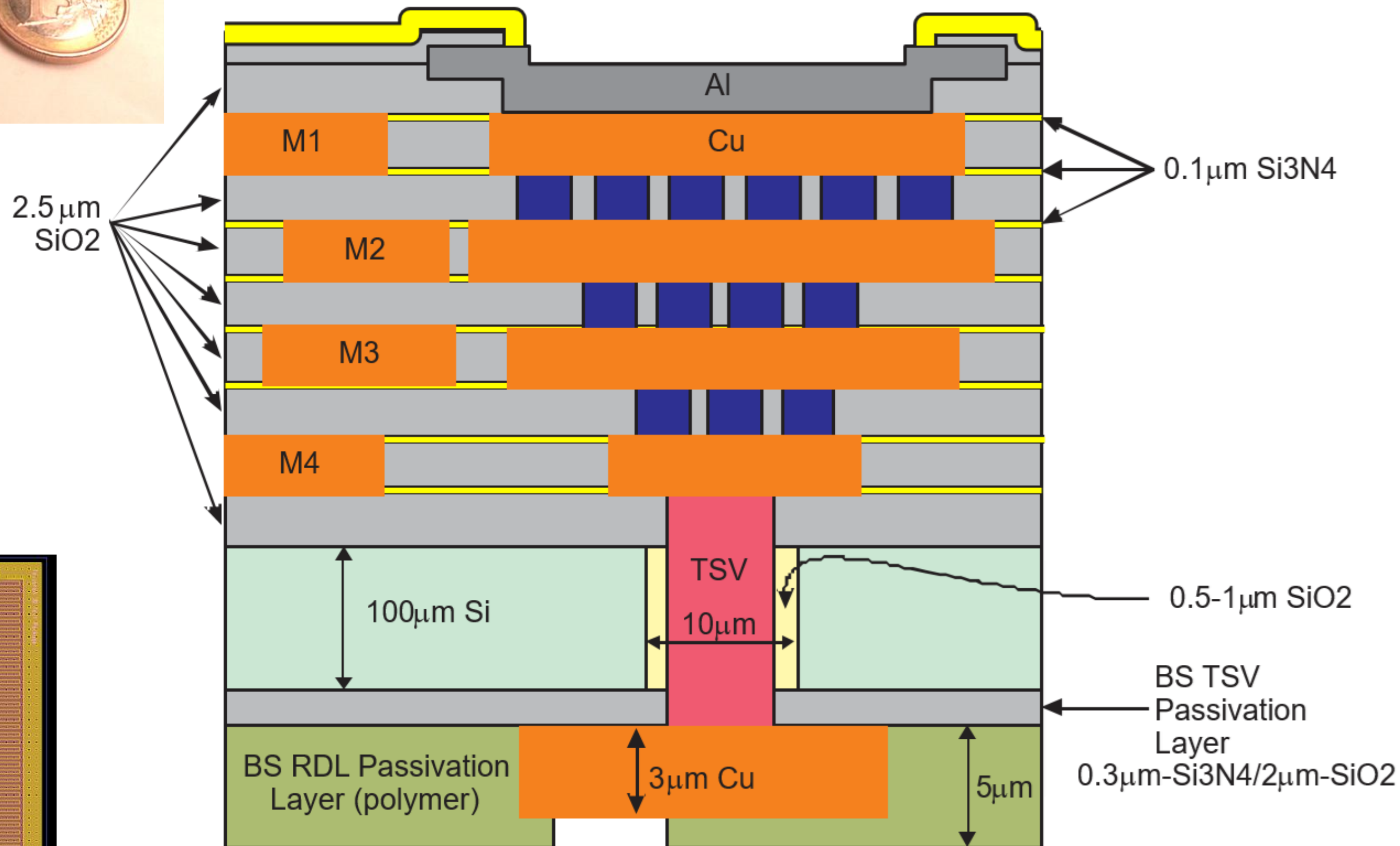
AP Elements: Interposers

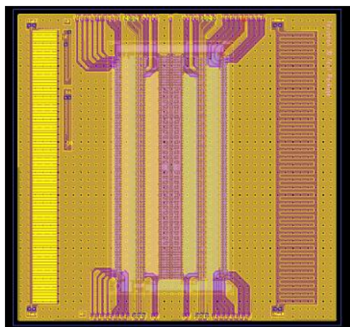
- ➢Bigger, Better, Faster
- ➢Lower Power

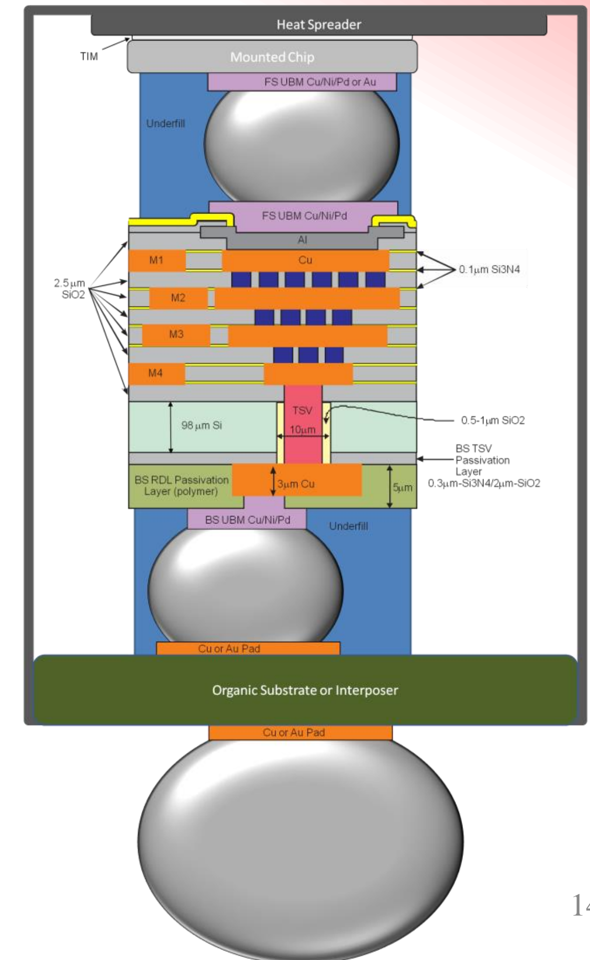
Mosaic Microsystems











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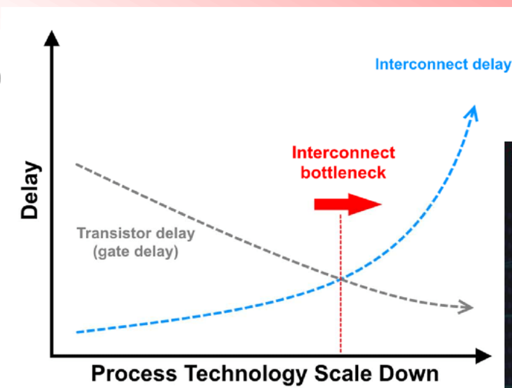
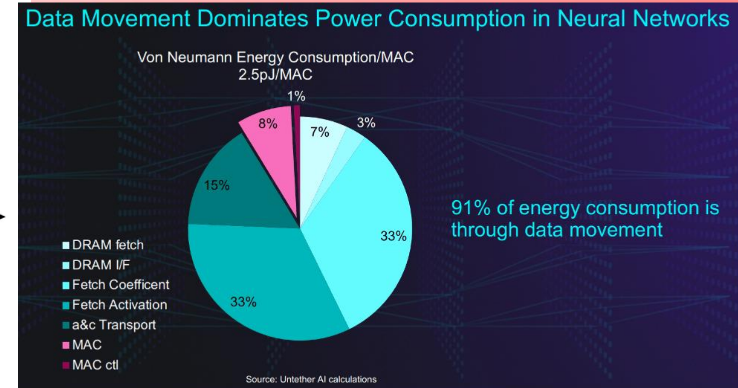
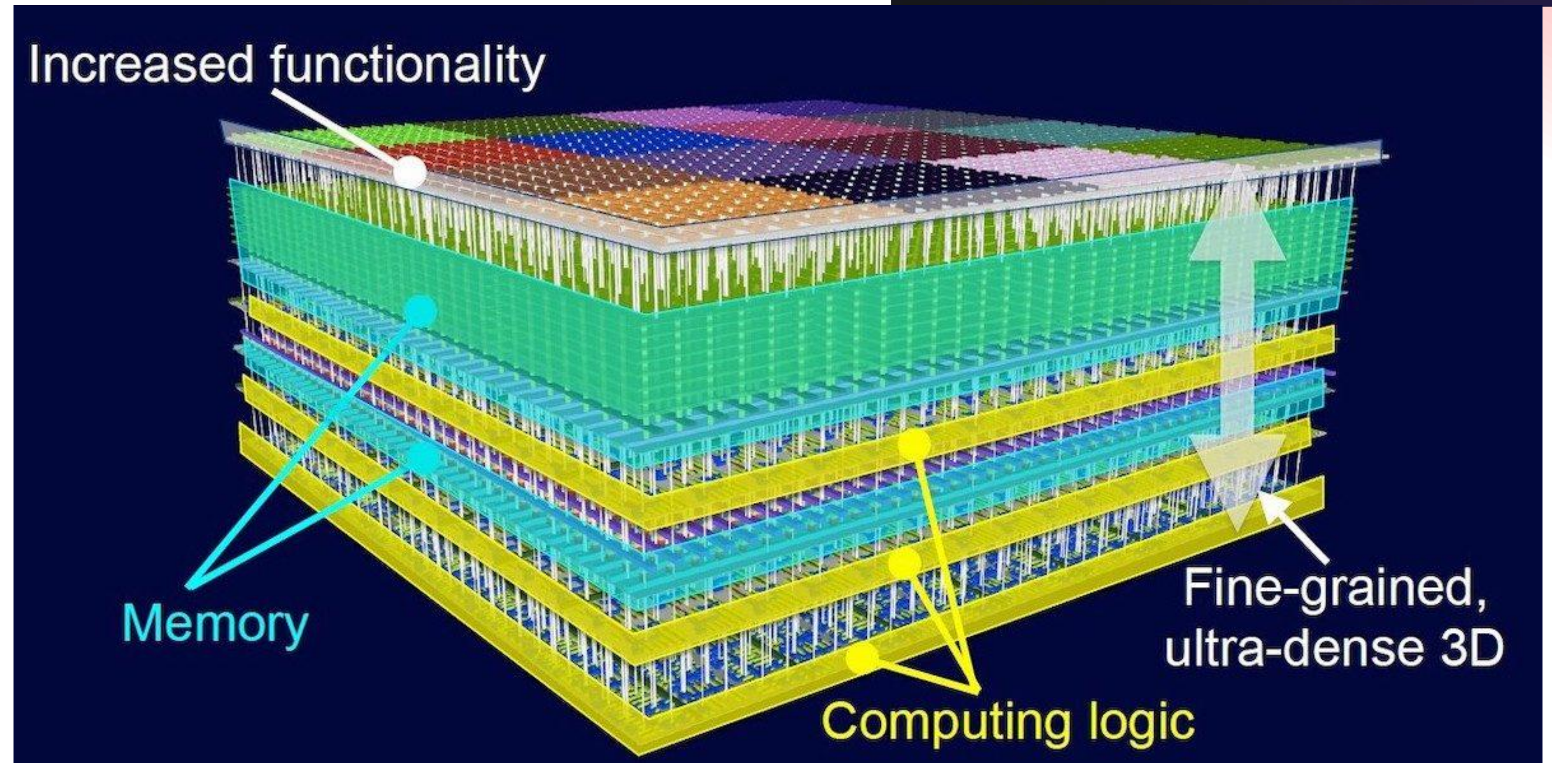
AP Elements: Wiring (Metallization)

- Wire length controls the delay
  - Span of control
- Accounts for majority of power usage
  - Memory fetch







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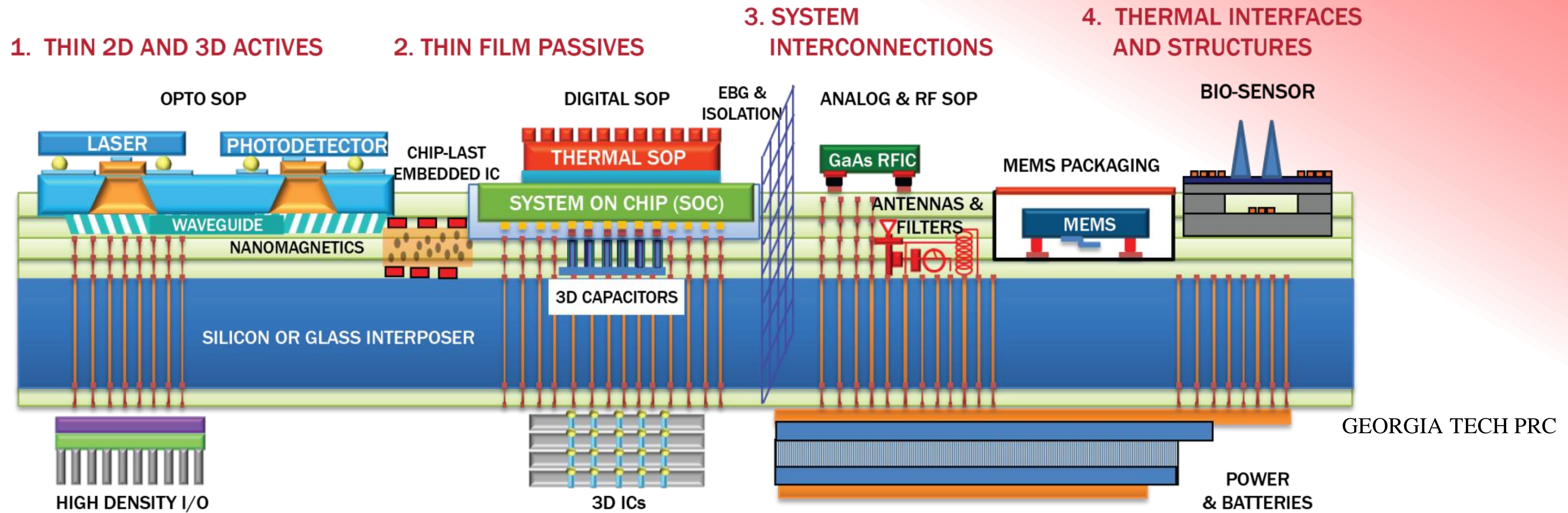
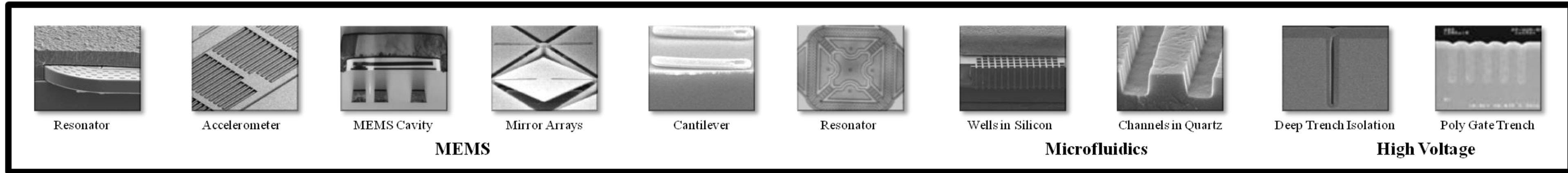
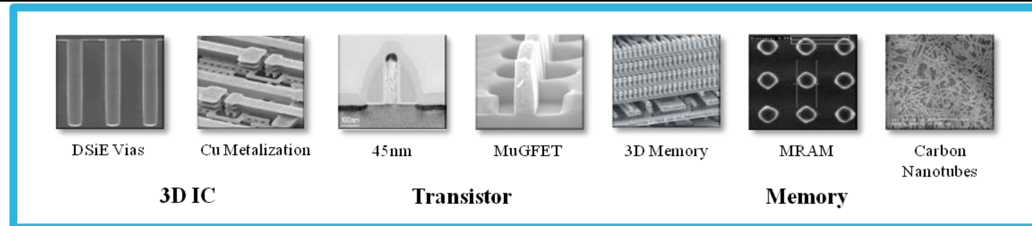
3DInCities

More Than Moore Technologies

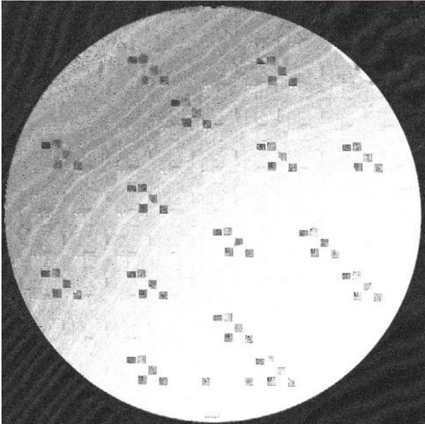


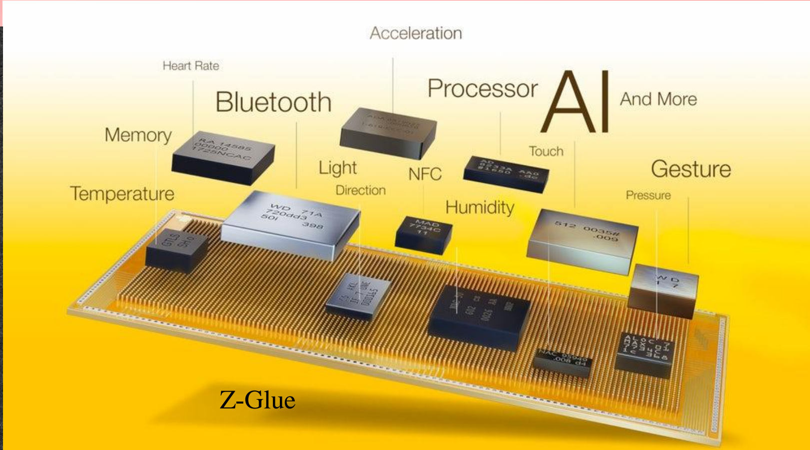




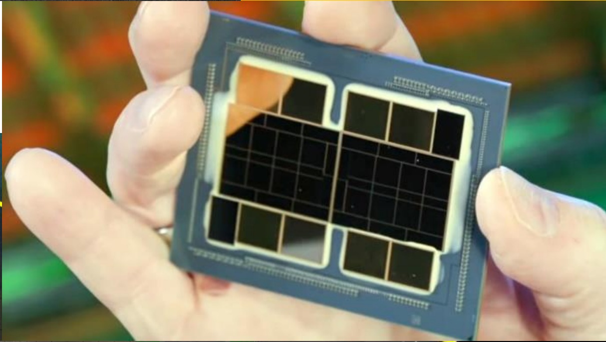
AP Components: Chiplets

- Best of Class Everything
- Easy retargeting
- Lower risk
- IP reuse
- Lower cost

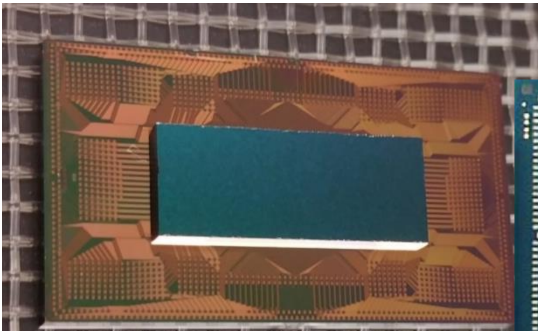


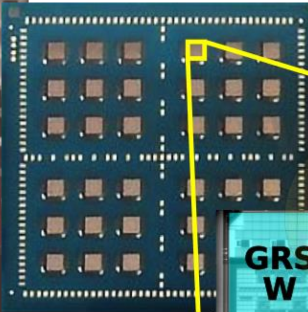


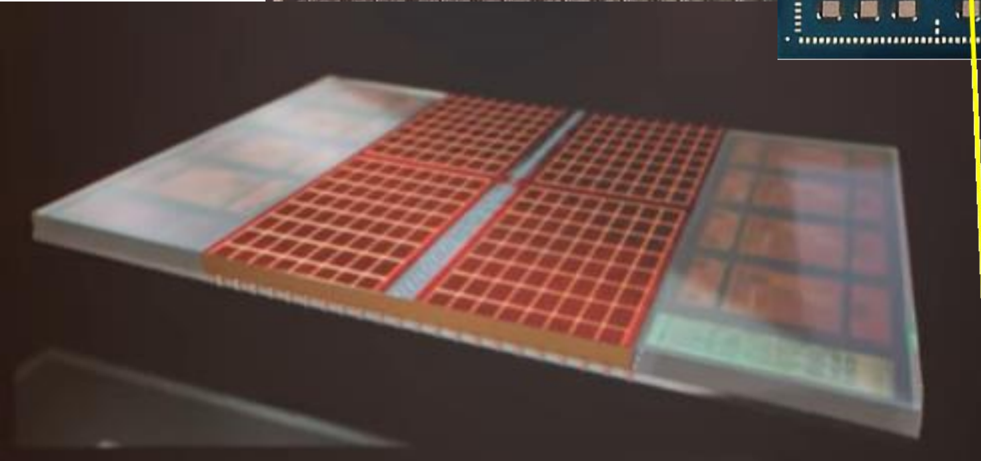
Z-Glue



Intel







AMD

nVidia

Intel

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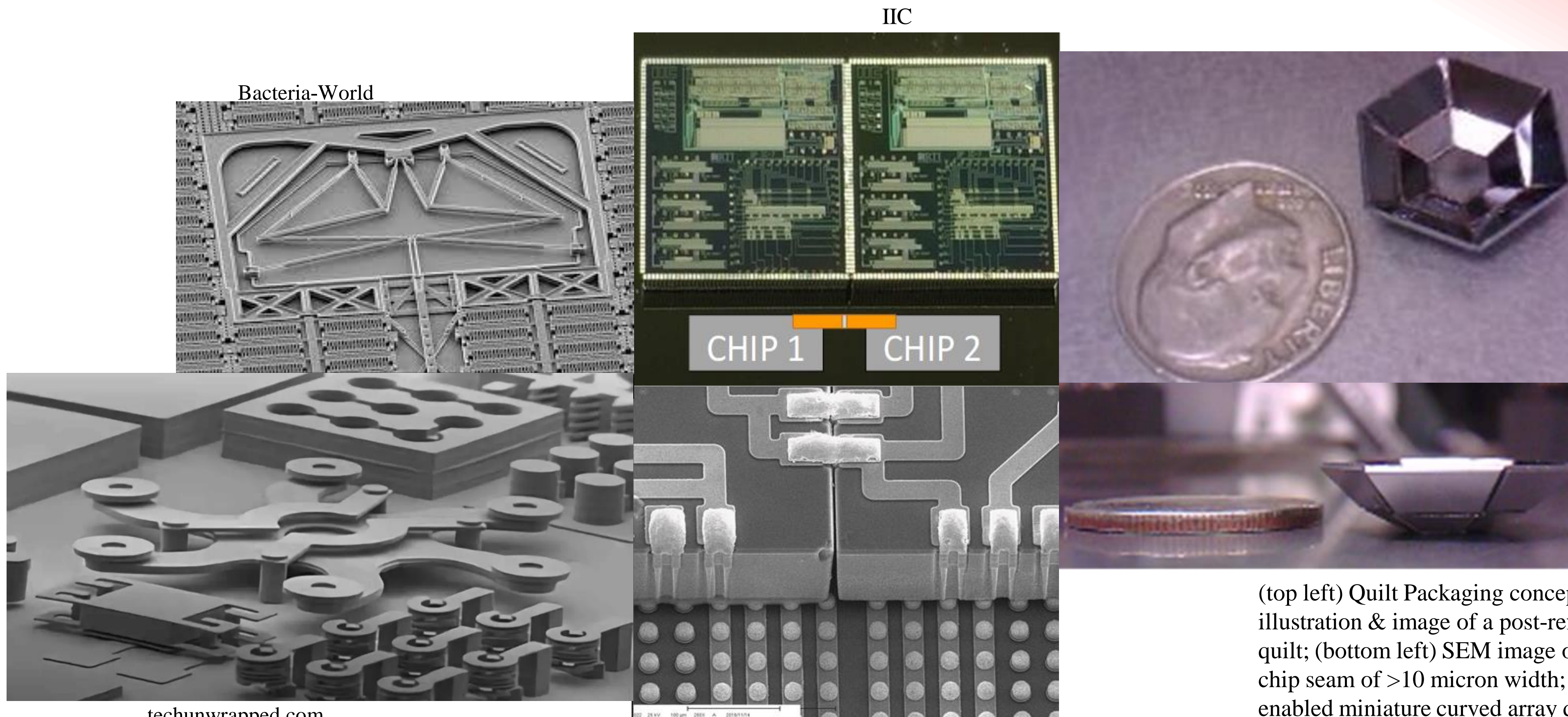
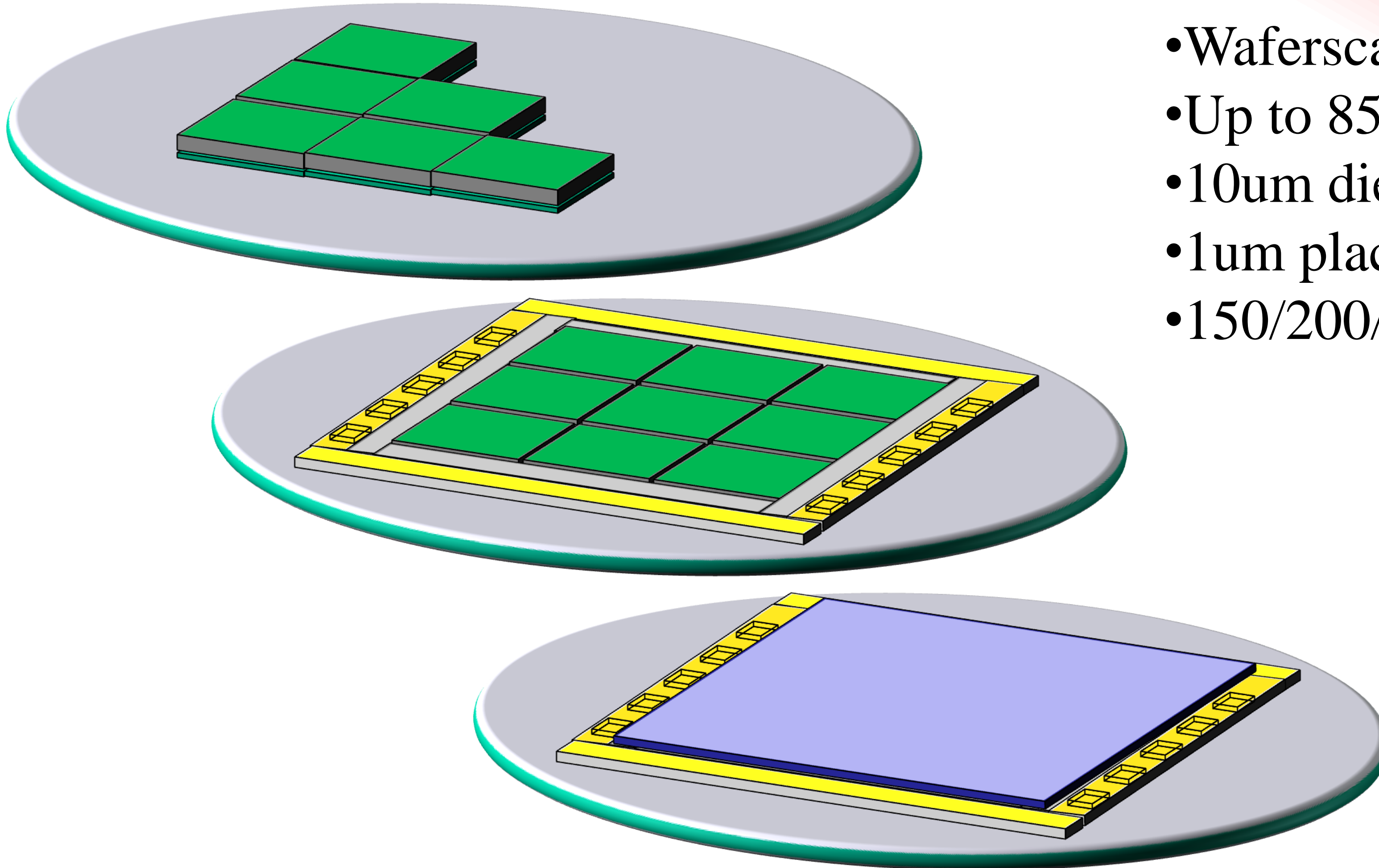
AP Components Micro-Connections and 3D Structures

MEMS + Precision Electronics



(top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

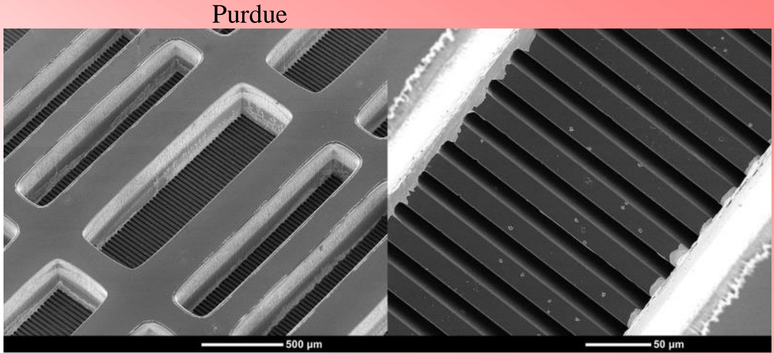
Wafer-scale Mosaic FPAs



- Waferscale integration
- Up to 85 die assembly
- 10um die space
- 1um placement
- 150/200/300mm

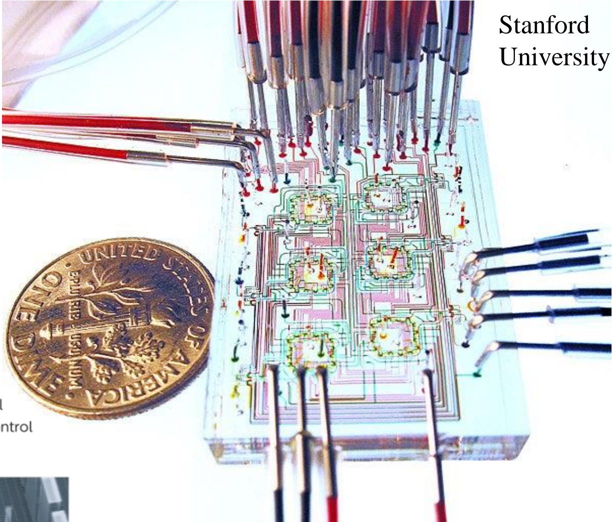
NHANCED SEMICONDUCTORS

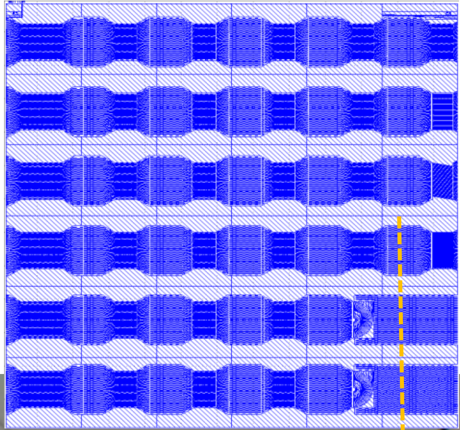
AP Components: Microfluidics and Cooling

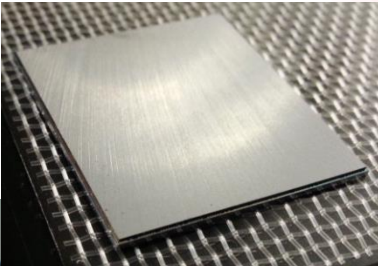


Chip Scale Cooling
For Ultra-Dense Electronics

Biology + Electronics

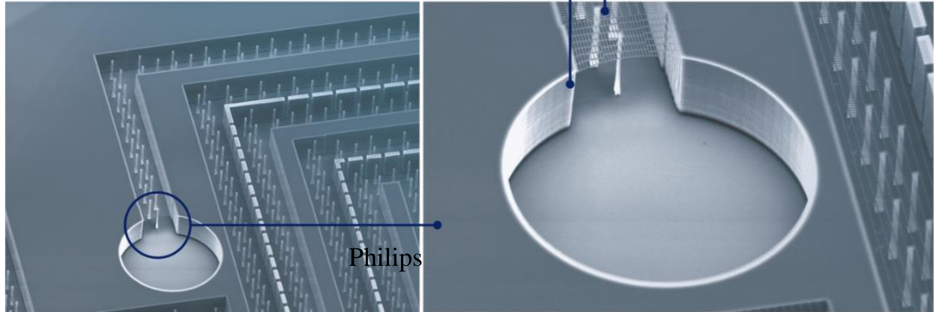






Our state-of-the-art tool set enables us to create microfluidic structures with accurate control:

- <5 degree slope control
- Sub-µm feature size control
- µm range feature size



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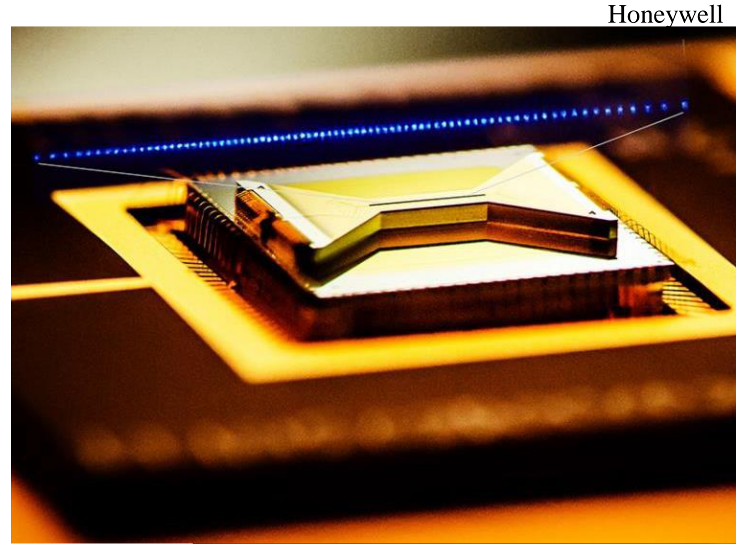
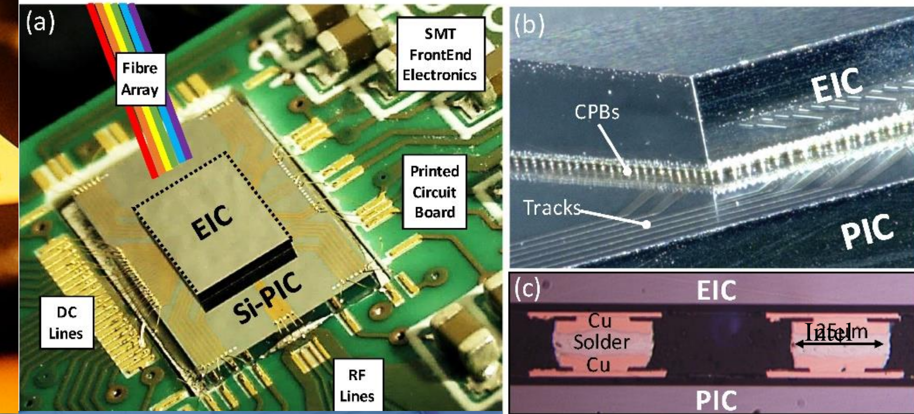
AP Components: Photonics & Quantum

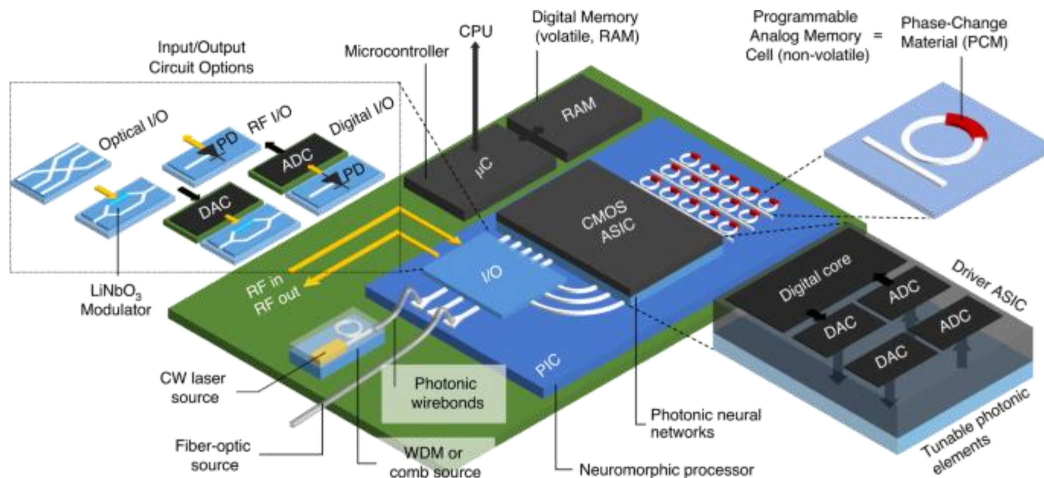
- I/O
  - Tb/s, <<100fJ/b
    - SiP 500ff I/O Load
    - 2.5D 25ff I/O Load
    - 3D 3ff I/O Load
- Processing
  - "Quantum Leaps"

Honeywell

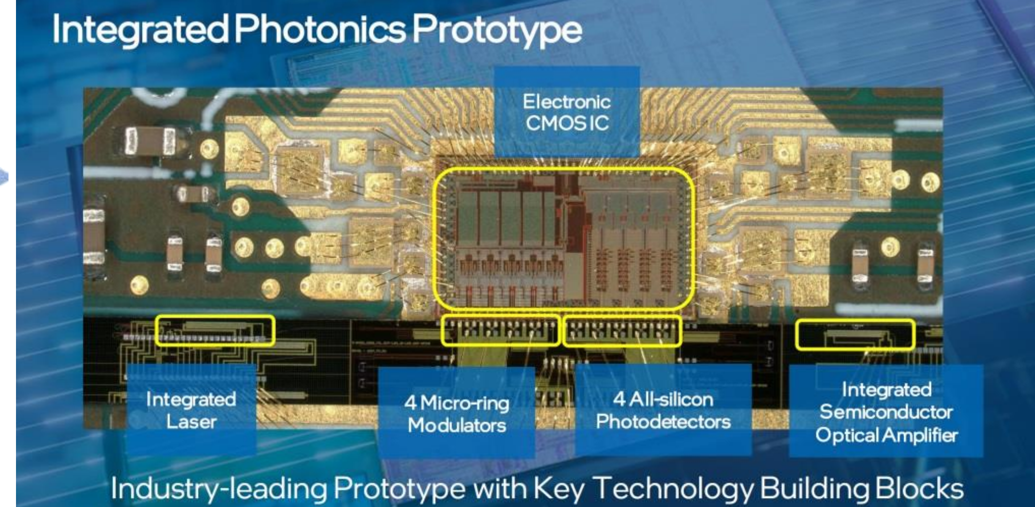


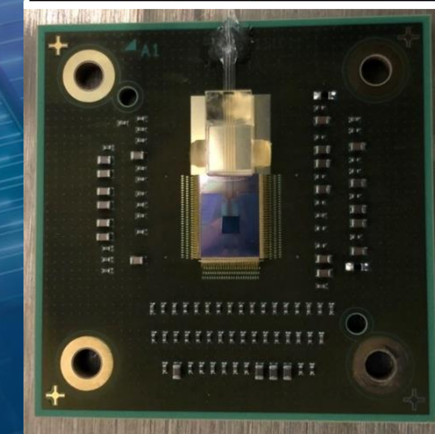
Tyndall National Institute Carroll et al





Nature 29 January 2021 Shastri

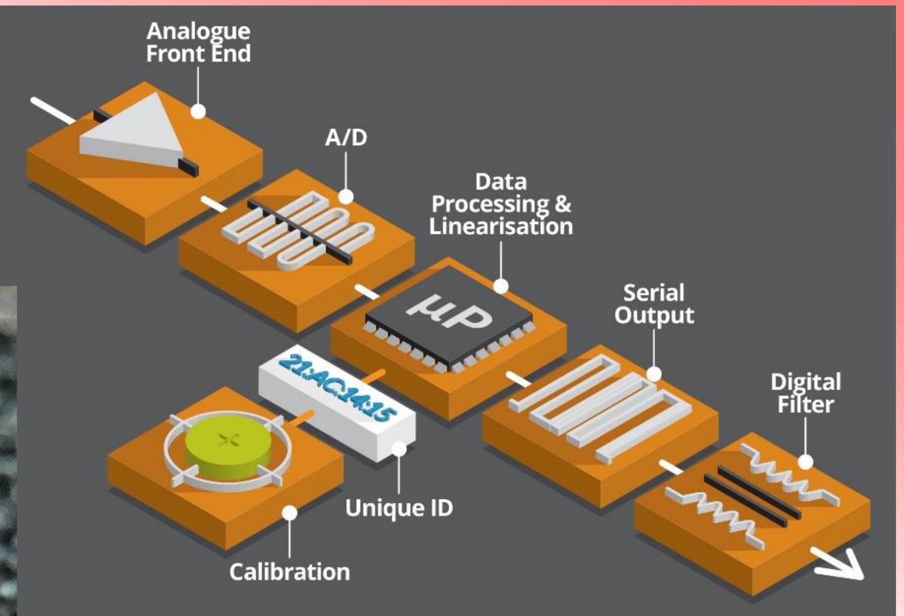




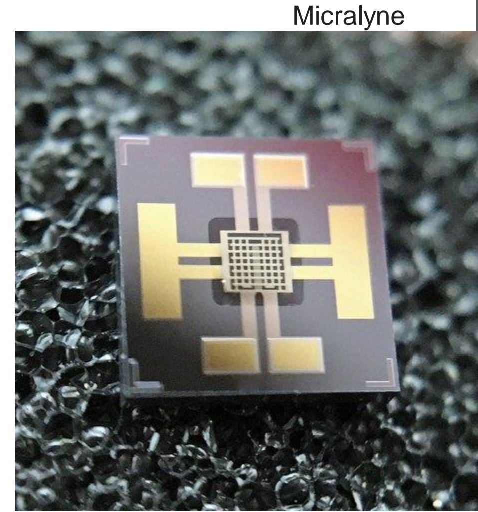
NHANCED SEMICONDUCTORS

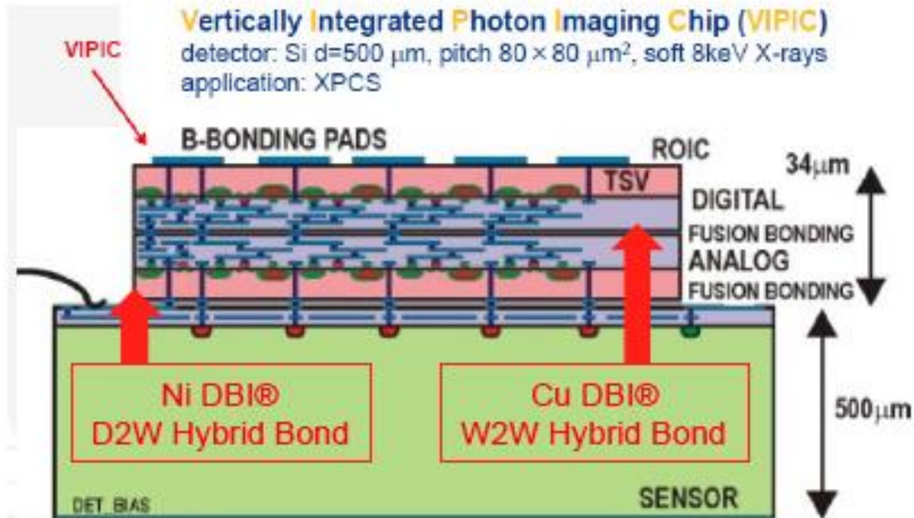
Intelligent Sensors and Edge Compute

- Communication is limited
  - Data movement costs power
  - Data movement costs time
  - Data movement costs money
  - You can't aways "phone-home"

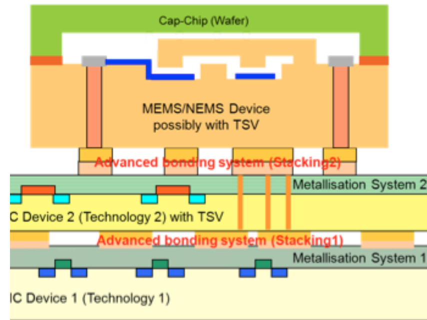


tek-troniks

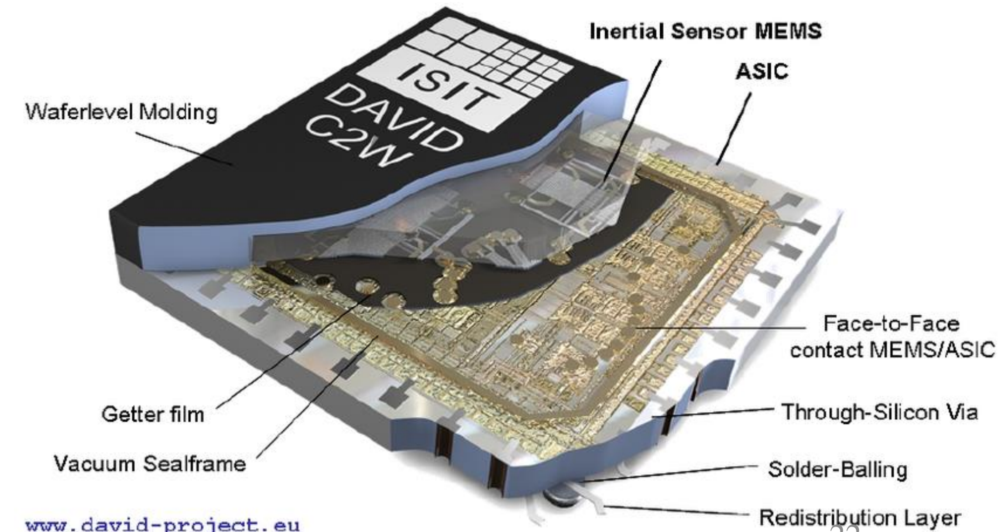
Micralyne




FermiLab



3DinCites

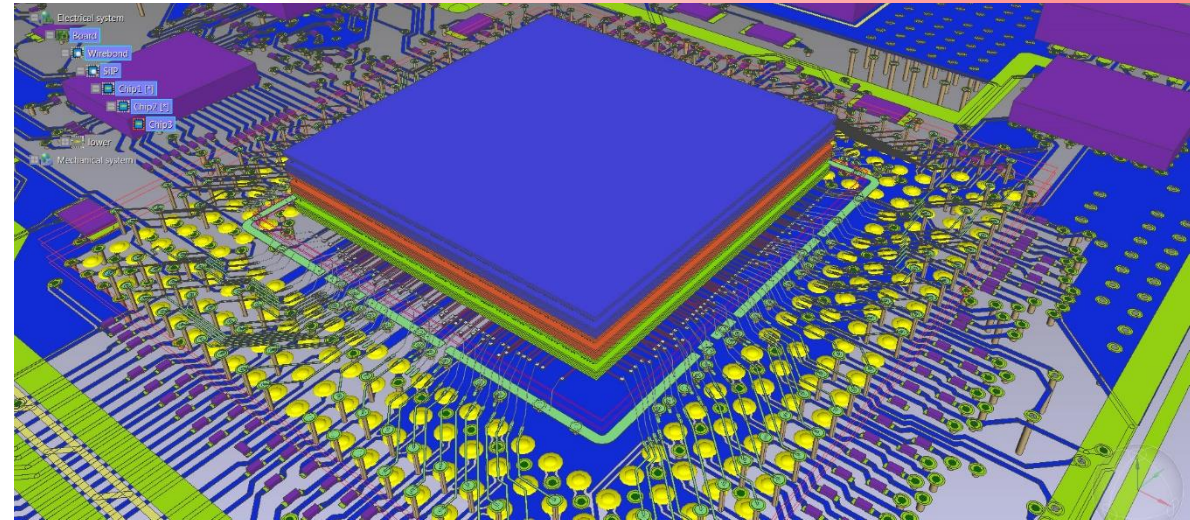


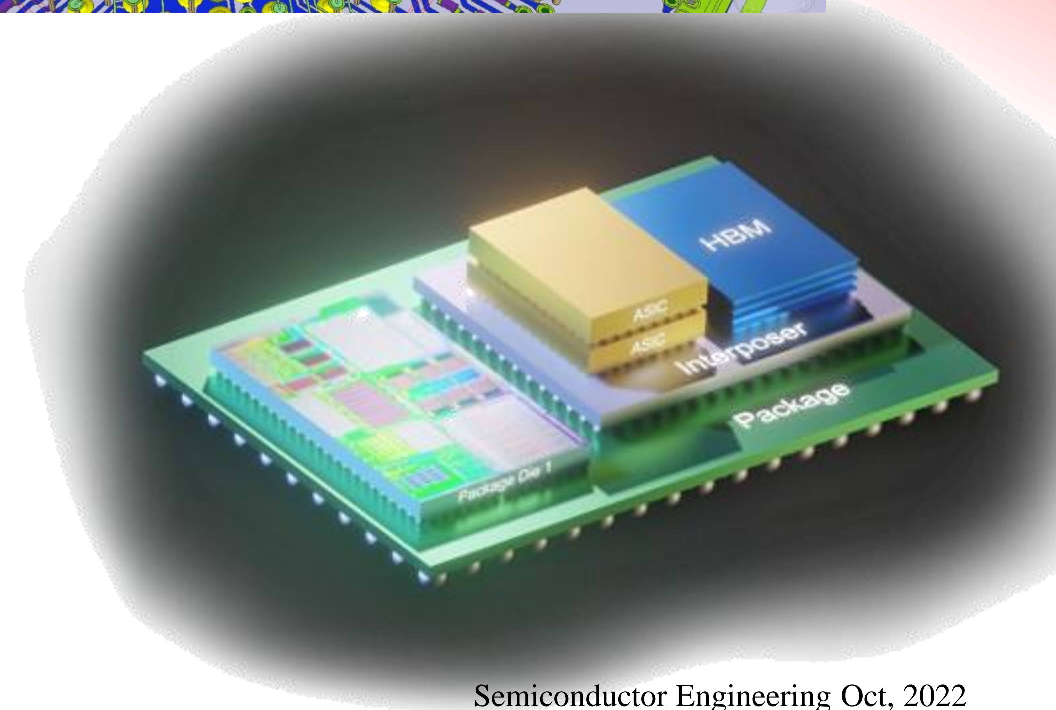
NHANCED SEMICONDUCTORS

Co-Design and Multi-Physics

- Multi-Dimensional Tools
  - Scale
    - Nanometers to centimeters
  - Electrical
    - Power
    - Signal Integrity
  - Heat
  - Mechanical
    - CTE
    - Modulus
  - Cost
  - Photonics
  - MEMS
  - Liquids

Zuken



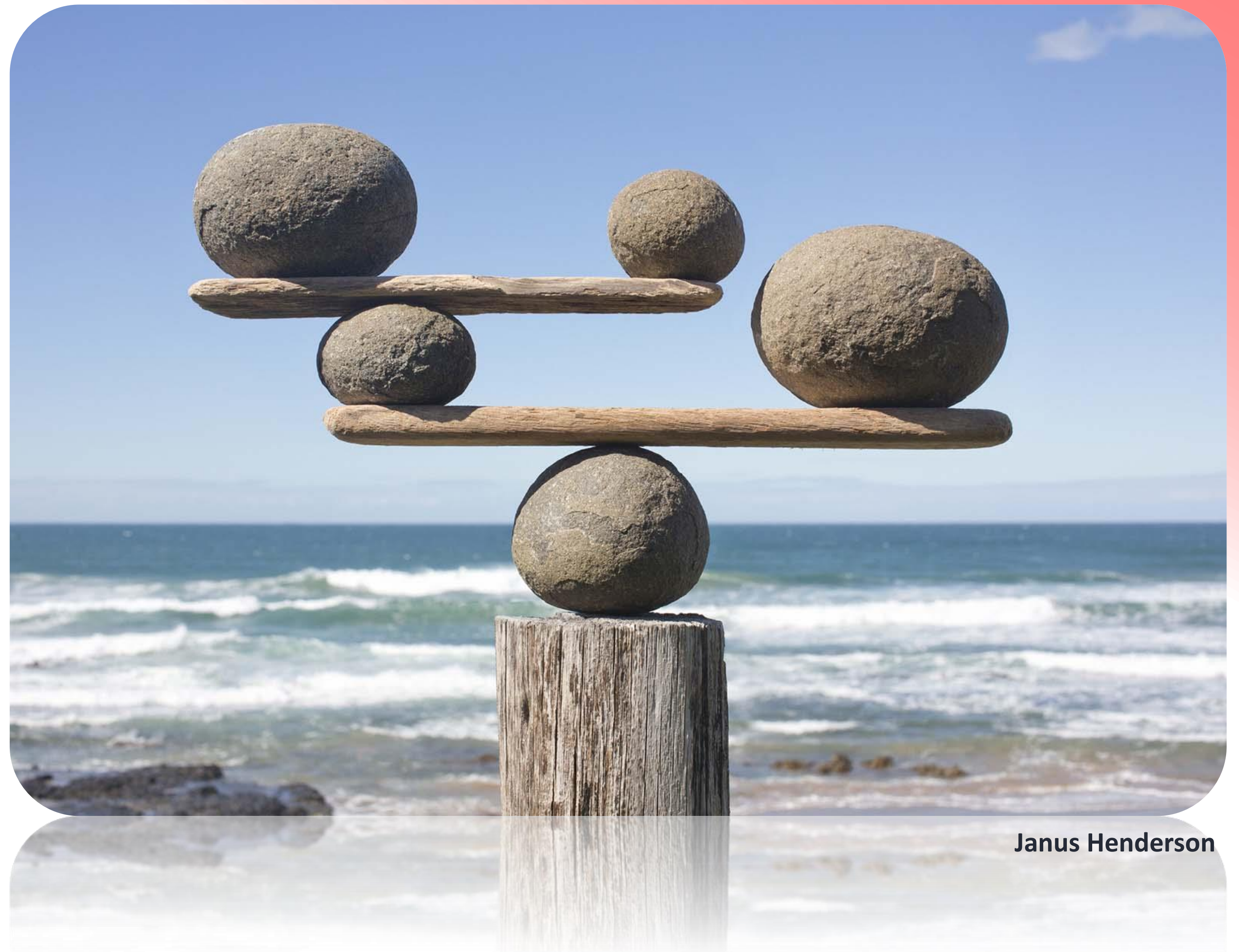


Semiconductor Engineering Oct, 2022

NHANCED SEMICONDUCTORS

The Balancing Act

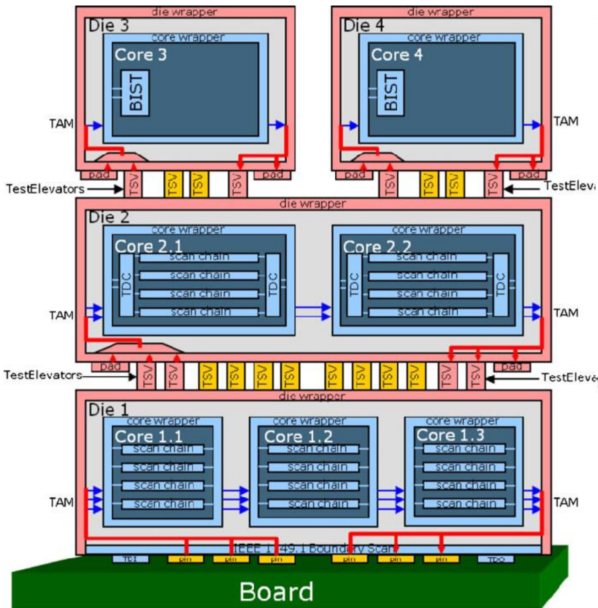
- Process
- Voltage, I/R Drop
- Temperature Sensitivity
- Power Dissipation
  - Cooling
- The more unique materials, - the greater the complexity
  - CTE



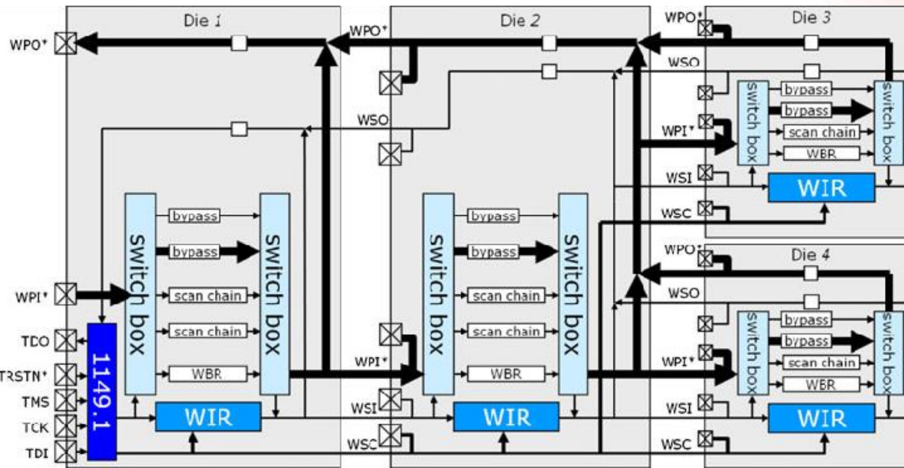
Janus Henderson

Addressing Rel/Qual with DFT + 2.5/3D PCM

Images from: A DfT Architecture for 3D-SICs Based on a Standardizable Die Wrapper; Erik Jan Marinissen et al



Physical



Logical

IEEE 1500 is well defined 2.5/3D DFT starting point building on 1394 standard. Plan is to add 1149.4 analog features targeting device manufacturing integrity.

Augmented JTAG based on IEEE 1500: Add alignment sensing, 3D interconnect R/C measurement, power, temperature, perhaps DARPA SHIELD like items… Being work by NEPP task group with others (NRO, AFRL, Honeywell, Tezzaron, Novati,...) Objective is to “prove” specific device quality and improve reliability data.

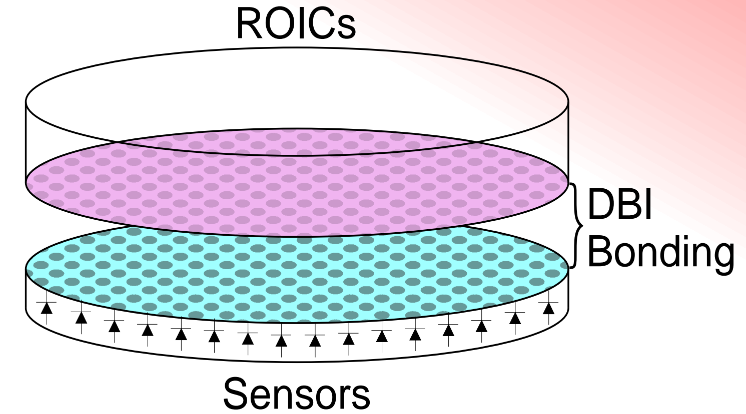
NHANCED SEMICONDUCTORS

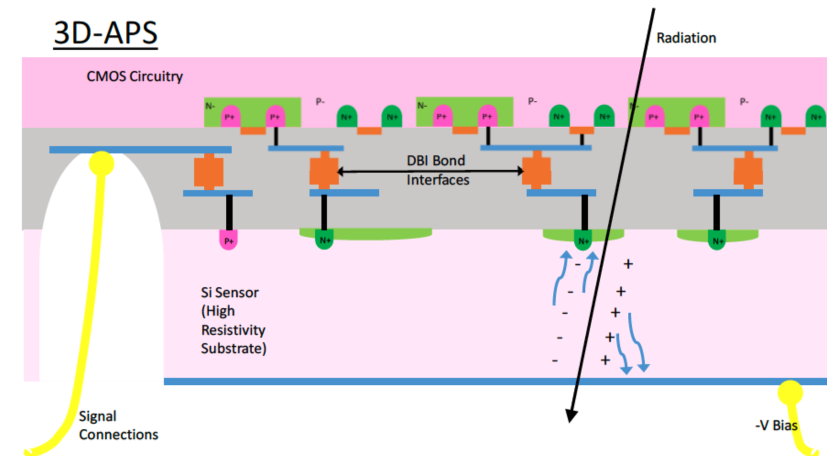
Background: 3D-AHD Development

Sensor tier:
Physical implementation
Fabricated at NHanced on high resistivity silicon wafer.
Thinned down to 100um to 20um at NHanced.

ROIC tier:
Proof of concept and designed by NHanced and Fermilab
Physical implementation
Fabricated with RHBD

3D-AHD detector:
Final integration at NHanced fab





NHANCED SEMICONDUCTORS

Induced current – Simple example – X-rays

The current pulse reflects charge motion deep in the detector

Data from 3dPixel_2m_400.log

Current #1 (A)
Current #4 (A)
Current #5 (A)

Central pixel

Initial Current Spike

Edge neighbor (diffusion collected charge)

Corner neighbor 0 collected charge

Y-axis: -2×10^{-06}, 0, 2×10^{-06}, 4×10^{-06}, 6×10^{-06}, 8×10^{-06}, 1×10^{-05}, 1.2×10^{-05}, 1.4×10^{-05}

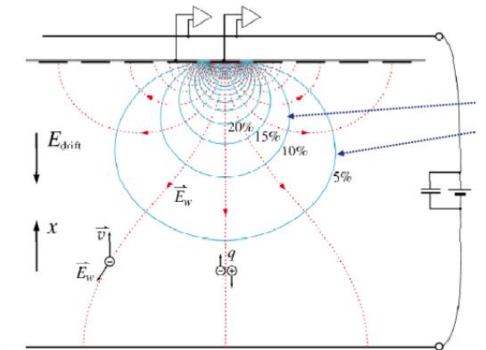
X-axis: 0, 1×10^{-09}, 2×10^{-09}, 3×10^{-09}, 4×10^{-09}, 5×10^{-09}, 6×10^{-09}, 7×10^{-09}

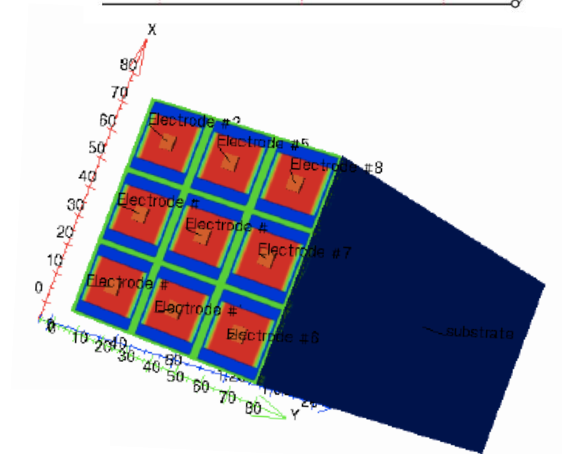
Ramo's theorem

$$i = -q\vec{E}_w \times \vec{v}$$

$$Q_s = \int i\,dt = q\int \vec{E}_w d\vec{x}$$

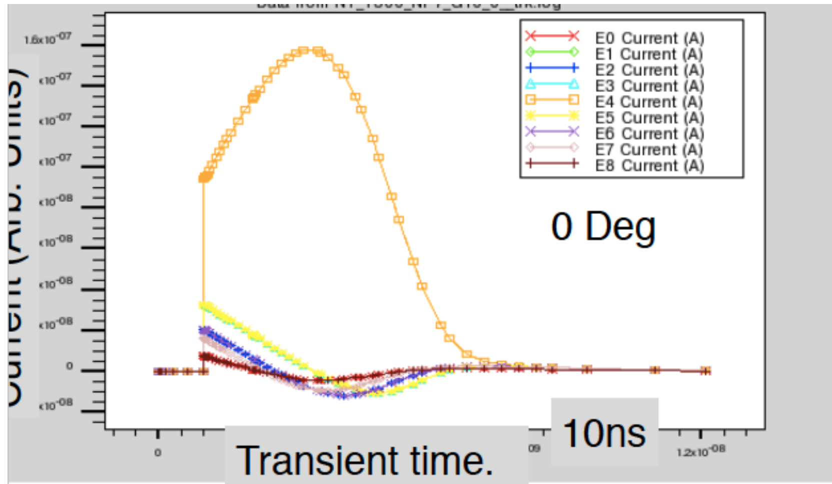
$$Q_{1\to 2} = q(V_{w2} - V_{w1})$$

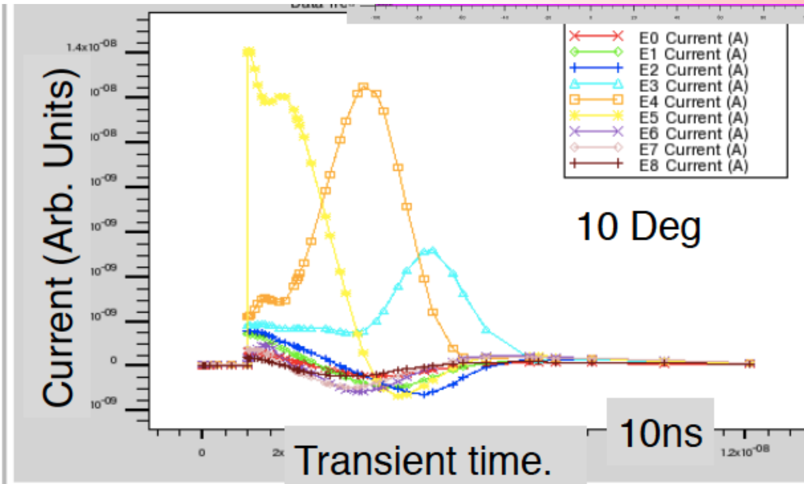


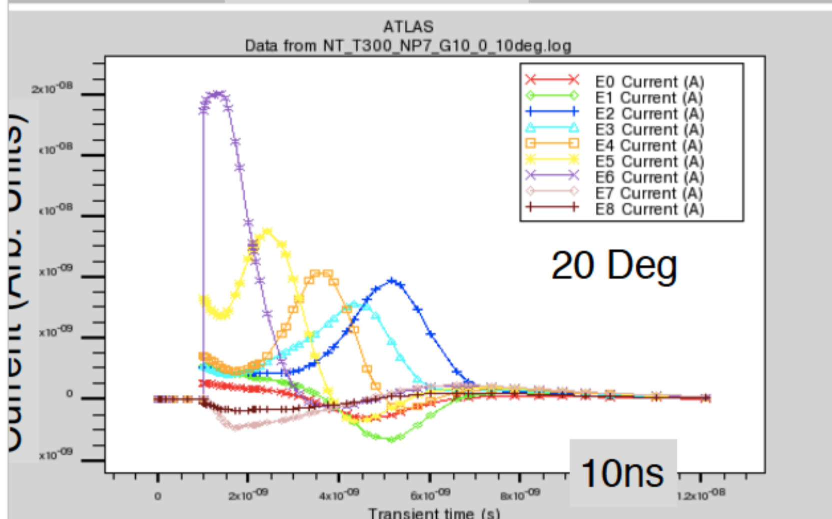


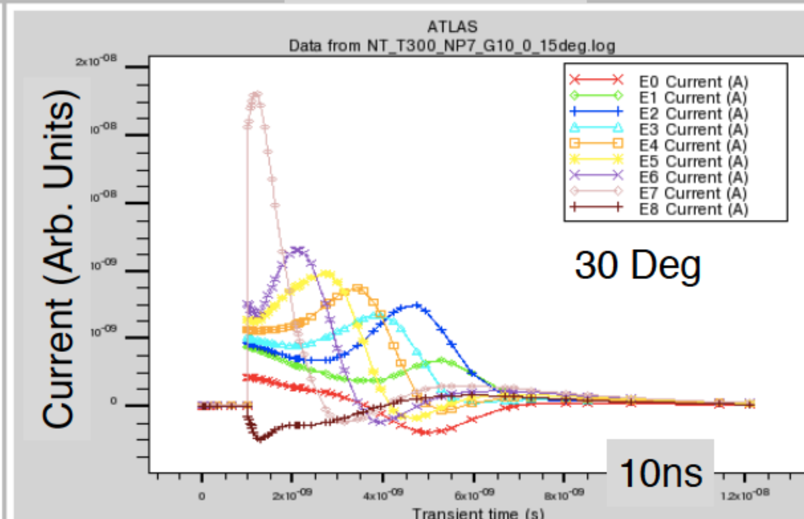
NHANCED SEMICONDUCTORS

Induced current - MIPs at various angles:









Ron Lipton
FermiLab

NHANCED SEMICONDUCTORS

Summary – The Road Ahead

- System level Moore's Law future
- Advanced Packaging is driving an industry revolution
  - Enablement of Next Generation Semiconductors
- Advanced Packaging has SWaP+++
  - Ultimately driven by economics

NHANCED SEMICONDUCTORS