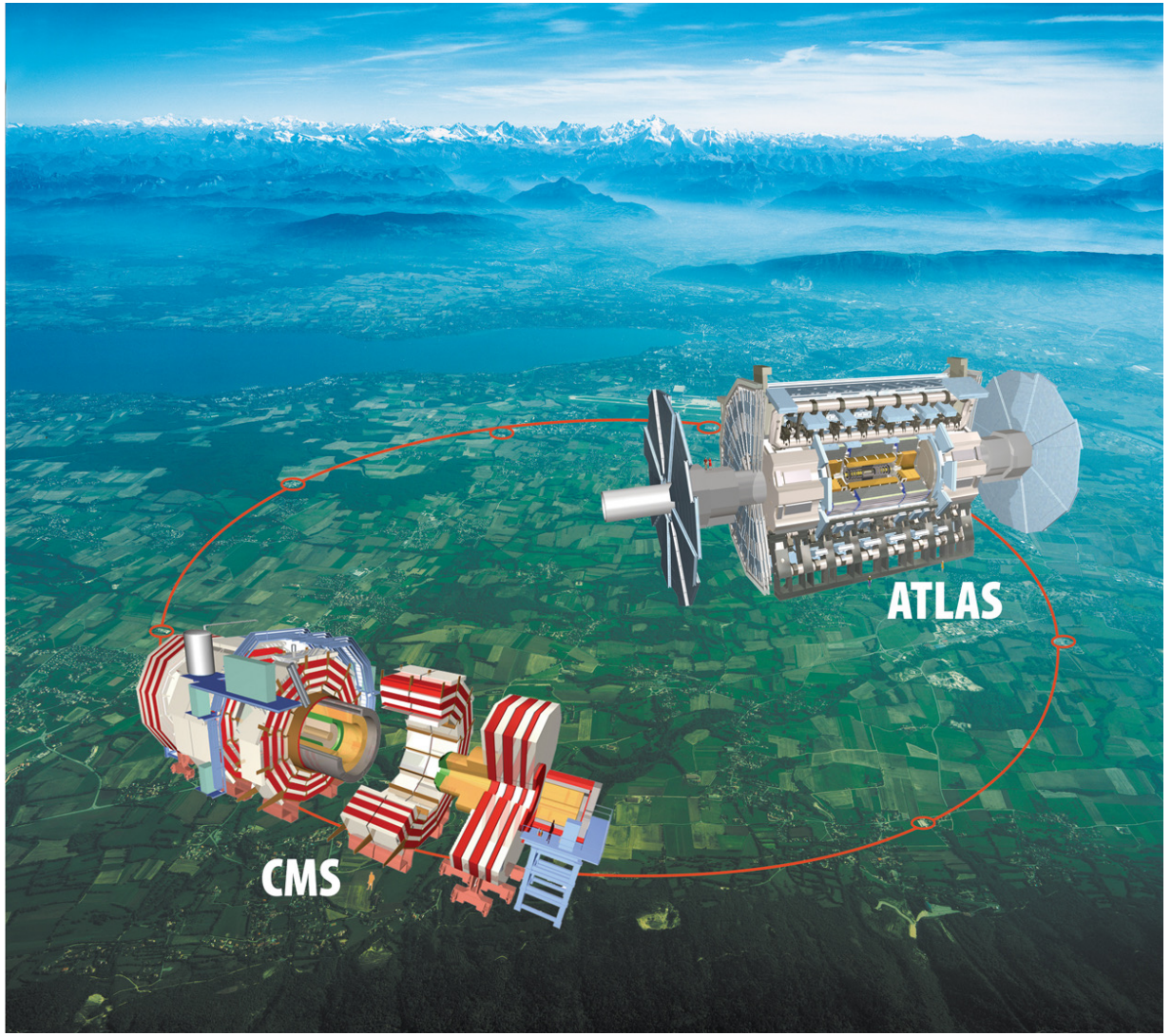
Lab: FPGA-based Track-Trigger for HL-LHC

Context: CMS detector upgrade for HL-LHC

- LHC is 14 TeV proton-proton collider, with two general purpose experiments ATLAS & CMS, famous for Higgs boson discovery.
- "High-Luminosity LHC" is a major upgrade, due to start running in 2029.



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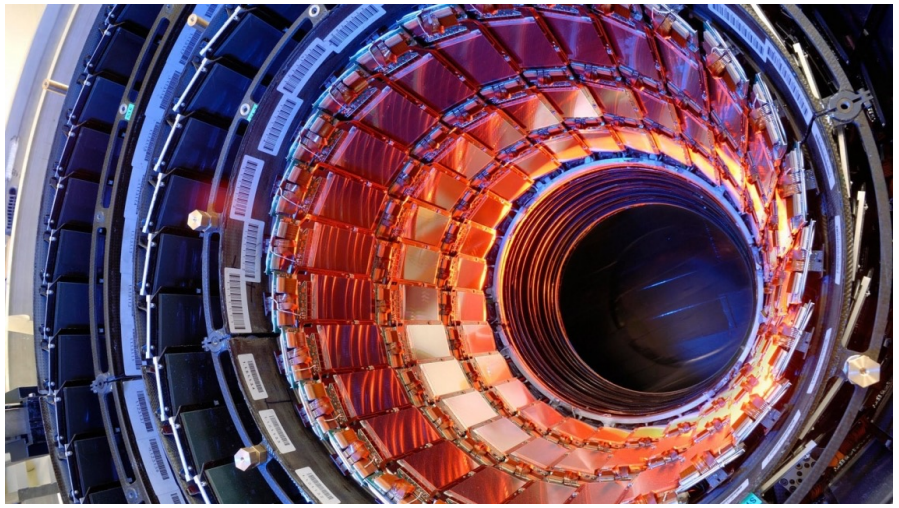
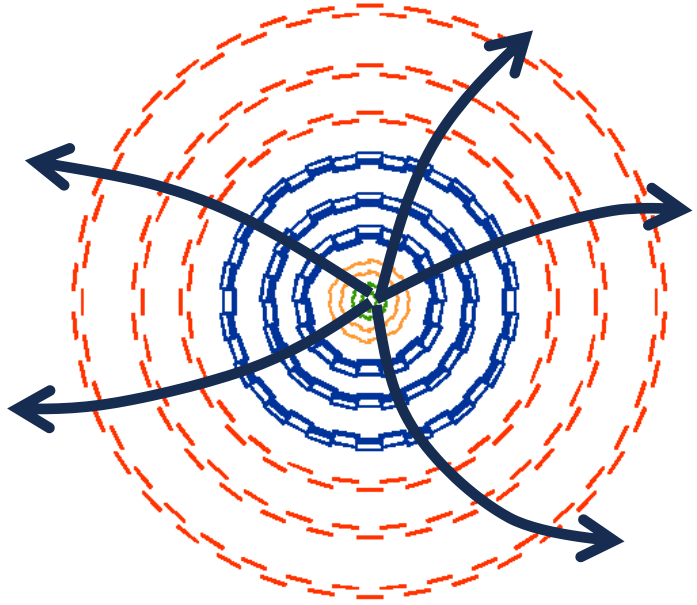
Context: CMS detector upgrade for HL-LHC

- At heart of CMS is Tracker detector, consisting of several cylindrical layers of silicon surrounding p-p collision point.
- Charged particles produced in the p-p collision produce a "hit" as they cross each layer, and these hits are read out by the CMS electronics.
- At HL-LHC aim to reconstruct all particle trajectories (tracks) from hits in < 4μs , so can use to identify the small fraction of p-p collision events that contain interesting physics and are worth writing to disk.
- Very challenging. Must process 1 trillion hits per second. Employ commercial, high-speed programmable, FPGA electronics chips, (widely used in science & industry).





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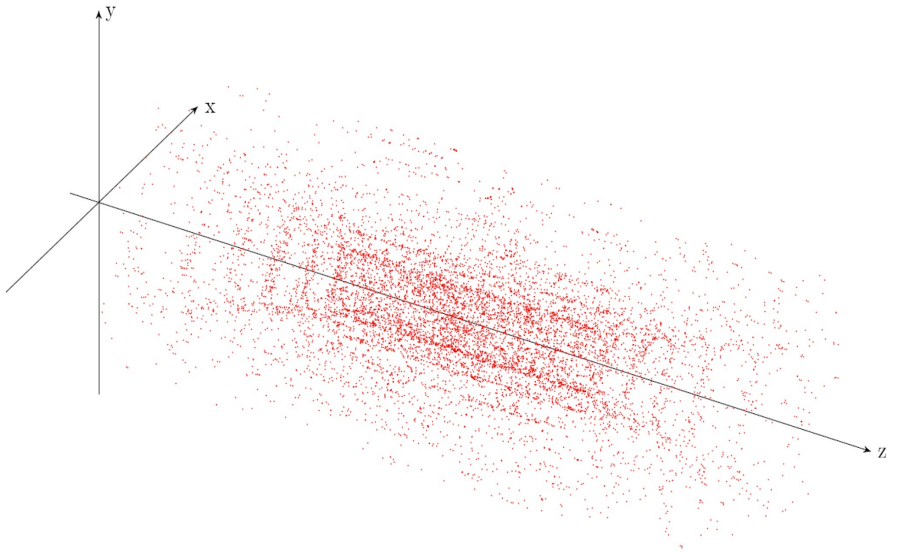
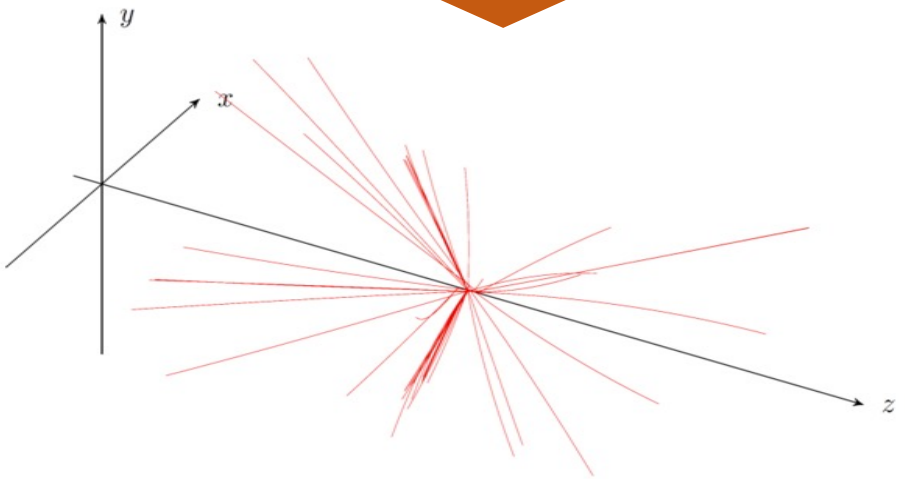
Context: CMS detector upgrade for HL-LHC (≥ 2029)

- Track reconstruction is a game of “join the dots”.
- Each p-p collision event contains ~20k hits in Tracker, produced by thousands of particles.
- Must figure out which of these were produced by the same particle, and so should be used to form a track.
- Has taken CMS physicists several years to develop algorithm!



INFIERI Lab: Track reconstruction in an FPGA.

- Optimise a simple tracking algorithm, based on those used in CMS, implemented in the Vitis-HLS language, and run it in an FPGA.
- Can you find all the tracks? How fast does your algorithm run? Does it make efficient use of FPGA resources?
- 3 hours work by INFIERI student???



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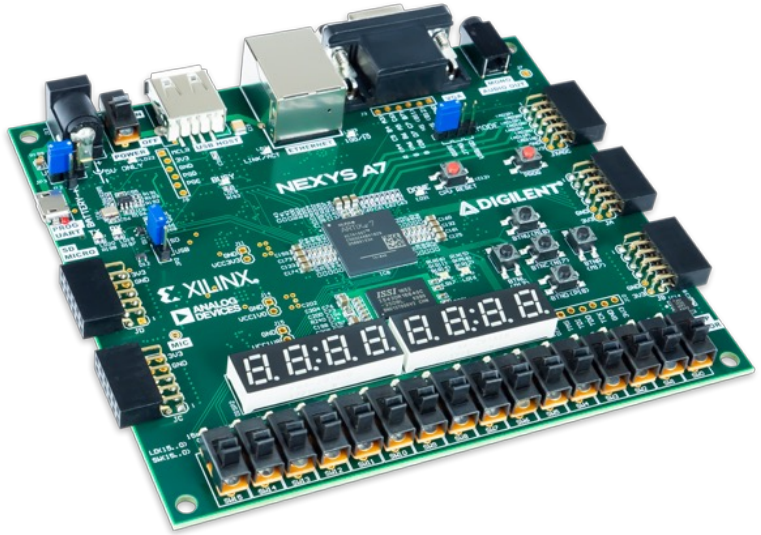
Lab. setup

- Hit data simulated from random particles crossing a multi-layer Tracking detector.
- A Xilinx Artix-7 FPGA on a (commercial) Nexys A7 board will read hits, reconstruct tracks & transmit them over serial link to a Linux computer. It will show the number found on the Nexys A7 LCD display.
- The FPGA algorithm is written in HLS code (+ a little VHDL).
  - You are given a basic algorithm, and asked to understand, optimise & improve it.



Programming skills

- This lab. will give you experience of Vitis-HLS programming of an FPGA & of the Vivado tool for compiling it. No previous experience of these is required. But you should already know C or C++.

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