# The Road Ahead

September 9, 2023

Robert Patti
rpatti@NHanced-semi.com
630-561-6813

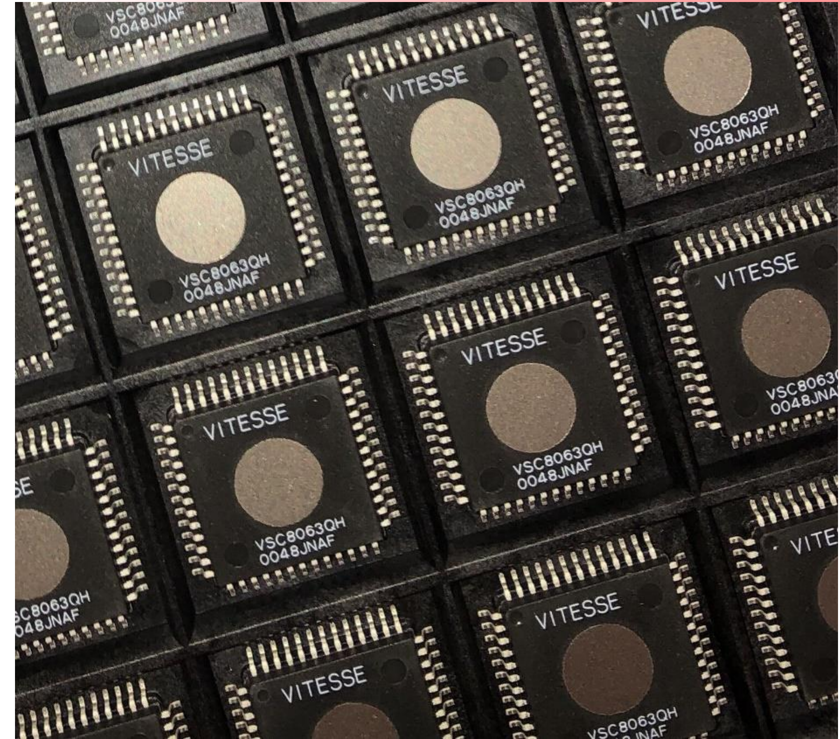
# How It Started…

1988
2,000 gate equivalent
325MHz FF Toggle Rate
~2M Transistors
1.2um 2 metal CMOS Process

NHANCED SEMICONDUCTORS

# We Are Going to Build a 0.8um GaAs 3020!

- 0.8um DCFL
- 2V – Stacked logic
- FF Toggle Rate >2GHz




It failed…

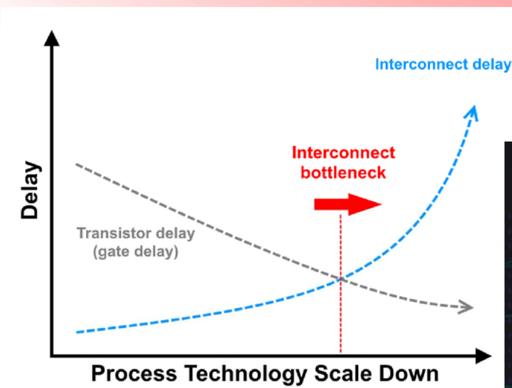
The Xilinx 4000 Series came out and it run faster even though the FF toggle rate was only ~30% of the GaAs.

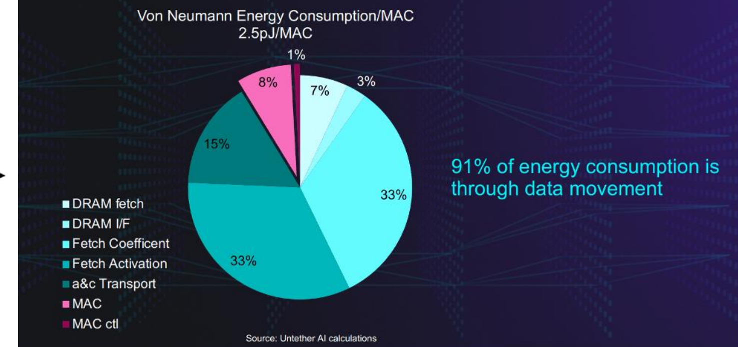
Why?

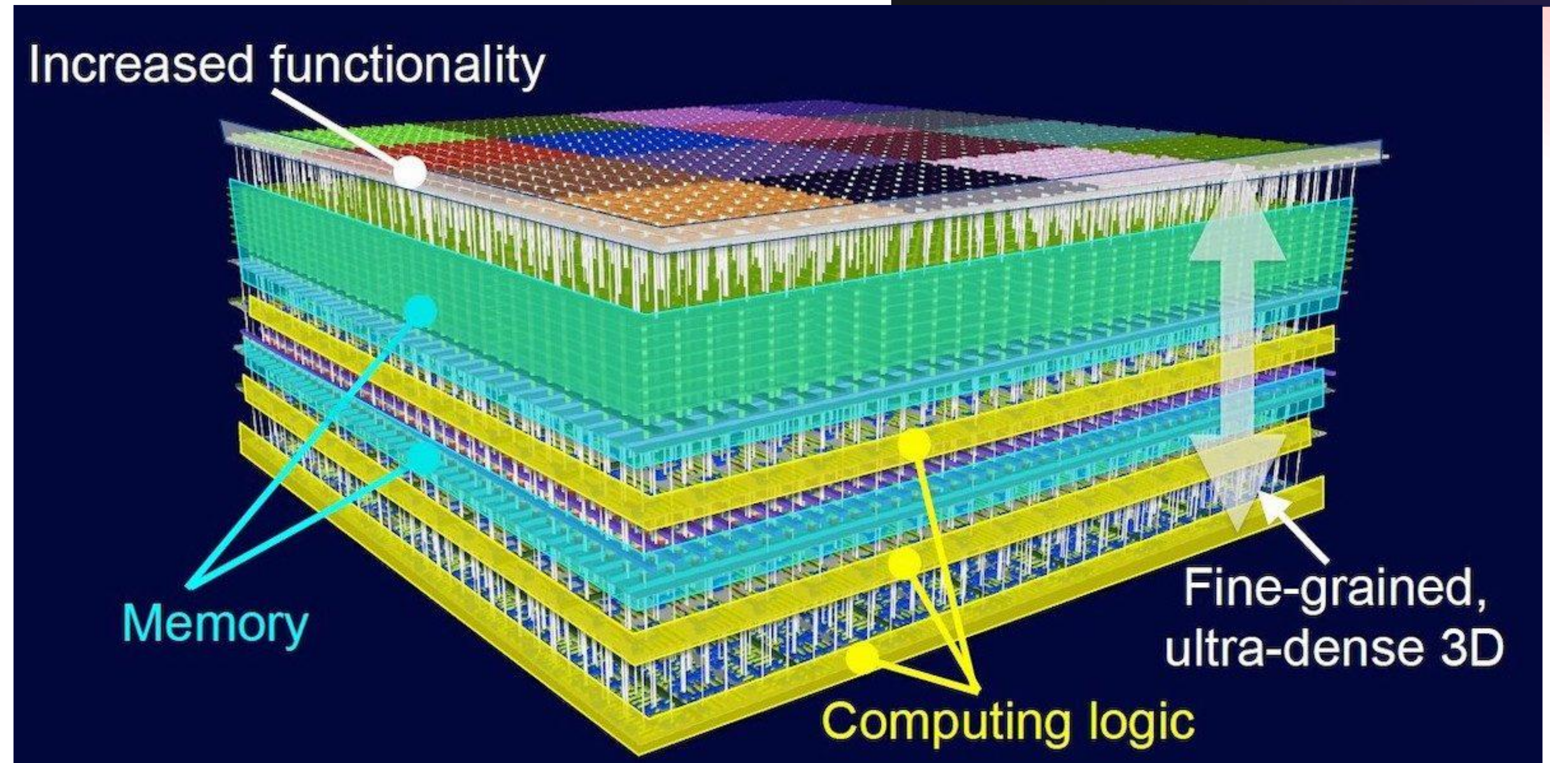
NHANCED SEMICONDUCTORS

# Its All About The Wire

- Wire length controls the delay
  - Span of control
- Accounts for majority of power usage
  - Memory fetch



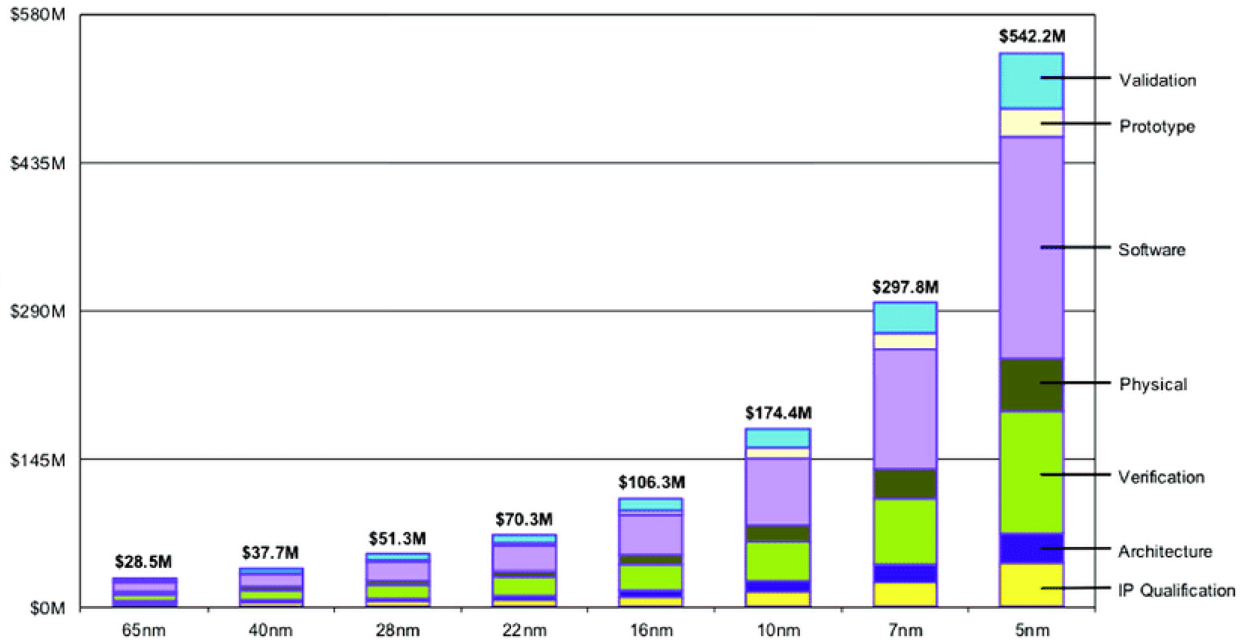





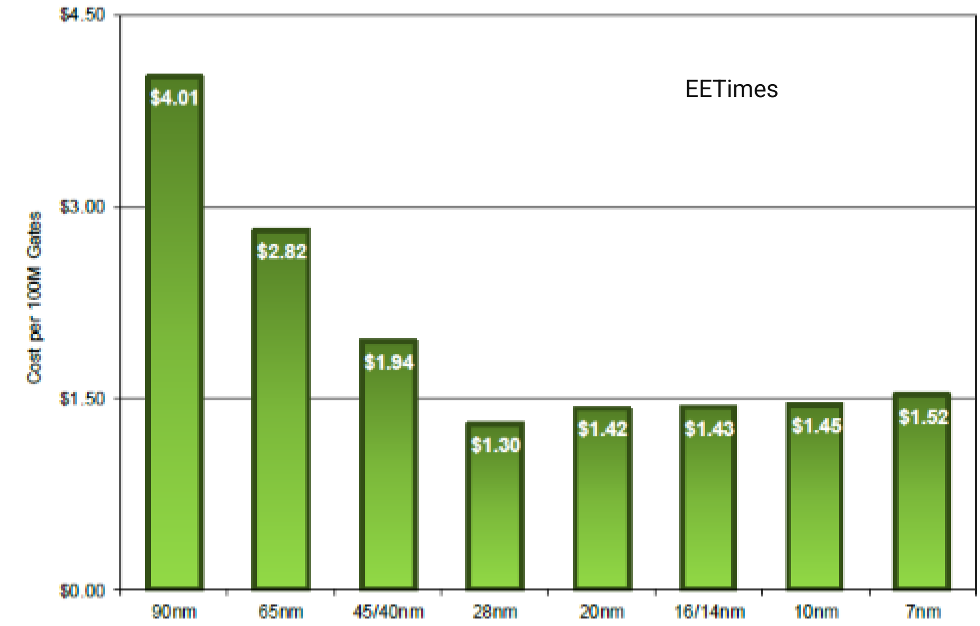

3DInCities

NHANCED SEMICONDUCTORS

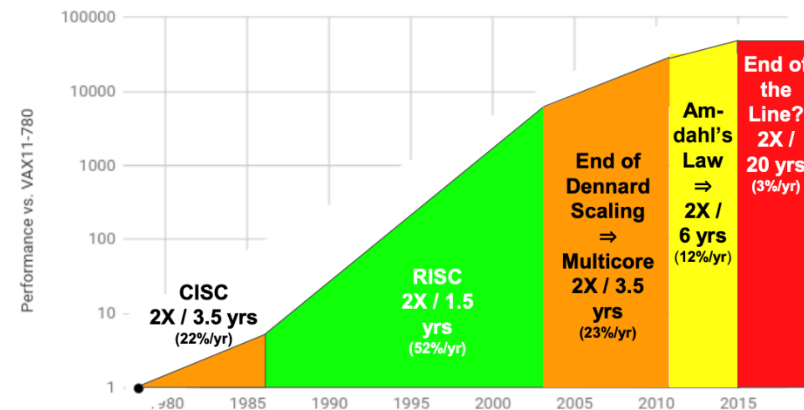
# Moore's Law




Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS




## End of Growth of Single Program Speed?




Apple A12 single thread performance (RISC ISA) = x86 Skylake single thread perf (SPEC), at much lower power, *Anandtech* 10/8/18

# Effective End of Moore's Law

Moore's Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

- This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
- Today we can indeed shrink transistors further, but the cost per transistor no longer declines.

  We can get something a little more compact
  - Perhaps a little less power
  - But we pay more for these features now.

# What Does This Mean?

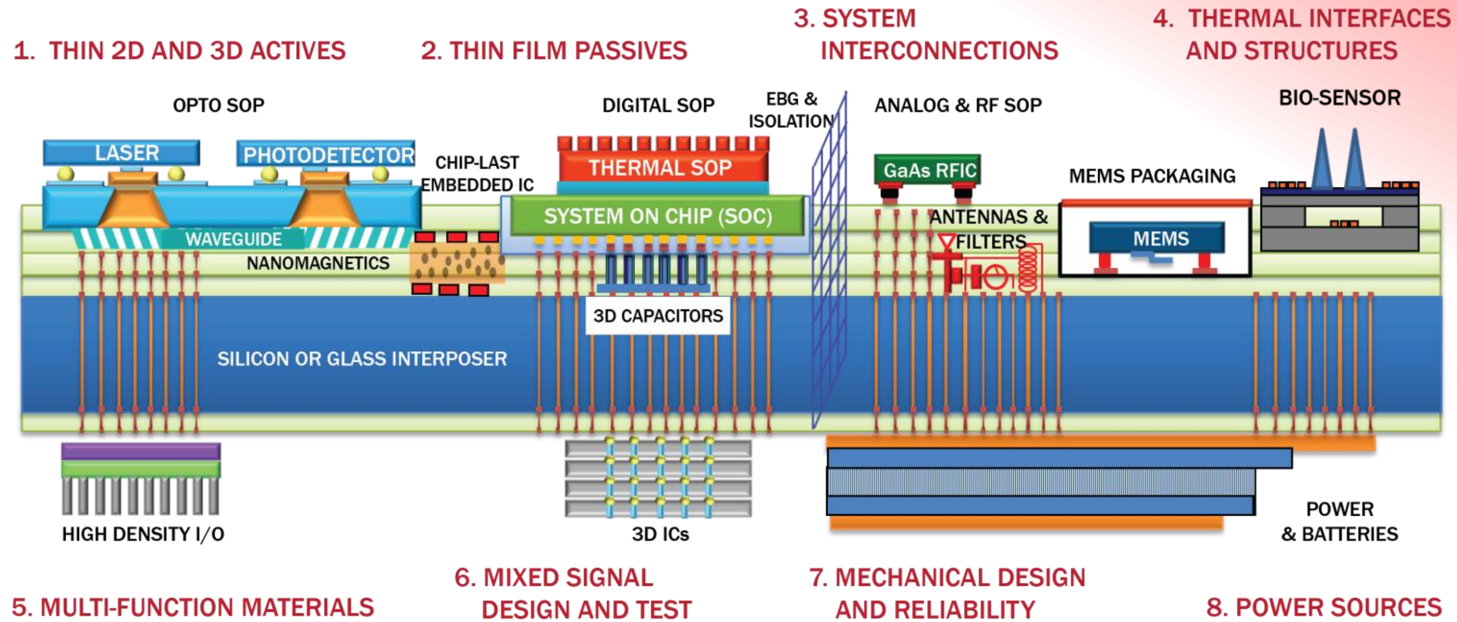
The semiconductor industry is about to undergo a sea change.

- New ways of accomplishing Moore's law economics and performance are needed.
  - The industry is now looking to use advanced packaging to drive future semiconductors.
    - Better Cost
    - Better Performance
    - Better SWaP

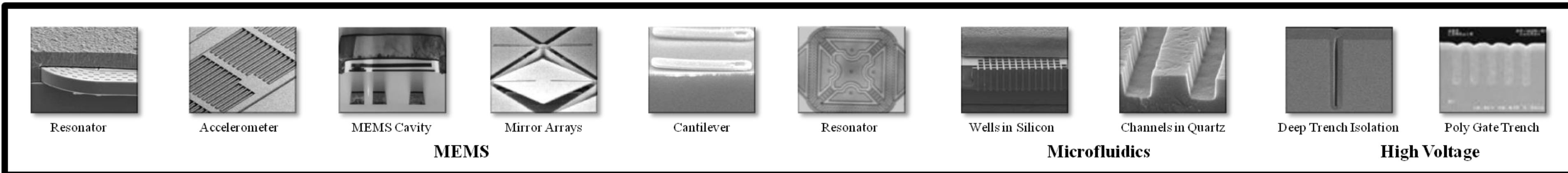
# Internet Of Things

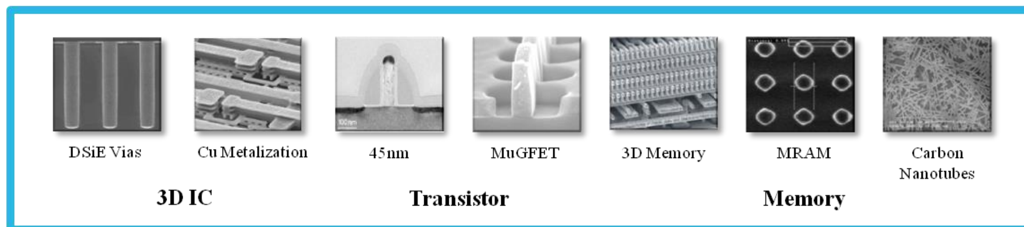
NHANCED SEMICONDUCTORS

# More Than Moore




GEORGIA TECH PRC



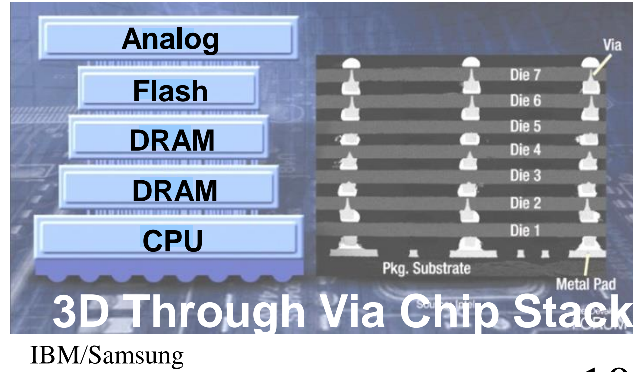




NHANCED SEMICONDUCTORS

# ADVANCED PACKAGING

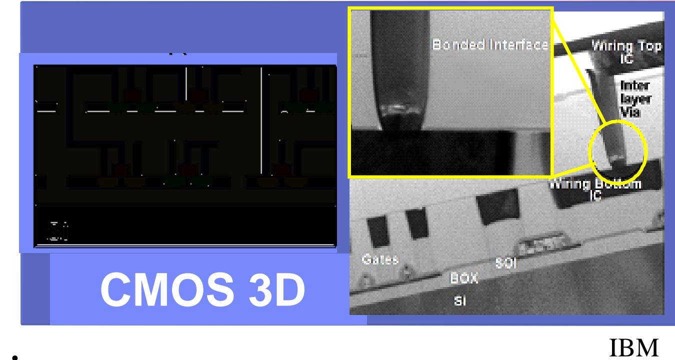
# Span of Advanced Packaging

Packaging




IBM/Samsung

Wafer Fab




IBM

3D-ICs

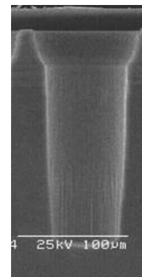
100-1,000,000/sqmm

1000-10M Interconnects/device

1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors



100,000,000s/sqmm

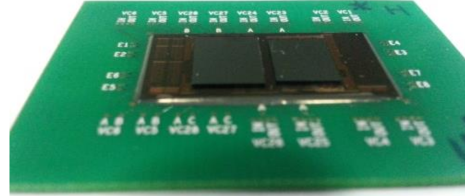
Transistor to Transistor

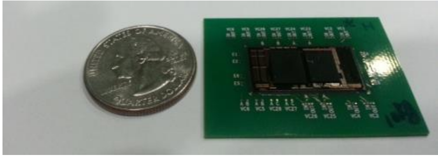
- Ultimate goal

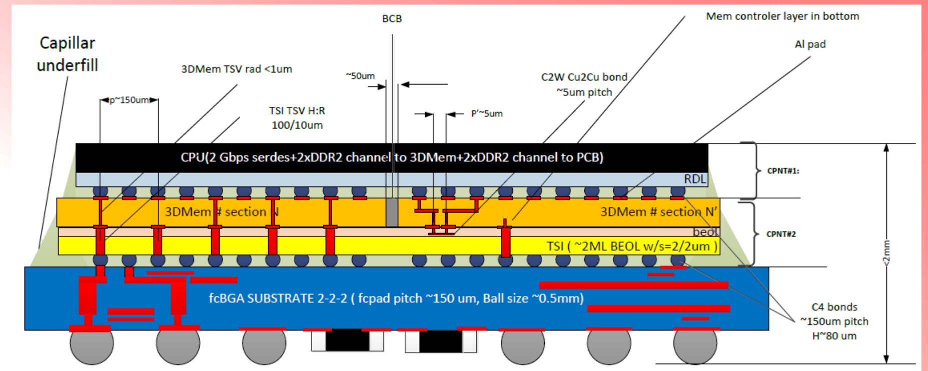
NHANCED SEMICONDUCTORS

# Many Choices!

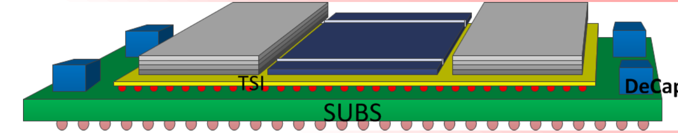
IME A-Star /
Tezzaron
Collaboration








IME A-Star / Tezzaron Collaboration




μBumps

Die to Wafer Cu Thermal Diffusion Bond

C4 Bumps

3 Layer 3D Memory

2 Layer Processor

FPGA (4Xnm)

level#4

level#3

C

Active Silicon Circuit Board

C

level#2

Organic Substrate

level#1

level#0

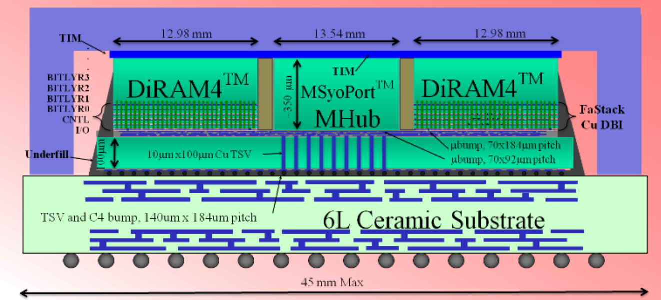
Solder Bumps

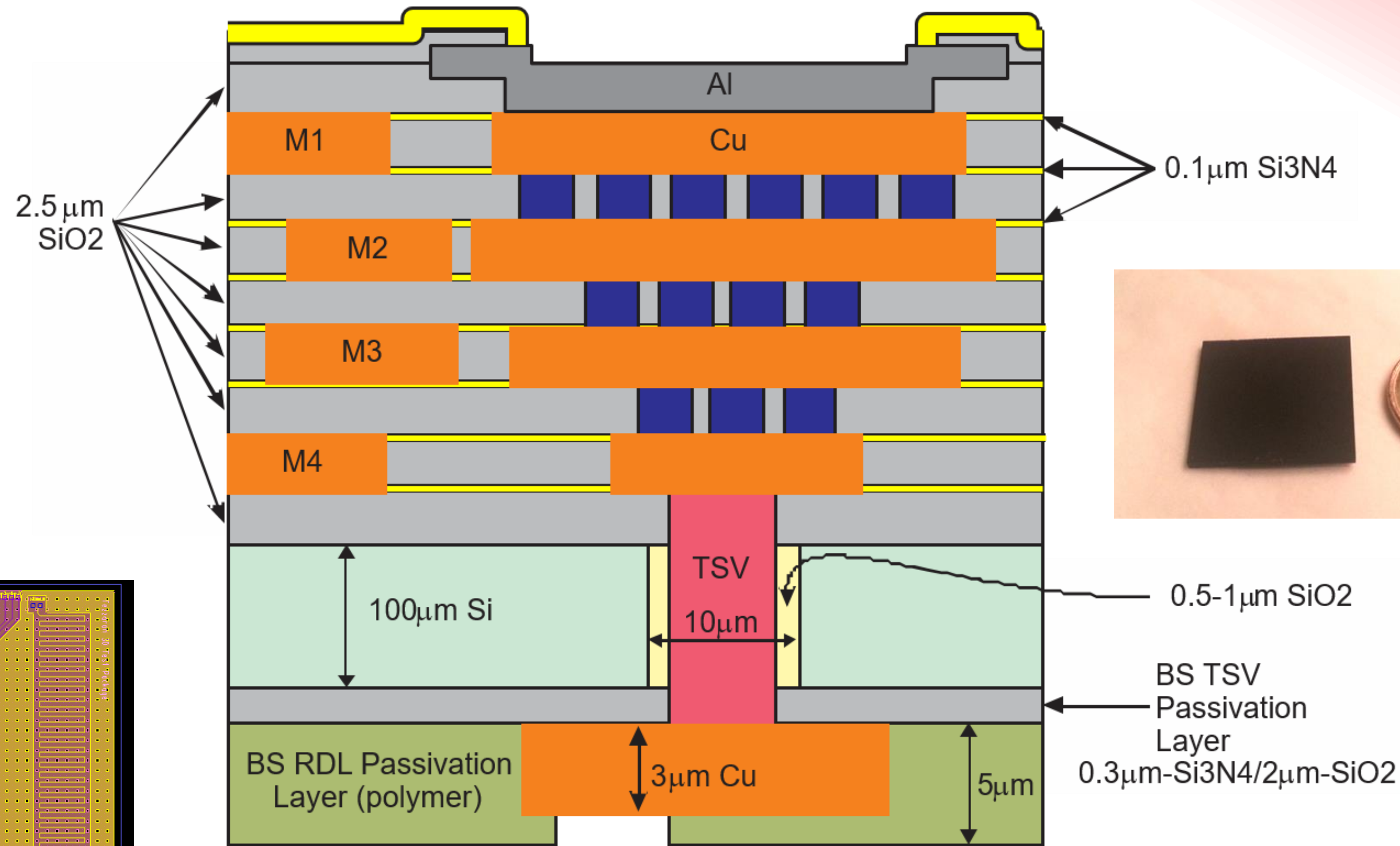
NHANCED SEMICONDUCTORS

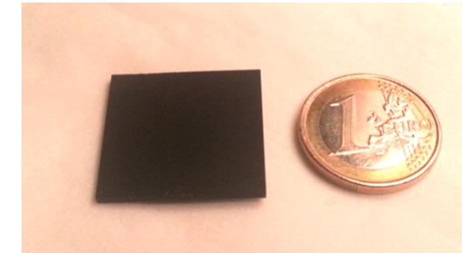
# Interposers

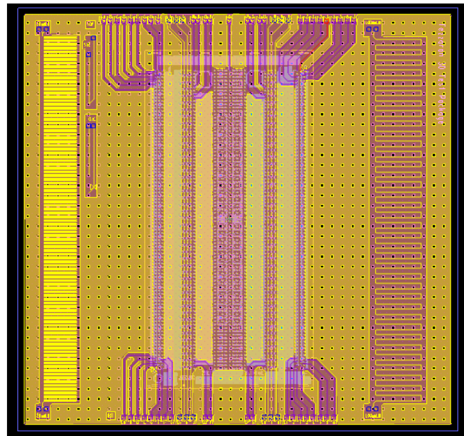
Bigger, Better, Faster

>50x50mm, many wiring layers, lower R,L,C







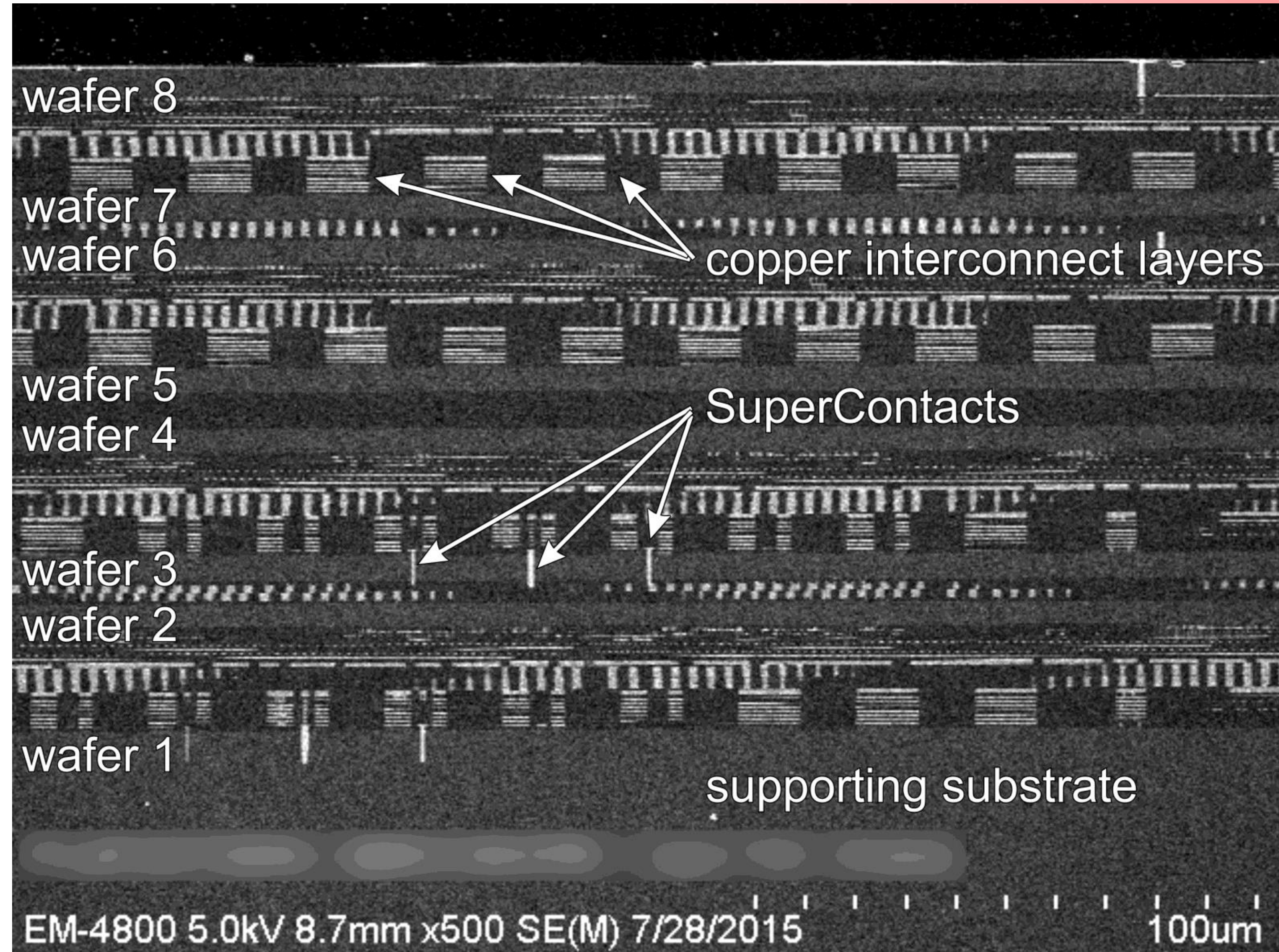
Silicon
Organic
Glass
Fused Silica
Metal

NHANCED SEMICONDUCTORS

# Bonding Technologies

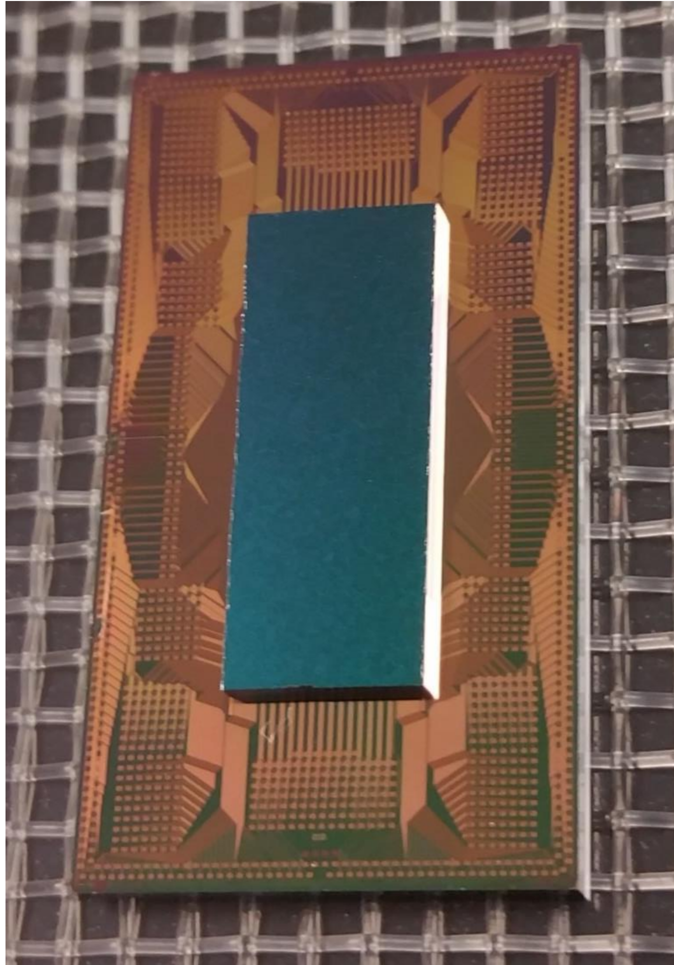
Wafer to Wafer
Die to Wafer
Die to Die

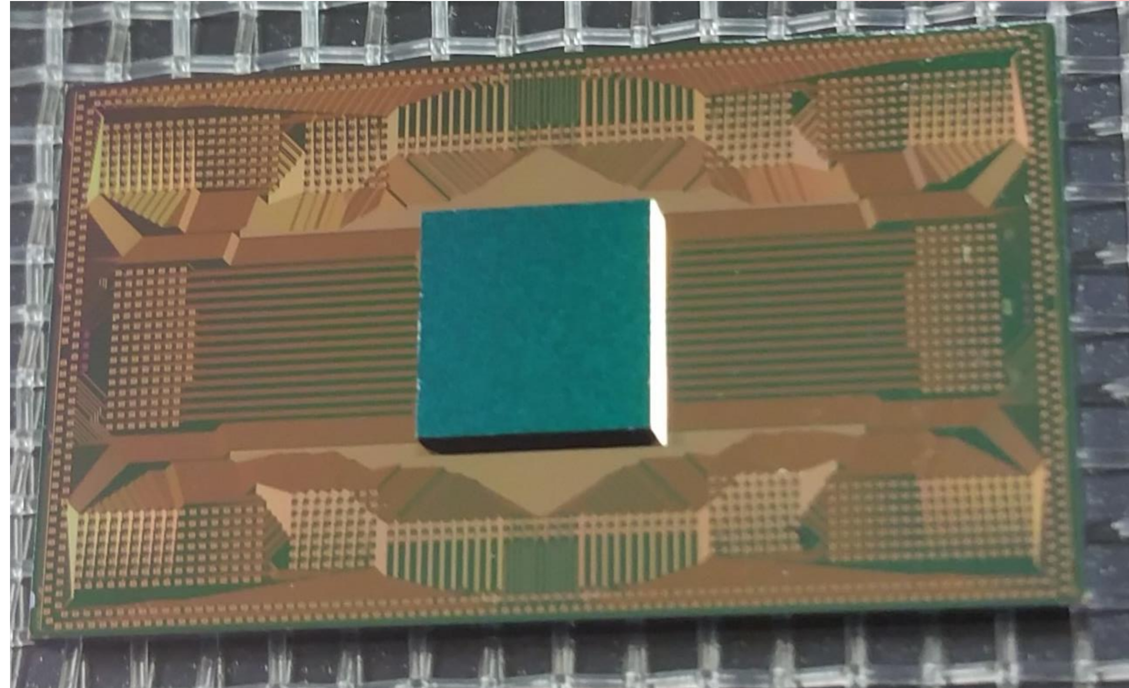
Silicon
GaAs
GaSb
GaN
SiC
InP
LiNbO3




NHANCED SEMICONDUCTORS

# 5.5D Systems

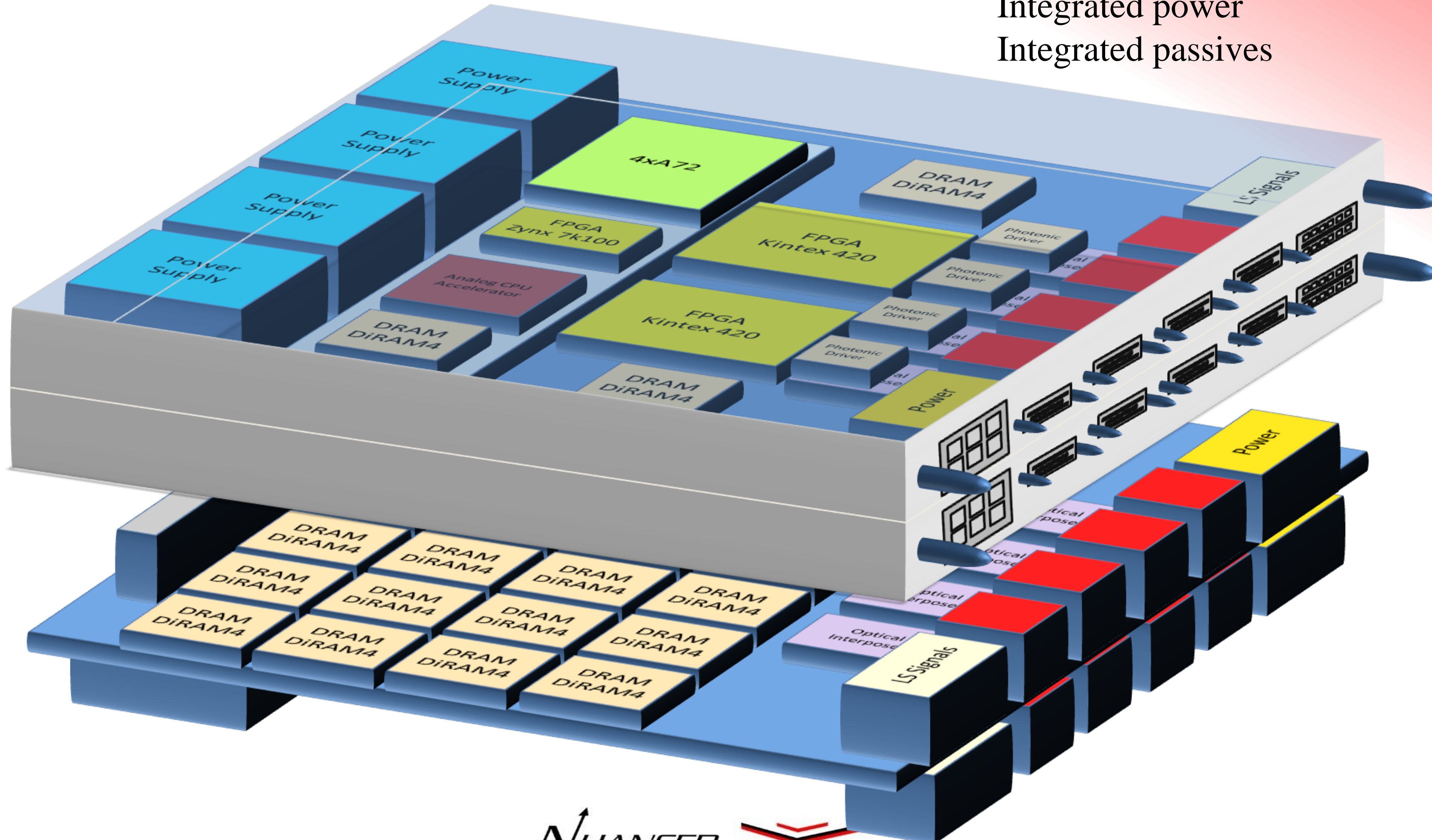




NHANCED SEMICONDUCTORS

# System Densification

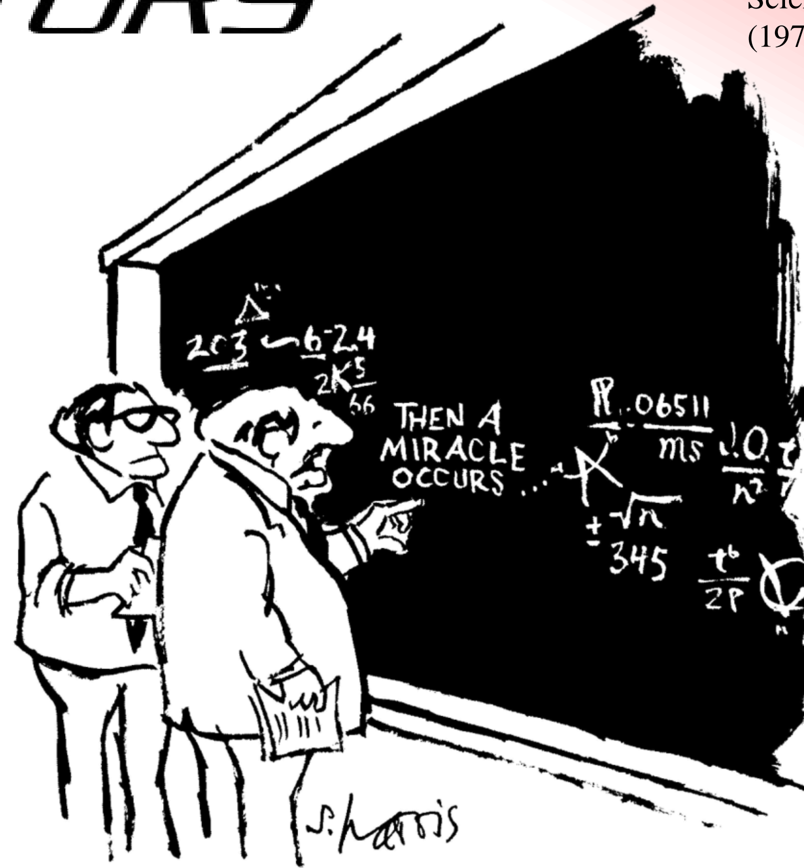
Integrated Photonics
2.5D
3D
Integrated power
Integrated passives




NHANCED SEMICONDUCTORS

NHANCED SEMICONDUCTORS

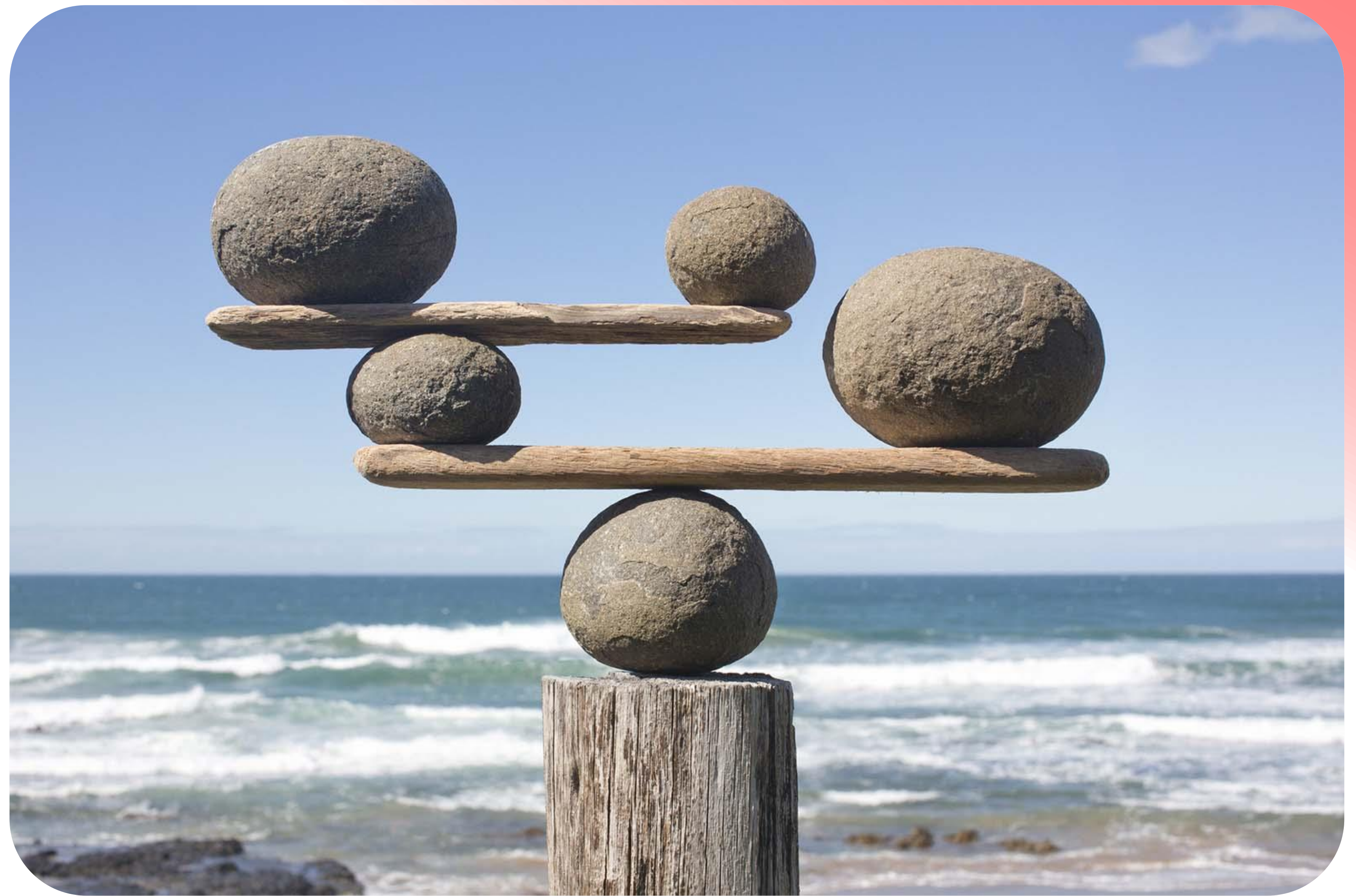
What's so Funny about Science? By Sidney Harris (1977)



"I think you should be more explicit here in step two."

# SOUNDS GREAT! WHAT'S THE CATCH?

# Sensitivities



Janus Henderson

- Stress
- Planarity
- Thermal
  - Memory
    - 85-95C
  - Logic
    - 85-125C
  - 3/5 Materials
    - SiC @ 400C
  - Sensors
    - 70-175C
- The more unique materials the greater the complexity

# Considerations

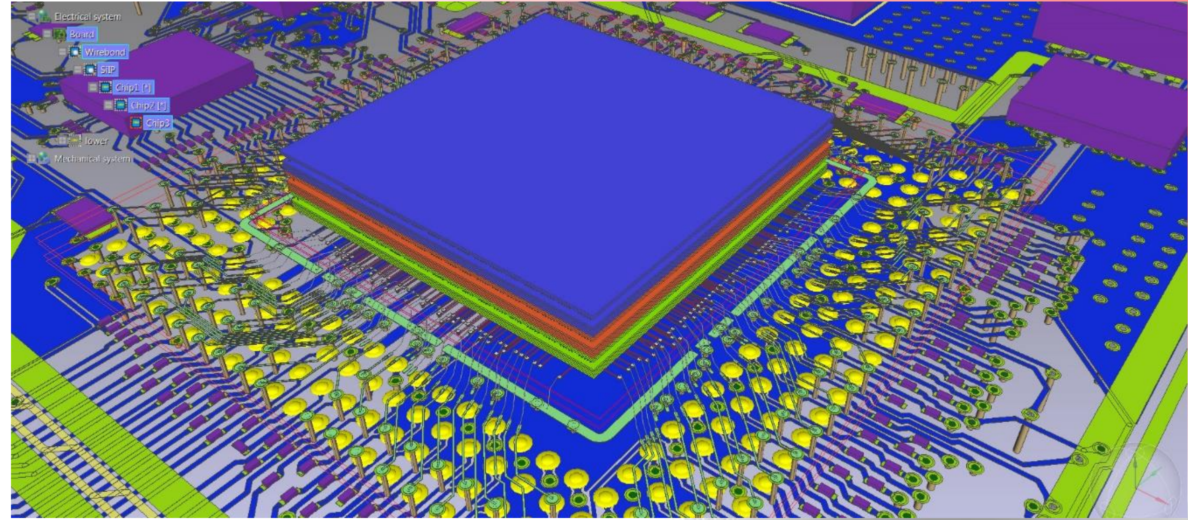
- EDA and Multiphysics
- Power distribution
- Cooling
- Technology interactions
- Yield
- Reworkability
- Supply chain resilience
- Environmental
- Test
- Pros / Cons of assembly methods and materials

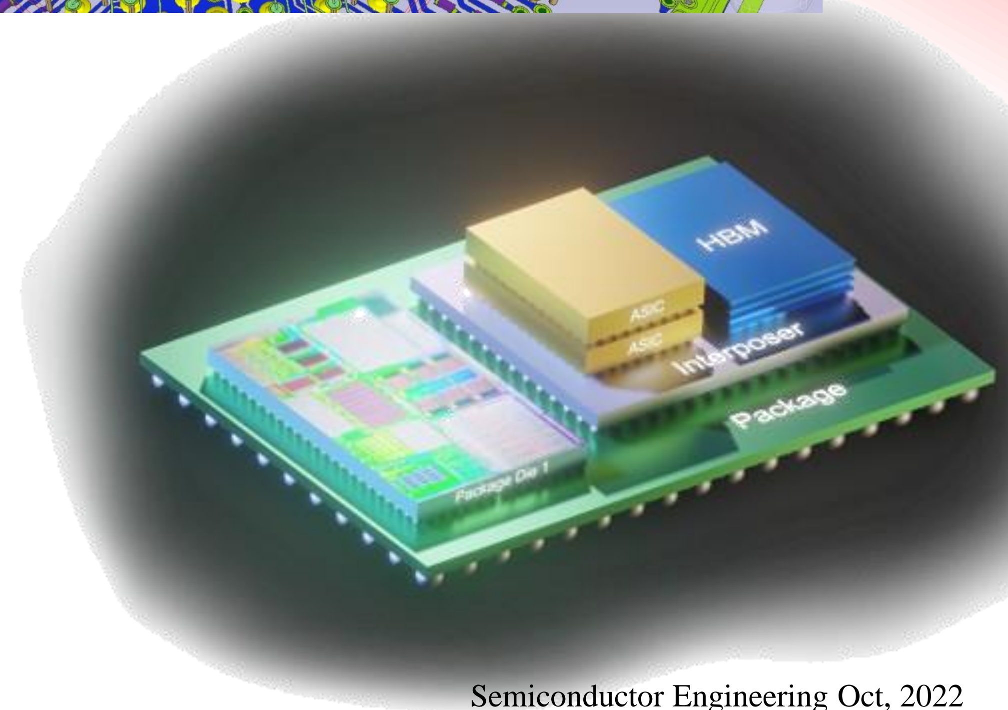
MIT Tech Review

# Co-Design and Multi-Physics

- Multi-Dimensional Tools
  - Scale
    - Nanometers to centimeters
  - Electrical
    - Power
    - Signal Integrity
  - Heat
  - Mechanical
    - CTE
    - Modulus
  - Cost
  - Photonics
  - MEMS
  - Liquids

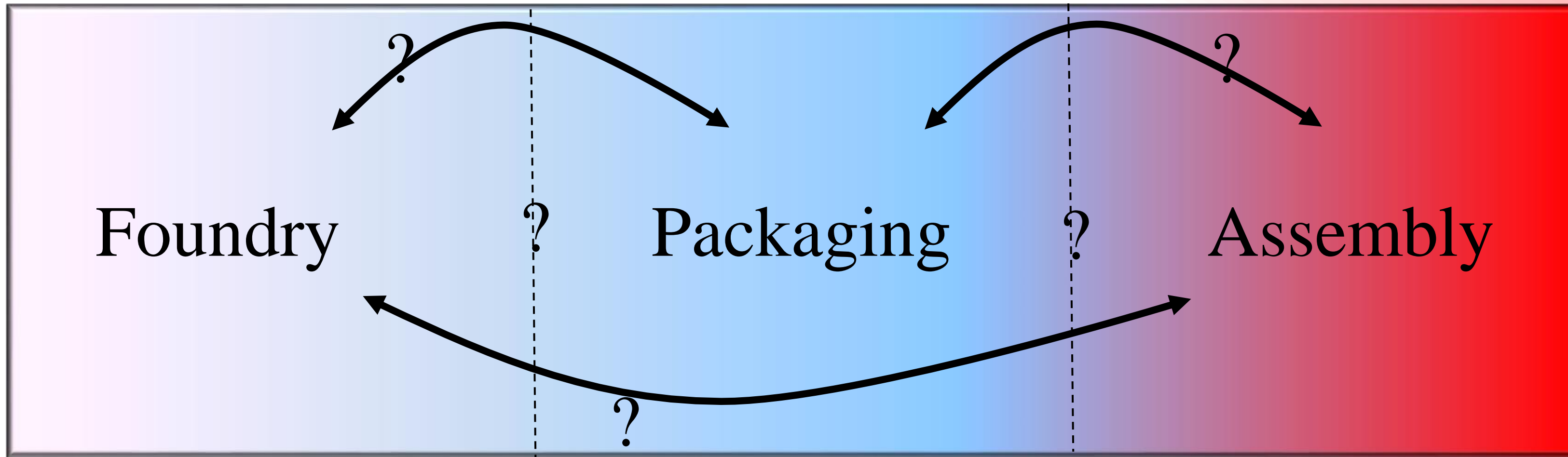
Zuken

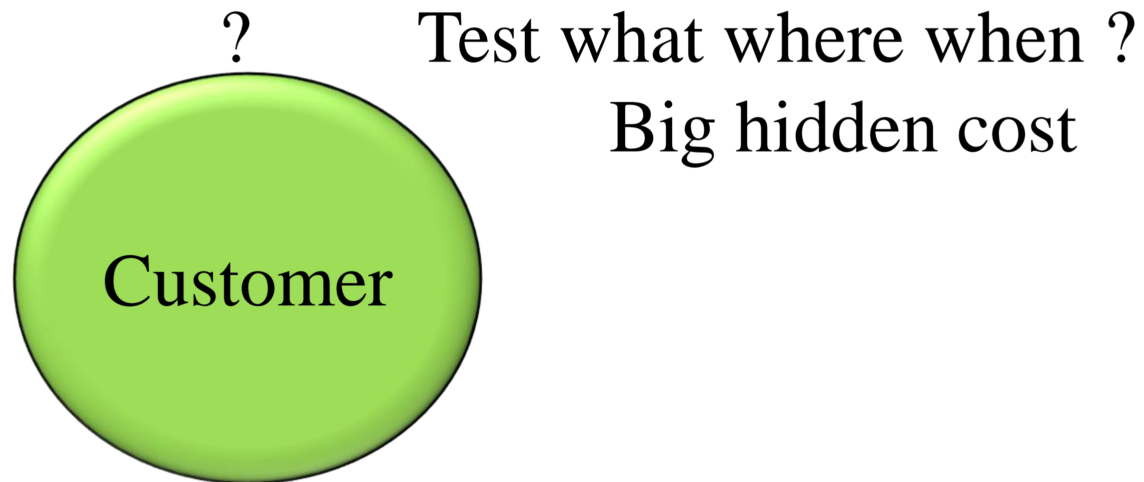





Semiconductor Engineering Oct, 2022

# Mixing Fab, Packaging and Assembly




NHANCED SEMICONDUCTORS

# Testing

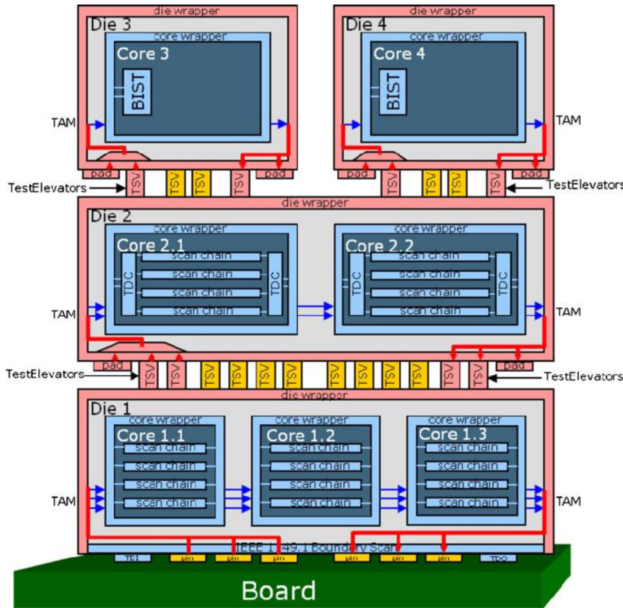
- Significant planning required
- Careful analysis of yield cost
- New methodologies
  - High I/O count requires self-test
  - Deep embedding requires more effort for visibility
  - At speed test alternatives
- Embedding memory has numerous test issues
  - Standard test interface required.
- Self-repair / Self-redundancy

NHANCED SEMICONDUCTORS

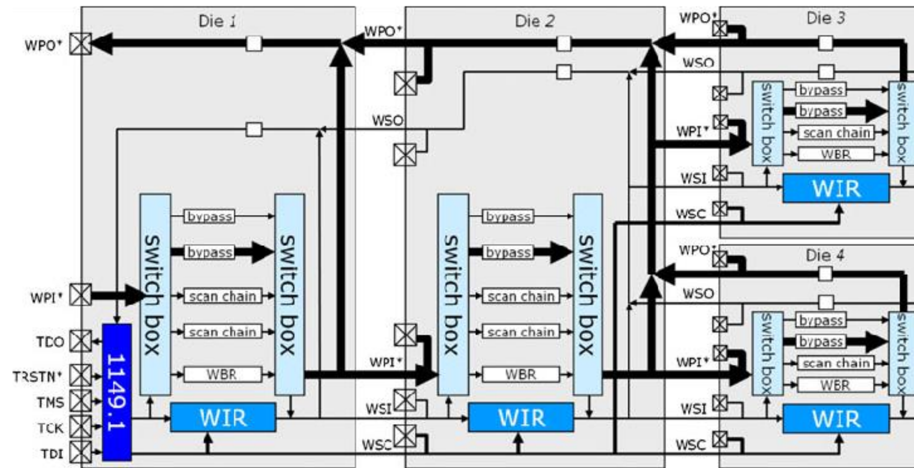
# One Slide:

***Use Standardized DFT + 2.5/3D PCM methods to test Quality and derive Reliability***
***Use repair and redundancy to create KGD and obtain yield.***

**Images from: A DFT Architecture for 3D-SICs Based on a Standardizable Die Wrapper;** Erik Jan Marinissen et al




Physical

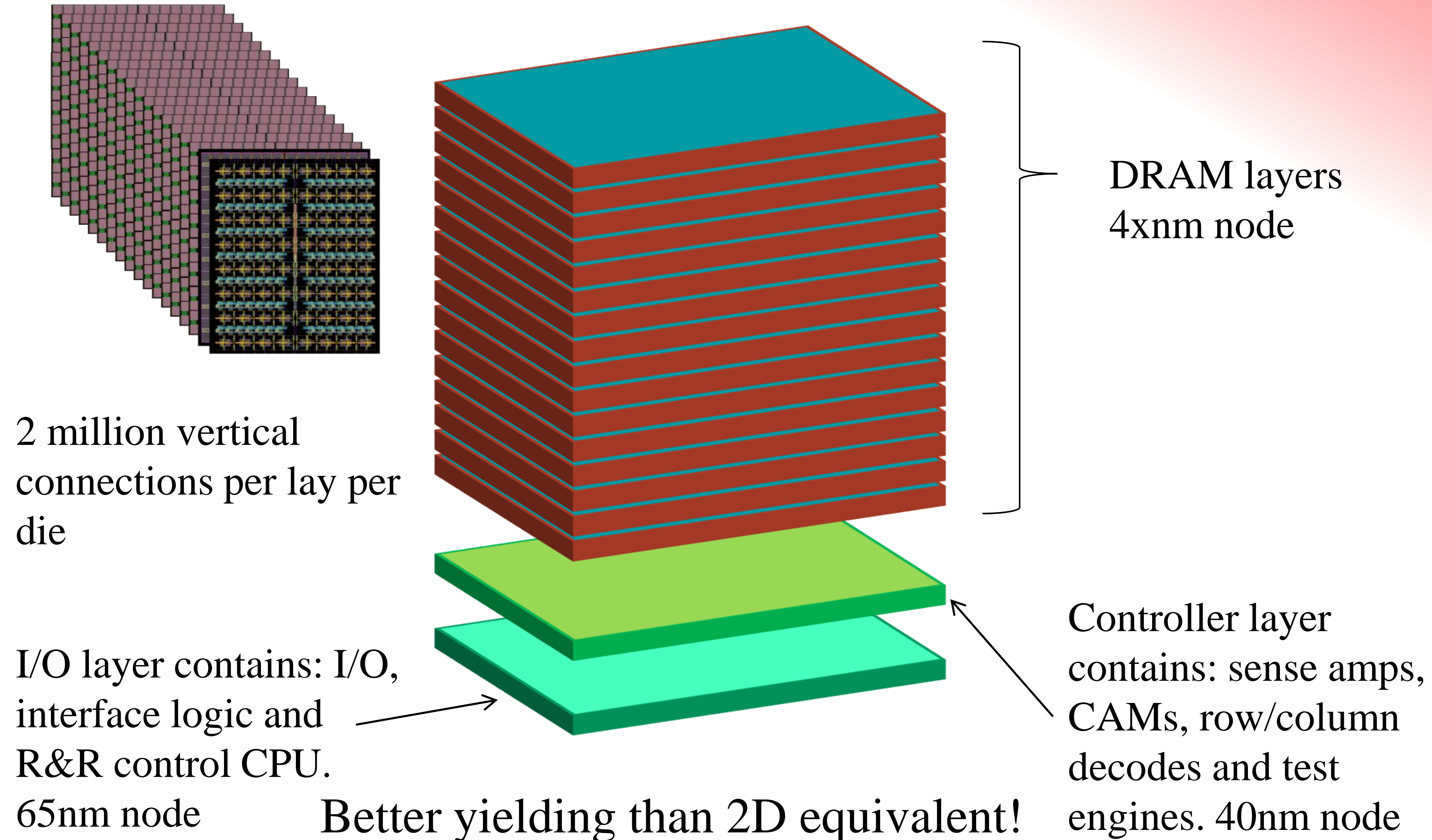



Logical

IEEE 1500 is well defined 2.5/3D DFT starting point building on 1394 standard. Plan is to add 1149.4 analog features targeting device manufacturing integrity.

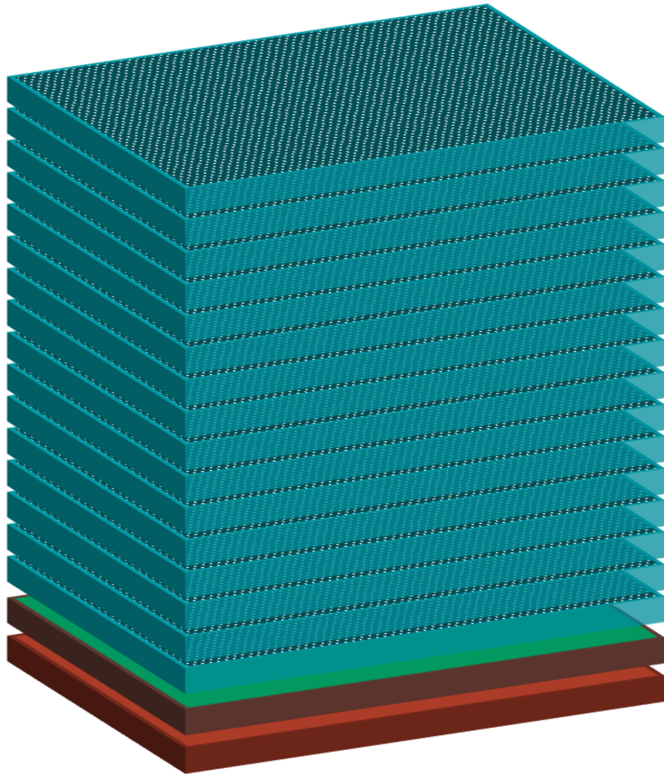
Augmented JTAG based on IEEE 1500: Add alignment sensing, 3D interconnect R/C measurement, power, temperature …
System level test, configuration, repair and validation
Objective is to “prove” specific device quality and improve reliability data.

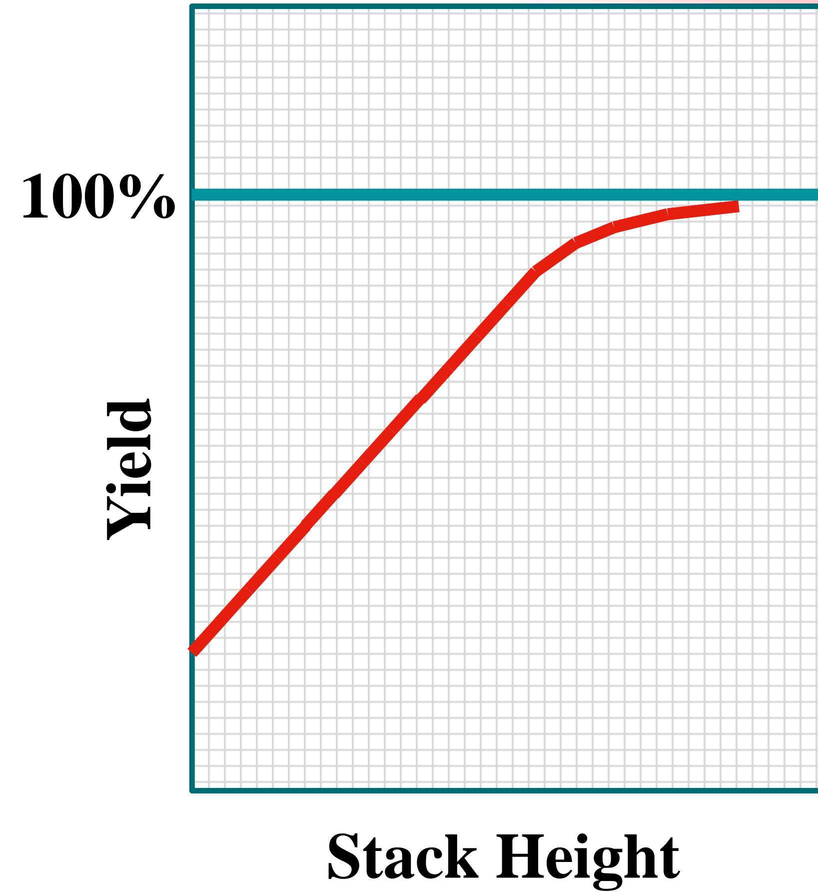
# “Dis-Integrated” 3D Memory




NHANCED SEMICONDUCTORS

# Bi-STAR Repair Improves Yield






NHANCED SEMICONDUCTORS

# A Change In Perspective

- Focused on next generation semiconductors created by
  - Advanced Packaging
  - Additive Semiconductor Manufacturing
  - True heterogenous integration
  - Interconnect focused – all BEoL additive
    - Better ROI
    - Lower development costs
    - Lower CAPEX
  - Leveraging existing foundries
    - Split Fab
  - More Than Moore Technologies
    - IP Centric
    - Intrinsic value based – not cost of capital

Split Rock Lens – StackExchange