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Power Electronics-Engineering :: Paul Scherrer Institut (PSI)

PS for SLS2

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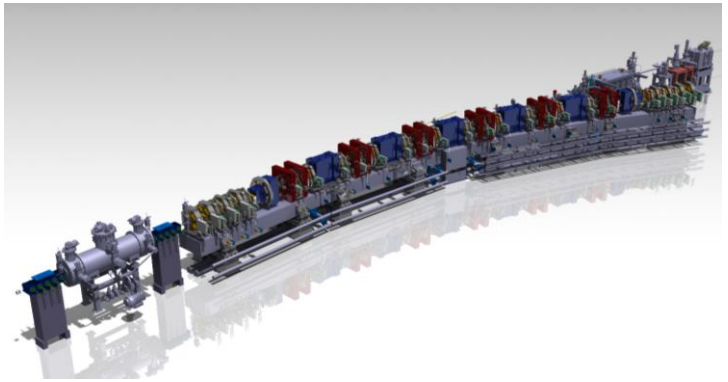
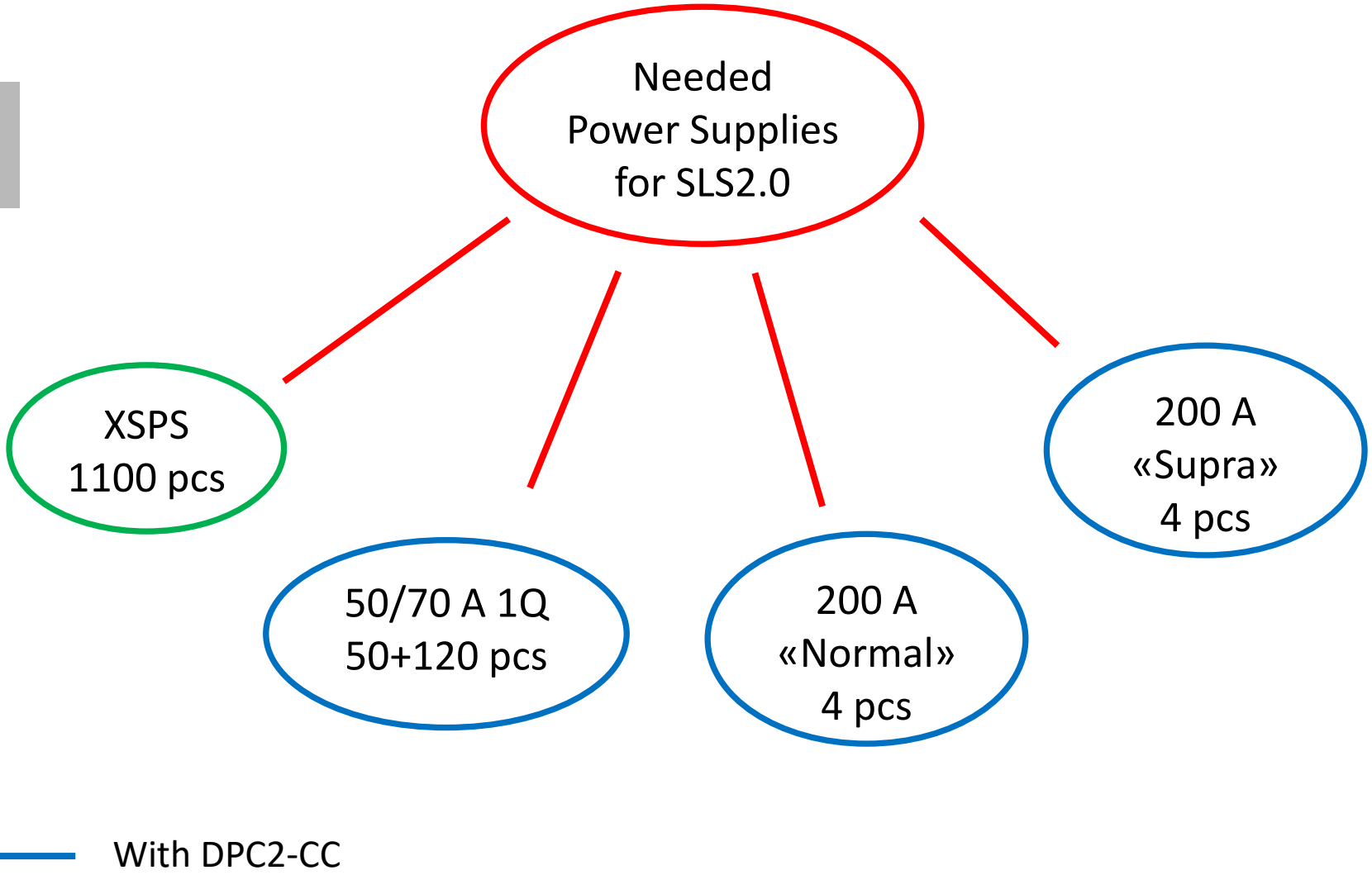
Simon Richner, Beat Ronner

Pocpa 2023, Wiener Neustadt

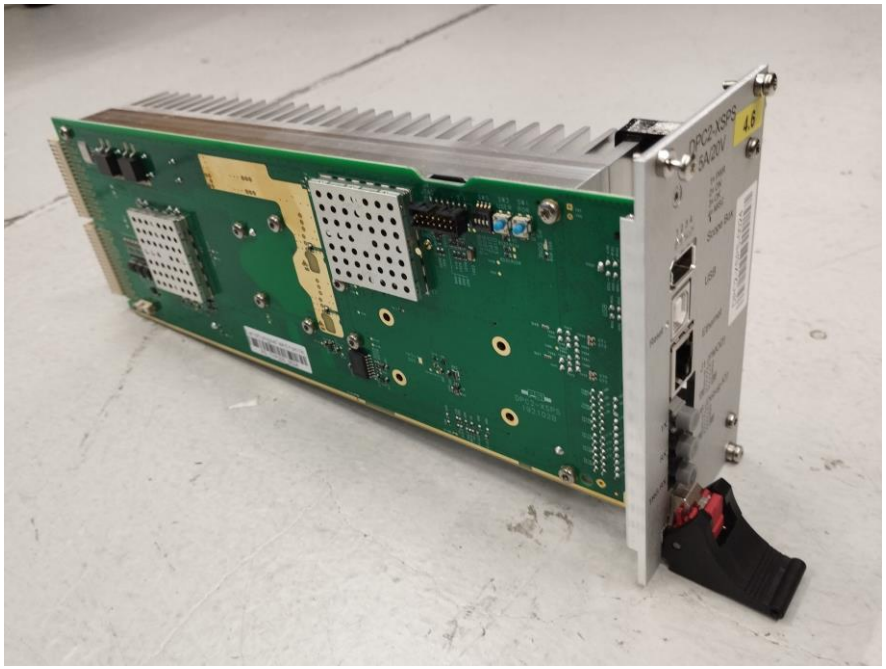


PS for SLS2


Needed
Power Supplies
for SLS2.0
XSPS
1100 pcs
50/70 A 1Q
50+120 pcs
200 A
«Normal»
4 pcs
200 A
«Supra»
4 pcs
With DPC2-CC

XSPS

- 5A, 20V, 4Q power supply with controller & shunt current measurement on one PCB
- Up to 36 fit into one 19’’ rack
- Figure of merit: Noise & ripple (0..10 kHz) < 5 ppm RMS (with inductive load)



XSPS Power part: Challenge 1

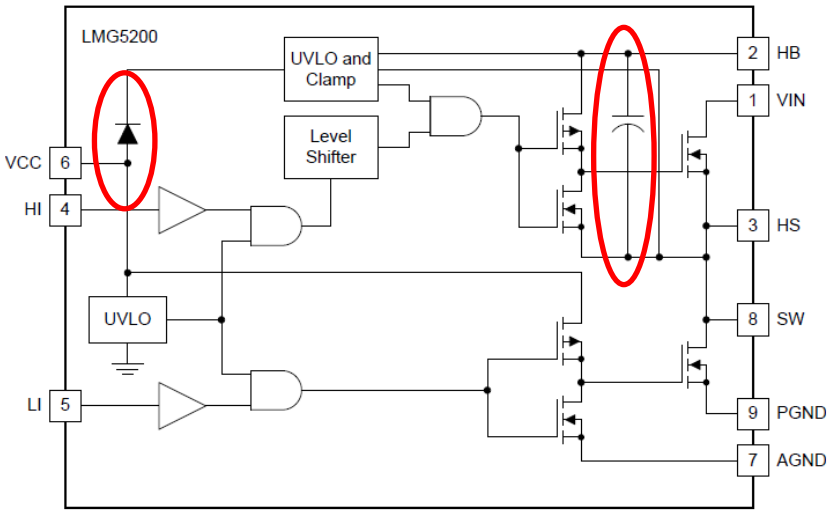
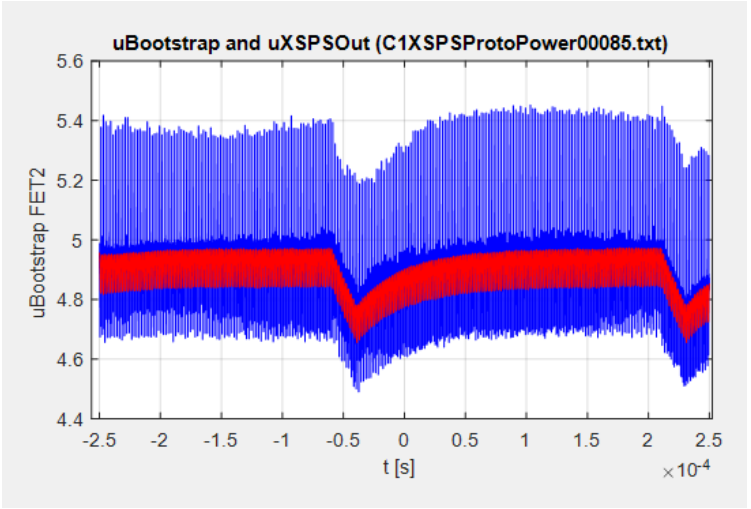


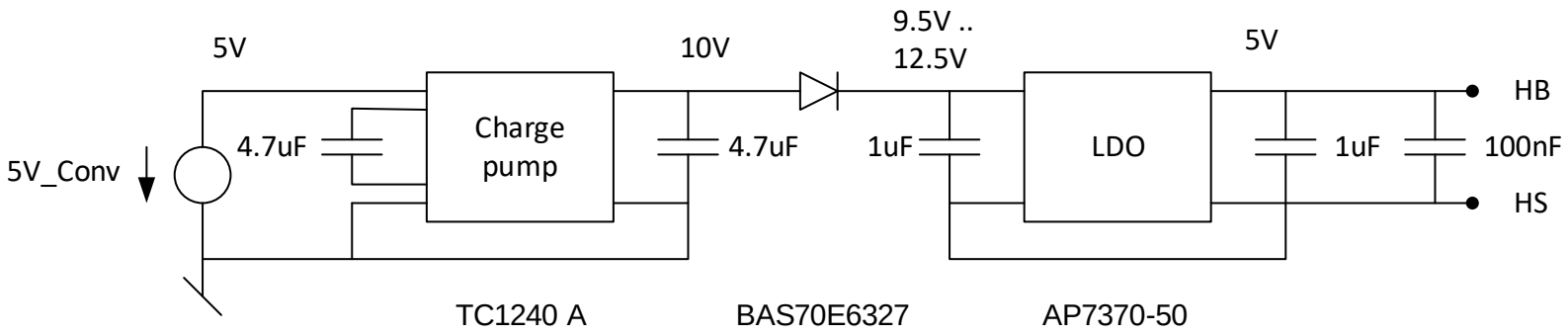
Figure 10. Functional Block Diagram



Problem:

- FET Halfbridge module LMG5200 has an internal bootstrap-supply for the supply of the driver of the upper FET
- This supply is implemented as 2-point (bang-bang) controller
- The frequency of this 2-point controller could be seen as 16 .. 34 kHz component on the output voltage

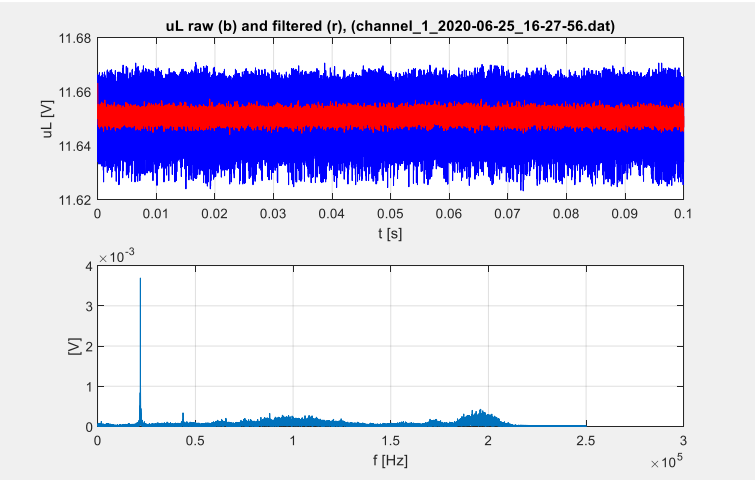
XSPS Power part: Challenge 1



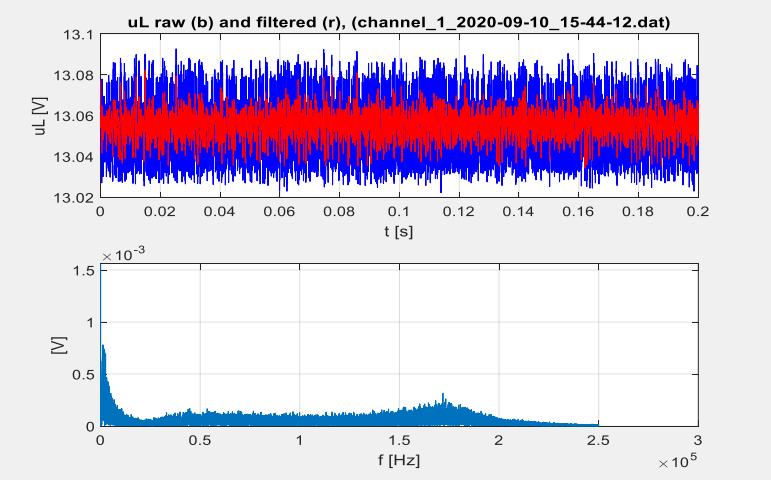
Solution:

- Made own, LDO-based bootstrap-supply for upper FET

Before



After



200 A PS

For SLS2.0, only two 1Q configuration of the 200 A PS is needed:

- 200A, 23V, 1Q (for «normal» magnets)
- 200A, 7V, 1Q (for superconducting magnets)

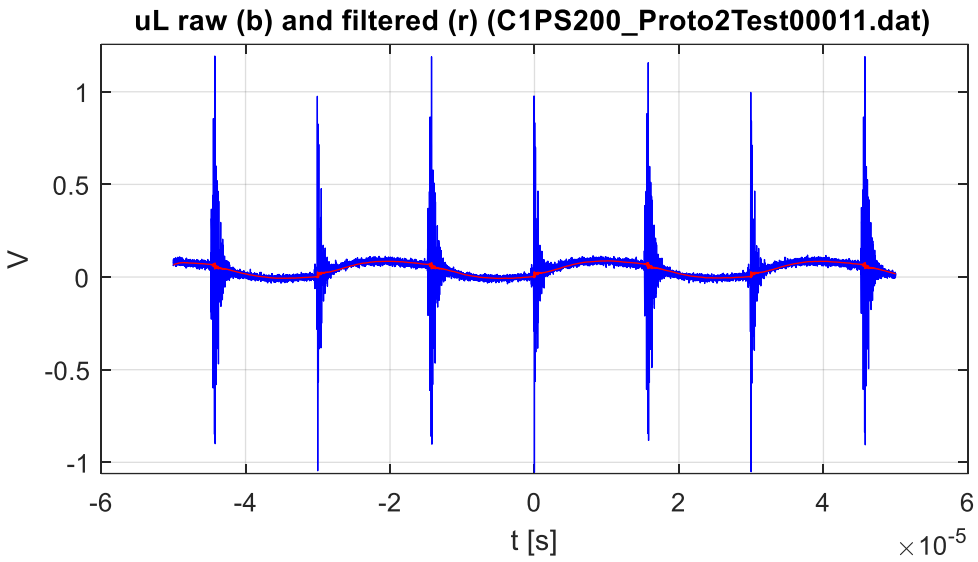
In course of the project, also a

- 200A, 120V, 4Q configuration

has been developped and tested.

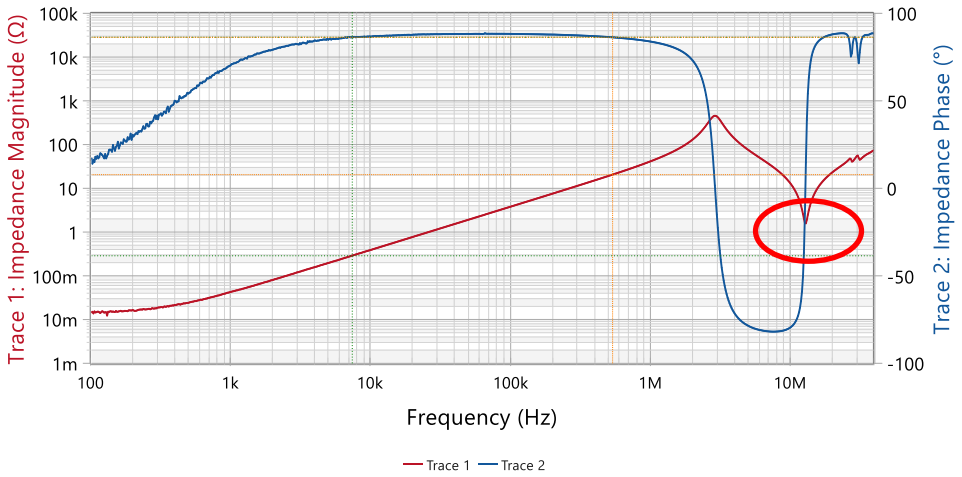
200 A PS

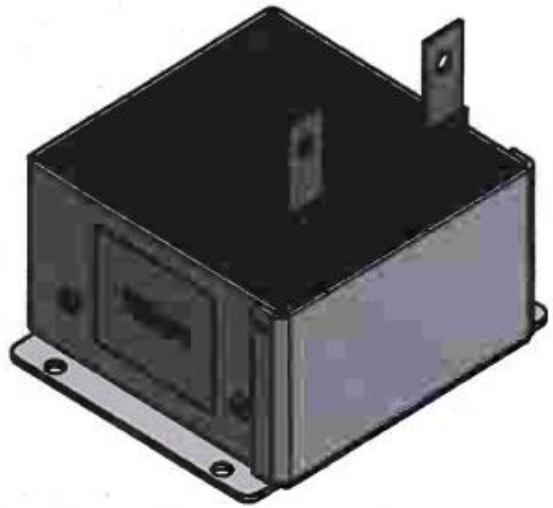
One item that needed some focus during the development of the 200 A PS was the output inductors: The first inductor had a rather high coupling capacitance between the windings, which showed up in high peaks on the output voltage in the switching moments.

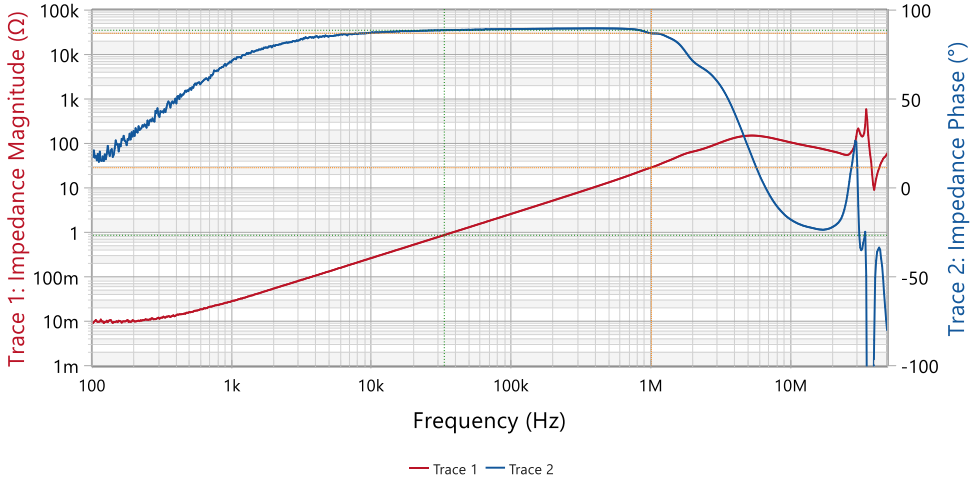


200 A PS


STS
MDR006U16
SN 0001
Engineering Sample


Trace 1: Impedance Magnitude (Ω)
Trace 2: Impedance Phase (°)
Frequency (Hz)
100k
10k
1k
100
10
1
100m
10m
1m
100
1k
10k
100k
1M
10M
100
50
0
-50
-100
Trace 1
Trace 2




Trace 1: Impedance Magnitude (Ω)
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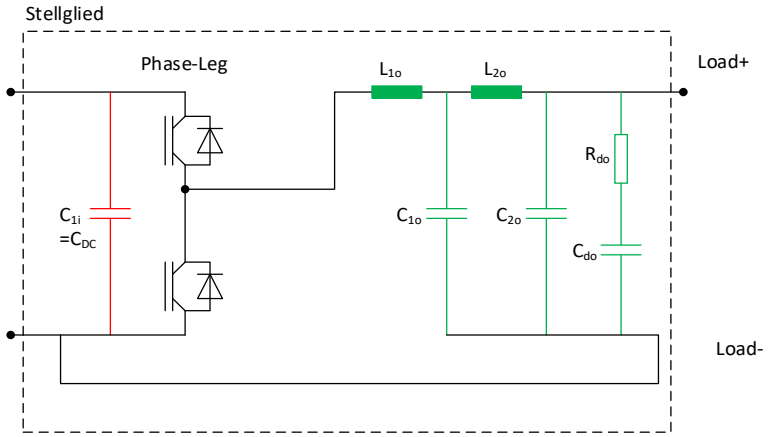
Frequency (Hz)
100k
10k
1k
100
10
1
100m
10m
1m
100
1k
10k
100k
1M
10M
100
50
0
-50
-100
Trace 1
Trace 2

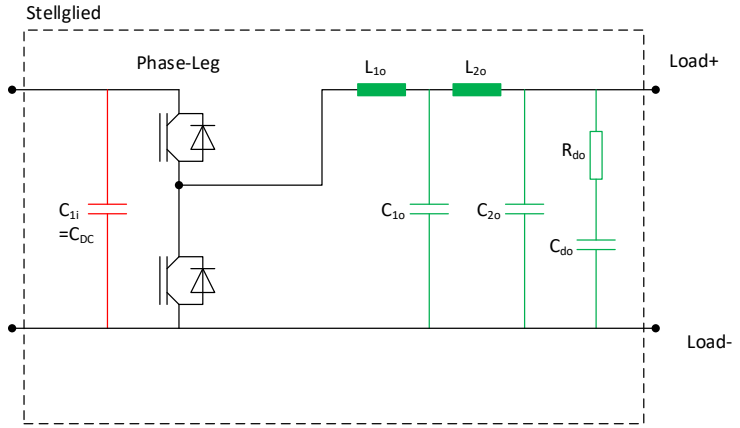
200 A PS

Change of the inductor alone helped, but did not solve the problem completely.

The 2nd contribution was the layout of the «minus» busbar:

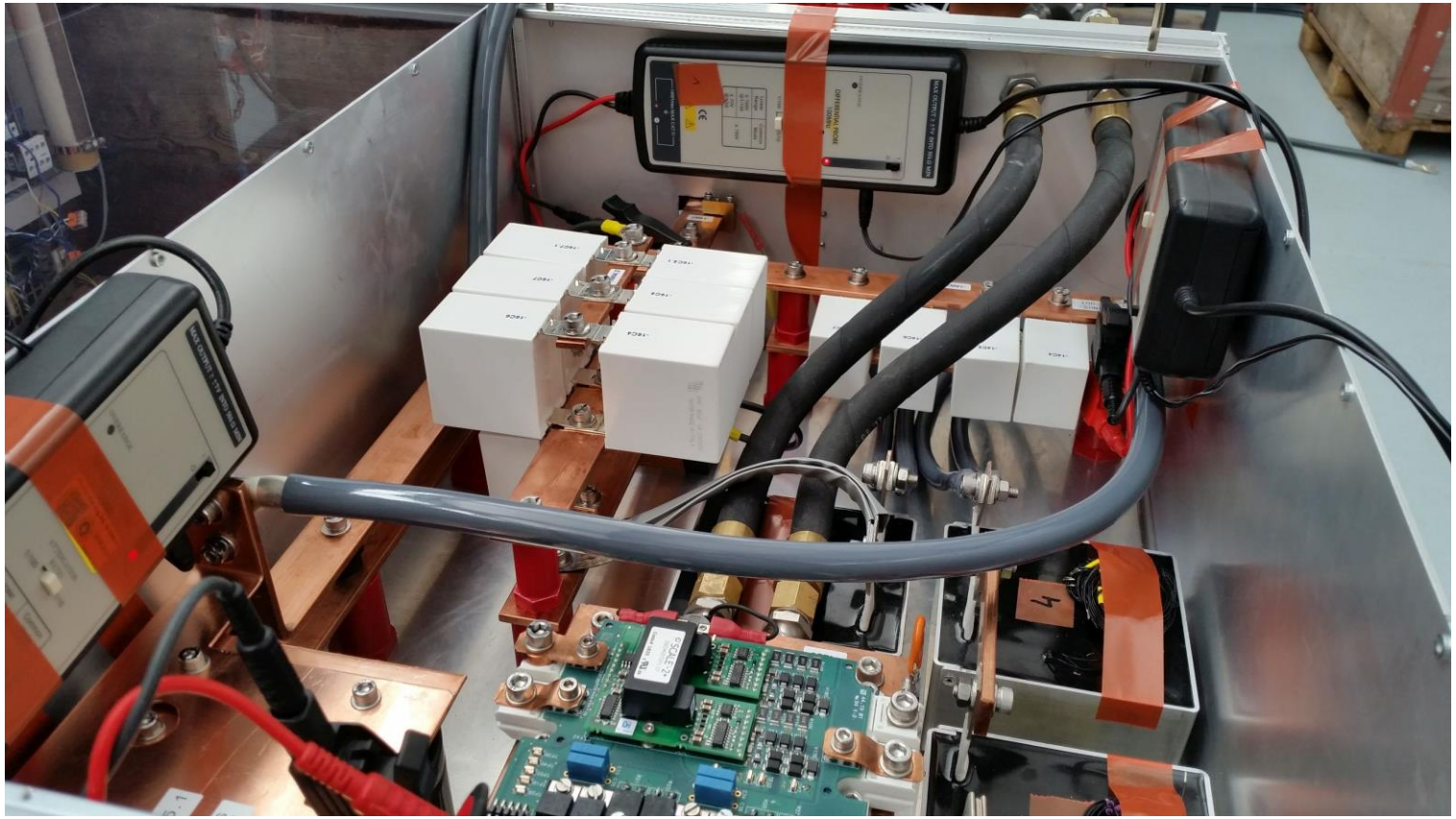
- In the first version, the minus was connected back to the input
  This made that all the loop currents of the first filter stage took their path over the output
- In a 2nd version, the minus busbar was connected as in the picture on the left side, which improved the situation





200 A PS

«Minus» connections in the first version, but «improved» with a cable.



50-70A converter: Design concept

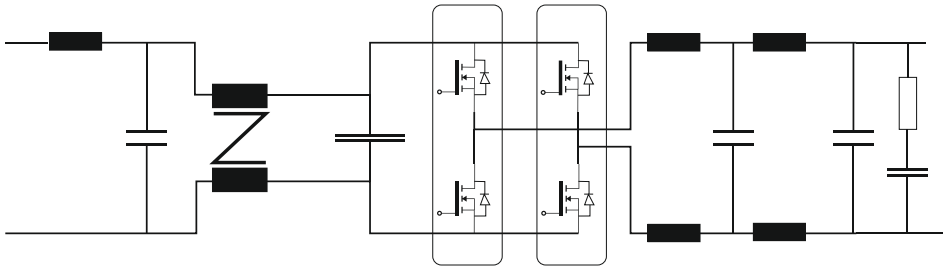
Develop the same PCB to achieve either:

- 50A / 72VDC unipolar power supply
- PS 70A / 28 VDC unipolar power supply
- PS 50A / 72 VDC bipolar power supply

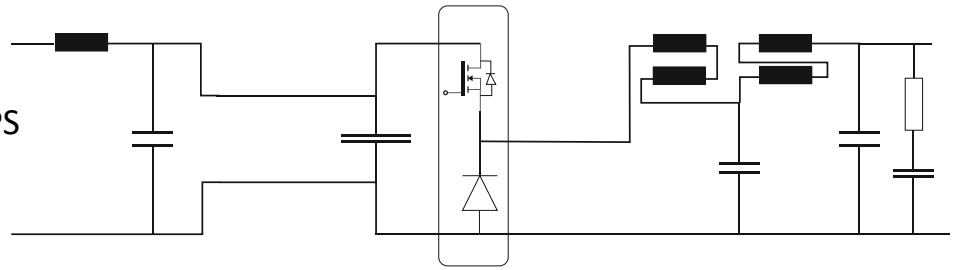
The same passive components can be used for all 3 different power supplies versions.

The 50A bipolar version is finally not required for SLS 2 but will be used later in another facility.

50A bipolar PS



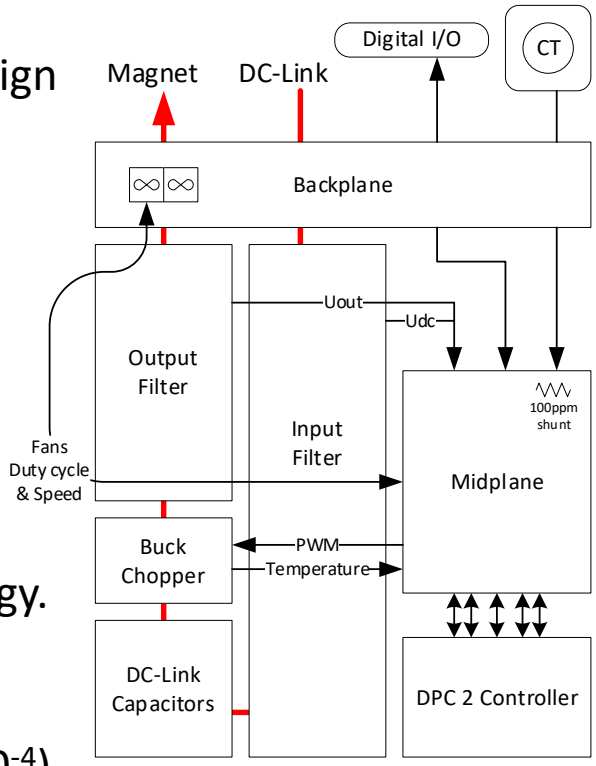
50/70A unipolar PS



Description & Achievements

Specification:

- Topology: 100 kHz hard-switching buck chopper design using Microsemi FREDFET and Schottky diodes.
- Realization: Full PCB design
- Features:
  - I2C bus for redundant fans control and temperature monitoring.
  - Input & output passive current filtering.
  - Notch filtering of PWM frequency.
  - Built-in controller card.
  - Overvoltage protection for the bipolar topology.



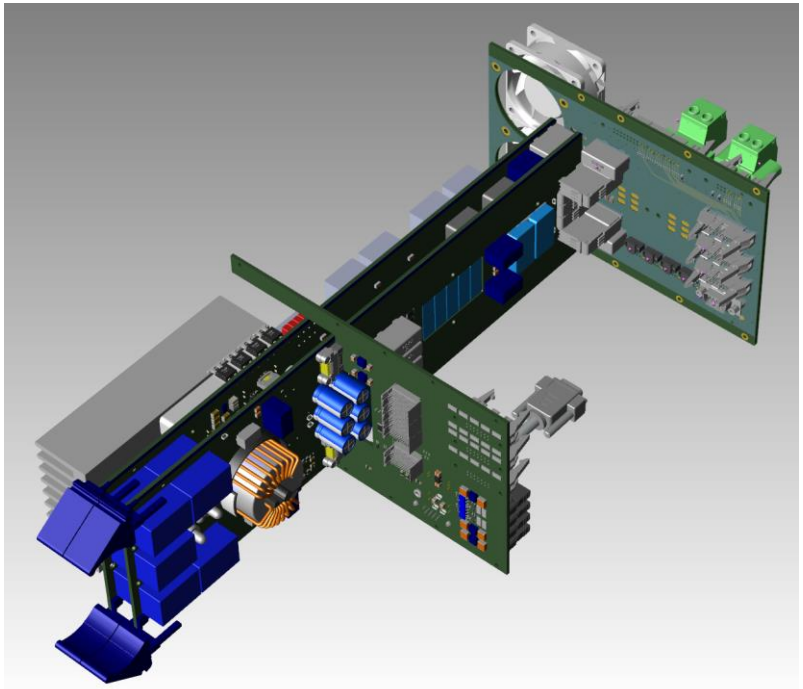
Power supply block diagram

Achievements:

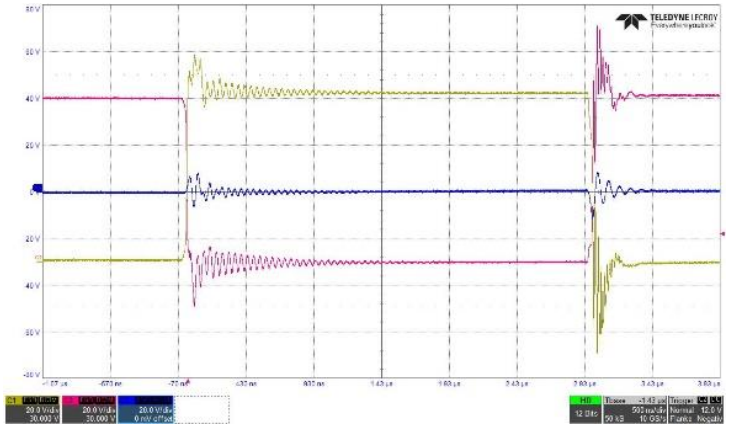
- Output voltage ripple: Damping ratio < – 63 dB (7.10^{-4}).
- Current ripple : 100-150 ppm rms ripple on a resistive load, ≈ 85 ppm rms on an inductive load
- 96 % efficiency for the 50A version and 93 % for the 70A
- I2C bus for temperature monitoring and fans control operating flawlessly.

PS 50/70A: Challenge Crosstalk

- Due to high passive filter efforts and high current, long PCBs (400mm) are necessary.
- Avoid long paralleled routes of power and signal nets.
- Solution: “Exit” paths of signal lines in Z-axis by using two backplanes:
  - Backplane for power connections
  - Midplane for critical signals to controller DPC2-CC
- Noisy high power circuits (MOSFET, filter inductors etc.) and signal circuits are separated on different PCB sides.



Problems



Y/R: V_{DS} switching – B: DCCT shunt voltage

Current absolute error vs. setpoint

Issues:

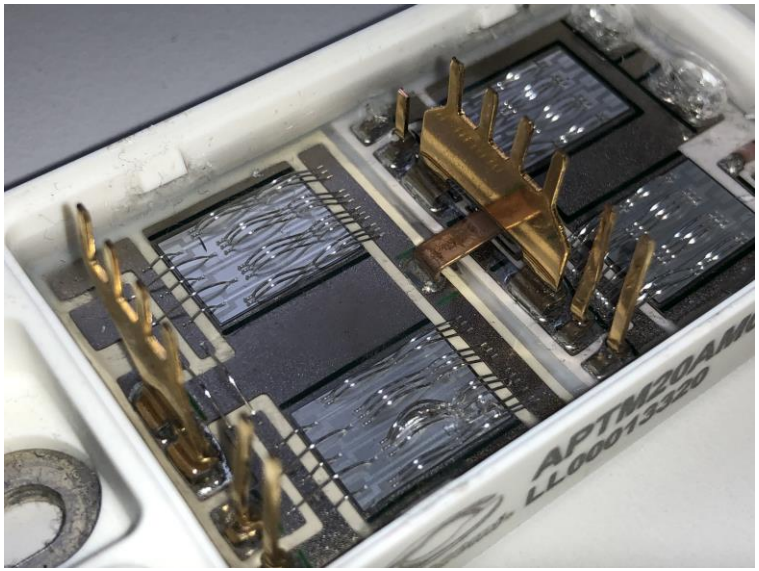
- High dv/dt commutation edges of MOSFET in conjunction with abrupt recovery effect of the free-wheeling body diode are leading to high frequency ringing of the commutation cells.

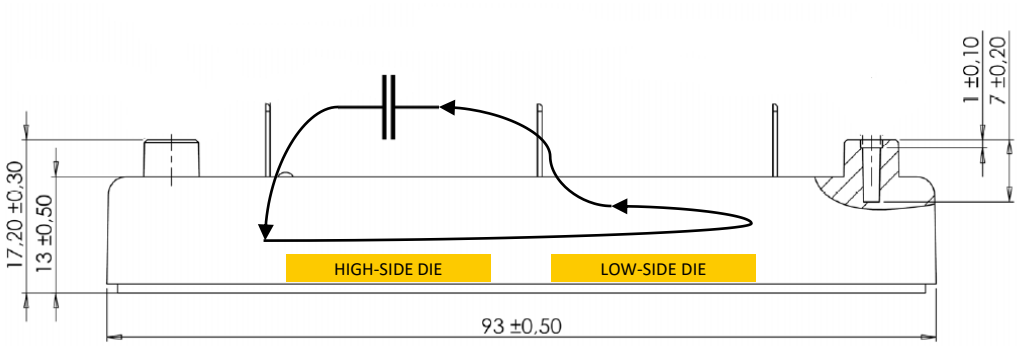
- Commutation noise is coupling into the auxiliary power supplies and ultimately in the DCCT control signal.

- The DCCT signal noise can cause inaccuracy in the output current when the sampling of the signal occurs simultaneously with the switching

PS 50/70A: Challenge Parasitic Inductance

- Relatively big MOSFET package results in higher parasitic inductance.
- Overall commutation loop through high- and low-side FET die is large.
- Parasitic inductive loop increases MOSFET drain-to-source peak voltage spike and SW node ringing.
- Reverse recovery effect of MOSFET parasitic diode was highly noticeable and interacts with parasitic inductance.





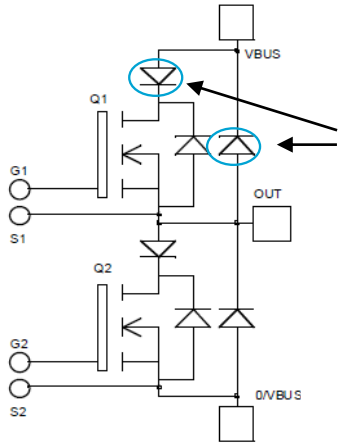
Solutions

Solutions:

- Partial issue mitigation is done using series and free-wheeling schottky diodes to bypass the body diode.

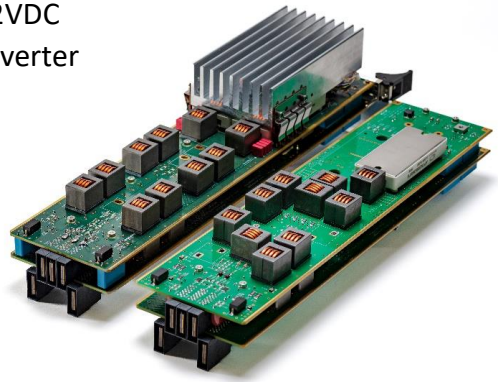
- For a given current working point, shifting the sampling clock with respect to the PWM clock helps overcoming the instability.

- Improve filter performances (common mode & DCCT signal)

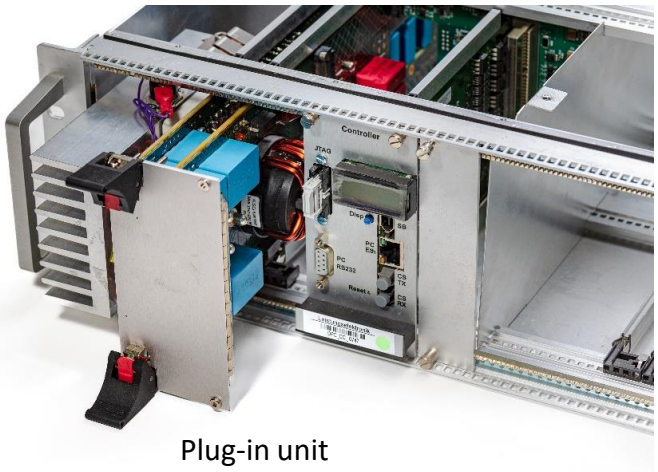


Half-bridge arrangement for 4Q

50A/72VDC
4Q converter



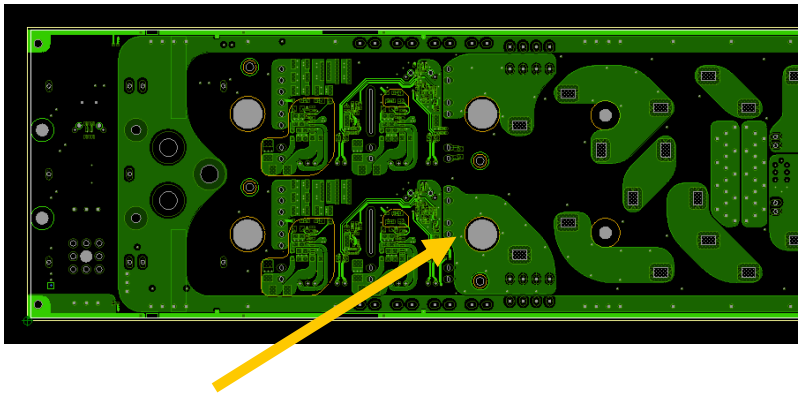
50-70A/28-72VDC
1Q converter

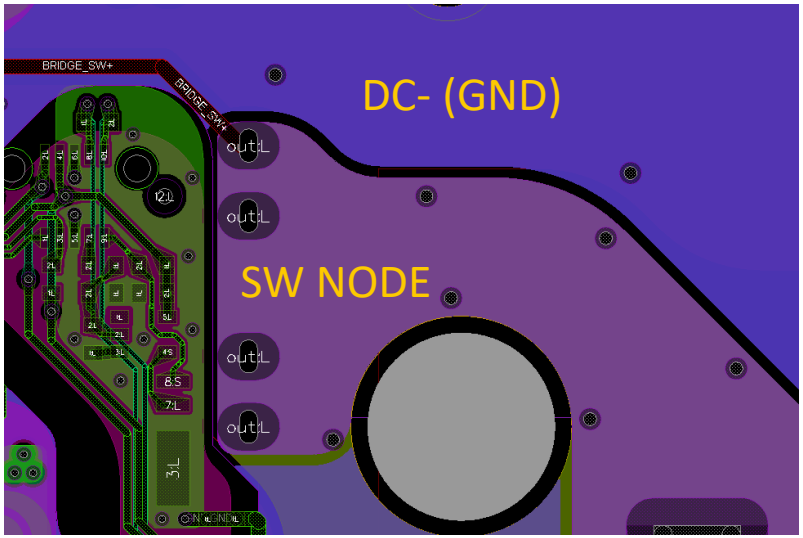


Plug-in unit

PS 50/70A: Challenge EMI

- High dv/dt at switch node of MOSFET needs a careful layout.
- Design tradeoffs between high current support and small SW copper areas.
- Uncertainities:
  - Keep it away from other copper planes and traces, minimize capacitive coupling?
  - GND planes below SW node area for defined return current path and therefore higher capacitive coupling?
  - «Sandwich» structure: SW node between DC-link planes?





Controller Card – DPC2-CC

3rd Generation of Digital Power Supply Controller

DPC vs DPC2: Main differences

DPC	DPC2
Custom FPGA / DSP / Memory System (onboard)	Pluggable SoM (System on Chip Module - Xilinx Zynq Ultrascale+ MPSoC)
HighPrecision ADC on separate Card, Temperature Stabilization	HighPrecision ADC on Controller Card
12x 16Bit SE ADC channels (isolated island)	16x 18Bit Differential channels

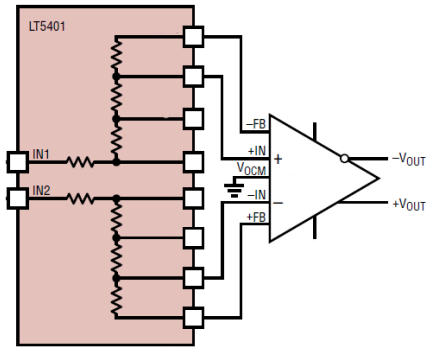
DPC2-CC: Summary I/O

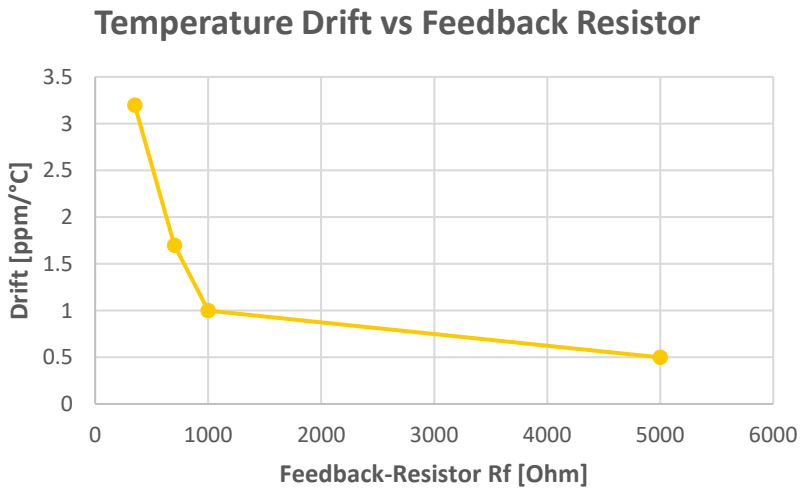
ADC	
1	±10V Differential (24Bit, 2MSps), Isolated
16	±10V Differential (18Bit, 200kSps),
PWM	
15	Outputs
13	Inputs
24V I/O	
8	Outputs
20	Inputs
Comm	
1	Ethernet Gigabit
1	USB 2.0
	POF RX/TX, Trigger
	I2C, M-LVDS,…

DPC2-CC: Temperature Drift

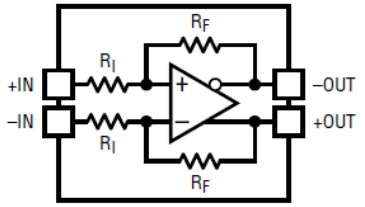
Amplifier with external Resistor Network

- Gain Drift 1.7ppm/°C,
  expected 0.2ppm/°C
- Unclear correlation with feedback resistance





Use fixed gain amplifier with higher noise but actual gain drift 0.2ppm/°C (n=1)



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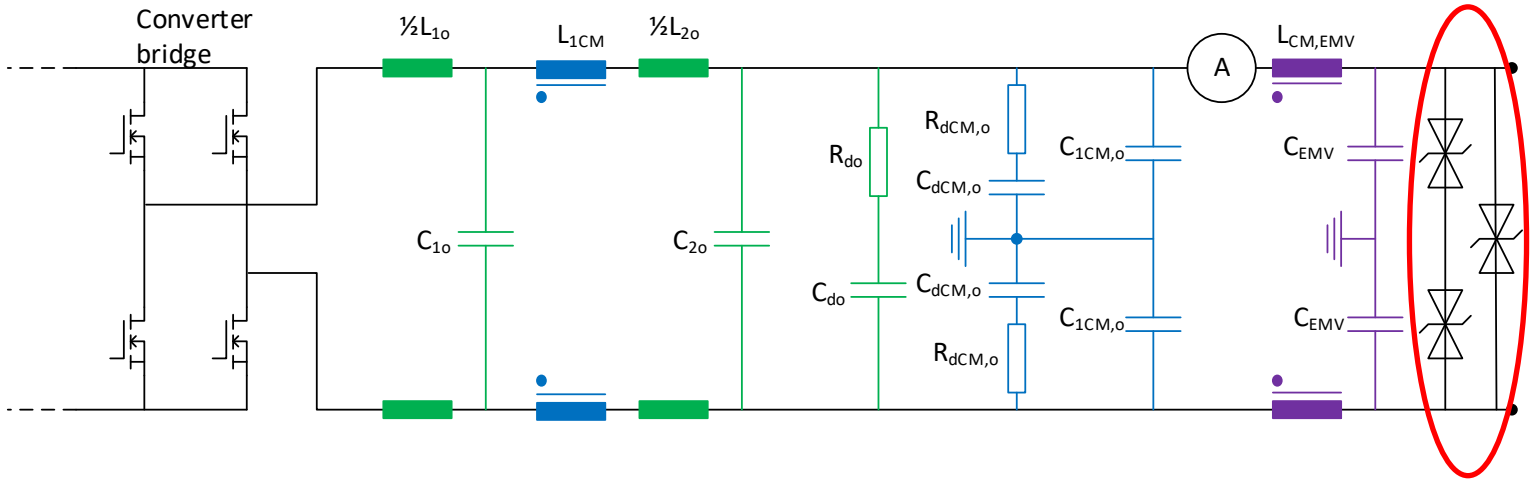
Wir schaffen Wissen – heute für morgen

Questions?

Please ask!

XSPS Power part: Challenge 2



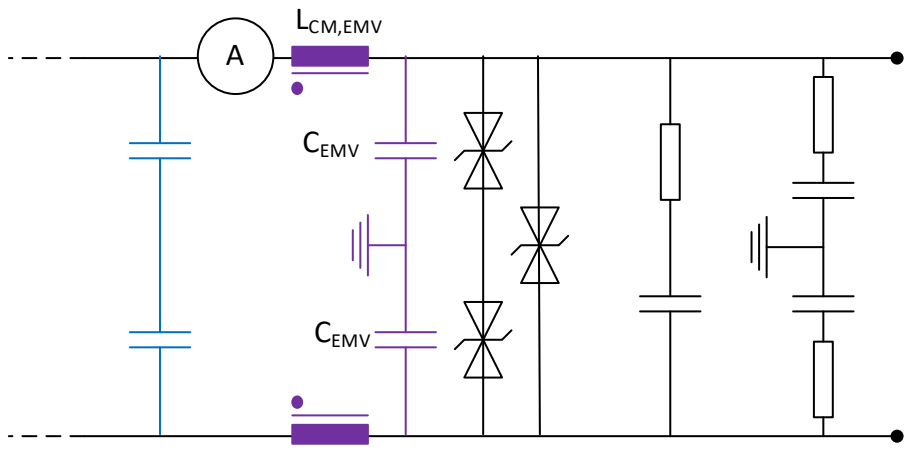
Problem 1:

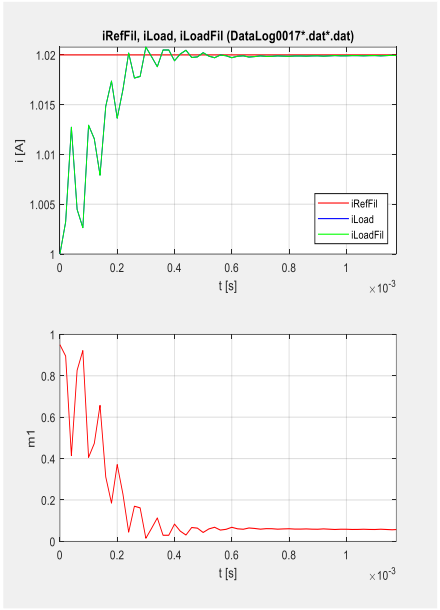
- Parasitic C of TVS-Diodes at output form an oscillation loop with LCM,EMV and C1CM,o / C2o

Solution 1:

- Provide damping legs (for CM and DM)

XSPS Power part: Challenge 2





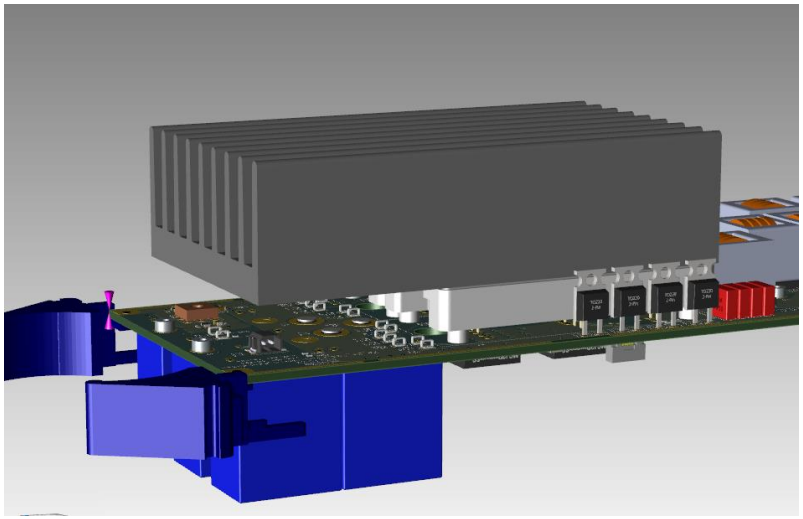
Problem 2:

- All the C in the output (after the current-measurement) form sort of a D-part in the current control loop)
- This limited the bandwidth of the current control loop

Solution 2:

- Leave TVS-diodes and damping legs away for series
- Provide footprint for TVS-diodes with lower capacitance values

PS 50/70A: Challenge EMI



- High dv/dt and di/dt due to hard switching MOSFETs.
- Heatsink mounted to MOSFETs sees capacitive coupled noise.
- Different approaches tested:
  - Heatsink connected to PE
  - Heatsink connected to DC-
  - Heatsink floating
- Expectation: Heatsink connected to PE via 0Ω should be the best solution.
- Test results: Heatsink connected via 100kΩ to PE showed less noise.