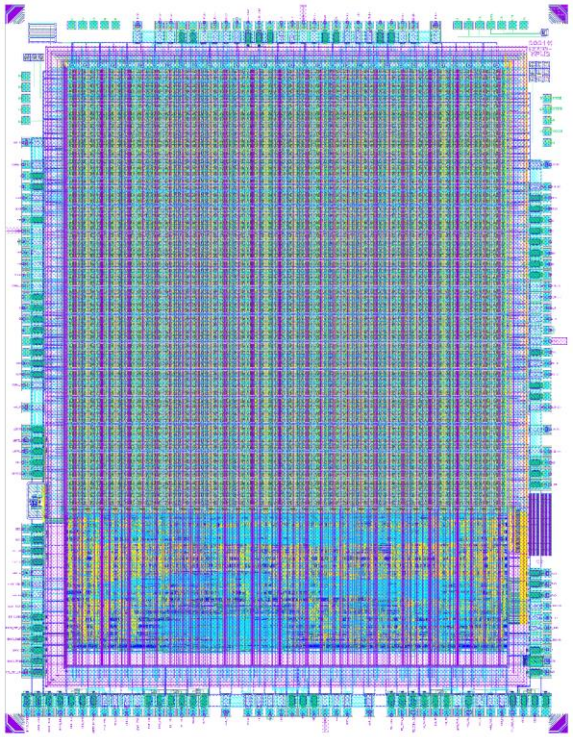
RD50



# Testbeam Analysis

Patrick Sieberer, on behalf of the RD50 CMOS working group

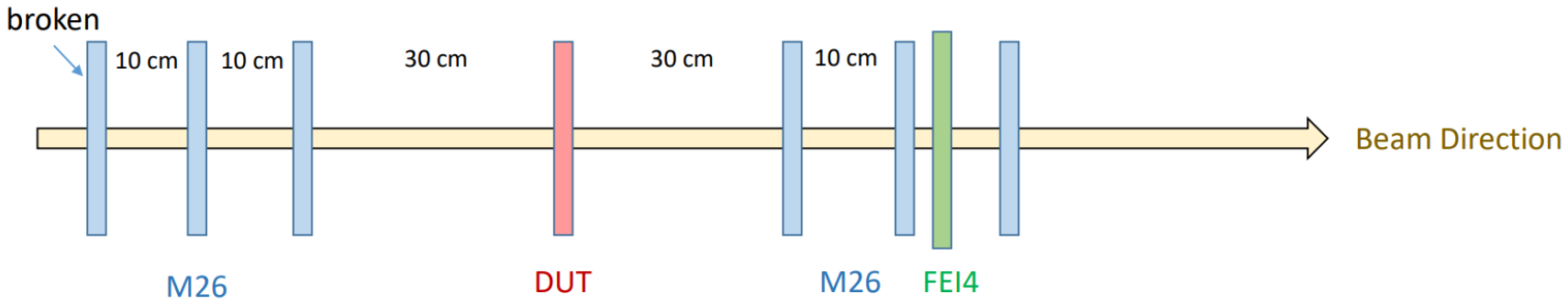
# Introduction



- This is a continuation to my talk last week: https://indico.cern.ch/event/1220741/contributions/5135400/attachments/2544999/4382676/Testbeam_Data_Taking_Analysis.pdf
  - Details about setup and the analysis framework can be found here
- What did change?
  - Noisy pixels masked using the MaskCreator from Corry
    - Less background in plots
- Lot of input from Uwe, Bojan and Bernhard

# Setup

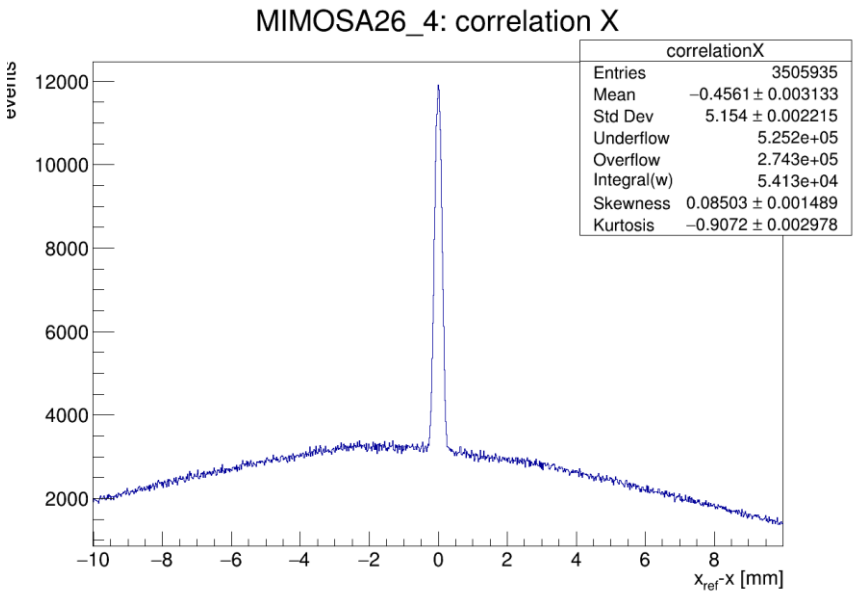


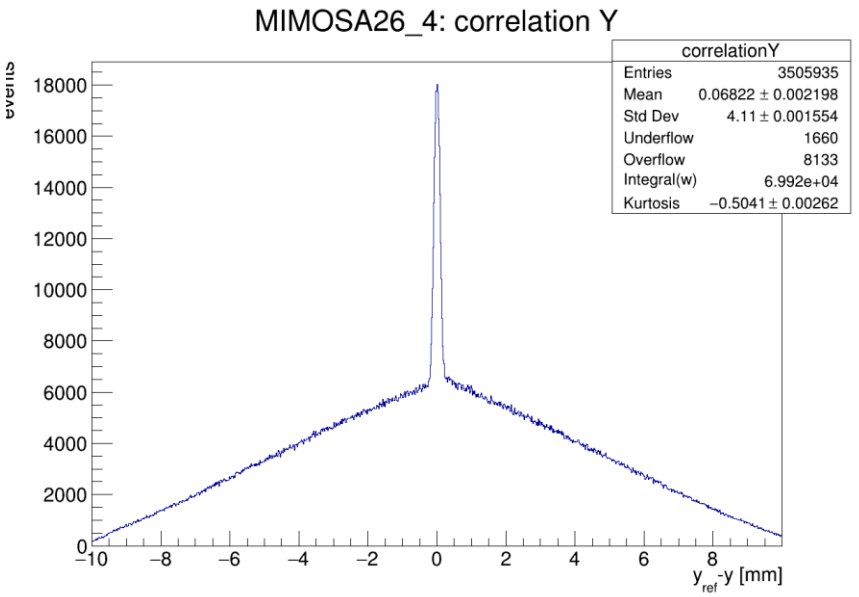



Plot taken from Bojan Hiti

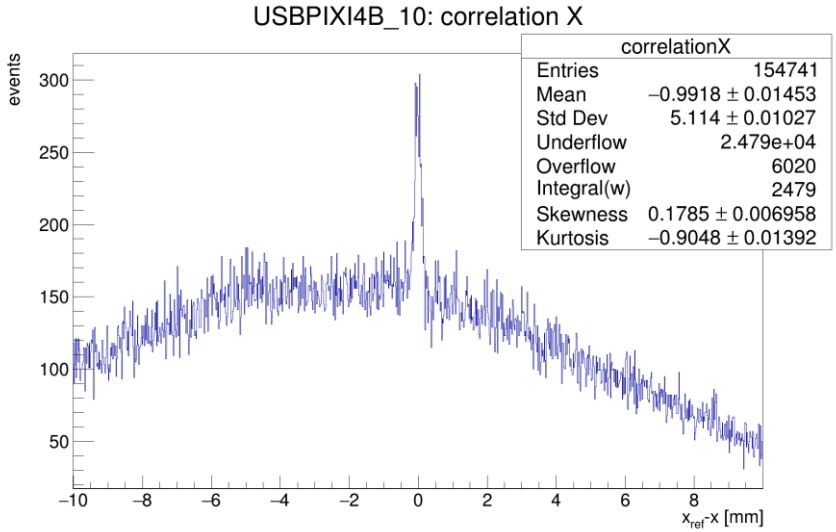
# Correlations M26

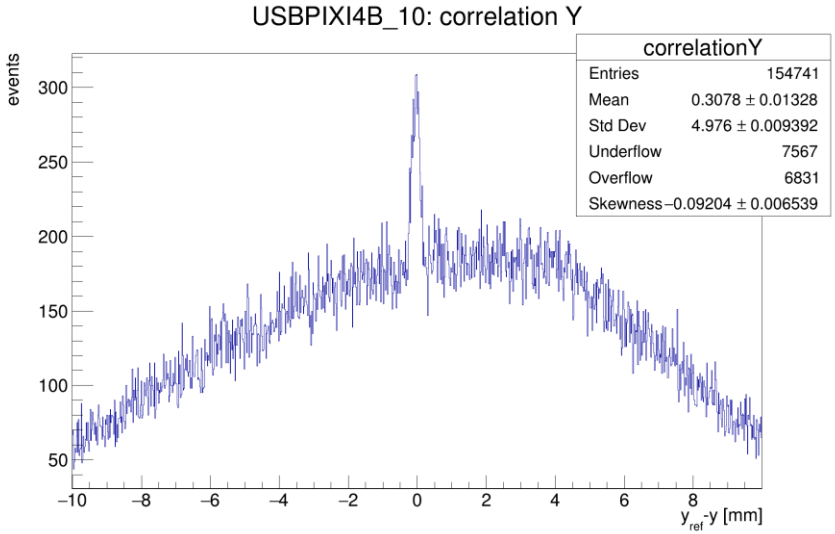




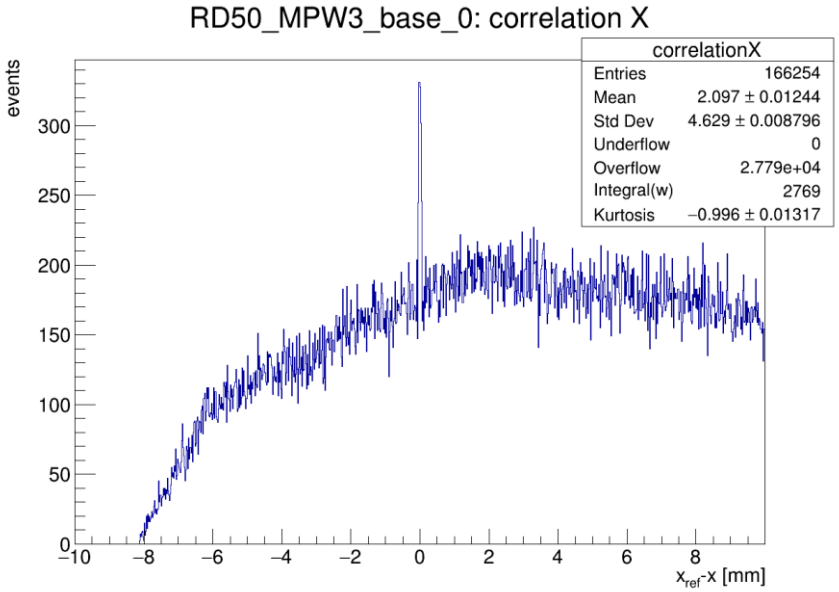



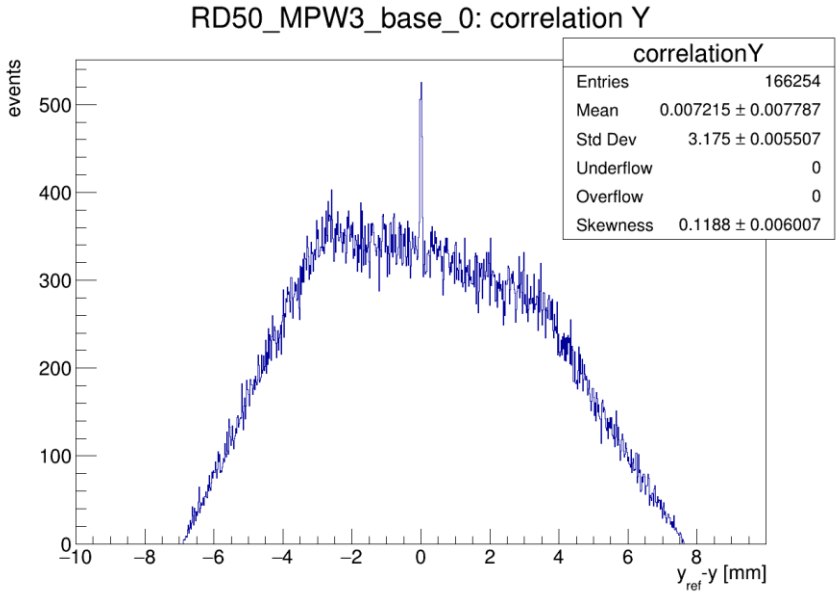
# Correlations FEI4



# Correlations MPW3



# Alignment procedure



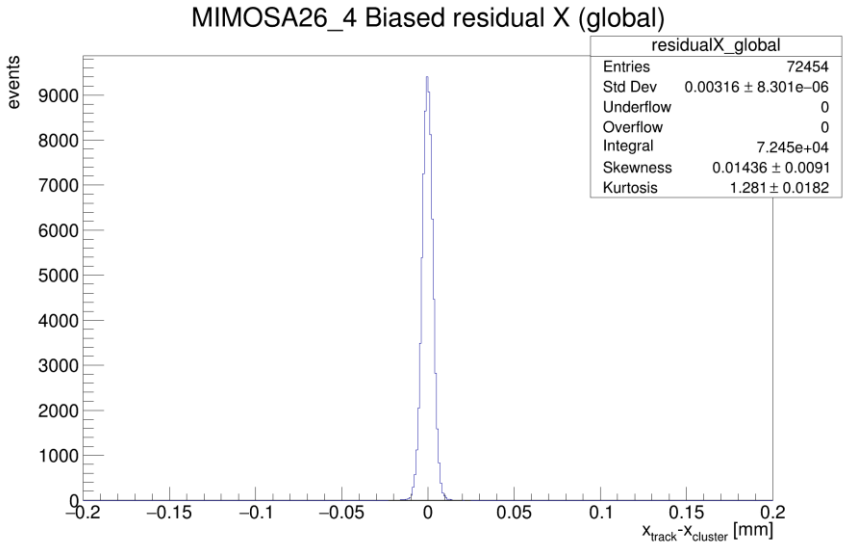
- M26 used as ‘golden standard’

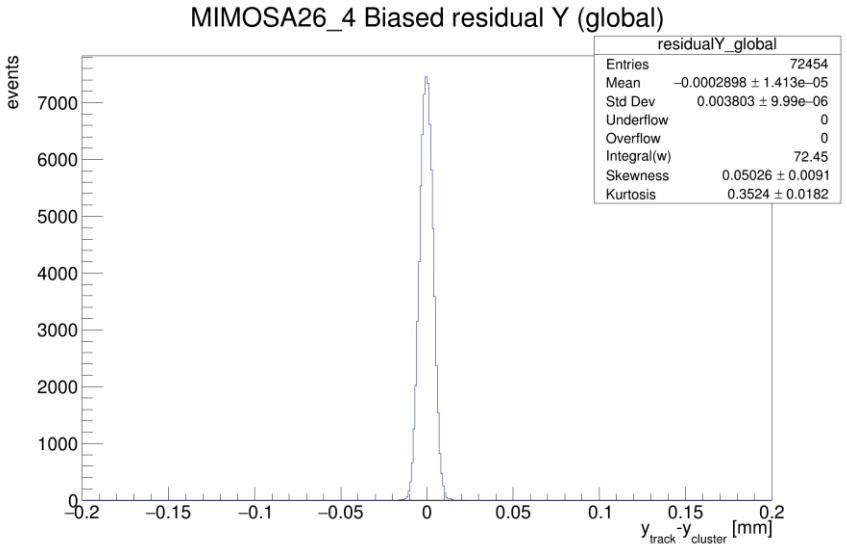
1. Prealignment (all detectors in parallel)
2. Align M26 only (2 steps)
3. Align FEI4 (2 steps, alignment of M26 slightly changed as well)
   - Requiring hits in all 5 M26 planes
4. Align MPW3 (2 steps)
5. Analysis

- 2 + 3 can be done in on step -> To be checked

# Residuals M26

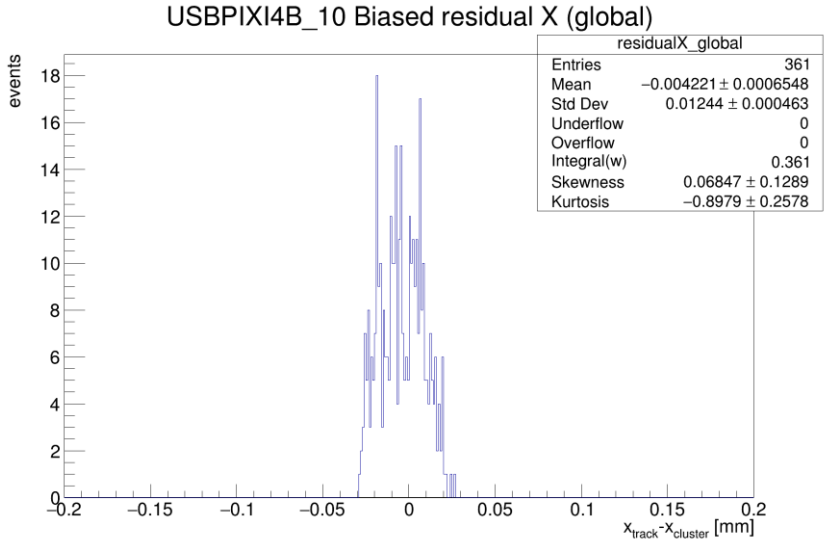


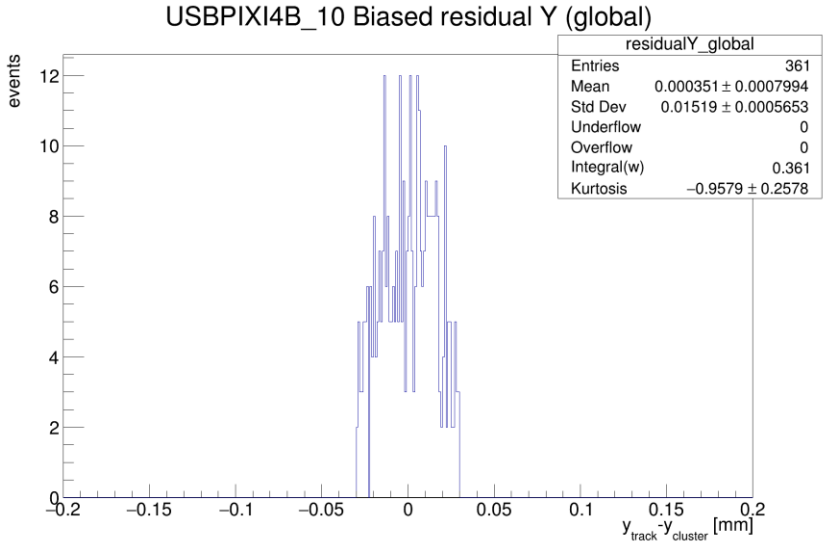


# Residuals FEI4

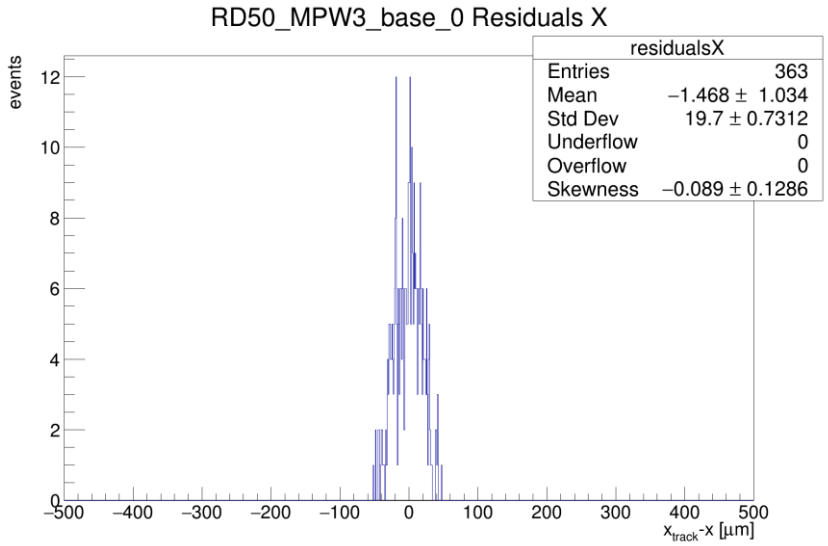


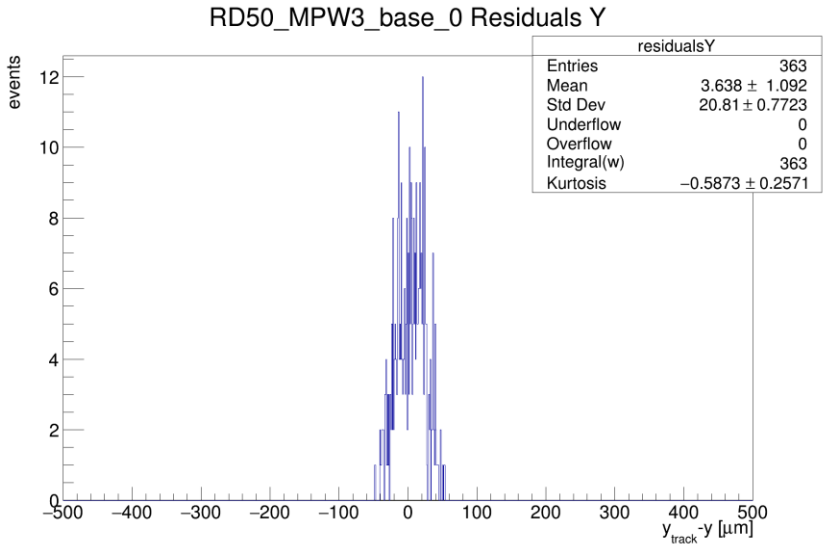


# Residuals MPW3

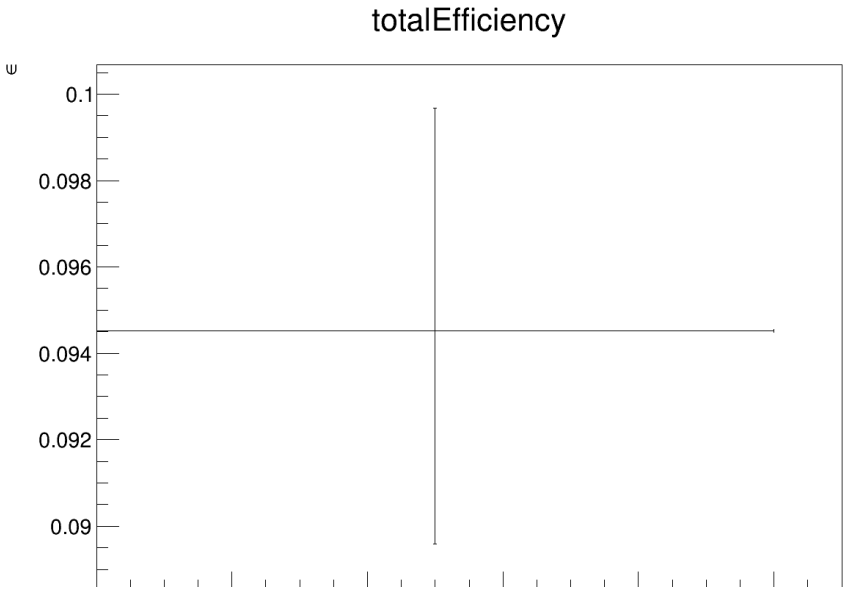





*Attention: Different scale on x-axis than in previous plots!*

# Analysis MPW3




- Without FEI4
  - 3D tracking only
- Efficiency: around 9.45%
  - Very high threshold!
  - Preprocessing to be checked
- FEI4 can help with checking the preprocessor
  - 4D Tracking not yet working…

Take home message: RD50-MPW3 is ready for testbeam, be can integrate the DAQ system, synchronize (somehow ;) … ) and analyze efficiency.

# WHERE TO GO?

# RD50-MPW3



- Shall we design a new Chipboard?

- Shall we test the piggy board?

# RD50-MPW3



- Shall we design a new Chipboard?
  - Yes, we need more boards anyway
  - Ricardo: Modifications easy to implement
- Shall we ~~test~~ *produce* the piggy board?
  - Yes, but we want to check first if modifications needed
    - Most likely not
  - Only small number -> Only useful for testbeam
- Funding?

# RD50-MPW4



Another MPW run is a reasonable option. Current design is not yet ready for engineering run.

- Fixing current issues of RD50-MPW3:
  - Interface between matrix and periphery
    - We know the problem and have a solution
  - Easy generation of global timestamp
    - We know the problem and have a solution
  - High noise in lower half of matrix
    - We have a hint where the problem is
- Adding more features for the future
  - Depends on where we want to go. Telescope? Future detectors (FCC)?
  - Thinning, backside processing
  - Scaling of the sensor (Does require detailed design study to identify limits)

- Can we already start designing? Who would be in?
  - I‘m not available for the digital design anymore
    - (unless somebody has money for a postdoc ;) )

- Need strategy for transition from RD50 to ECFA DRD scheme from 2024 onwards

# RD50-MPW4



Another MPW run is a reasonable option. Current design is not yet ready for engineering run.

- Fixing current issues of RD50-MPW3:
  - Interface between matrix and periphery
    - We know the problem and have a solution
  - Easy generation of global timestamp
    - We know the problem and have a solution
  - High noise in lower half of matrix
    - We have a hint where the problem is

Everybody agreed

We should absolutely try this

- Adding more features for the future
  - Depends on where we want to go. Telescope? Future detectors (FCC)?
  - Thinning, backside processing
  - Scaling of the sensor (Does require detailed design study to identify limits)

We should also try this

- Can we already start designing? Who would be in?
  - I'm not available for the digital design anymore
    - (unless somebody has money for a postdoc ;) )

No clear answer, but we should start thinking about this. Design must not stop measurements of MPW3, there is plenty to do!

- Need strategy for transition from RD50 to ECFA DRD scheme from 2024 onwards

# RD50-MPW4



*There was a lot of discussion if we (as designers of the chips + systems) should push in one direction or if this should be decided by the collaboration board alone.*

*The main outcome was: Let's wait for the collaboration board in Sevilla (which DRD?), but we want show that there are plans for the future of this group:*

- *For short term (2023) we plan to characterize MPW3 (maybe with backside processing) and can start designing MPW4 (at least fixing issues)*
- *For long term, there are various options were to go*

- Need strategy for transition from RD50 to ECFA DRD scheme from 2024 onwards