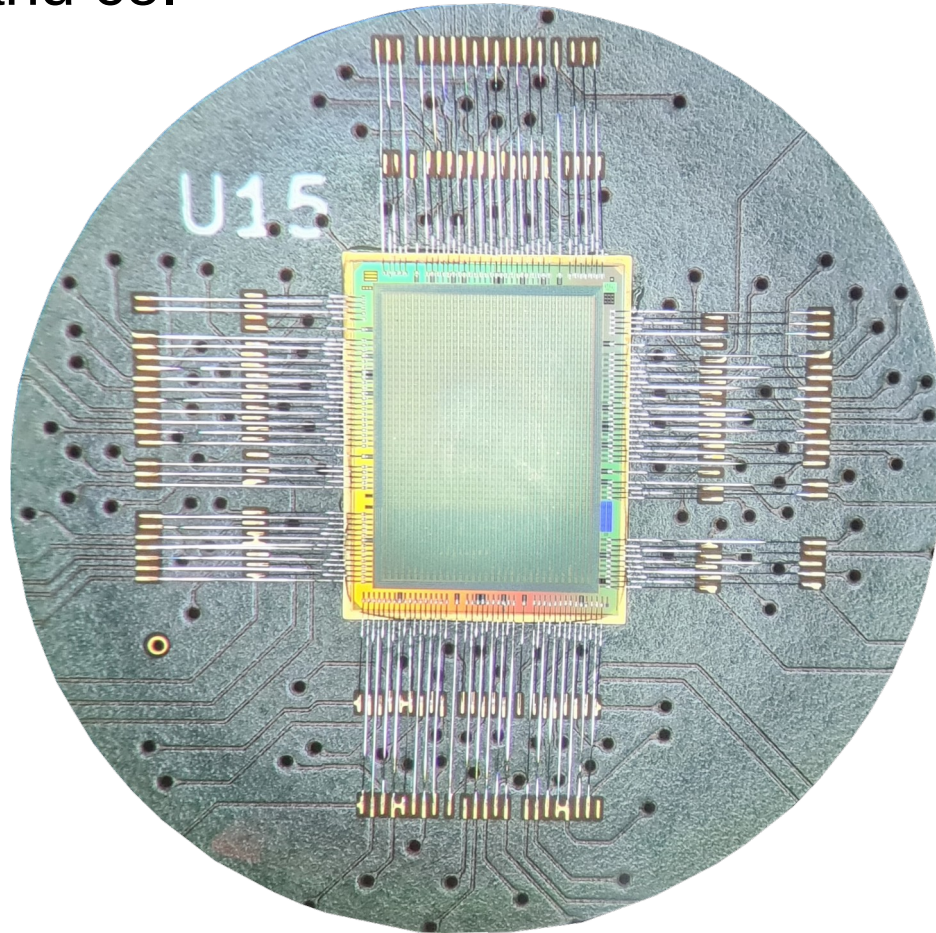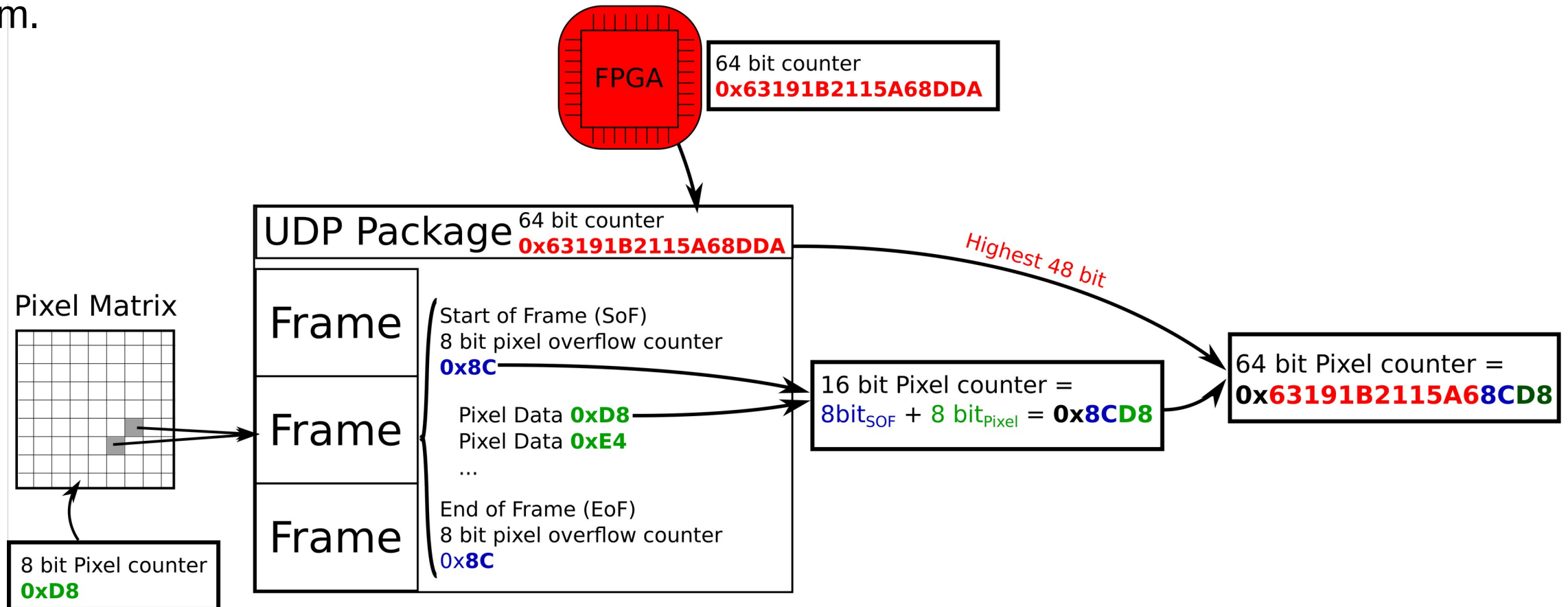# Further Testbeam Analysis

With lots of help and input from
Patrick, Bernhard, Bojan and co.

# Testbeam Data Synchronization

- Due to different readout methods of different devices, data synchronization requires some effort.
- As mentioned by Sam and Patrick, we added a "global pixel timestamp" during the test beam.
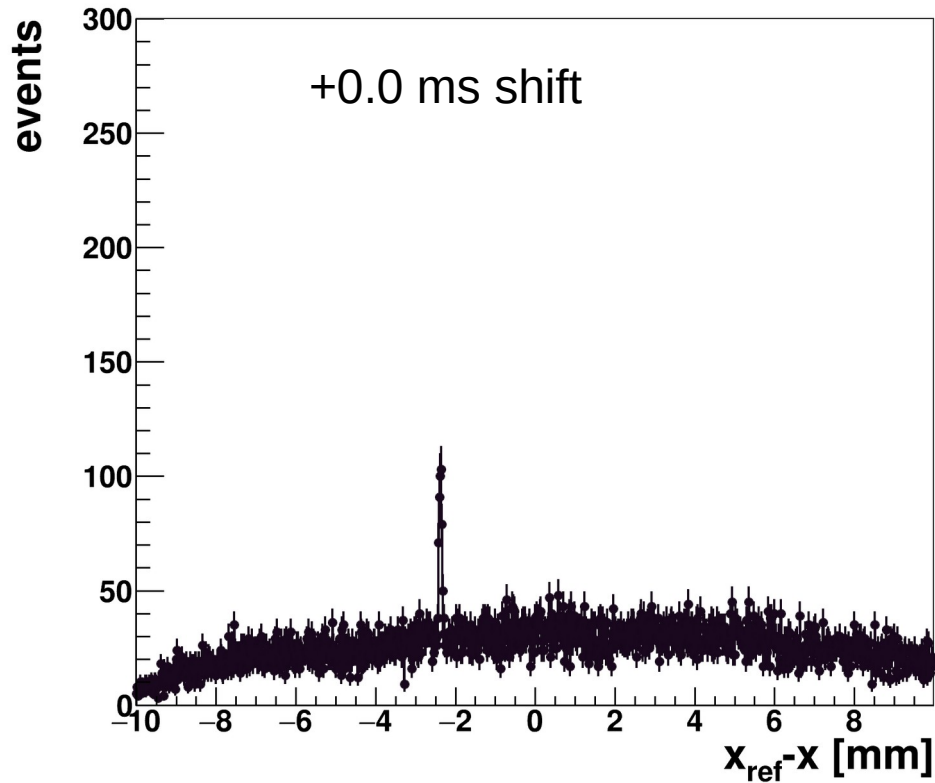
# Testbeam Data Synchronization

- This global pixel timestamp is then used to assign to the correct "event" which is defined by the AIDA TLU + Mimosa Telescope

- No correlations were visible during testbeam as such in offline analysis different time offsets were used to check for correlations
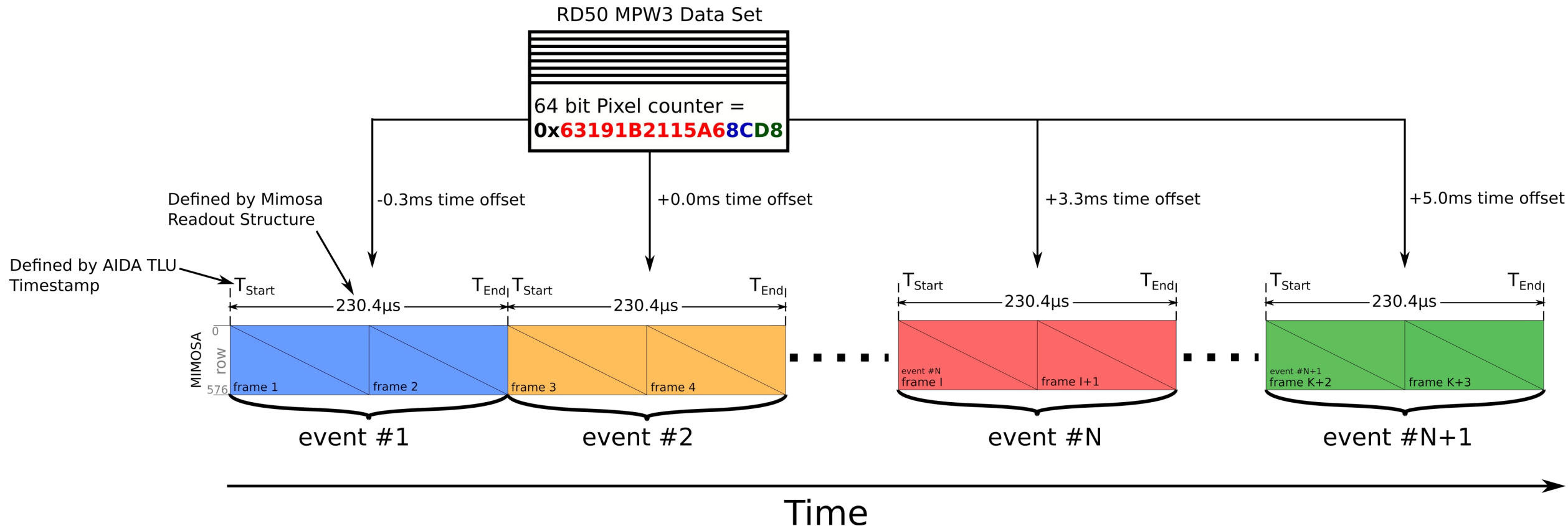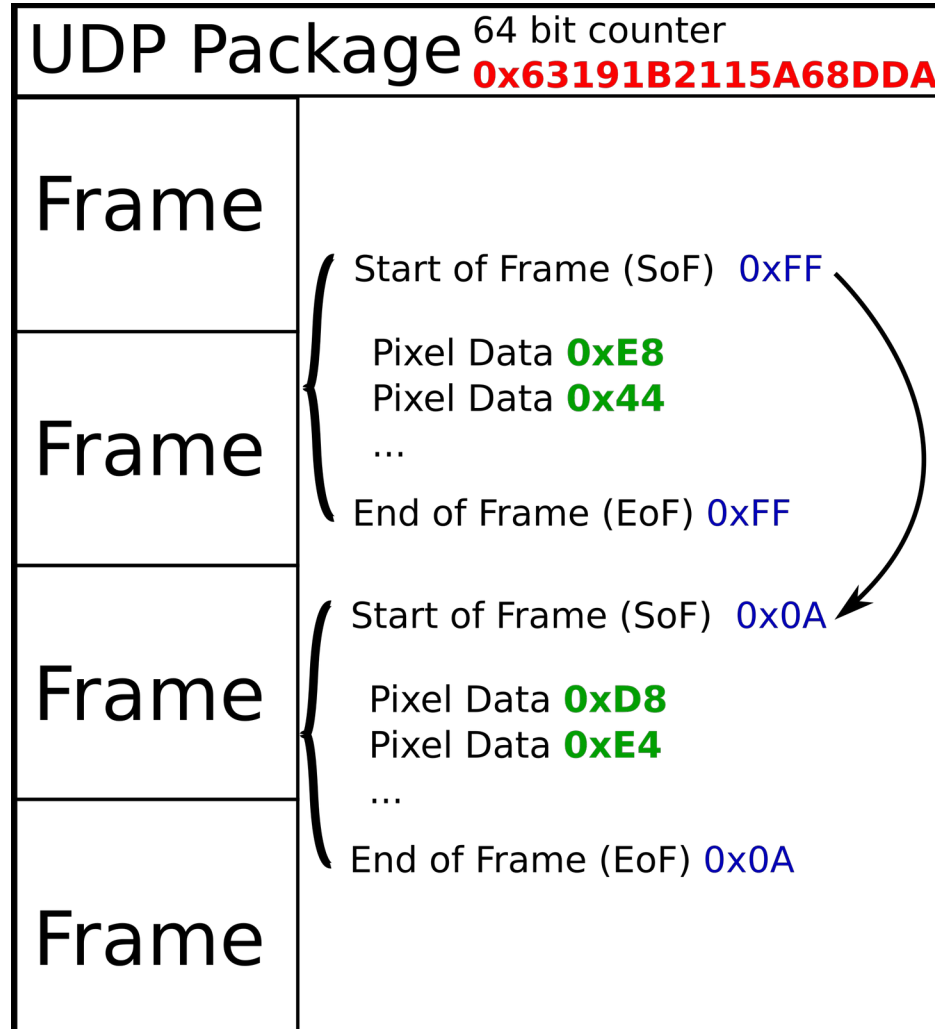
# Testbeam Data Synchronization

- Found correlations with an offset of ~3.2 ms for run 970 (already reported by Patrick last week).

- Found also correlations in run 973 with highest peaks at an offset of ~3.3ms and 0.0ms!

RD50 Weekly Meeting      Uwe Kraemer      Nik|hef
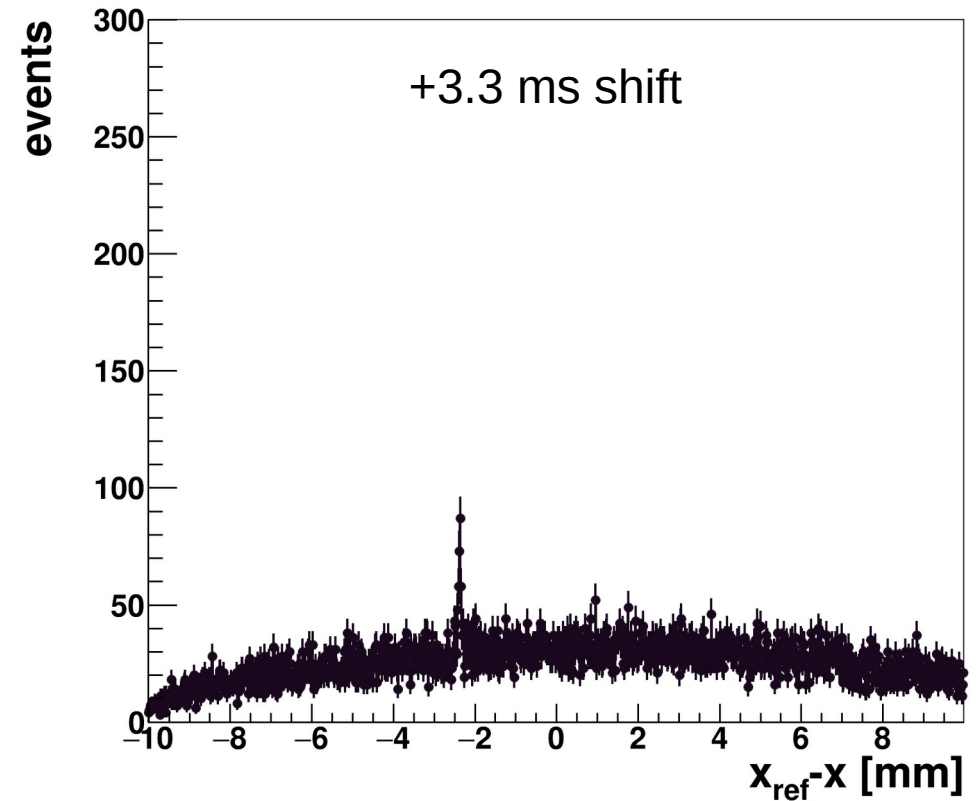
# Testbeam Data Synchronization

- Most likely due to overflow of 16 bit counter within UDP package

- Until this is fixed we artificially lower our efficiency for the system

- Could also mean some data is at a shift of 6.6 ms

UDP Package  64 bit counter
**0x63191B2115A68DDA**

Frame

Frame
- Start of Frame (SoF)  0xFF
- Pixel Data **0xE8**
- Pixel Data **0x44**
- ...
- End of Frame (EoF)  0xFF

Frame
- Start of Frame (SoF)  0x0A
- Pixel Data **0xD8**
- Pixel Data **0xE4**
- ...
- End of Frame (EoF)  0x0A

Frame

Overflow Within UDP package
Need to adjust 17th bit
(and possible higher for multiple OF)

**50ns * 2^16 = 3.2768 ms**

# Preliminary Efficiency

- Checked efficiency for run 973 for both 0.0 ms shift and 3.4 ms shift

- Track efficiency: $\eta = \dfrac{N_{tracks\_w\_hits}}{N_{tracks\_tot.}} = 6.5\% \text{ and } 4.2\%$
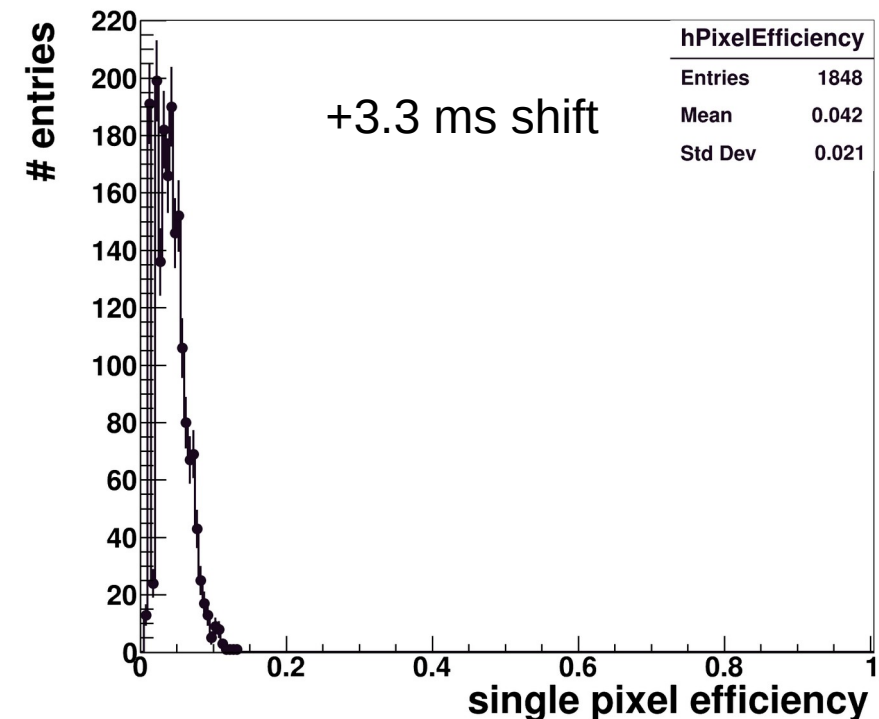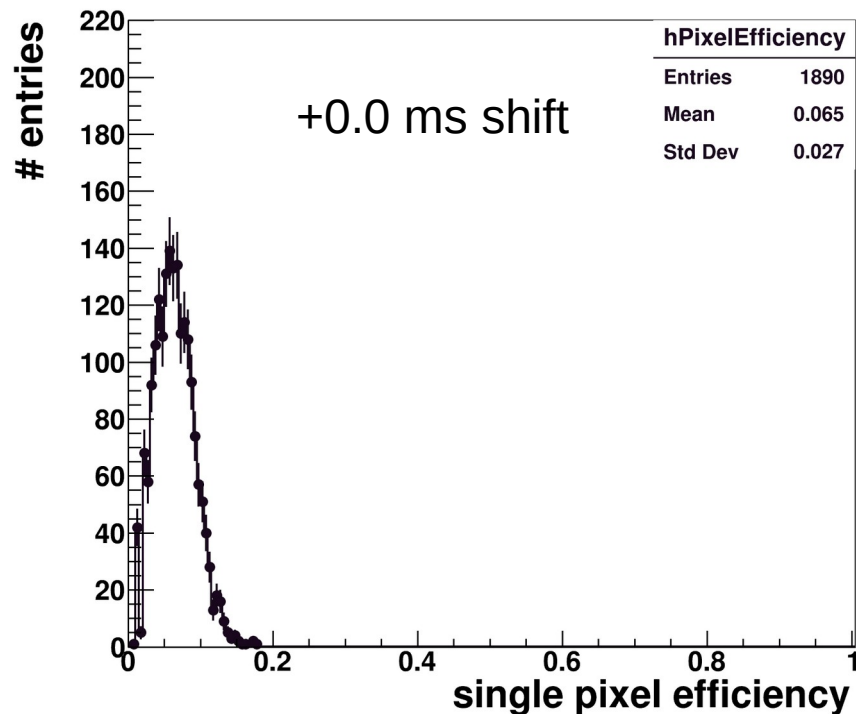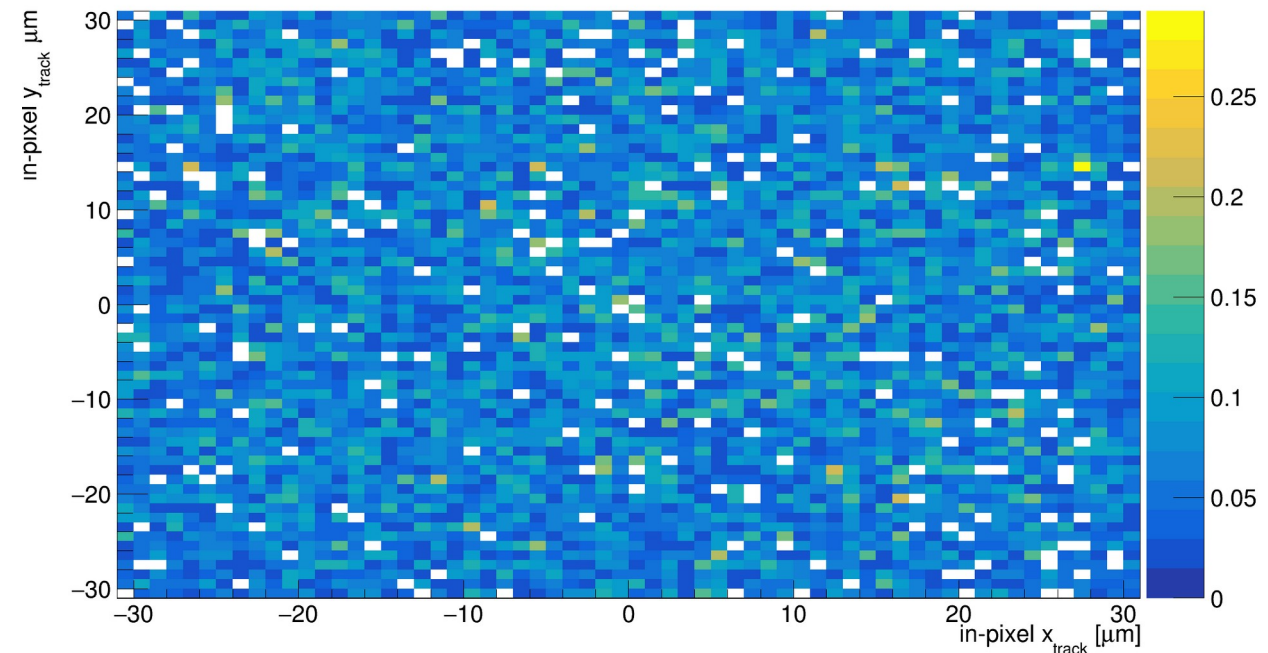
# In-Pixel and Chip Efficiency (0 ms shift)

- Overall number of entries is rather low though no major difference over the chip is seen

- In-pixel efficiency is also fairly homogeneous (expected drop to edges where charge is shared between 2 pixels meaning more likely to be below threshold?)



RD50_MPW3_base_0 Chip efficiency map
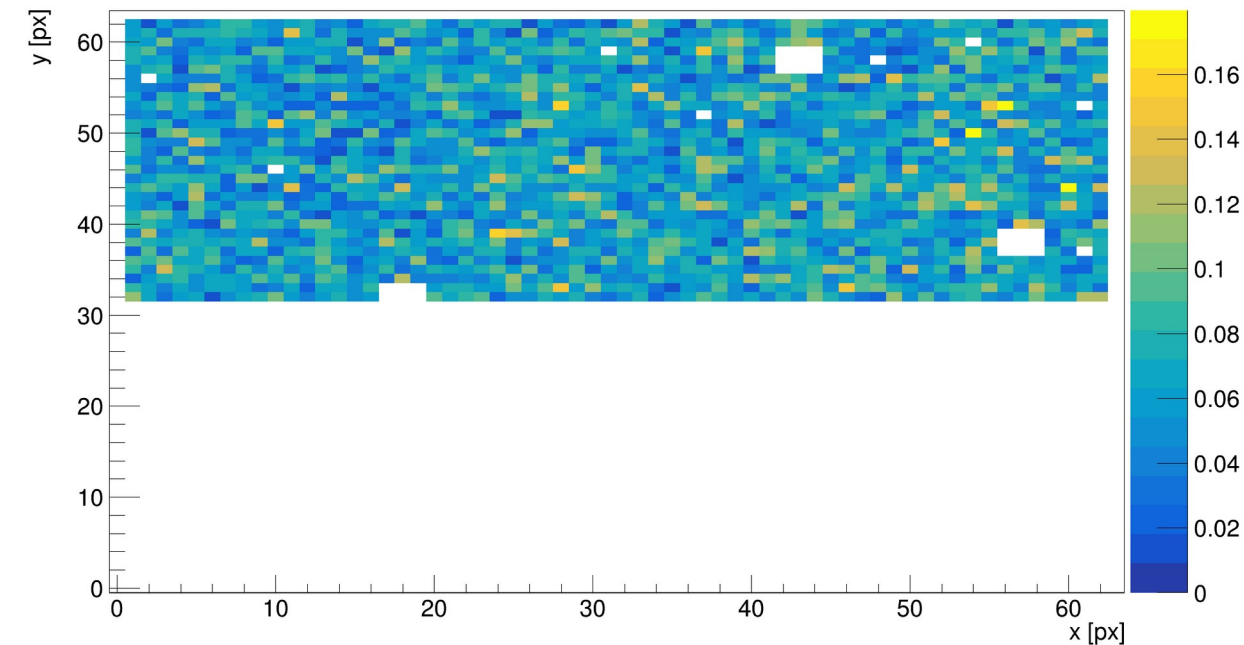


RD50_MPW3_base_0 Pixel efficiency map

# Backup slides

Uwe Kraemer