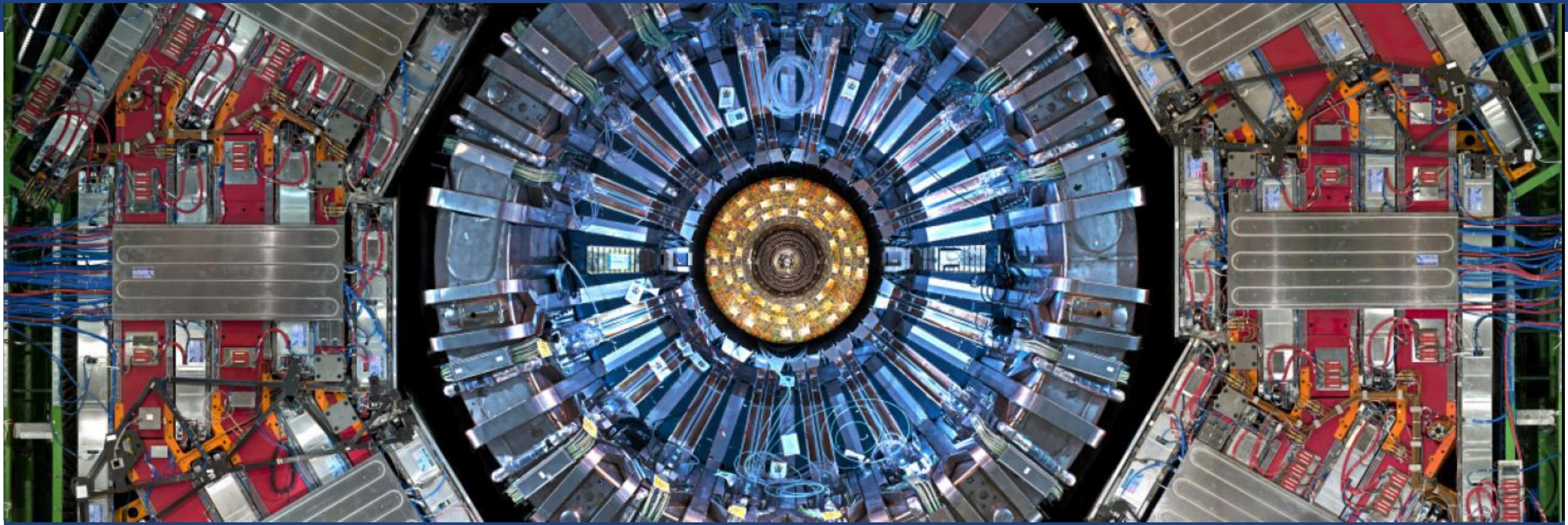


Serial powering for the Phase 2 upgrade of the CMS pixel detector and RD53A pixel module performance

Vasilije Perovic

symmetry
dimensions of particle physics

topics

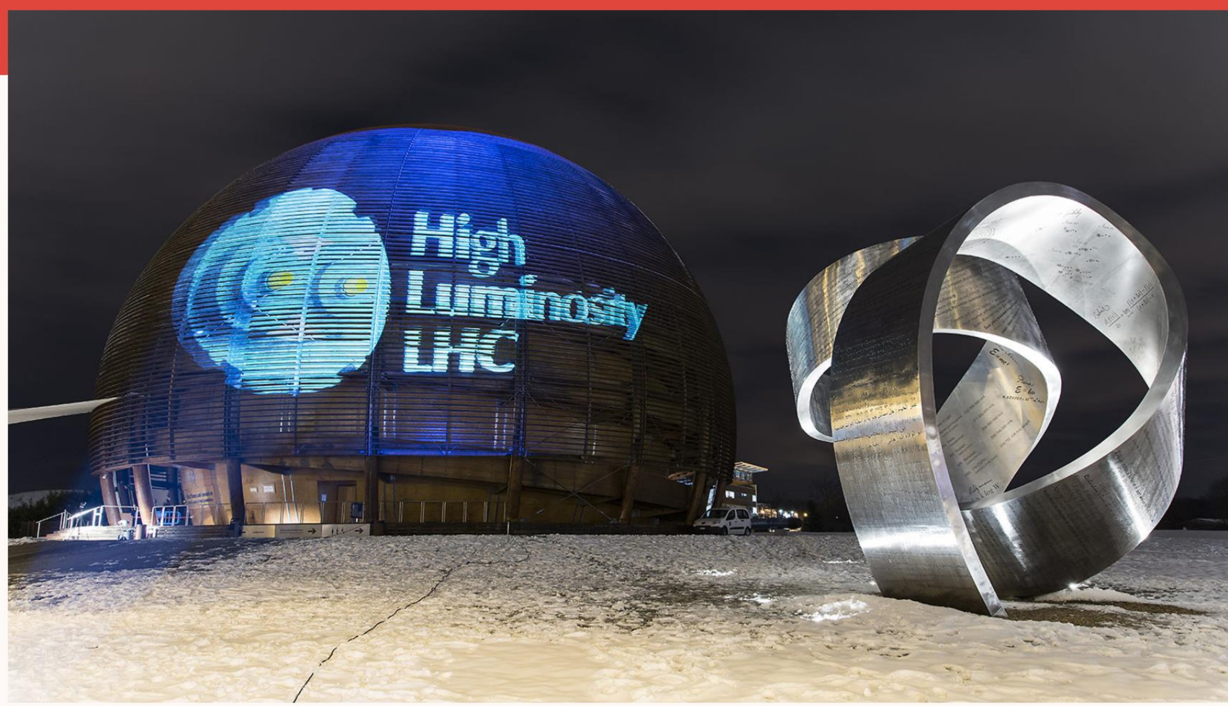
follow +

A joint Fermilab/SLAC publication

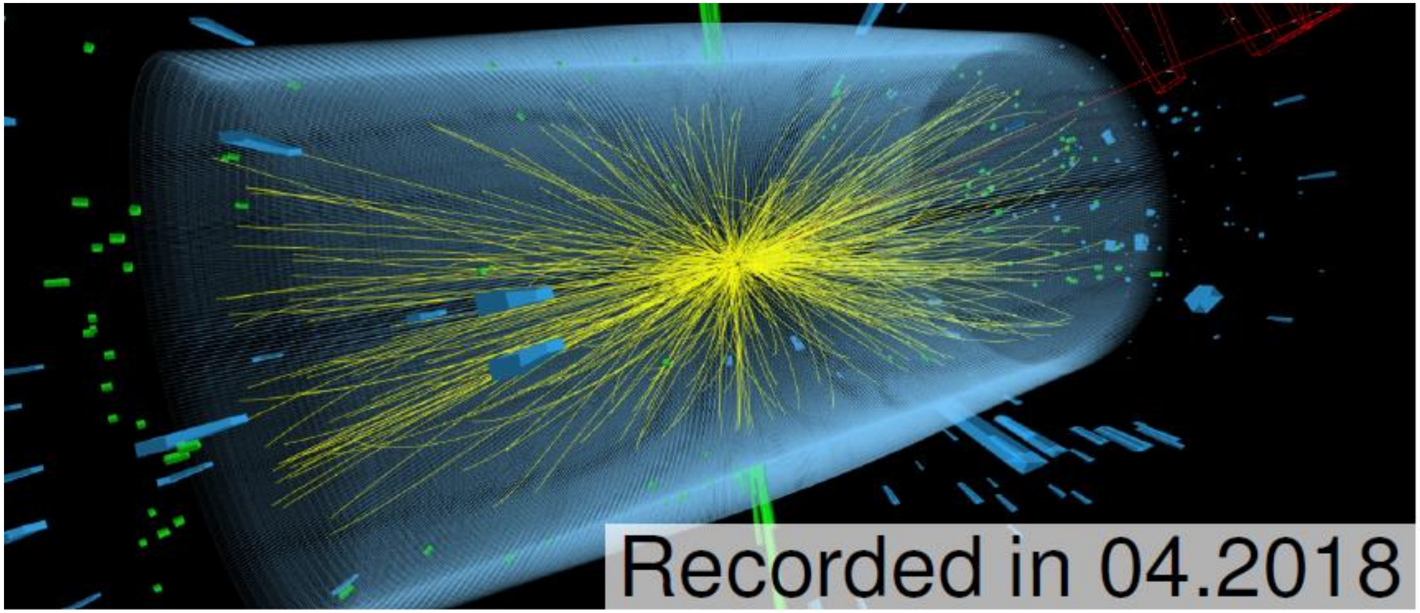
Next up: A turbocharged LHC

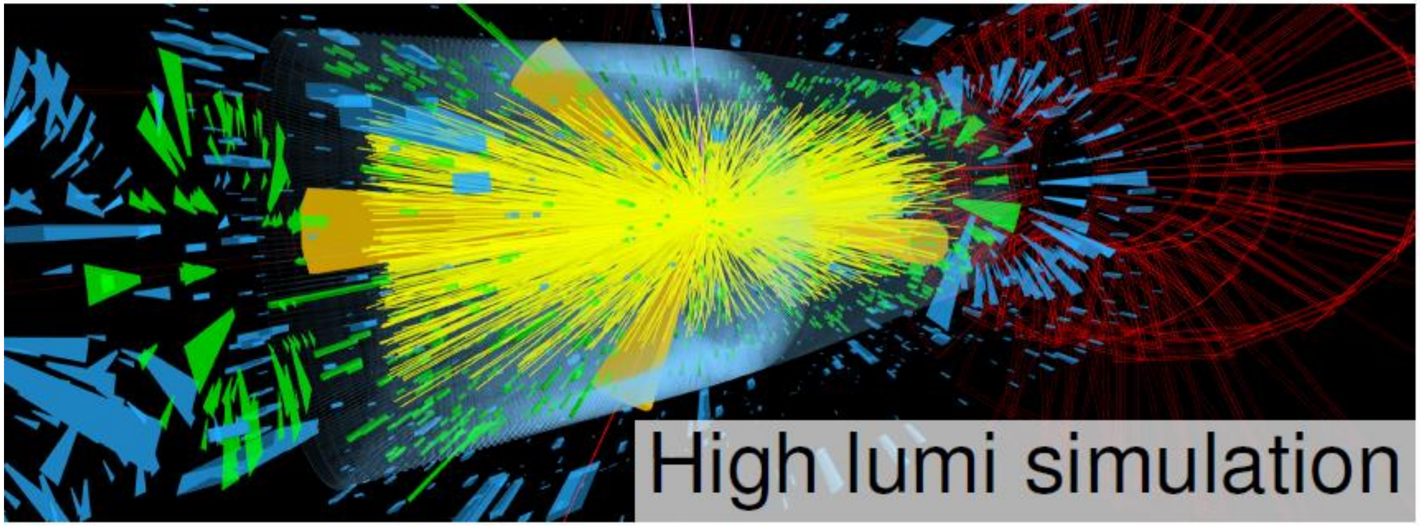
10/29/15 | By Sarah Charley

Physicists are already preparing upgrades that will increase the physics reach of the Large Hadron Collider in the next decade.

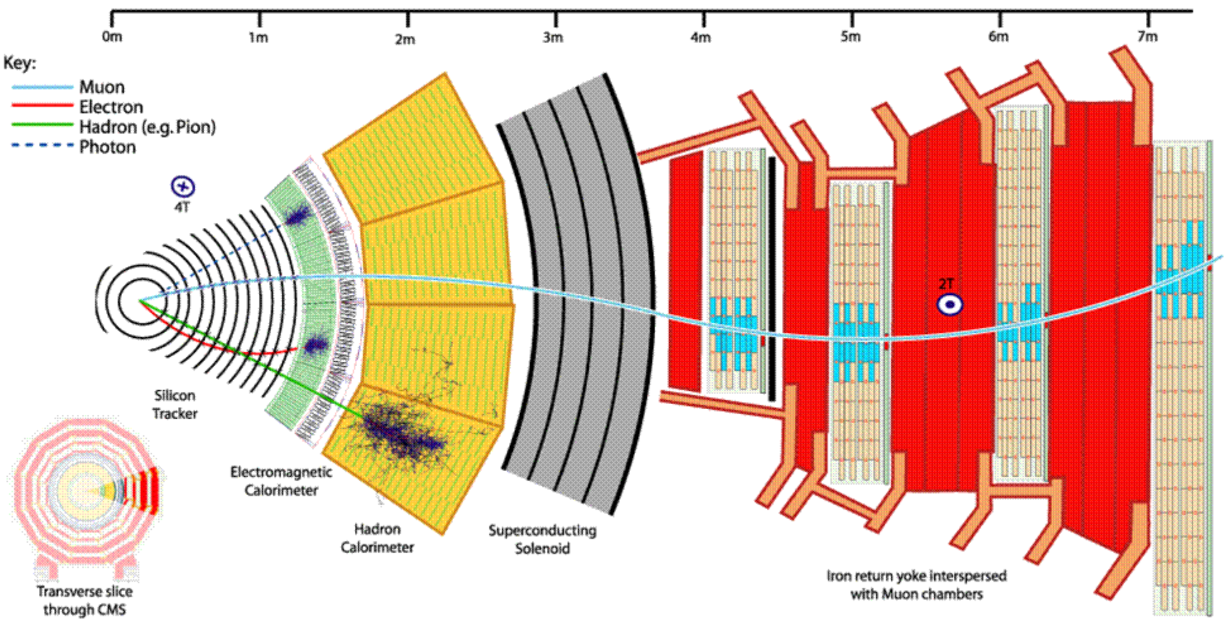


Maximilien Brice, CERN


Recorded in 04.2018

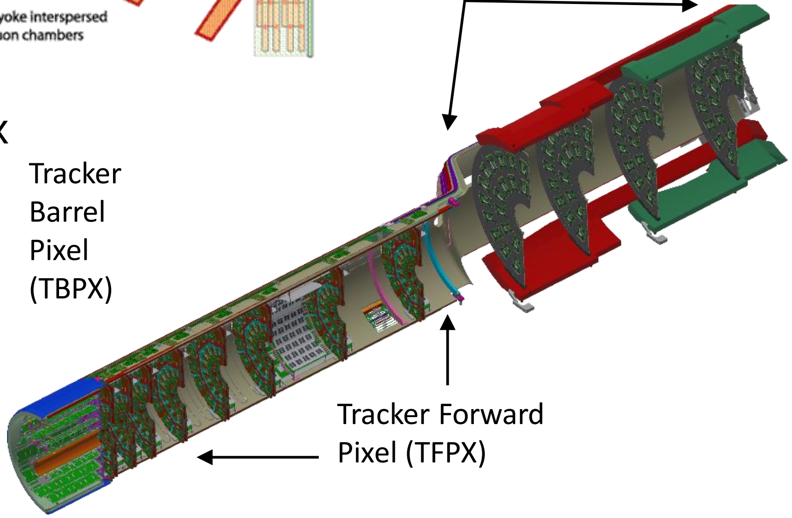

High lumi simulation

LHC plan and CMS upgrade



- Instantaneous luminosity (design) to increase 7.5x
- → Flux up to 3.2 GHz/cm^2
- → Required latency 12.5 μs

- **A number of technical novelties are needed**



Some of the challenges for the Phase 2 Inner Tracker

- High luminosity → **Radiation-hard design**
- Increased latency and hit rate → **High supply current (~2 A /chip, ~30 kA total)**
  - Smaller feature size (65nm CMOS)
  - Increased granularity
- Good tracking performance → **Low mass design**

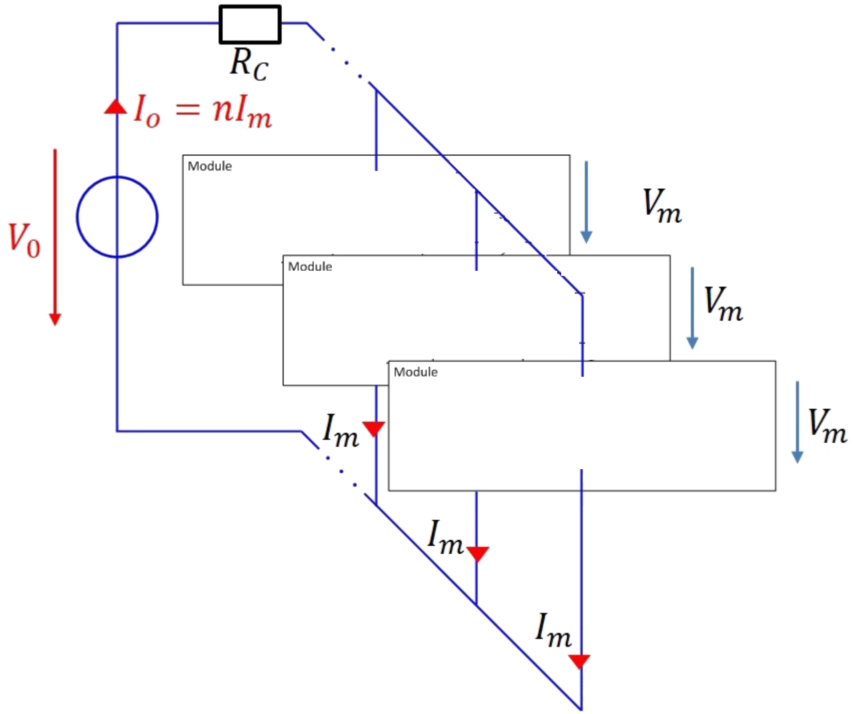
(High supply current and low mass design → **Serial Powering**)

Serial powering has never been attempted before in a HEP experiment.

JINST 12 (2017) no.03, P03004
Nucl.Instrum.Meth. A557 (2006) 445-459
Nucl.Instrum.Meth. A511 (2003) 174-179

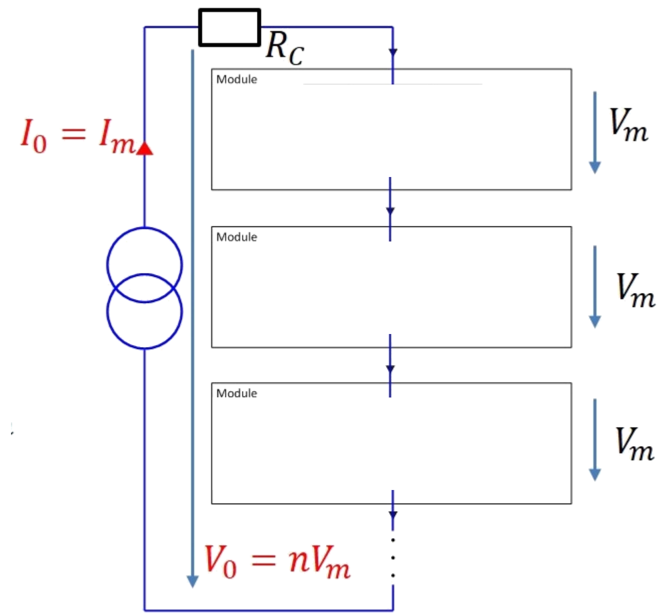
Serial powering

Parallel powering (current detector)



Power loss in parallel powering ~ $n^2 I_m^2 R_C$

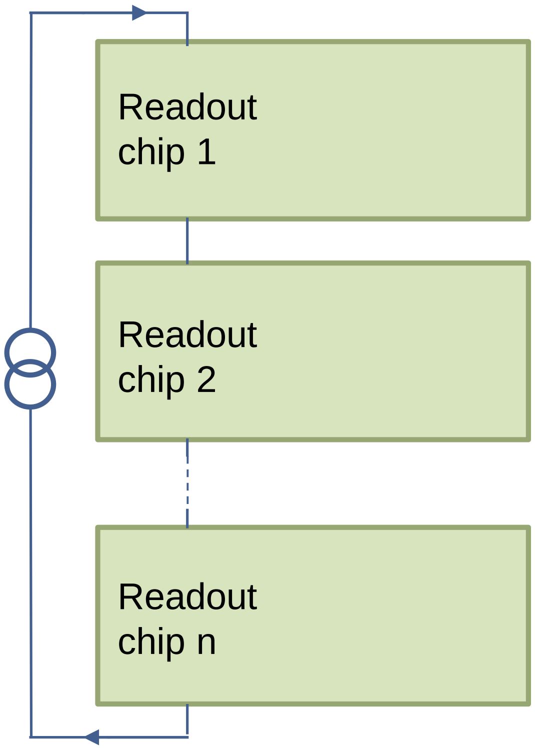
Serial powering (Phase 2 detector)



Power loss in serial powering ~ $I_m^2 R_C$

Serial powering

- Constant input current
- Different local grounds
  → on-chip reference needed



Serial powering

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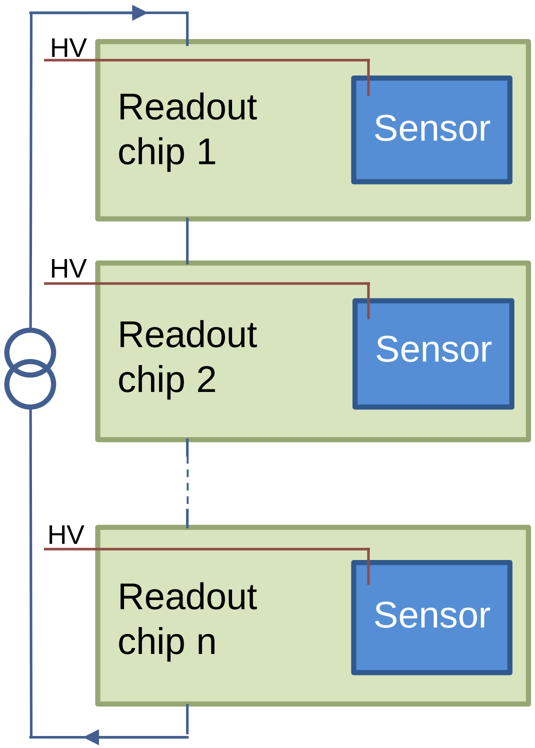
- High Voltage distributed in parallel
  - Planar sensors can work with this
  - 3D sensors require higher HV granularity



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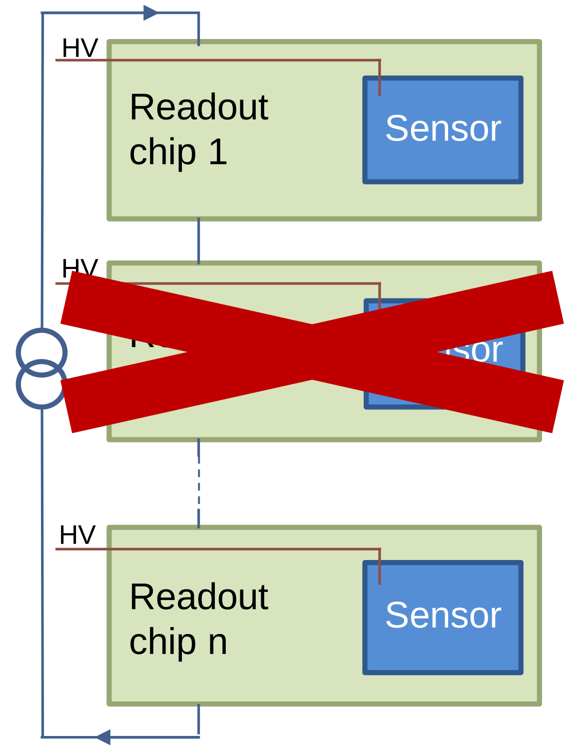
- Single failure can compromise the chain



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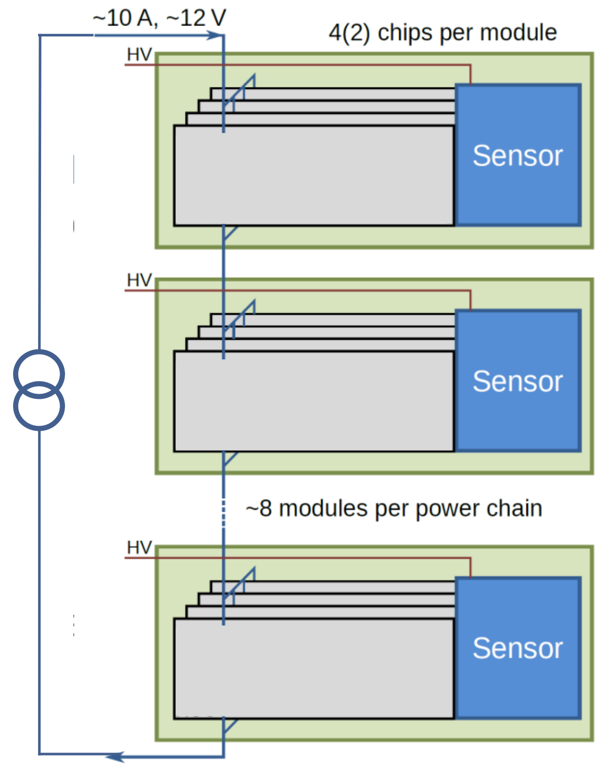
  → Modules with parallel-powered chips



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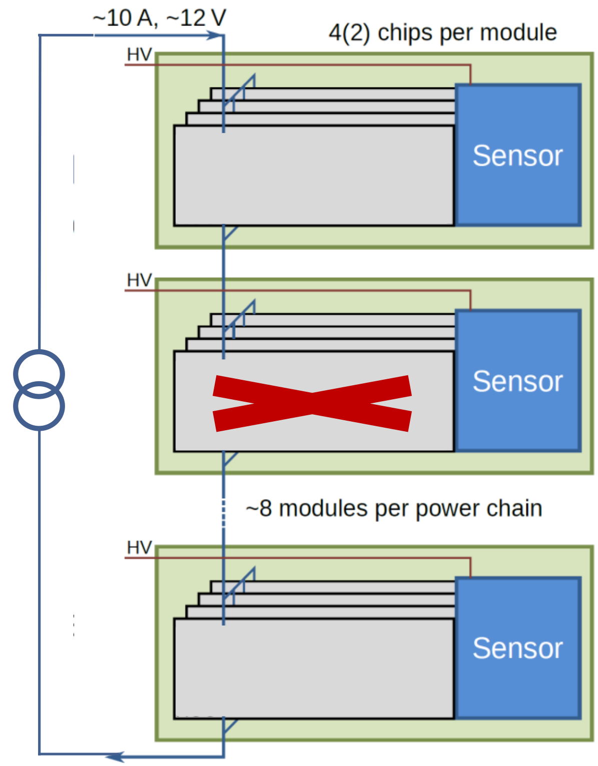
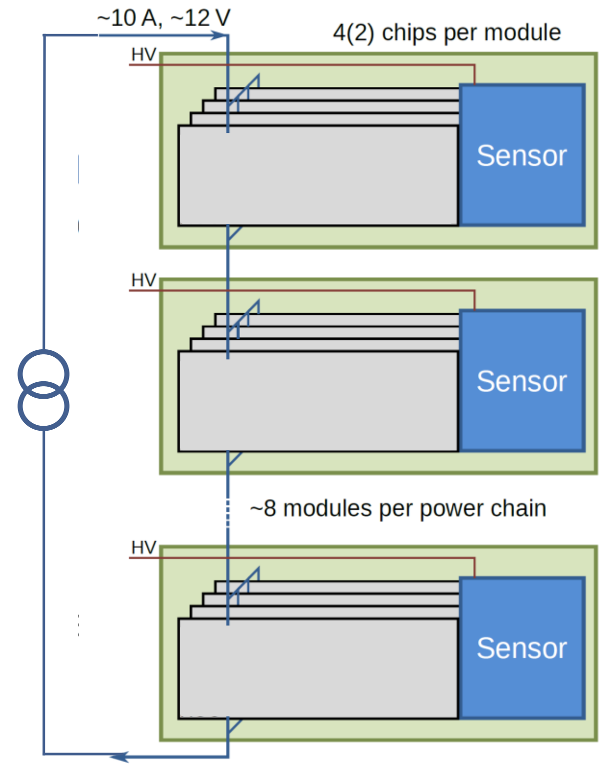


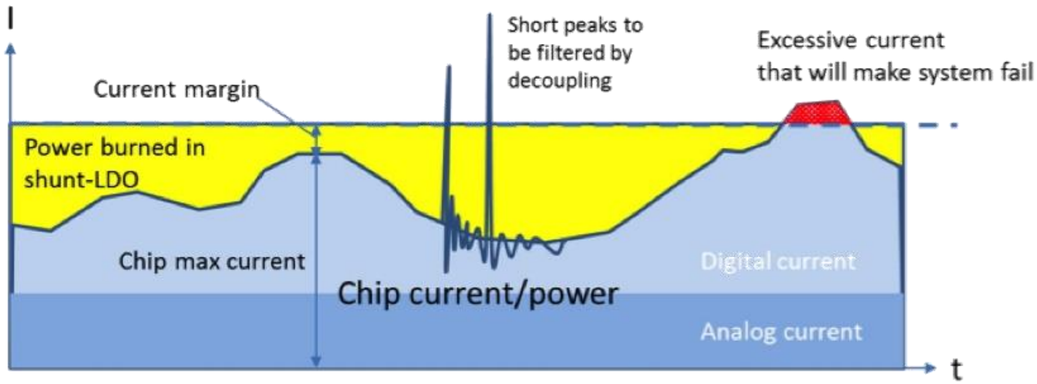
Serial powering

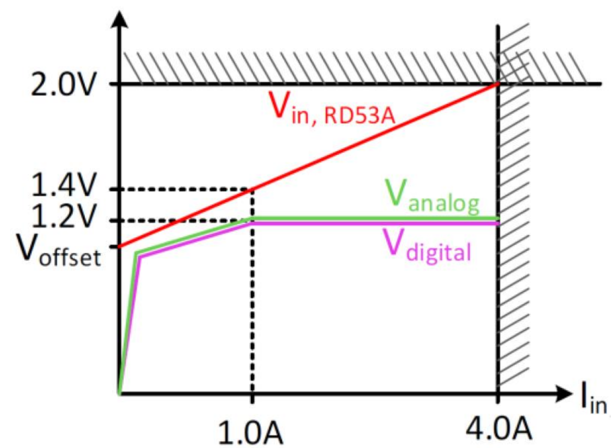
- **Constant input current**
- Different local grounds
  → **on-chip reference** needed
- High Voltage distributed in parallel
  - Planar sensors can work with this
  - 3D sensors require higher HV granularity
- Single failure can compromise the chain
  → Modules with parallel-powered chips
- **Ohmic load to the supply**



Serial powering – Shunt LDO regulator

- Constant voltage from the constant supply current
- Shunt + Low Dropout Regulator → ohmic behaviour is seen by the power supply

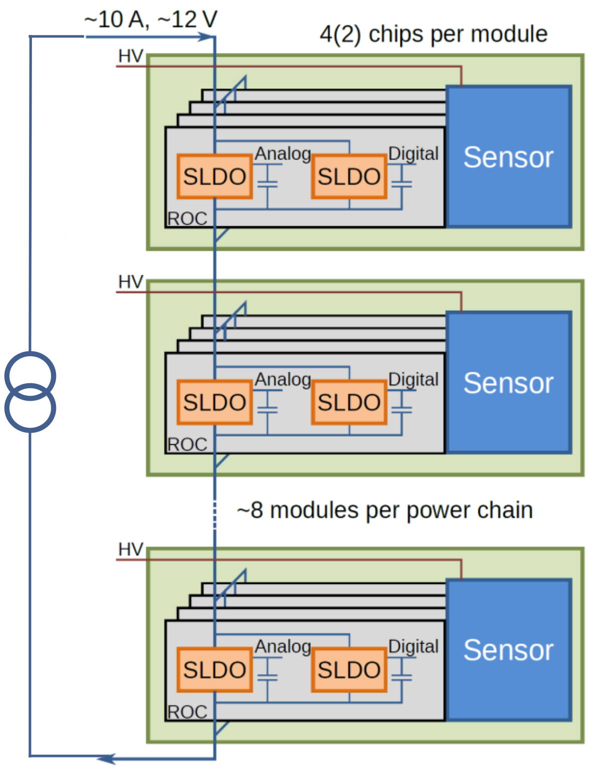




Serial powering

- Modules → **serial powering**
- Chips on modules → **parallel powering**
- HV distribution → **parallel** and referenced to the local grounds in the **serial** chain
- Communication → readout electronics referenced to global ground.

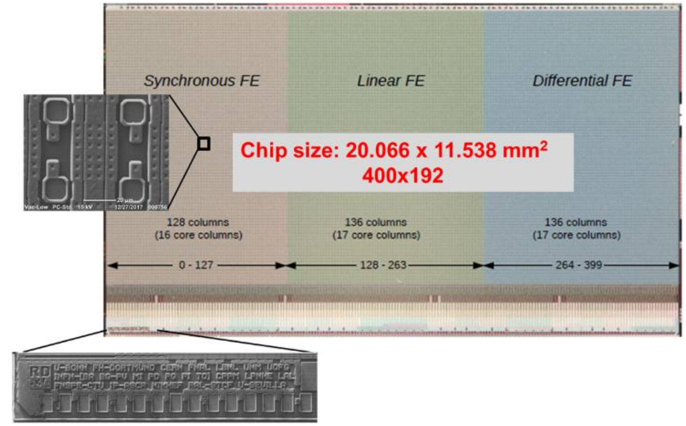
- *We will essentially use a <u>mixed powering scheme</u>*

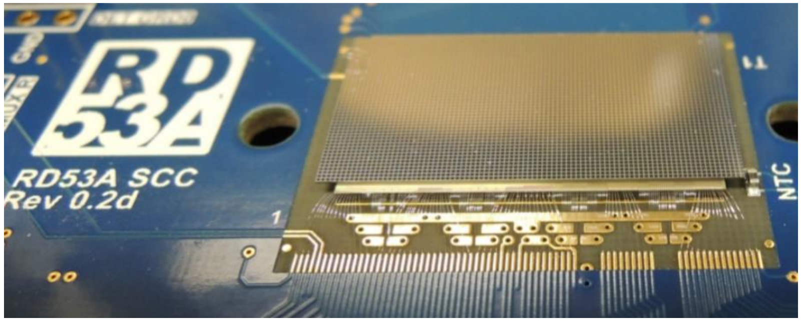


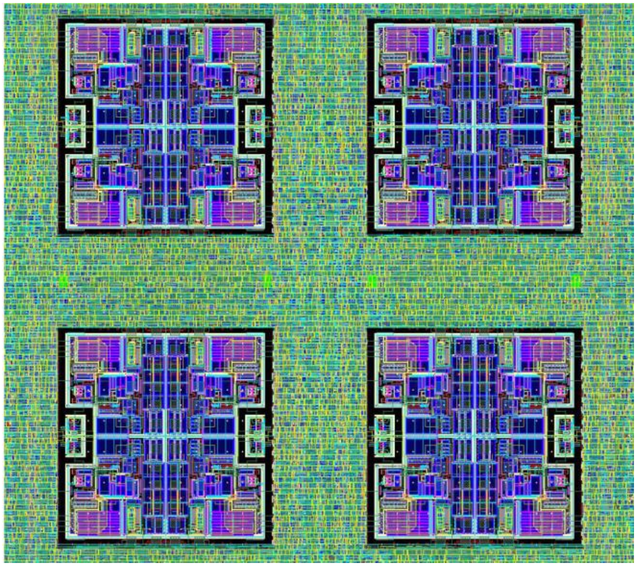
Prototype test chip – RD53A

- Joint ATLAS and CMS effort
- About ½ size of the final chip (~1 A current)
- 65 nm CMOS technology

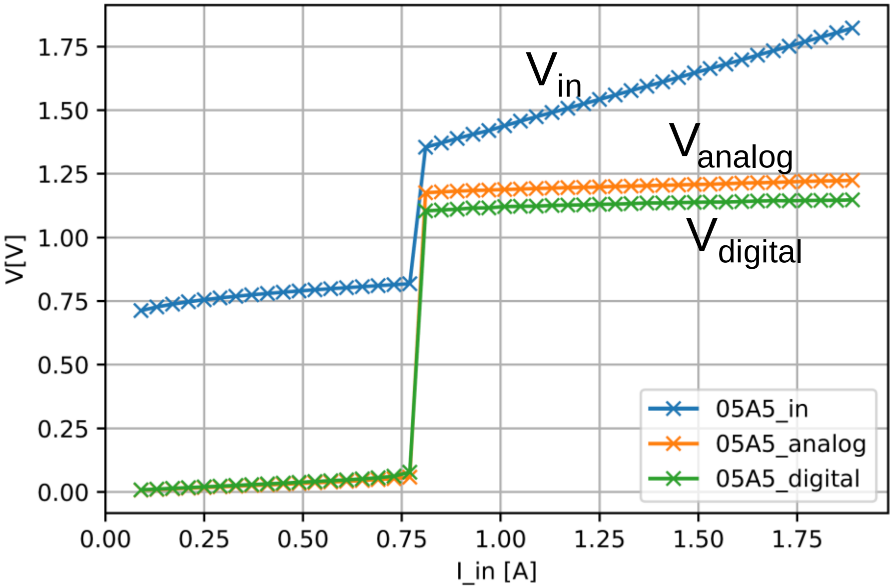
- “Analog islands in a digital sea”

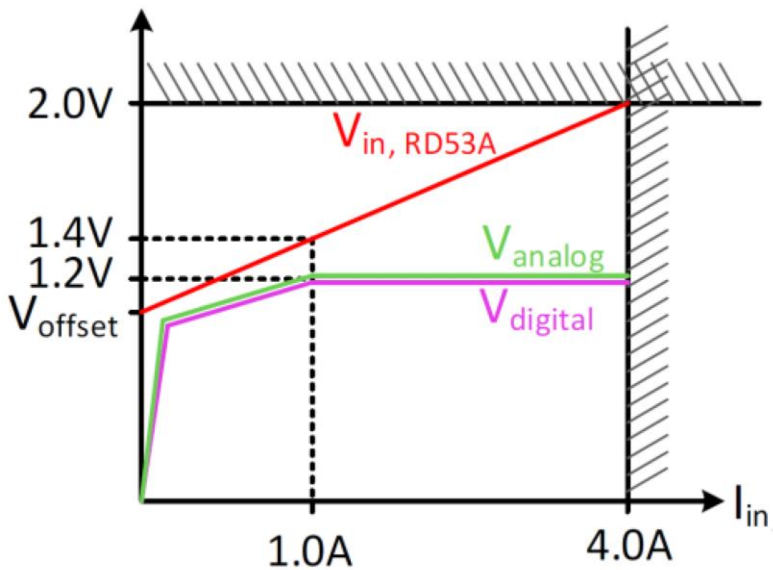






Serial Powering – RD53A SLDO regulator





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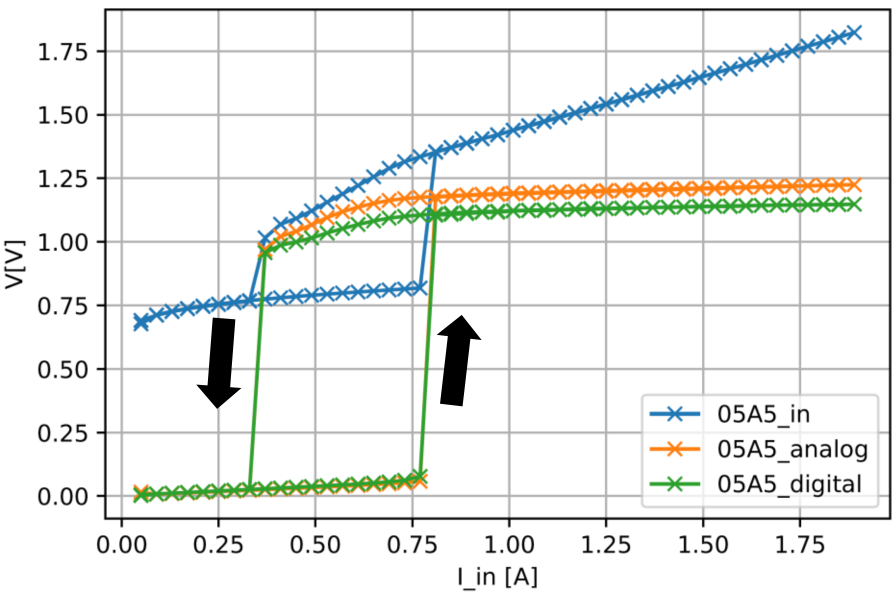
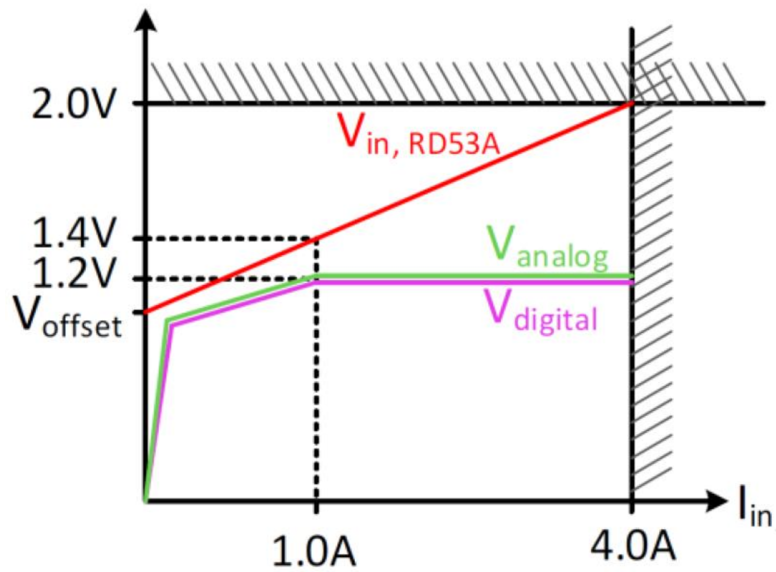
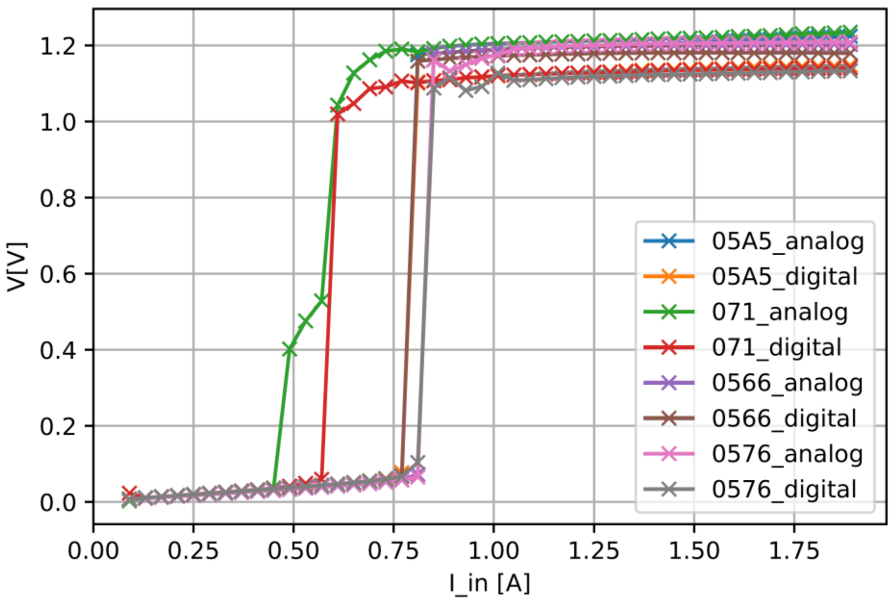


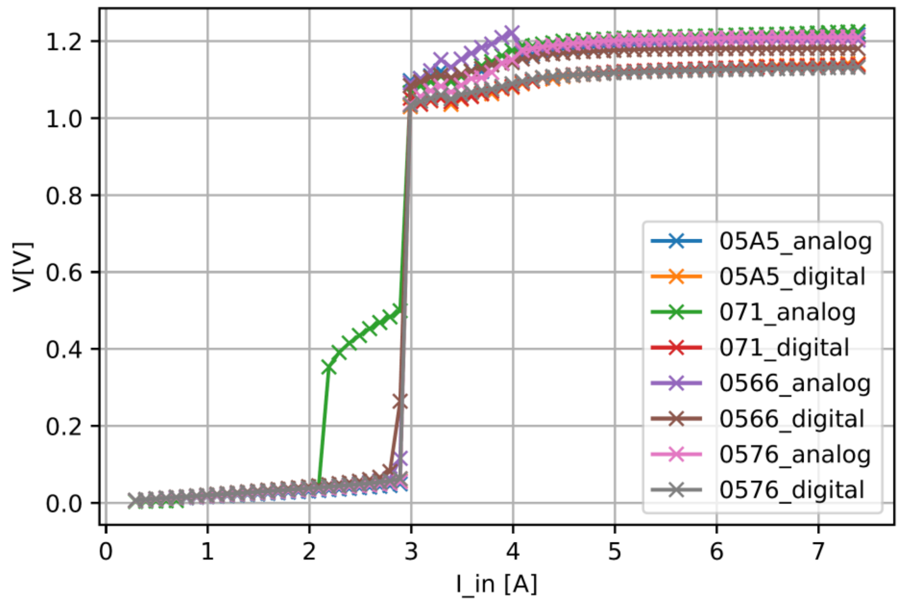


RD53A SLDO operation

Individual operation

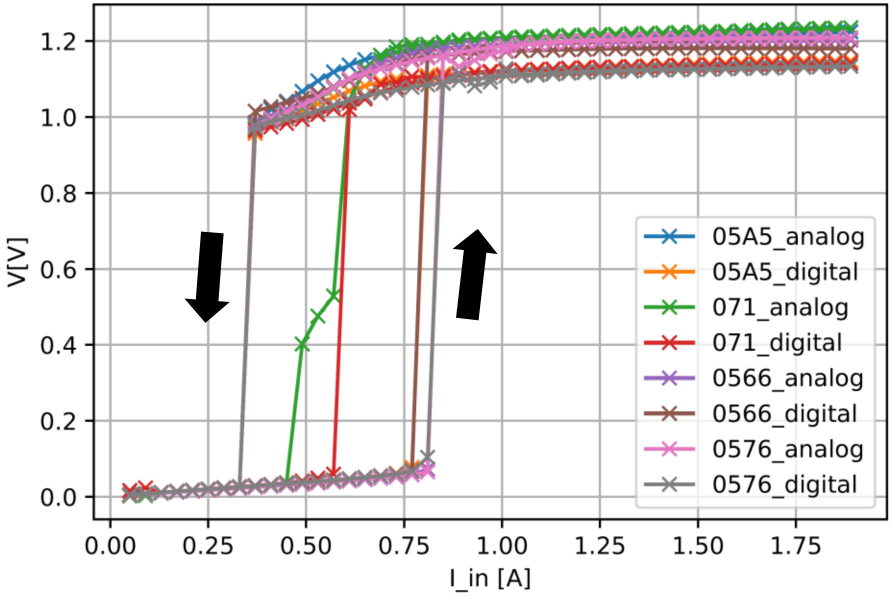


Parallel operation

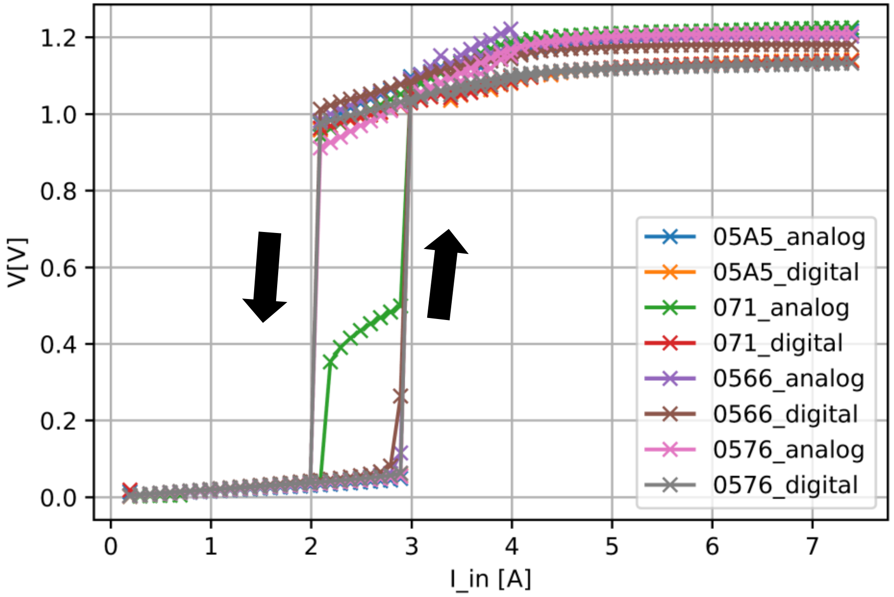


RD53A SLDO operation

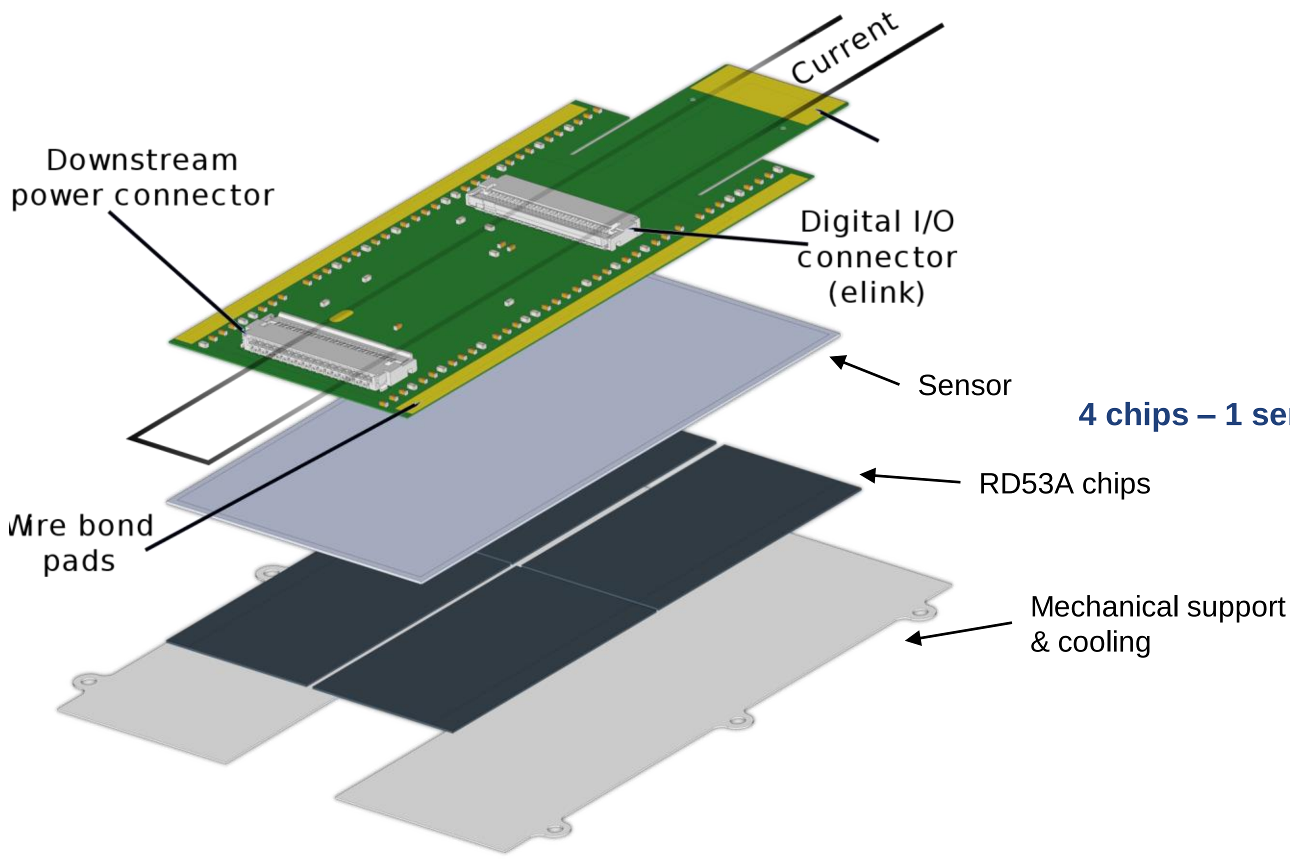
Individual operation



Parallel operation

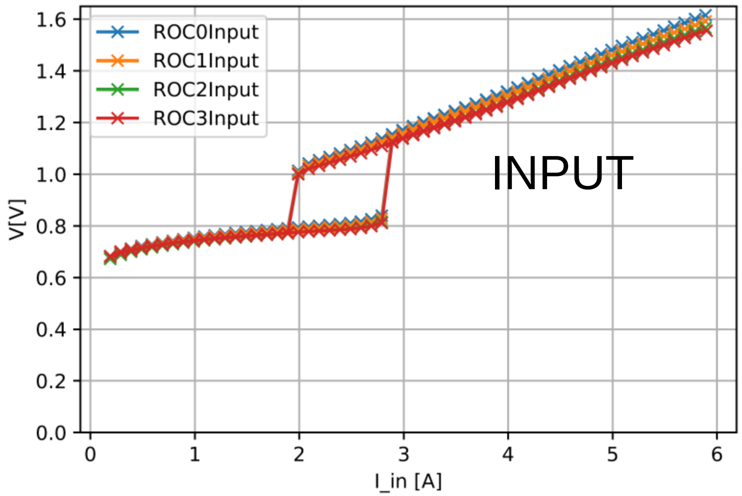


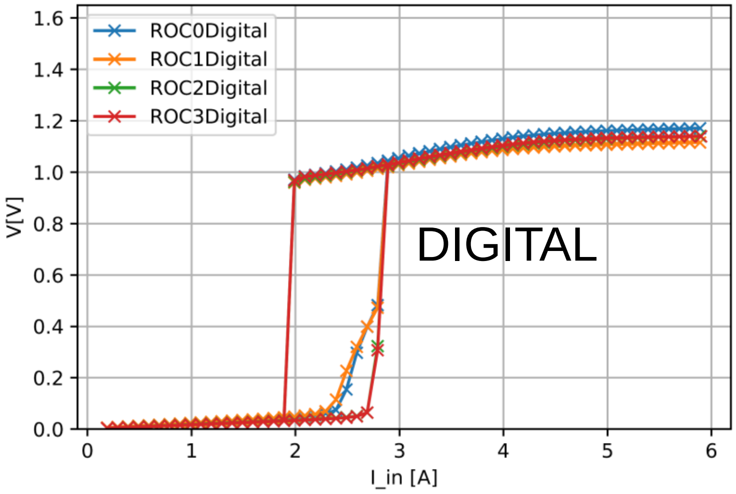
RD53A prototype modules

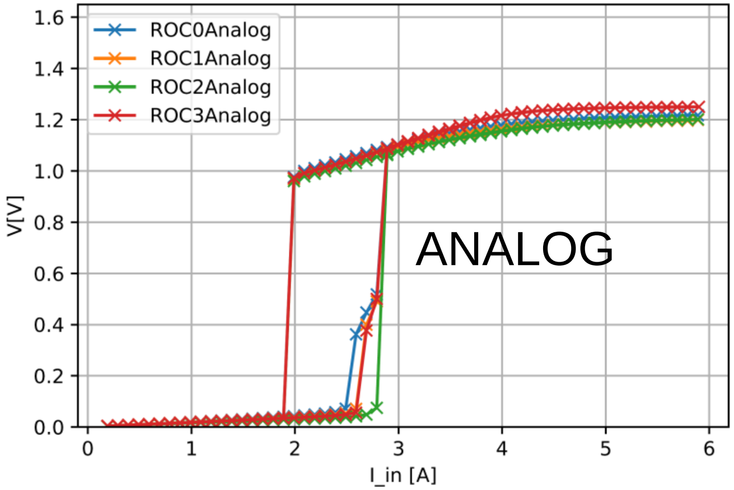


4 chips – 1 sensor

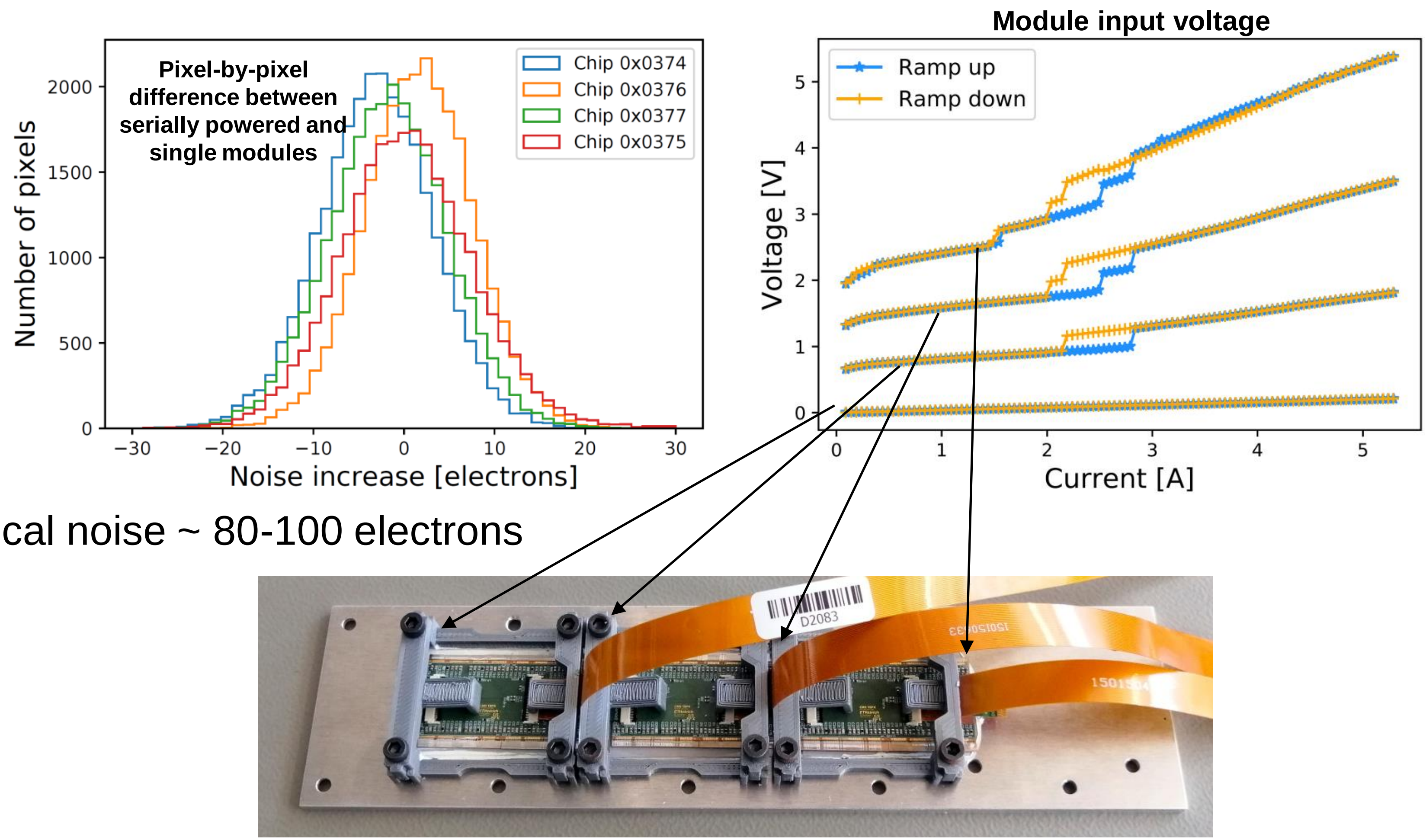
RD53A module SLDO operation







Serially powered RD53A modules



Typical noise ~ 80-100 electrons

RD53A performance

- RD53A modules can be powered serially ✓

- Charge is measured for each hit (resolution and track reconstruction improvement – required to meet the specifications)

- Efficiency in a high rate environment satisfies the specification

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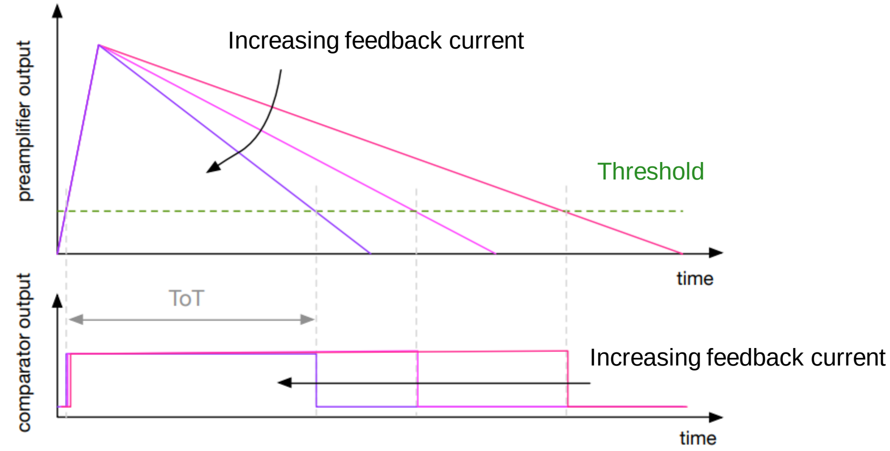
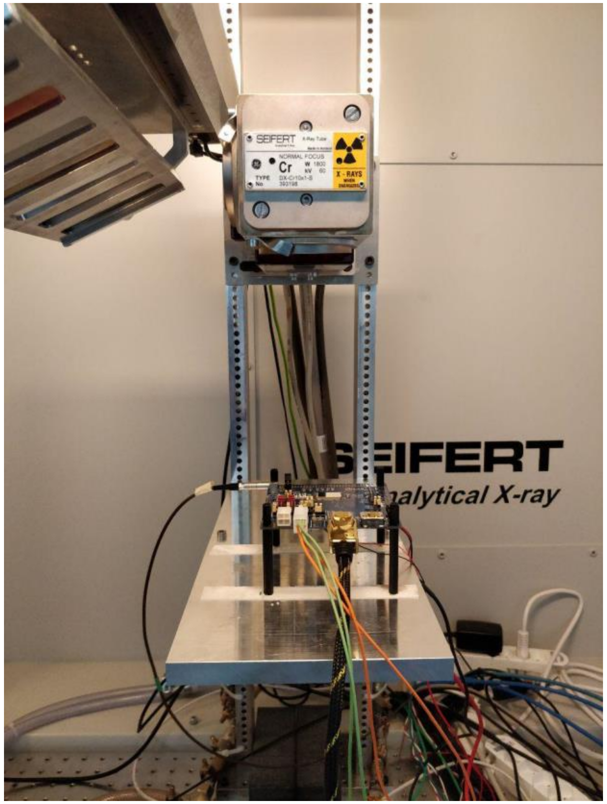
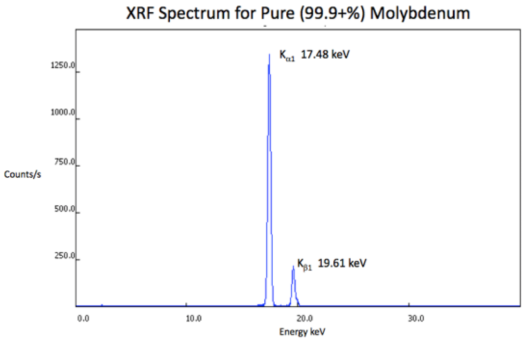
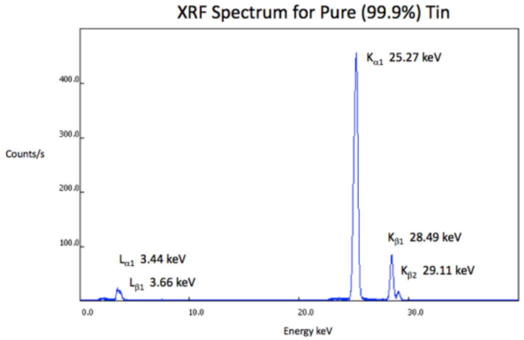
Charge calibration

- RD53A chip can inject charge internally
- Calibration with monochromatic x-rays





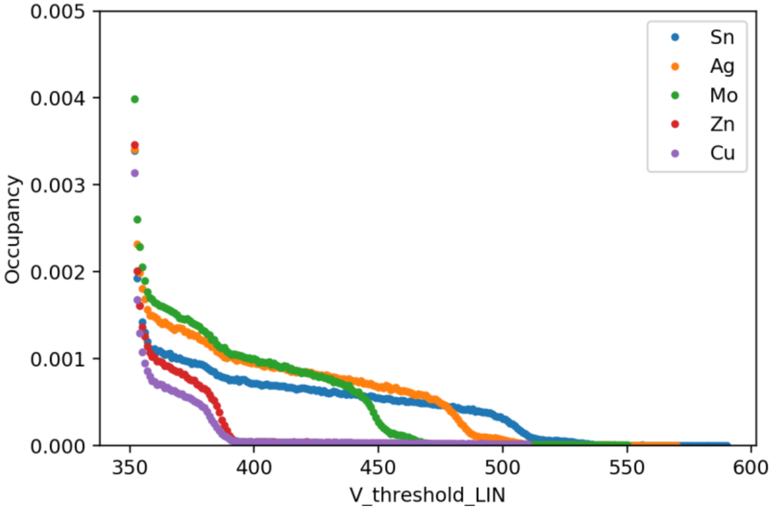


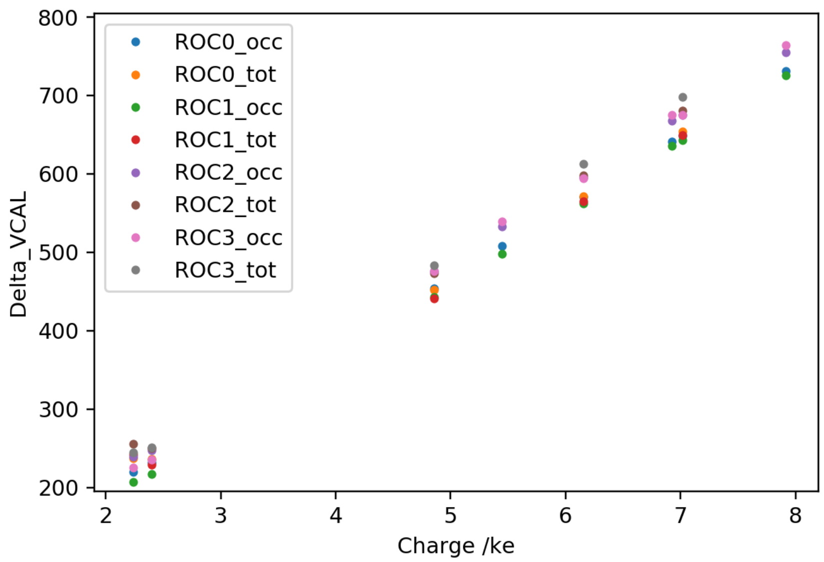


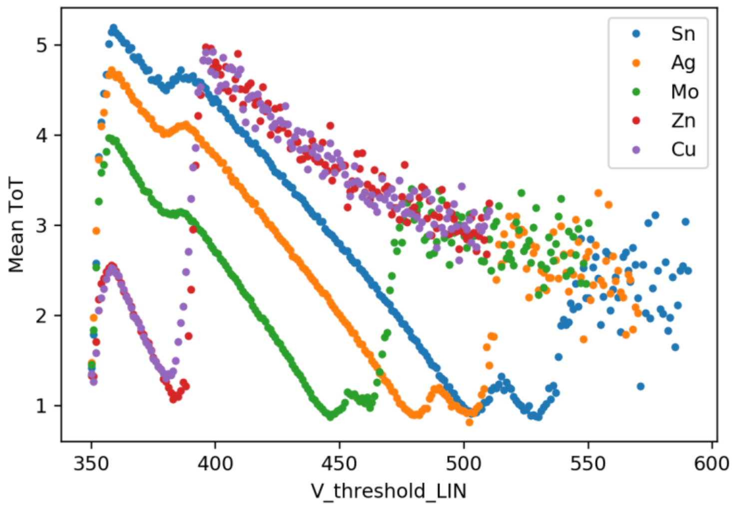
Charge calibration

- Occupancy and ToT are measured

- Conversion between the internal unit of charge and electron charge







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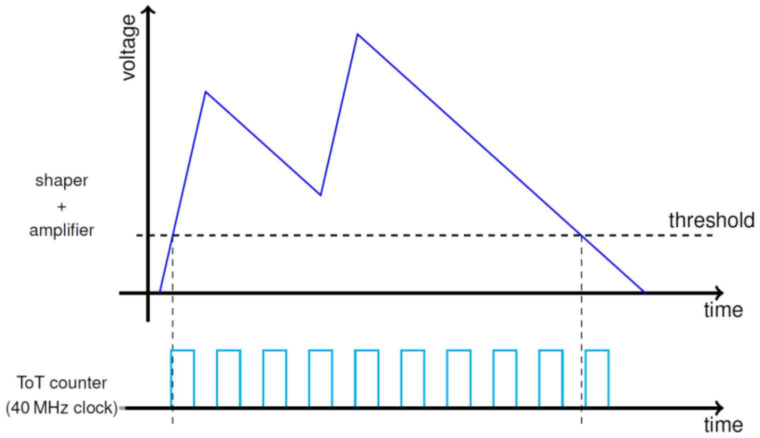
- Efficiency in a high rate environment satisfies the specification

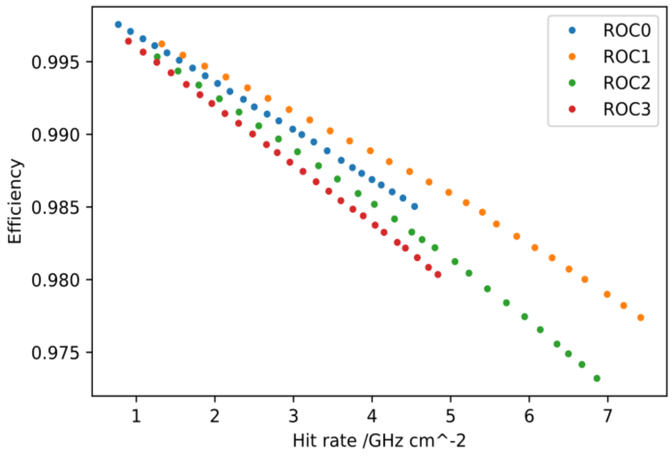
Efficiency in a high-rate environment

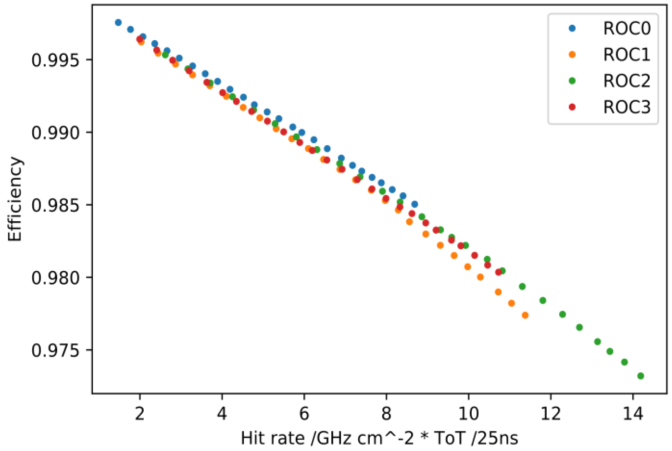
- Hit losses at higher rates due to:

1) Analog inefficiency – dead time during ToT (feedback-current dependent)
2) Digital inefficiency – full buffers

- Broad x-ray spectrum
- Low latency (3.2 μs) → analog inefficiency dominates



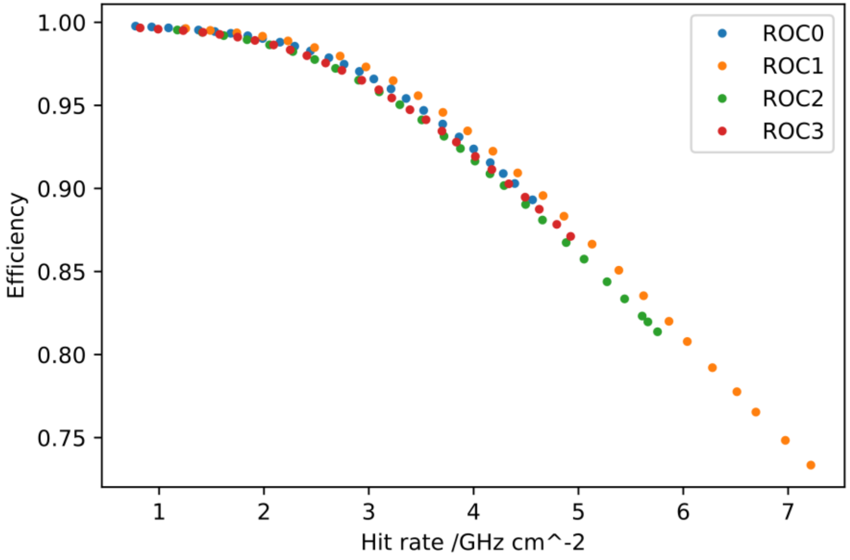




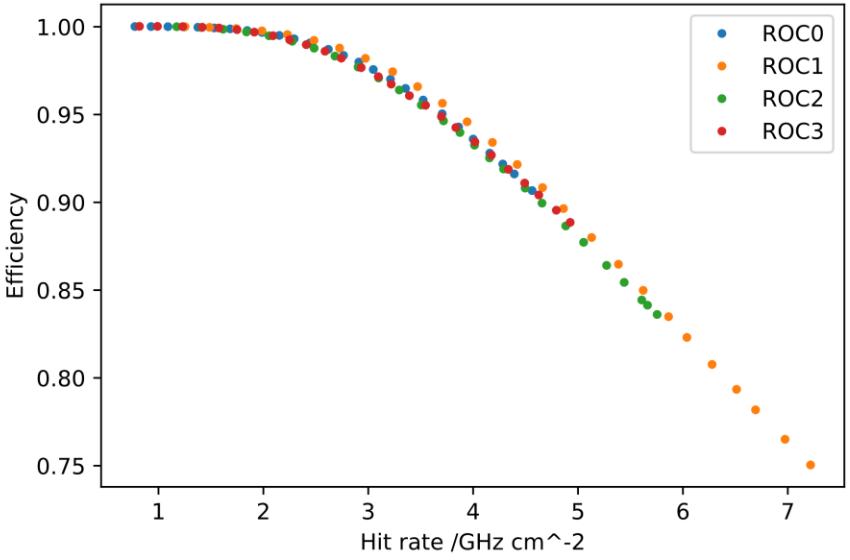
Efficiency in a high rate environment

- High (12.5 µs) latency → digital inefficiency dominates
- X-rays are the worst-case scenario for digital efficiency (no benefit of shared time stamps for clusters) → measured efficiency below 99%

Total efficiency



Total efficiency / Analog efficiency



RD53A performance

- RD53A modules can be powered serially ✓
- Charge is measured for each hit (resolution and track reconstruction improvement – required to meet the specifications) ✓
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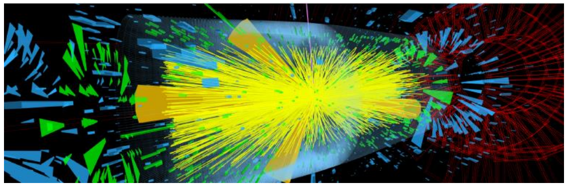
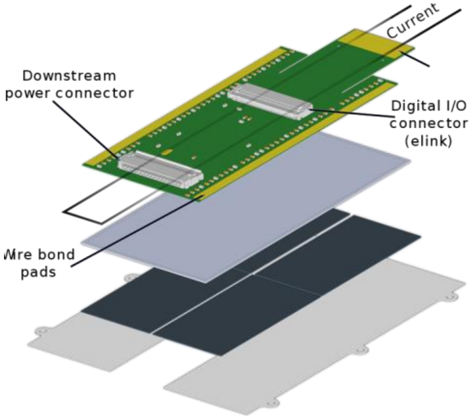
Summary

- High-Luminosity LHC → luminosity x7.5 → CMS upgrade
- Requires a different approach to powering → serial powering



- RD53A prototype readout chip (CMS and ATLAS)
- Serially powered quad modules have been built



- A chain of prototype modules has been operated and serial powering scheme successfully deployed.

- Qualified with x-rays charge measurement and high rate

- RD53A results used as input for the development of the successor (CROC)

BACKUP

- Efficiency measurement:

1) Choose a subset of pixels for injection (diagonal, 5 columns apart)
2) Set injection timing for optimal match to a single bunch crossing (readout trigger latency vs chip latency)
3) Expose the module to a high rate x-ray beam
4) Send triggers while injecting into the “injection pixel subset”
5) Compute the rate from neighbouring pixels (single row, four columns → pixel core)
6) Compute efficiency from the injection pixel subset
7) Correct the rate for the computed efficiency

- Repeat for higher latency (comparing 3.2 us to 12.5 us)

Efficiency in a high-rate environment

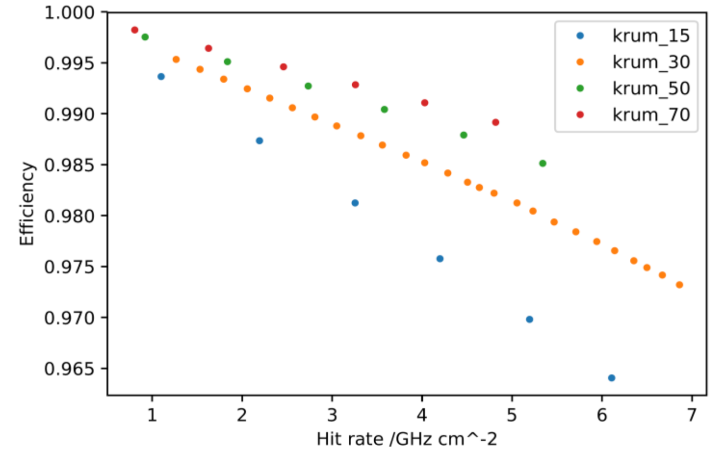
- Expecting hit losses at higher rates due to:

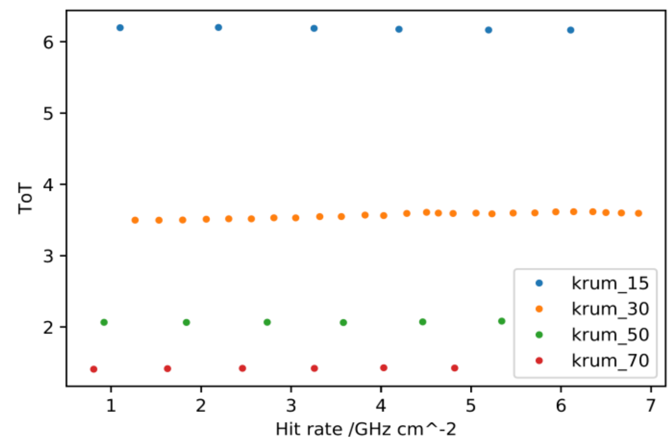
1) Analog inefficiency – dead time during ToT (feedback-current dependent)

2) Digital inefficiency – full buffers (latency-dependent)

- Broad x-ray spectrum (60keV electrons + Cr target)

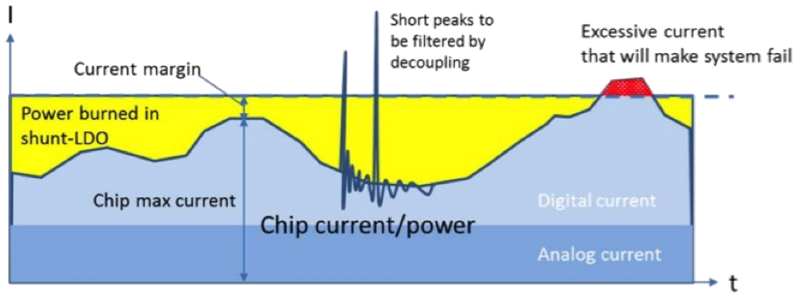
- At a low latency of 3.2 μs the inefficiency is almost entirely due to analog inefficiency.
- Chip-to-chip variation explained by ToT variation
- **Analog inefficiency is affected directly by ToT**

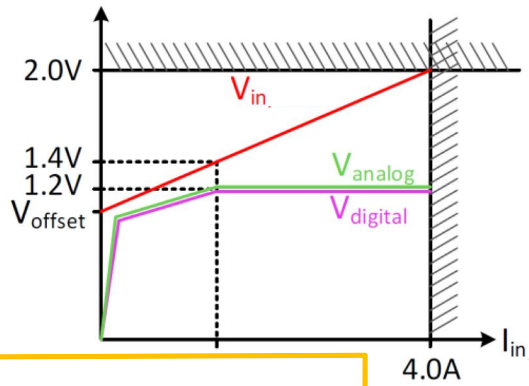


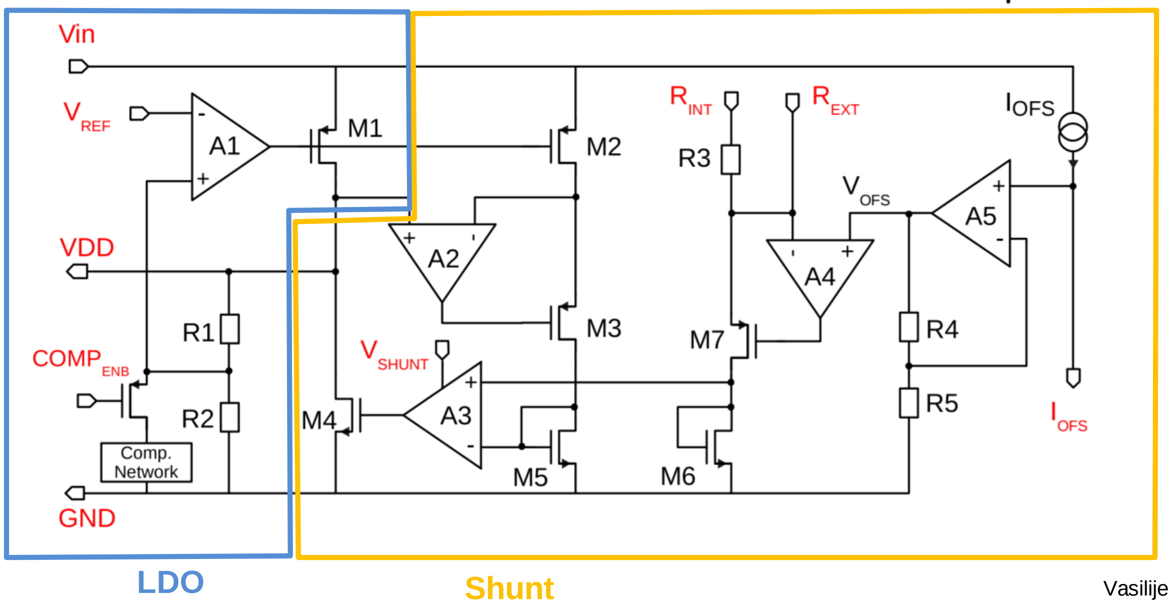


Serial powering – Shunt LDO regulator

- Constant voltage from the constant supply current
- Shunt + Low Dropout Regulator → ohmic behaviour is seen by the power supply

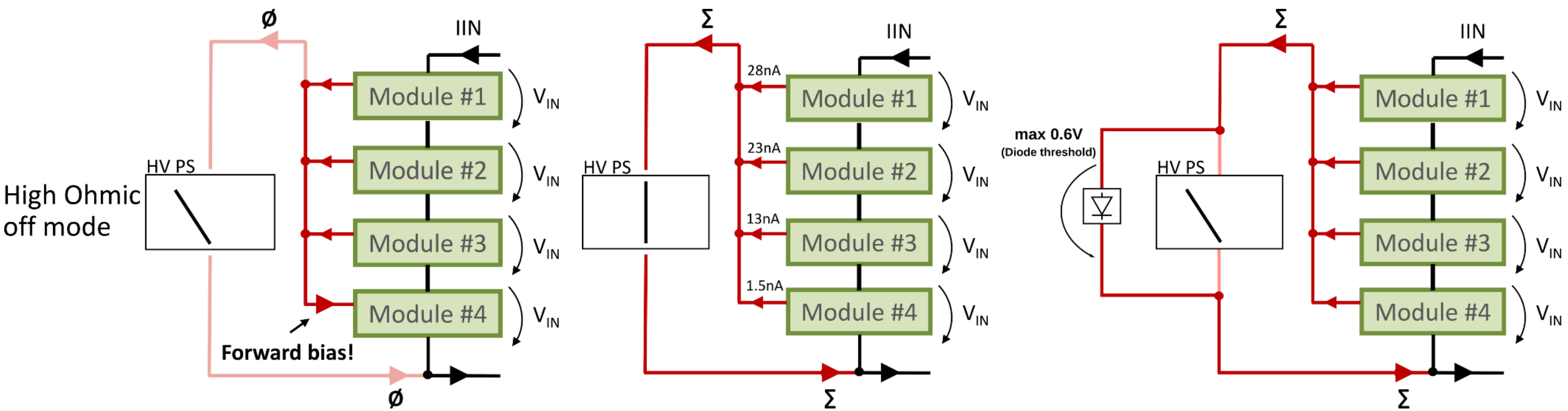






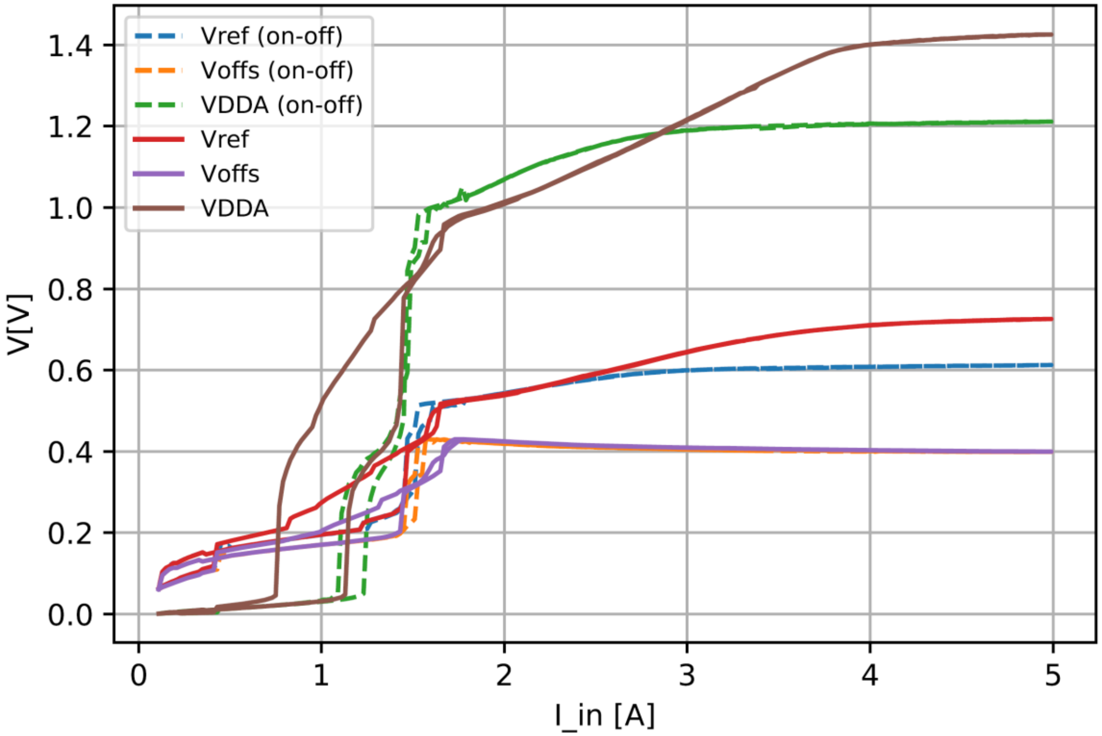
Serial powering

Possible forward bias with HV off (can be avoided)



RD53A SLDO operation

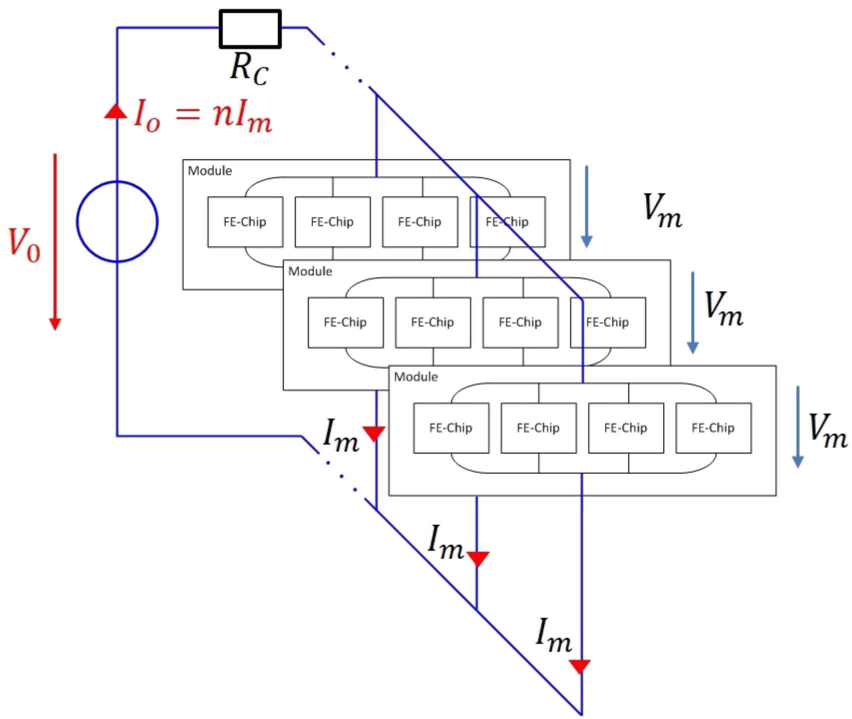
- Can fail if input is ramped → fixed in RD53B (next version)



ETH zürich

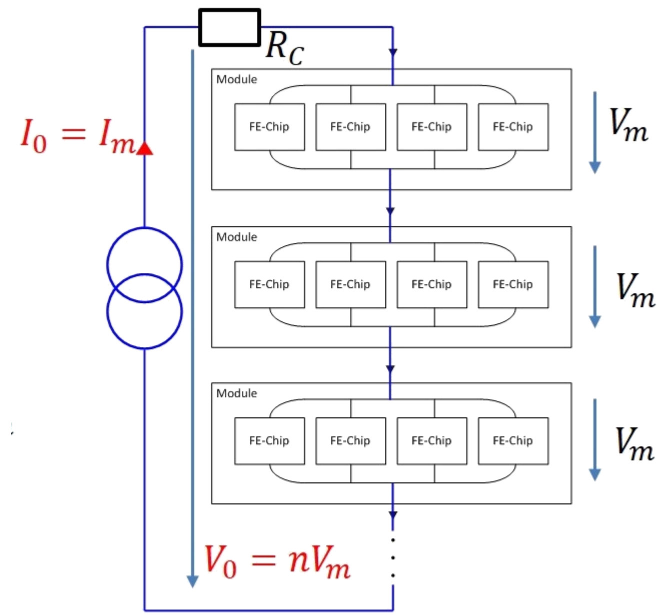
Serial powering

Parallel powering (current detector)



Power loss in parallel powering ~ $n^2 I_m^2 R_C$

Serial powering (Phase 2 detector)



Power loss in serial powering ~ $I_m^2 R_C$


EIFERT
Analytical X-ray