An ATCA Processor for Level-1 Trigger Primitive Generation and Readout of the CMS Barrel Muon Detectors

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Barrel Muon Trigger structure

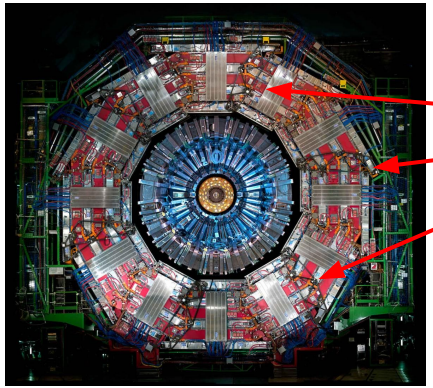
Barrel Muon Trigger (BMT) reconstructs muons of the CMS barrel

DETECTOR → **BMTL-1** → **GMT**

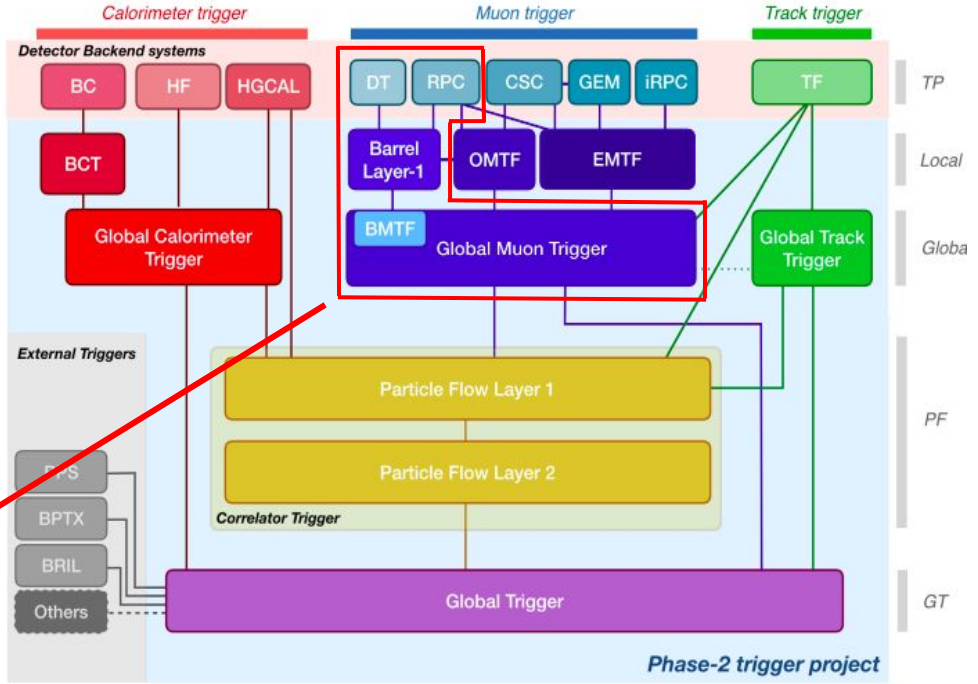
Drift Tubes (DTs) and Resistive Plate Chambers (RPCs) transmit muon hit data to BMTL-1

Builds DTs track segments and clusters RPC hits Merges both subsystem information into "super-primitives"

Matches track segments to reconstruct standalone muon objects

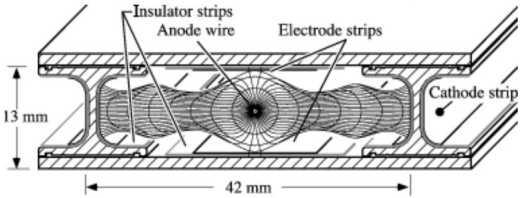


Barrel Muon Trigger



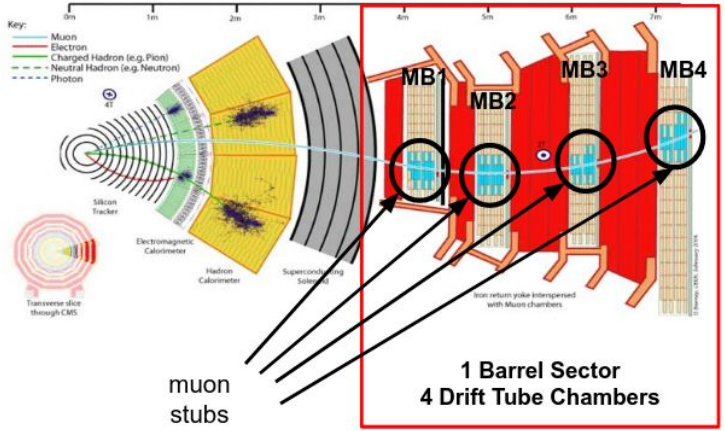
Barrel Muon Trigger structure

- On detector Board for Drift Tubes (OBDT) transmits detector data to BMTL-1
  - Time digitization of DT signals
- BMTL-1 processes hit information to produce Muon stubs (track segments)
  - Analytical Method (AM) algorithm processes TDC hits and generates Trigger Primitives
    - Bunch crossing, Stub Position, Bending Angle
- Stubs of the 4 chambers are received by GMT
  - Kalman Muon Track Finder (KMTF) algorithm matches tracks and reconstructs muon candidates
    - Assigns position and momentum



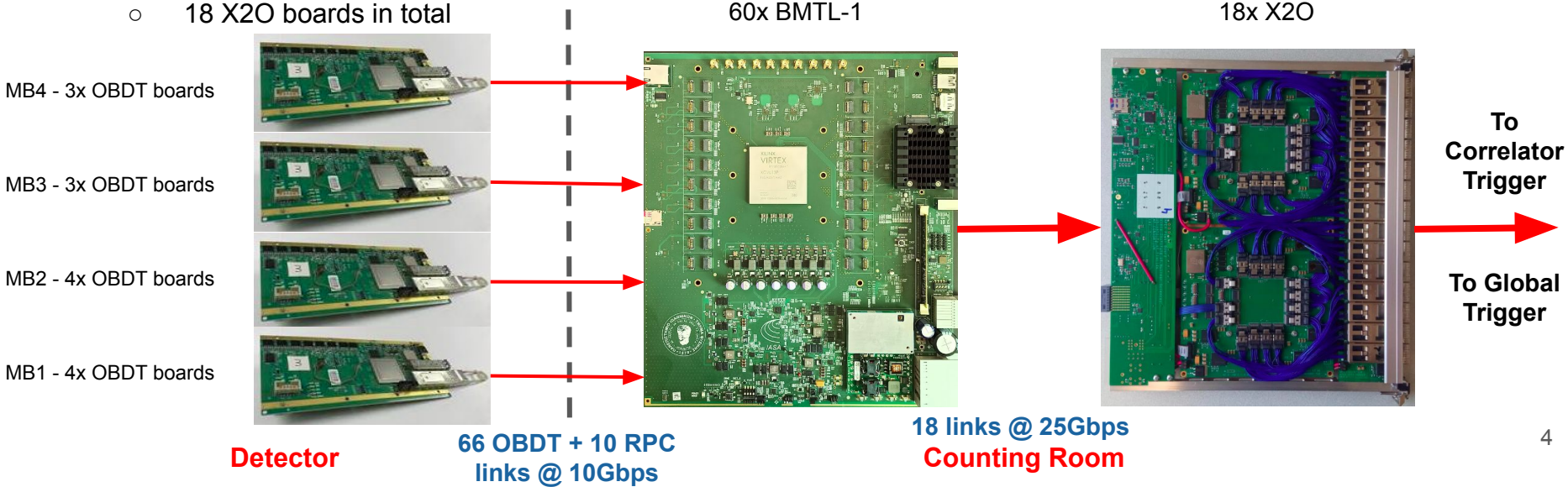
Drift Tube Cell

Detector		BMTL1 AM algorithm	GMT KMTF algorithm
Drift Tube Barrel Sector	Hits on Chamber 4	Stubs of Chamber 4	Reconstructed Muons of Sector
	Hits on Chamber 3	Stubs of Chamber 3	
	Hits on Chamber 2	Stubs of Chamber 2	
	Hits on Chamber 1	Stubs of Chamber 1	

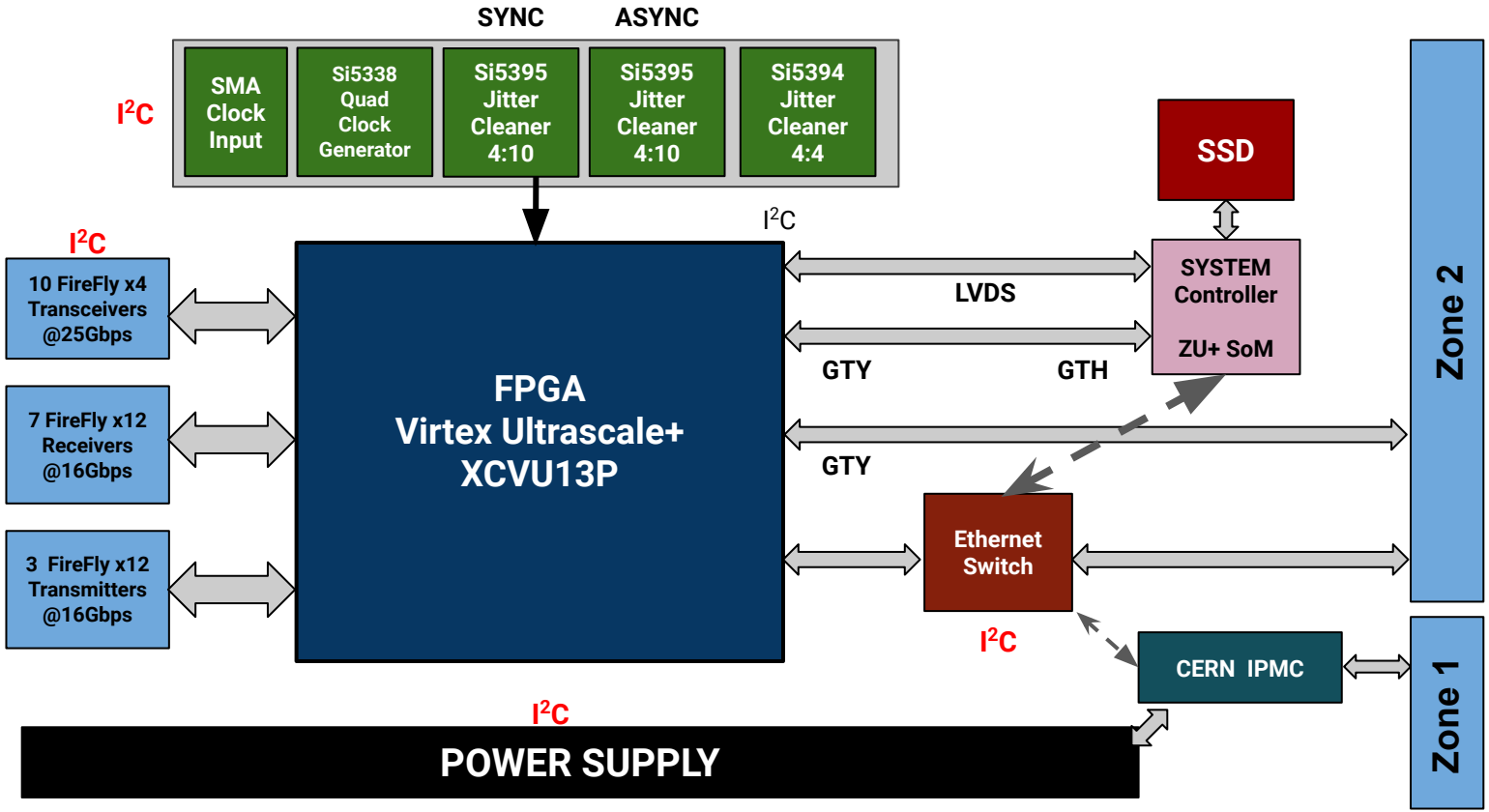


Barrel Muon Trigger structure

- CMS Barrel Muon system consists of 60 DT sectors
  - Each sector consists of 4 DT chambers
- OBDT boards transmit TDC hits to BMTL-1
  - 14 OBDT boards per sector
- Every BMTL-1 board processes data from 2 Sectors
  - 30 BMTL-1 boards needed for the whole barrel
- GMT receives primitives from BMTL-1
  - Using TMT18
  - 18 X2O boards in total



BMTL-1 ATCA board architecture



FPGA used - Xilinx XCVU13P

- **Xilinx XCVU13P FPGA**
  - *Ultrascale+ architecture*
  - *16 nm lithography*
  - *4 SLRs (Super Logic Regions)*
  - *1,728,000 LUTs*
  - *3,456,000 Flip Flops*
  - *12,288 DSP slices*
  - *128 GTY transceivers @ 28G*
  - *2577 ball BGA package*
  - *-1 speed grade*

- **38.3 TOP/s (DSP)**
  - Simultaneous usage of 12228 DSPs

- **Capability to use VU9P, VU11P**
  - Design is drop-in compatible with these two smaller FPGAs, with only compromise a slight drop in connectivity

XCVU13P FPGA mounted on the BMTL-1 ATCA board

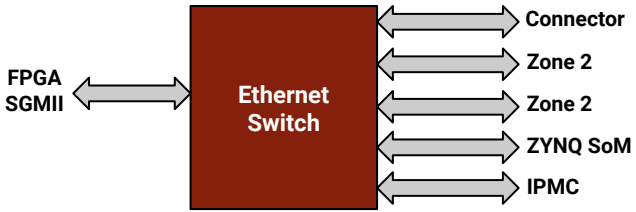
BMTL-1 ATCA board connectivity

Optical connectivity

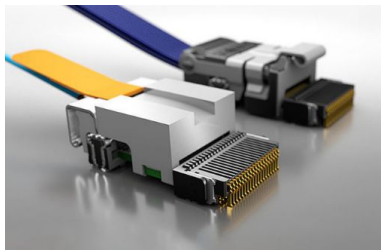
- **40 RX @ 25 Gbps** ⇨ *10 x BiDir FireFly Modules 25G*
- **40 TX @ 25 Gbps**
- **80 RX @ 16 Gbps** ⇨ *7 x Rx FireFly Modules 16G*
- **36 TX @ 16 Gbps** ⇨ *3 x Tx FireFly Modules 16G*

- **120** RX + **76** TX ~ **3.9** ***Tbps***

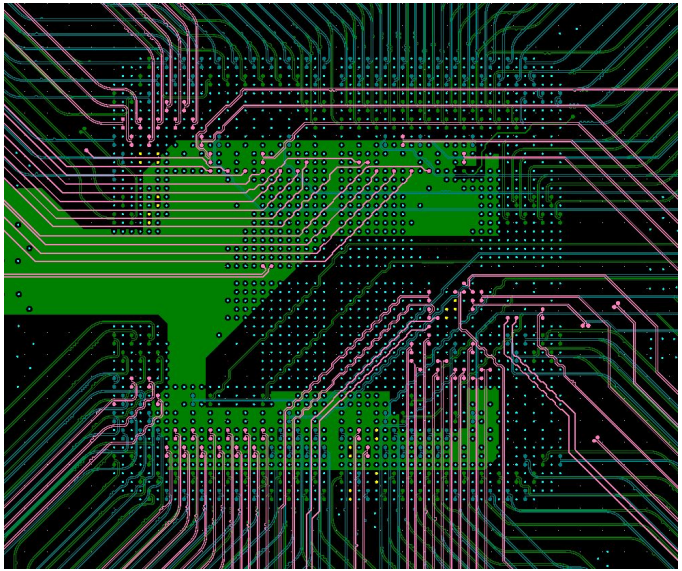
~200.000 ADSL connections
~100.000 VDSL connections
~4000 Gbit connections



Onboard Ethernet switch circuitry provides access to many subsystems on board



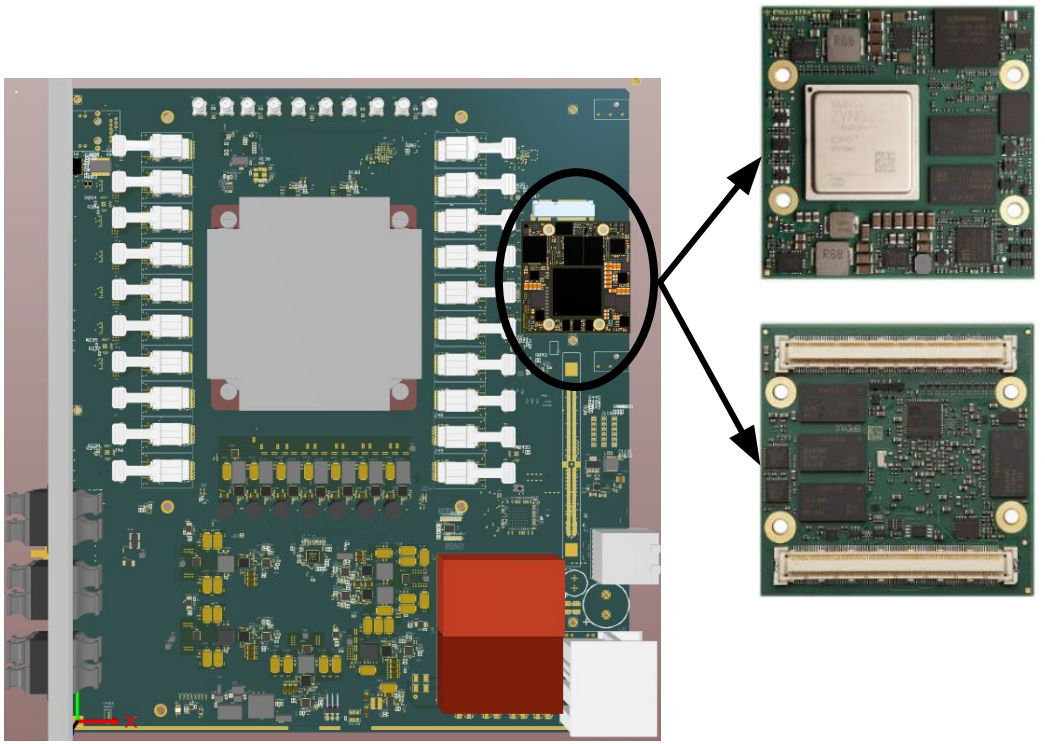
Samtec FireFly optical modules



Dense high-speed signal fanout under the FPGA

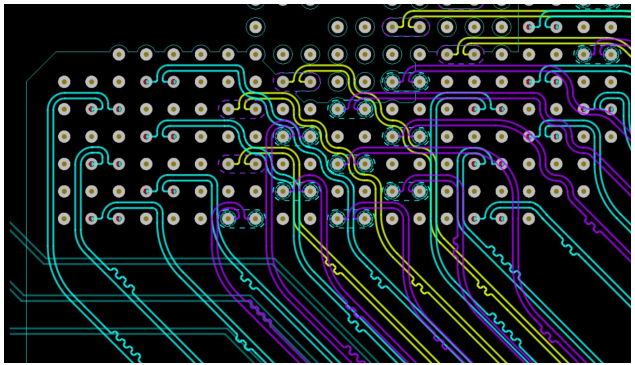
BMTL1 ATCA board system controller

- Enclustra Mercury XU5
  - *XCZU5EV-1FSVC784E SoC*
- Zynq Ultrascale+ architecture
- Quad core Arm Cortex A-53
  - *Capable of running Linux*
- Independent RAM on PS & PL
  - *2 GB (PS)*
  - *1 GB (PL)*
- Direct connections with the FPGA
  - 4 GTH MGTs @ 10G
  - 20 LVDS pairs
- SSD & SD storage

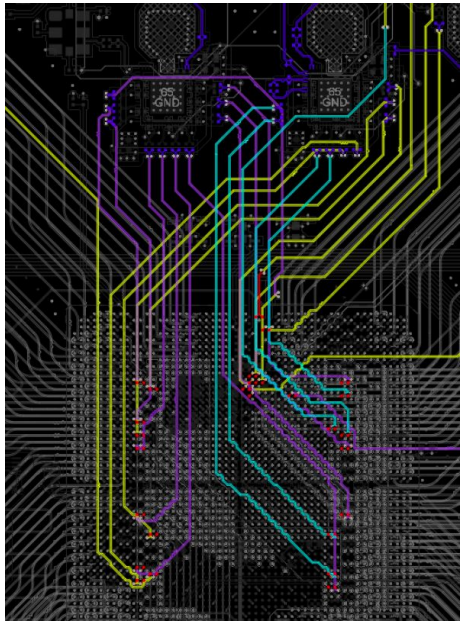


Design challenges

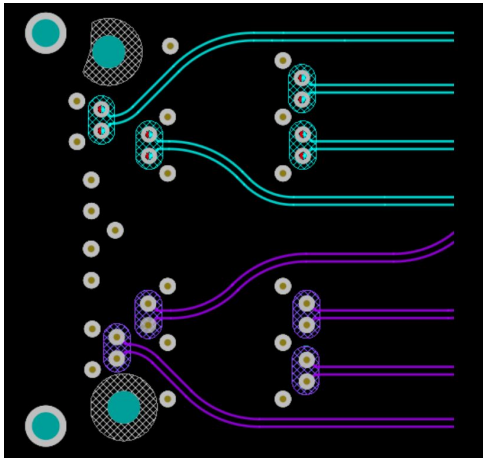
- Clocking
  - *Has to serve a large amount of links*
  - *Has to be very low jitter*
  - *Needs to be compatible with many operating scenarios*
- Signal integrity
  - *PCBs are very lossy at 25 Gbps NRZ*
  - *Low loss dielectric material being used*
  - *Special design considerations for RF frequencies*
  - *Special technologies for PCB fabrication*
    - *Blind vias*
    - *Backdrilling*



High speed signal fanout under FPGA



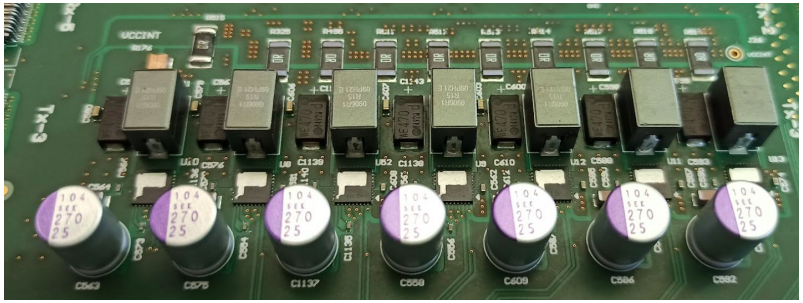
Highlighted part of the clocking network



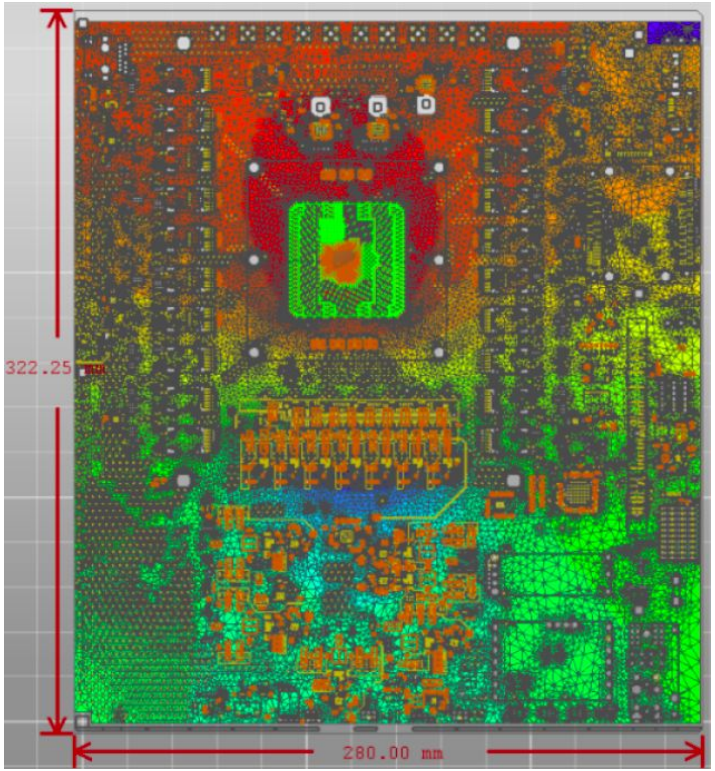
High speed signal routing detail

Design challenges

- Power delivery
  - *Core rail can consume current in excess of 200A*
  - *Generation and delivery of such currents is not trivial*
- Thermal design
  - *The FPGA can dissipate more than 200W*
  - *Firefly optics reliability sensitive to high temperature*
  - *Extensive simulation of the card's thermal performance*
    - *Allowed for optimal component placement and aids optimal heat sink design*
  - *Custom heatsinks under design*
    - *Independent block heatsinks for the FPGA and the FireFlies*

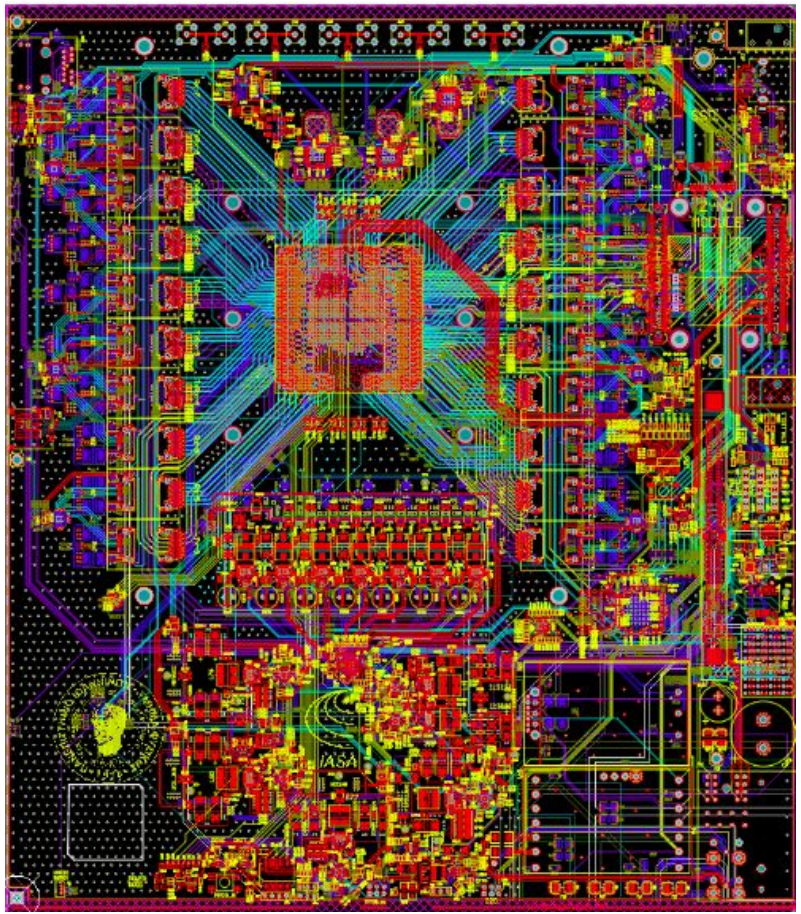


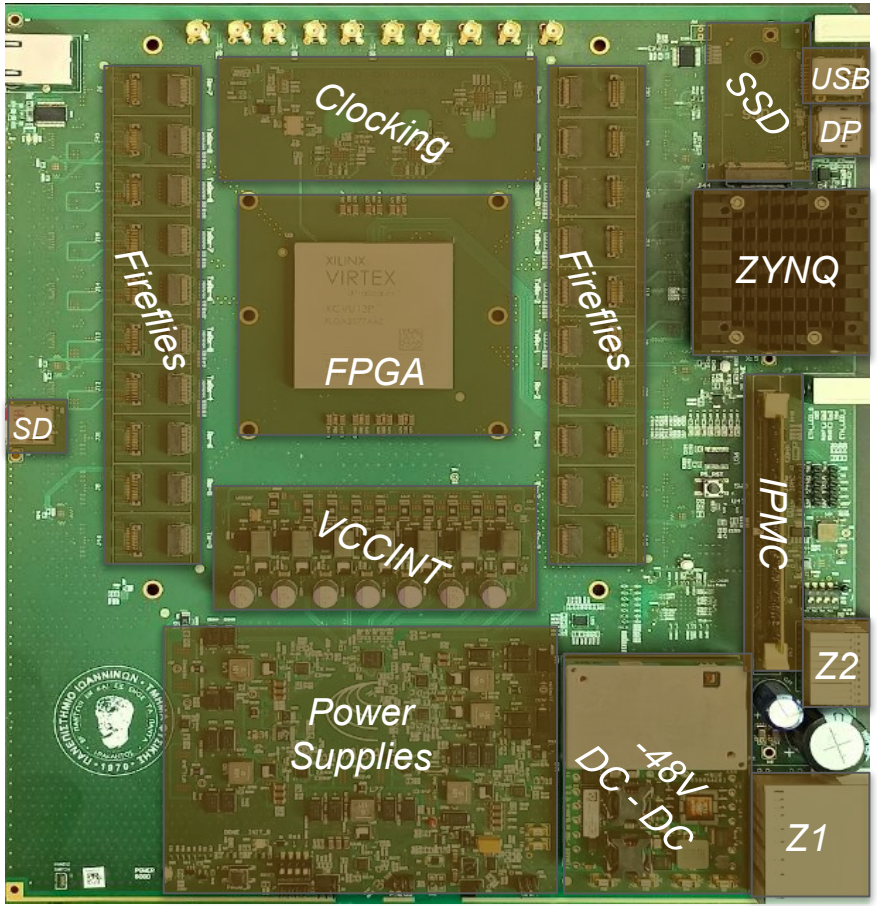
Core voltage power stage comprised of 7 phases



IR simulations proved very useful in optimizing current delivery and part placement

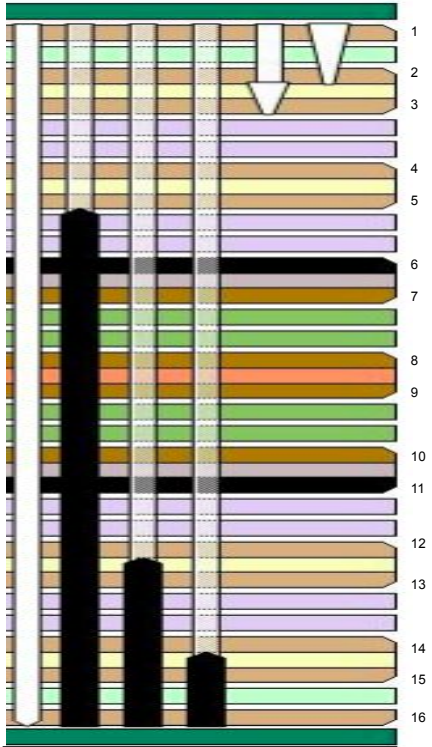
Board routing - annotation





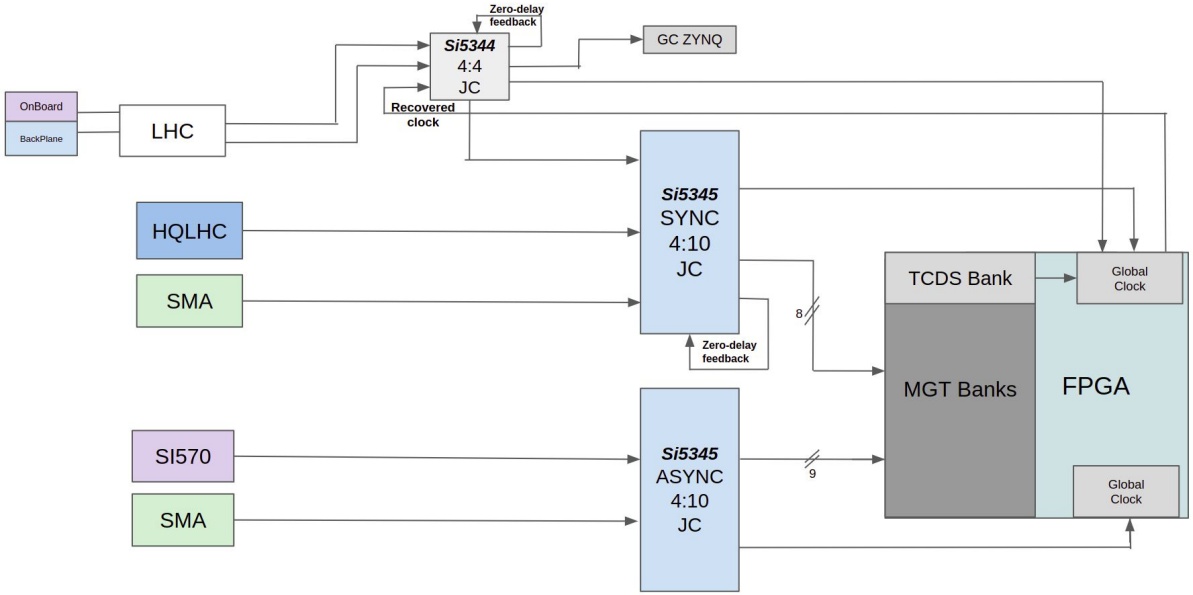
Technical aspects - PCB

- Layer stack
  - 16 layers
    - *6 ground*
    - *4 power*
    - *6 signal*
- Materials
  - Mix of dielectrics
    - ***ITERA MT-40*** *between signal layers*
    - ***FR-480*** *between power layers*
- HDI
  - Blind vias
    - *Layers 2-3*
  - Backdrilling
    - *Layers 5-12-14*
- **8 oz** total copper weight for power layers
  - *Reduced IR losses*

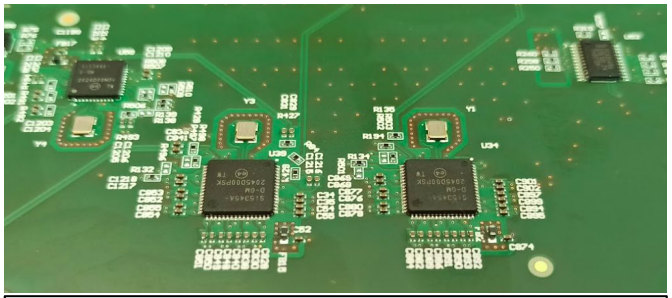


Layer stack

Technical aspects - Clocking network



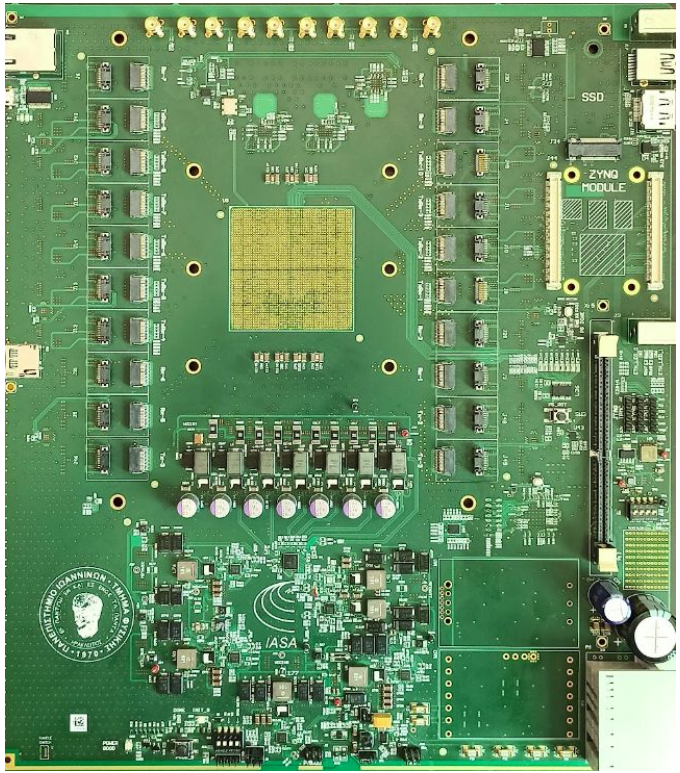
Clocking network block diagram

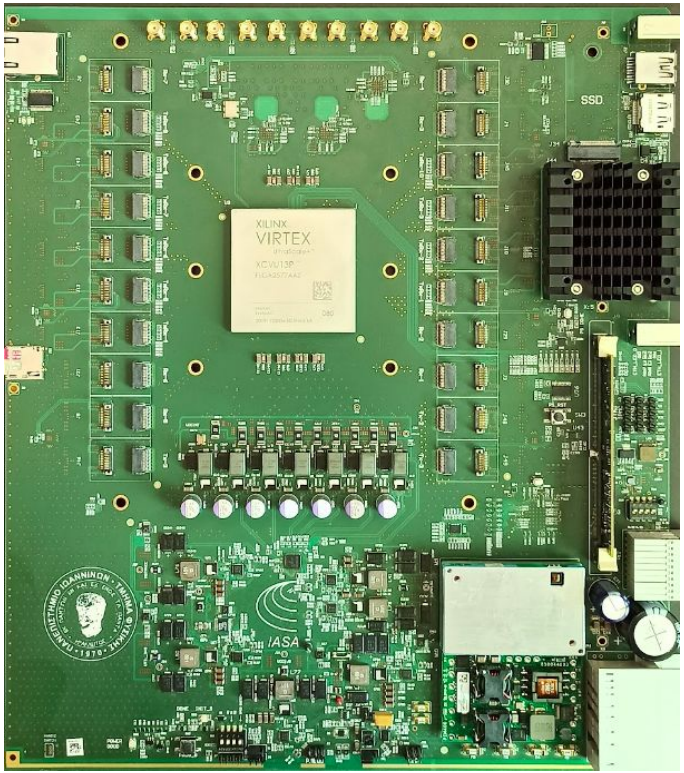


Clocking circuitry on the board

- *Each MGT quad is capable of operating either in synchronous or asynchronous mode*

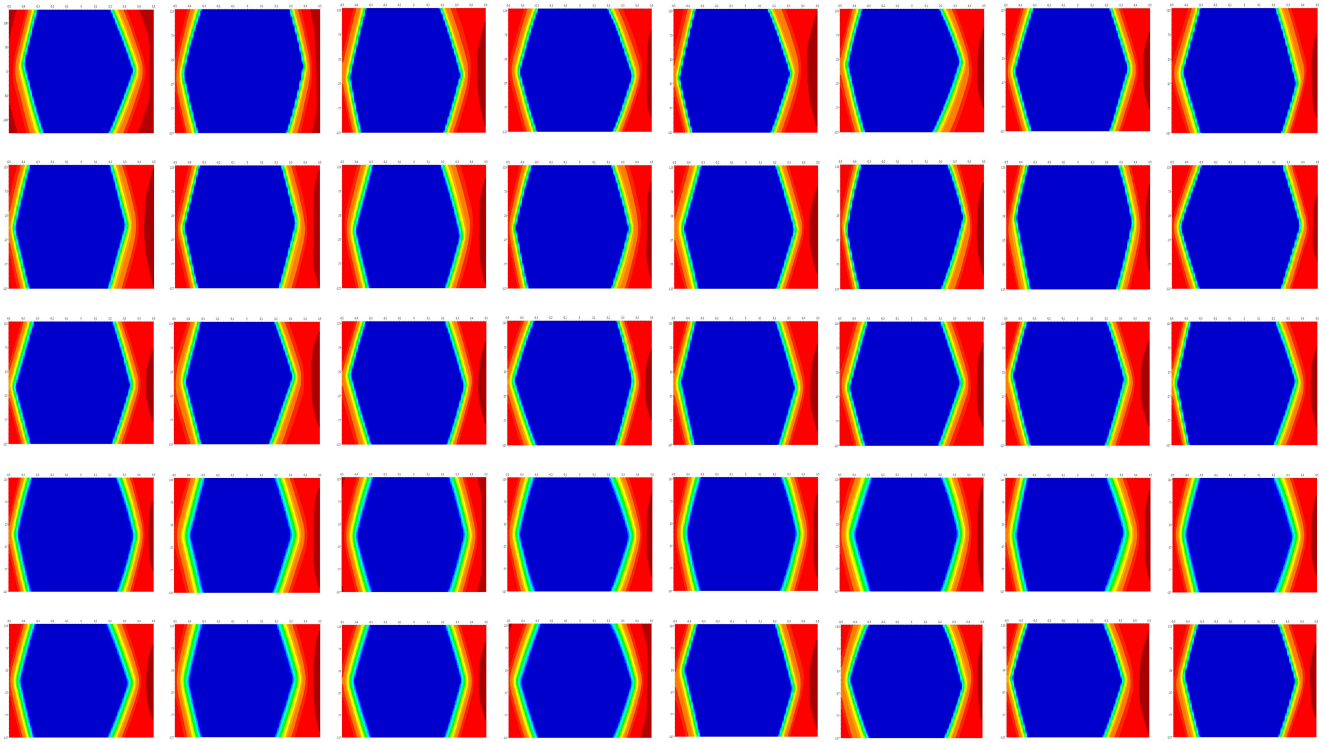
Manufactured hardware





2 boards assembled - one without the FPGA populated, and one fully populated

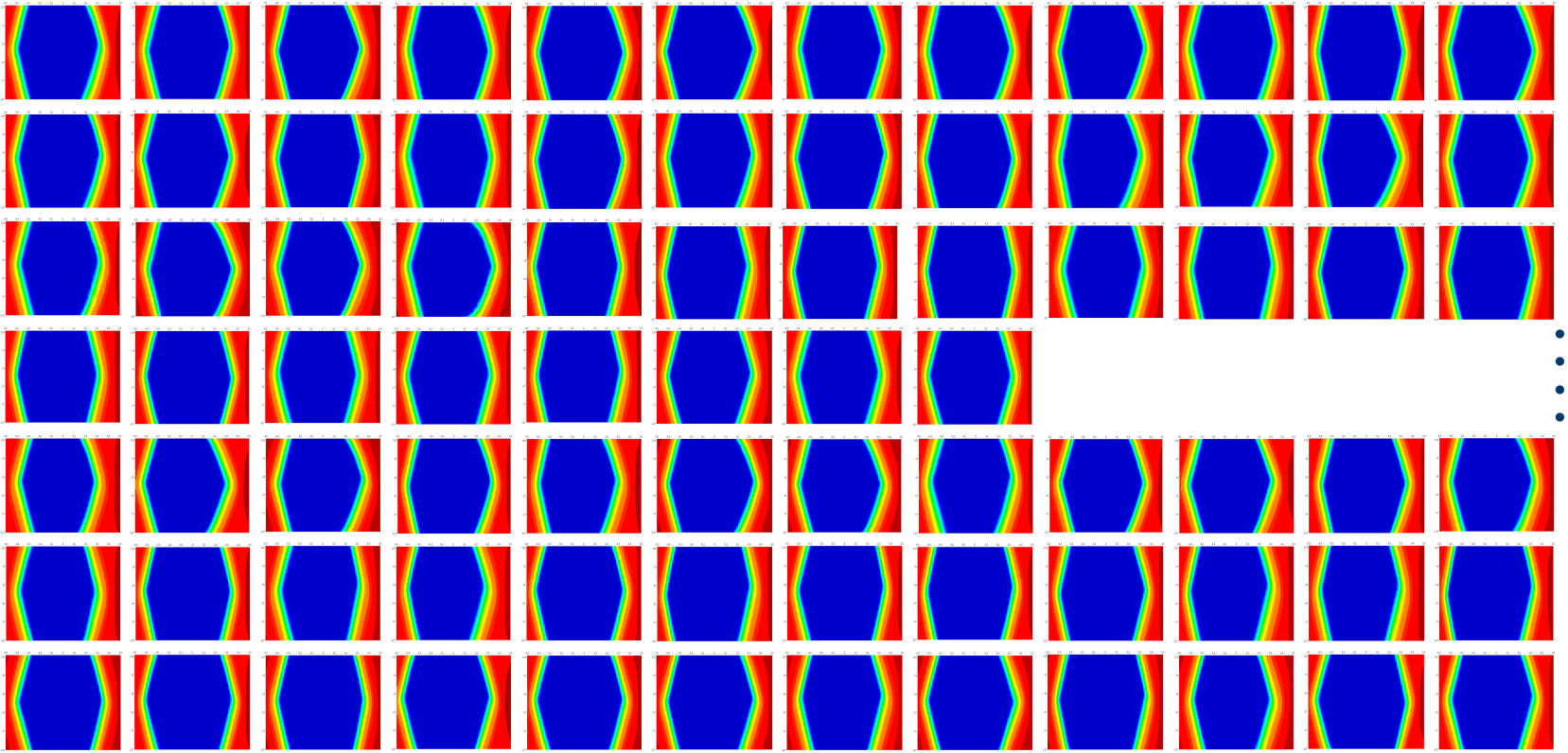
25G Eyescans



IBERT with all 40 25G MGTs instantiated and operating simultaneously

- **2 meter optic fiber**
- **25.6 Gb/s**
- **PRBS7**
- **Resolution 1**
- **Eyescan BER 1e-8**

16G Eyescans



IBERT with all 80 16G MGTs instantiated and operating simultaneously

- 12 meter optic fiber
- 16 Gb/s
- PRBS31
- Eyescan BER 1e-8

Endurance testing

Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

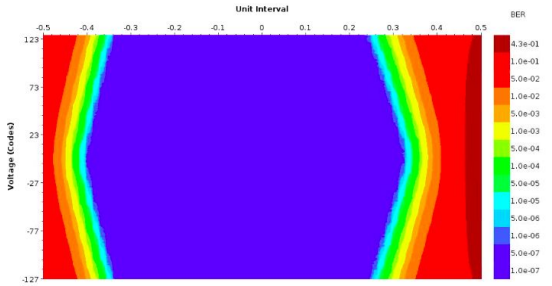
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	Loopback Mode	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status
Ungrouped Links (0)																			
Found Links (8)							Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset		
Found 0	MGT_X1Y46/TX	MGT_X1Y40/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 1	MGT_X1Y47/TX	MGT_X1Y41/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 2	MGT_X1Y44/TX	MGT_X1Y42/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 3	MGT_X1Y45/TX	MGT_X1Y43/RX	25.782 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 4	MGT_X1Y42/TX	MGT_X1Y44/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 5	MGT_X1Y43/TX	MGT_X1Y45/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 6	MGT_X1Y40/TX	MGT_X1Y46/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 7	MGT_X1Y41/TX	MGT_X1Y47/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	Loopback Mode
Ungrouped Links (0)										
Found Links (24)							Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 0	Quad_125/MGT_X0Y23/TX (xcvu13p_0)	Quad_120/MGT_X0Y0/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 1	Quad_124/MGT_X0Y18/TX (xcvu13p_0)	Quad_120/MGT_X0Y1/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 10	Quad_124/MGT_X0Y17/TX (xcvu13p_0)	Quad_122/MGT_X0Y10/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 11	Quad_123/MGT_X0Y12/TX (xcvu13p_0)	Quad_122/MGT_X0Y11/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 12	Quad_121/MGT_X0Y4/TX (xcvu13p_0)	Quad_224/MGT_X1Y16/RX (xcvu13p_0)	16.003 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 13	Quad_120/MGT_X0Y0/TX (xcvu13p_0)	Quad_224/MGT_X1Y17/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 14	Quad_120/MGT_X0Y3/TX (xcvu13p_0)	Quad_224/MGT_X1Y18/RX (xcvu13p_0)	16.002 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 15	Quad_121/MGT_X0Y5/TX (xcvu13p_0)	Quad_224/MGT_X1Y19/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 16	Quad_120/MGT_X0Y1/TX (xcvu13p_0)	Quad_225/MGT_X1Y20/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 17	Quad_121/MGT_X0Y6/TX (xcvu13p_0)	Quad_225/MGT_X1Y21/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 18	Quad_122/MGT_X0Y10/TX (xcvu13p_0)	Quad_225/MGT_X1Y22/RX (xcvu13p_0)	15.998 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 19	Quad_121/MGT_X0Y7/TX (xcvu13p_0)	Quad_225/MGT_X1Y23/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 2	Quad_125/MGT_X0Y22/TX (xcvu13p_0)	Quad_120/MGT_X0Y2/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 20	Quad_122/MGT_X0Y8/TX (xcvu13p_0)	Quad_226/MGT_X1Y24/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 21	Quad_122/MGT_X0Y9/TX (xcvu13p_0)	Quad_226/MGT_X1Y25/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 22	Quad_122/MGT_X0Y11/TX (xcvu13p_0)	Quad_226/MGT_X1Y26/RX (xcvu13p_0)	15.994 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 23	Quad_120/MGT_X0Y2/TX (xcvu13p_0)	Quad_226/MGT_X1Y27/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 3	Quad_124/MGT_X0Y19/TX (xcvu13p_0)	Quad_120/MGT_X0Y3/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 4	Quad_125/MGT_X0Y20/TX (xcvu13p_0)	Quad_121/MGT_X0Y4/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 5	Quad_125/MGT_X0Y21/TX (xcvu13p_0)	Quad_121/MGT_X0Y5/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 6	Quad_123/MGT_X0Y15/TX (xcvu13p_0)	Quad_121/MGT_X0Y6/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 7	Quad_124/MGT_X0Y16/TX (xcvu13p_0)	Quad_121/MGT_X0Y7/RX (xcvu13p_0)	15.998 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 8	Quad_123/MGT_X0Y14/TX (xcvu13p_0)	Quad_122/MGT_X0Y8/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None
Auto detected link 9	Quad_123/MGT_X0Y13/TX (xcvu13p_0)	Quad_122/MGT_X0Y9/RX (xcvu13p_0)	16.000 Gbps	3.073E14	0E0	3.254E-15	Reset	PRBS 31-bit	PRBS 31-bit	None

- *No errors have been observed so far*

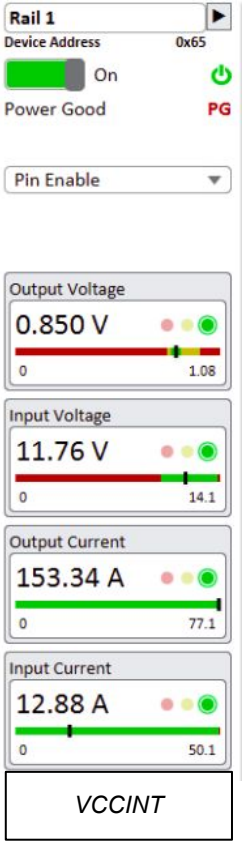
Further Operational Tests

- ✅ Power supplies
  - *All rails stressed up to 45A with external load*
  - *VCCINT stressed up to 180A*
  - *Excellent performance*
- ✅ Clocking network
- ✅ Mechanicals
- ✅ ZYNQ - FPGA connectivity
  - *GTH links & LVDS*



ZYNQ - FPGA eye diagram

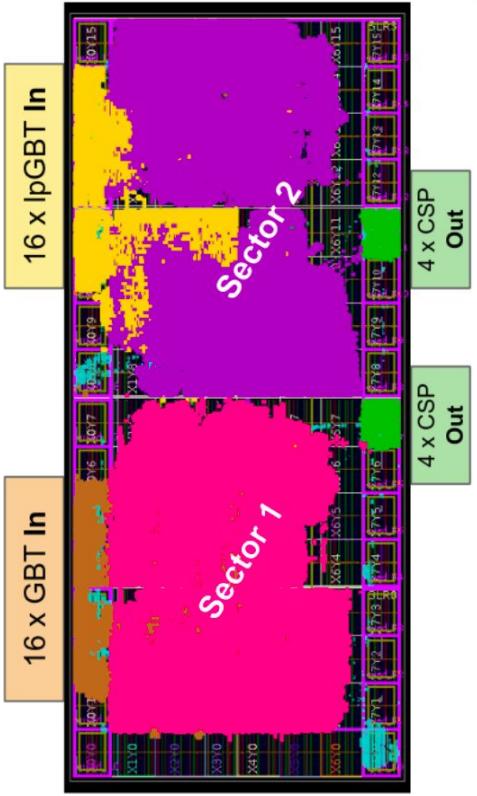
- ✅ All I2C devices
- ✅ All optics slots
- ✅ Ethernet (switch circuitry)
  - *Front Panel*
  - *Zone 2*
  - *ZYNQ*
- ✅ Zone 1 & 2
- ✅ ZYNQ peripherals



VCCINT

Infrastructure Developments

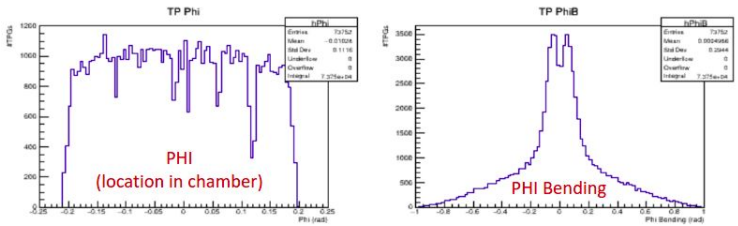
- ZYNQ - System Controller
  - Functionality for access/control/programming of the FPGA
  - IPBus over AXI
  - Software for controlling on-board peripherals
- FPGA - EMP Framework Integration
  - Provides control of the FPGA firmware over ZYNQ
  - Includes functionality such as CSP, GBT, LpGBT link protocols, TTC & TCDS2, etc.
- Analytical Method Algorithm Integration
  - 8 instances of the AM algorithm
  - Steady progress towards the final shape of the system



Utilization of the FPGA die for 2 barrel sectors (8 x Analytical Method algorithm instances)

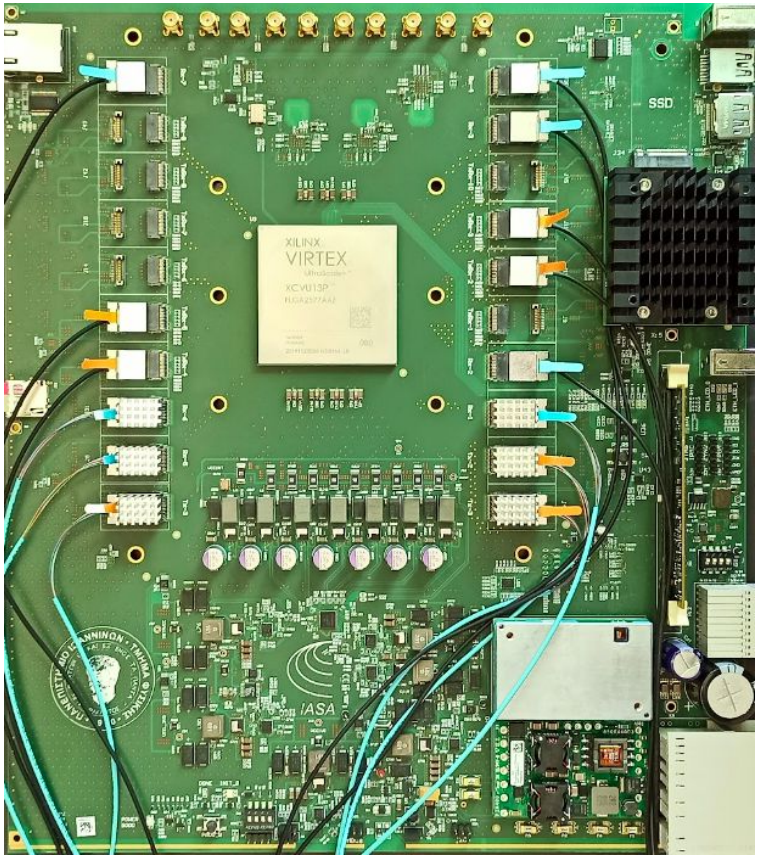
Integration

- The prototype board is in operation in SX5 (CMS surface) *24/7* since Fall 2022
  - *Algorithm integration & development*
- Collision data have been captured & processed with the board (Late 2022), instrumenting 4 DT chambers
  - *Installed in the BMTF rack of the CMS counting room*
  - *Shown excellent performance*
  - *Successfully demonstrated in realistic conditions a slice of the CMS Phase 2 Trigger*



Conclusion

- An ATCA board meeting the specifications of the BMTL-1 was designed
- 3 PCBs were produced
- 2 boards were assembled
- The functionality of the design was tested and verified
- 1 more board to arrive soon
- A lot of progress in system integration



Thank you!