The Monolithic ASIC for the High-Precision Preshower Detector of the FASER Experiment at CERN

Stefano Zambito, on behalf of the FASER Preshower Upgrade team

FASER

18th Trento Workshop on
Advanced Silicon Radiation Detectors
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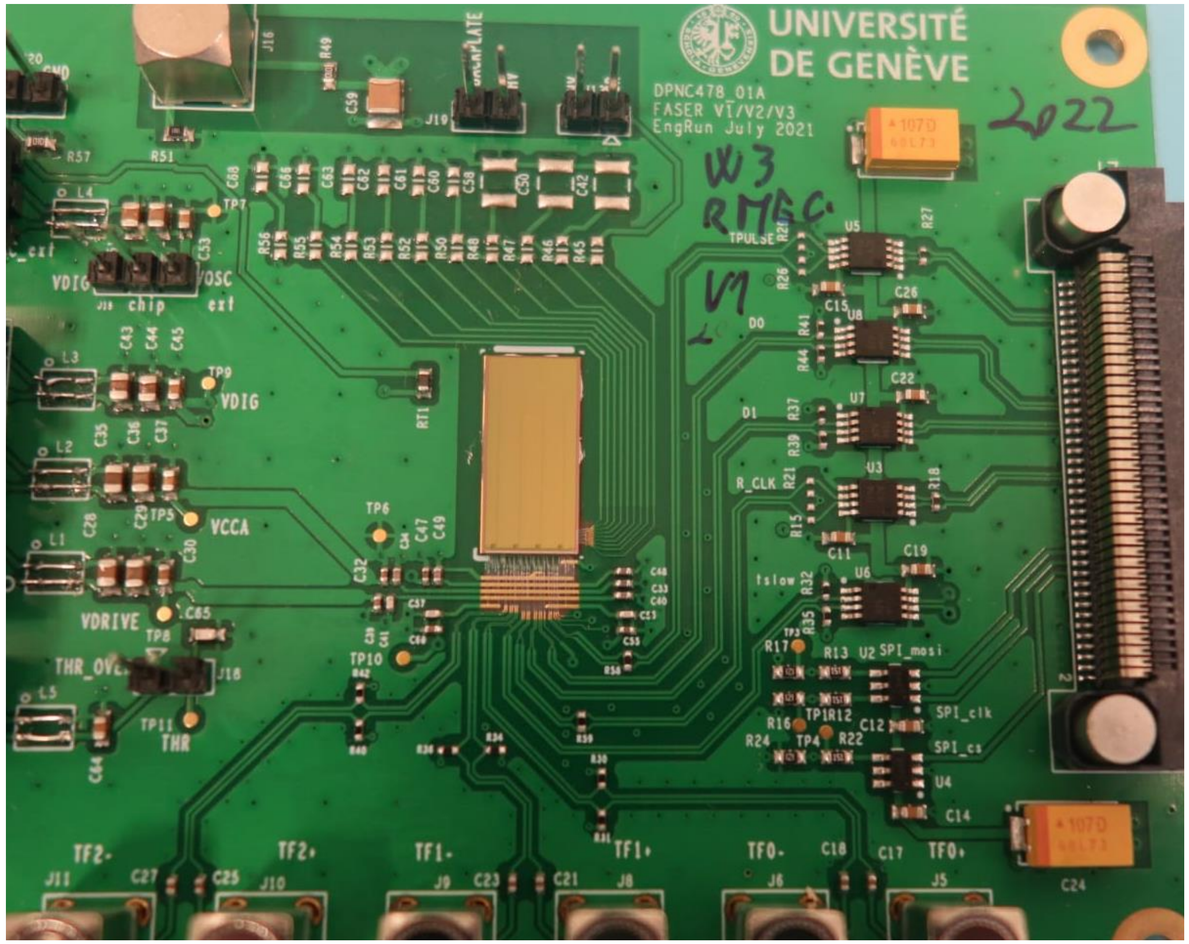
UNIVERSITÉ DE GENÈVE

Outline

Today's talk:

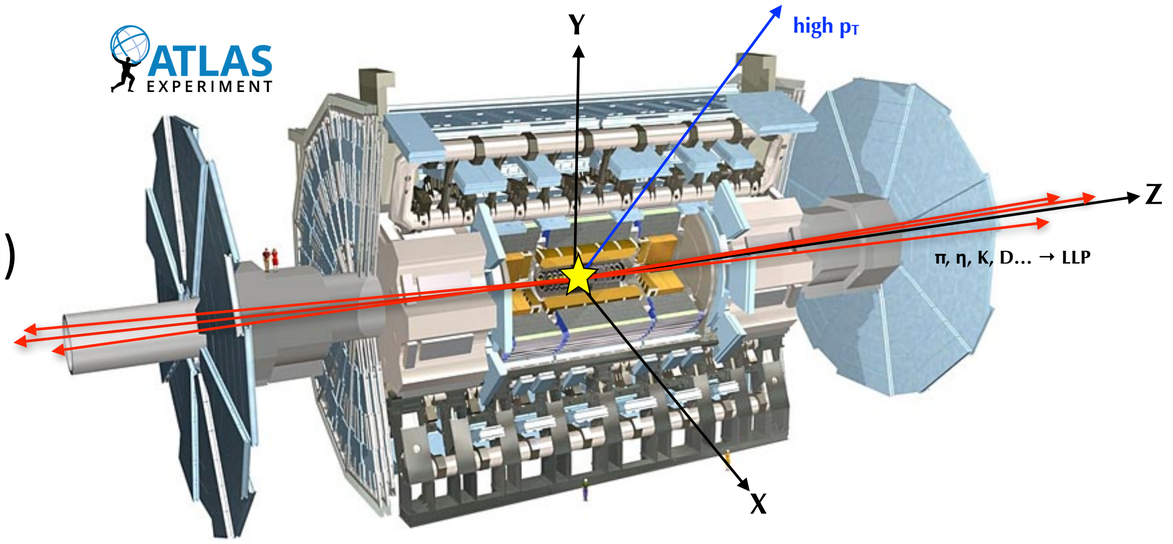
- The FASER experiment at CERN
- Upgrade of preshower detector
- Monolithic pixel ASIC
- Pre-production chip prototype
- Summary & outlook

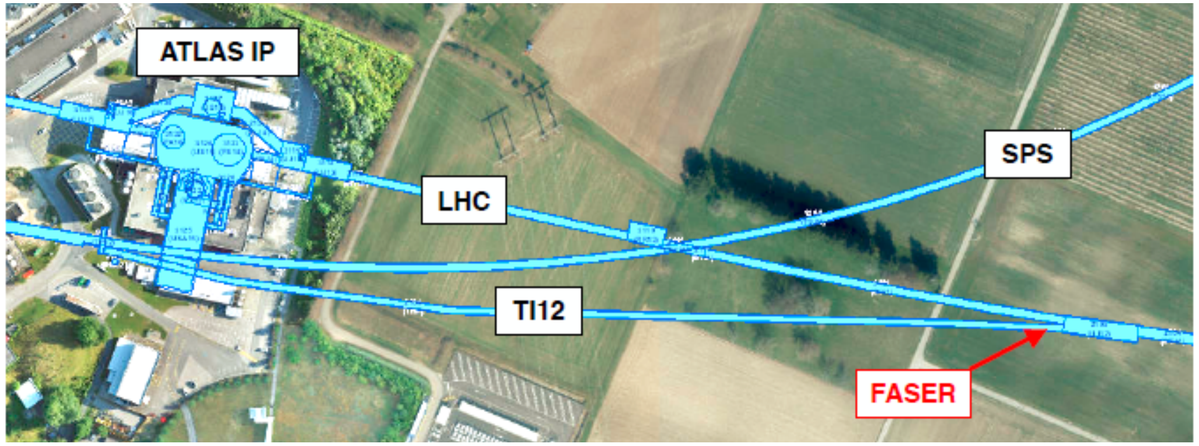


The FASER Experiment

The ForwArd Search ExpeRiment at the LHC

- located ≈480 m away from ATLAS IP, along beam axis
- search for light, weakly interacting new particles (LLPs)
  - mostly produced in the very forward region (θ∼mrad), from rare meson decays (π, η, K, D …)





Zero degrees angle → huge LLPs flux

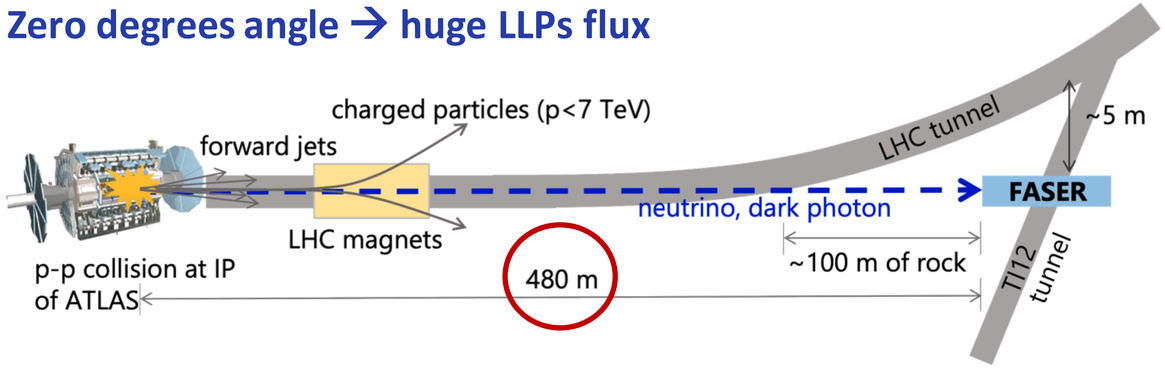
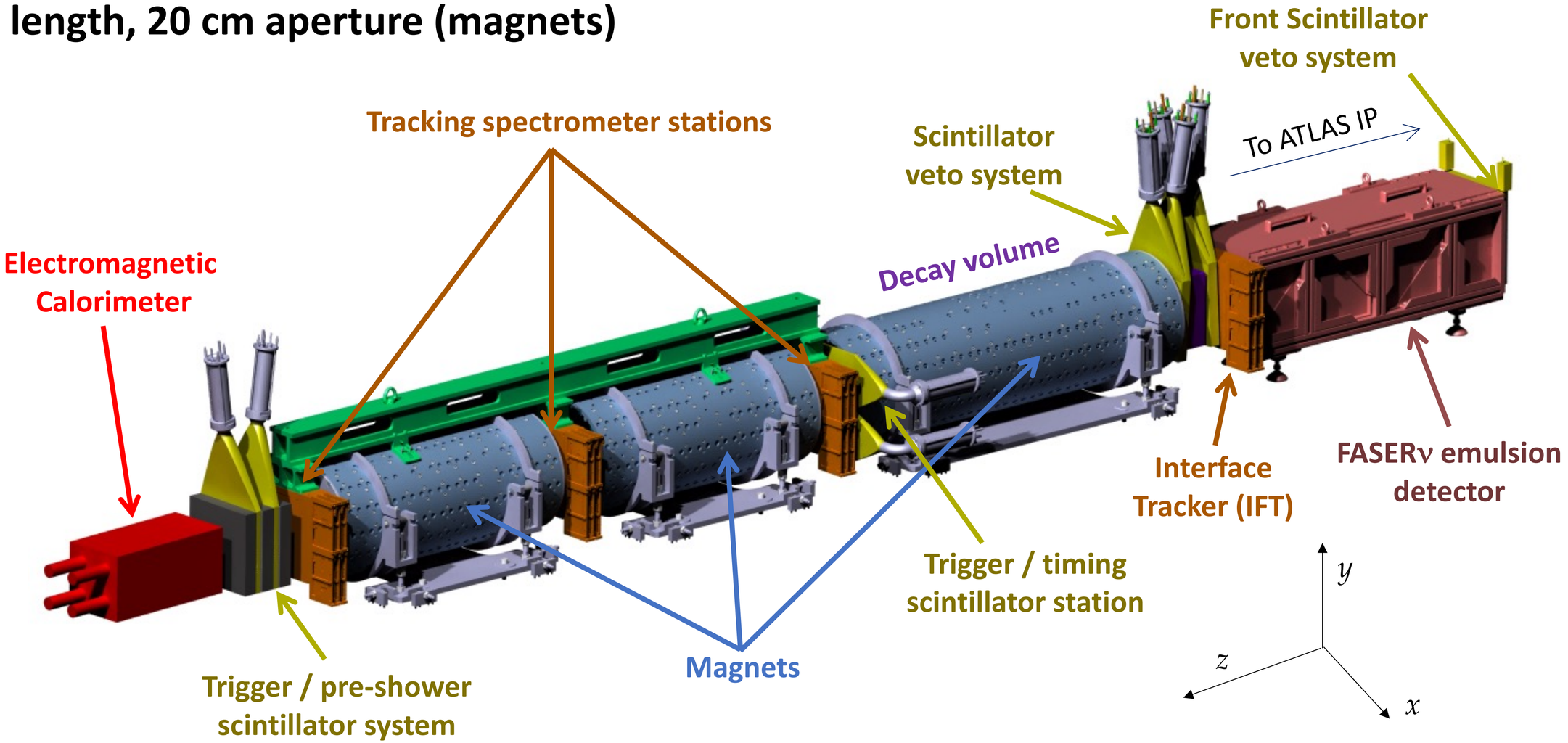


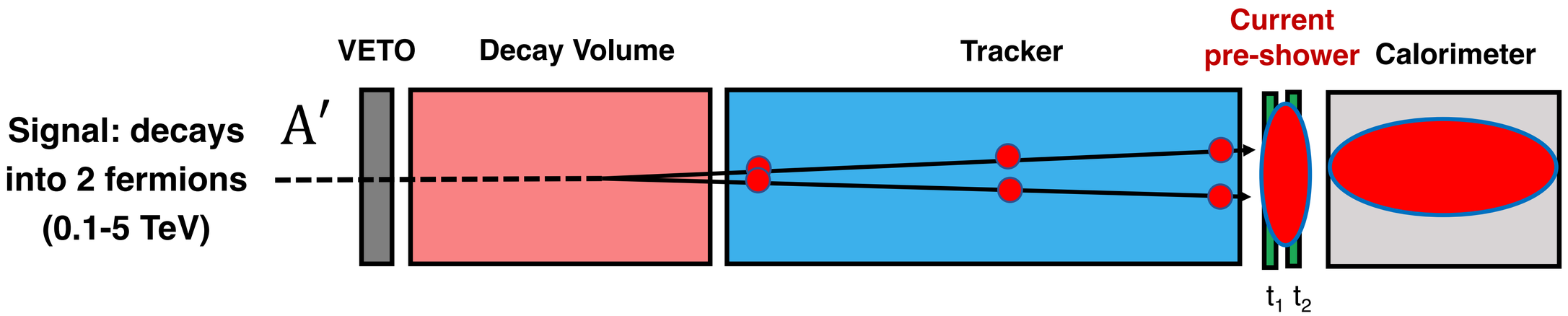
Figure: Location of FASER in the tunnel - schema is not in scale.

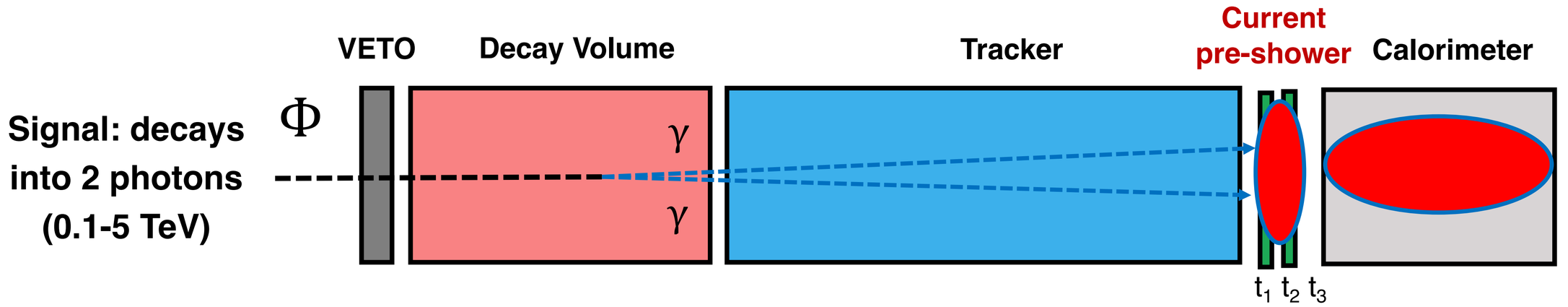
The FASER Experiment

5 m length, 20 cm aperture (magnets)

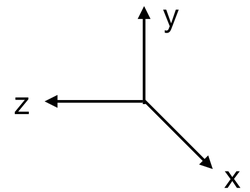


Current Detection Capabilities: Two Fermions

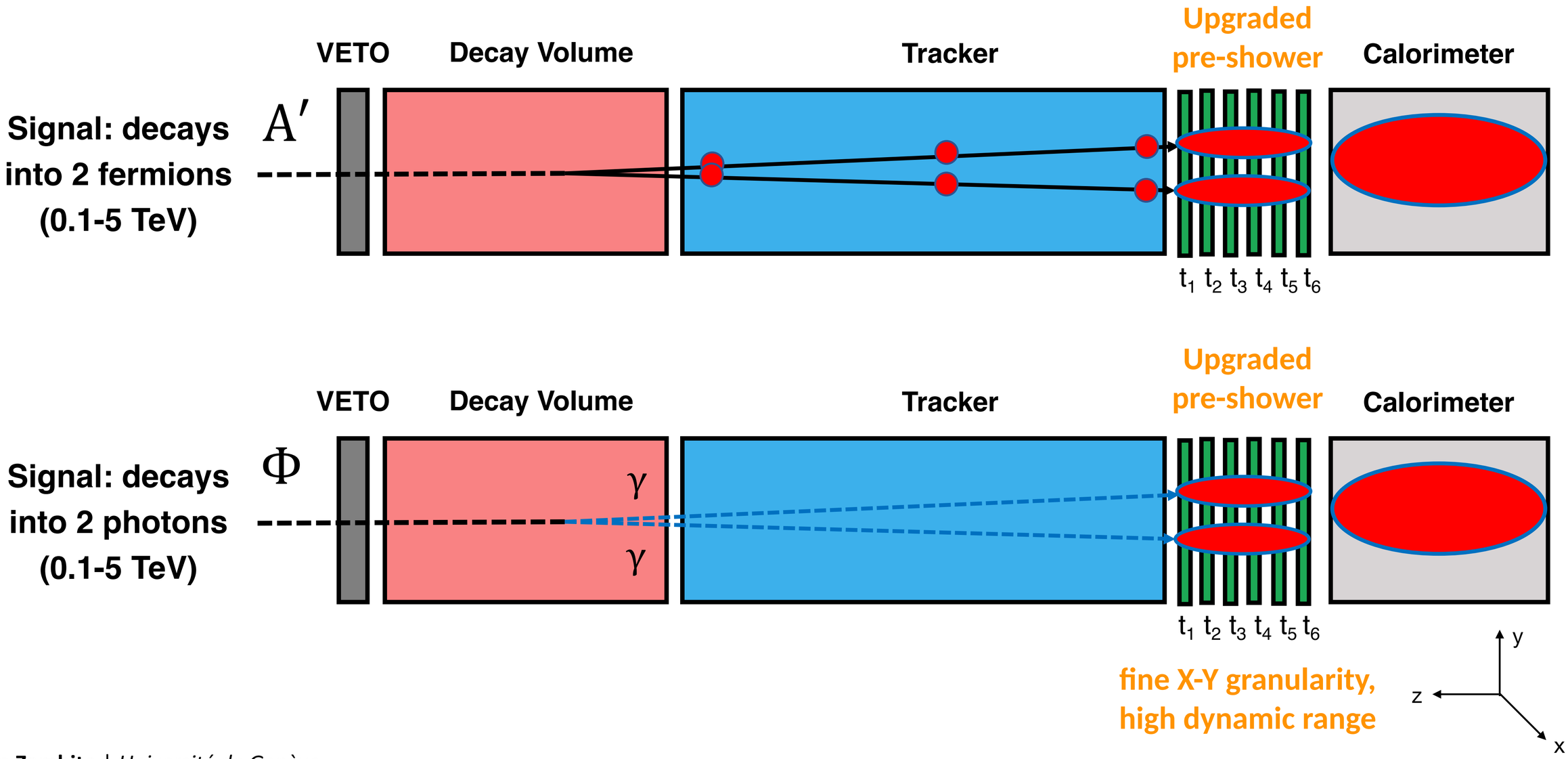




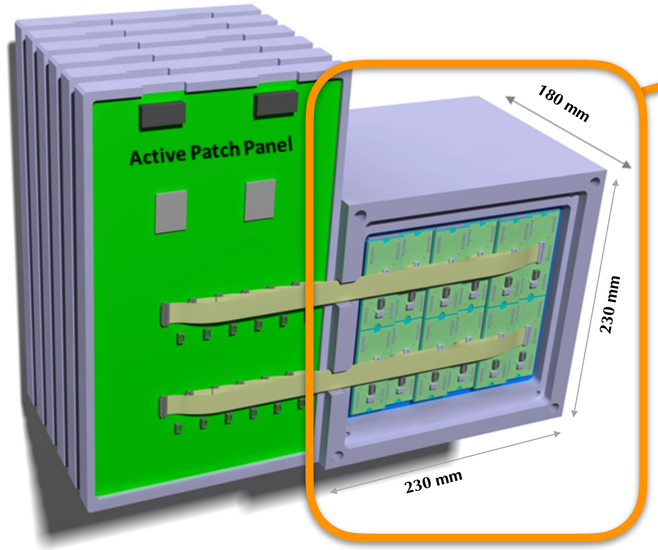
no X-Y granularity: unable to resolve diphoton events!



Desired Detection Capabilities: Two Fermions / Photons

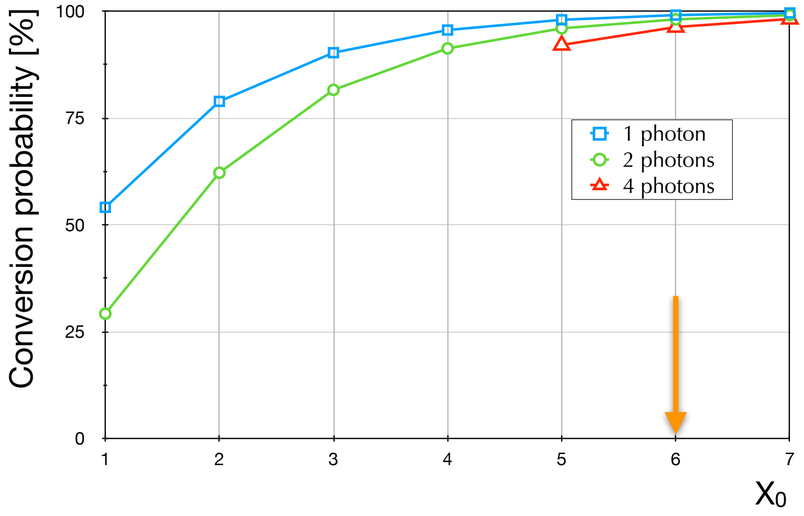


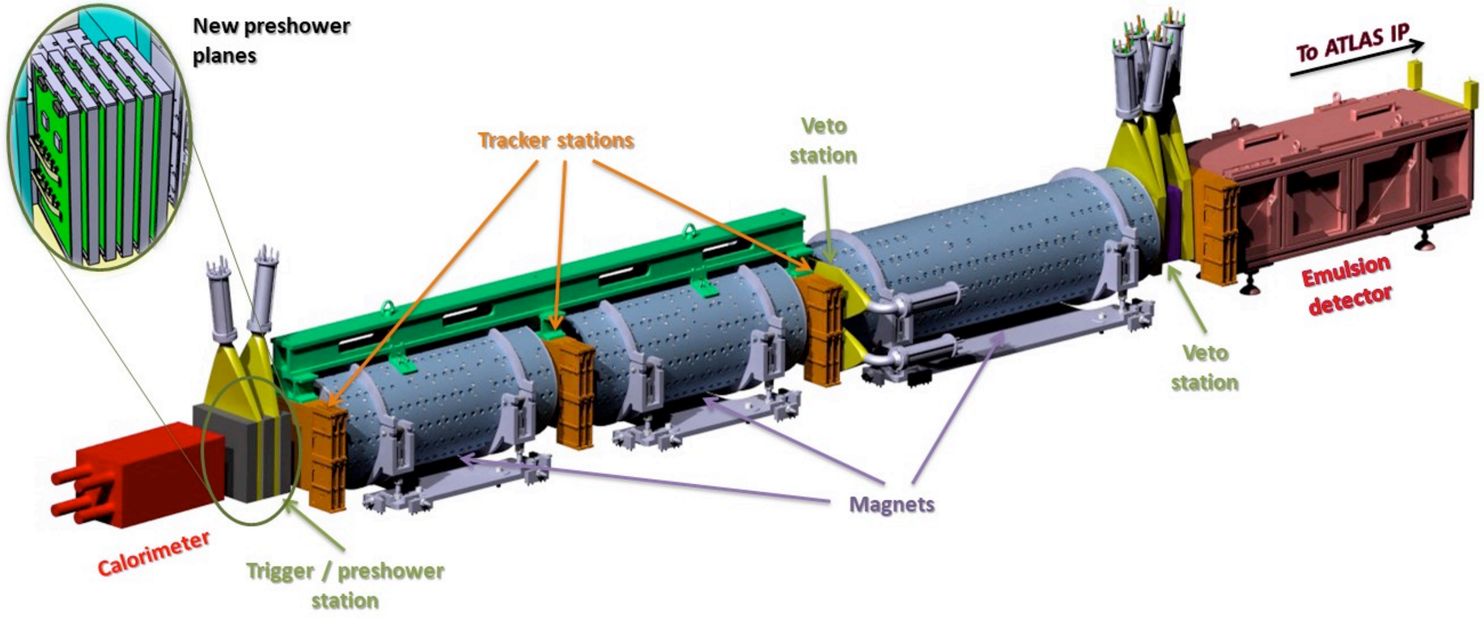
New Preshower Detector [I]



Upgraded preshower detector

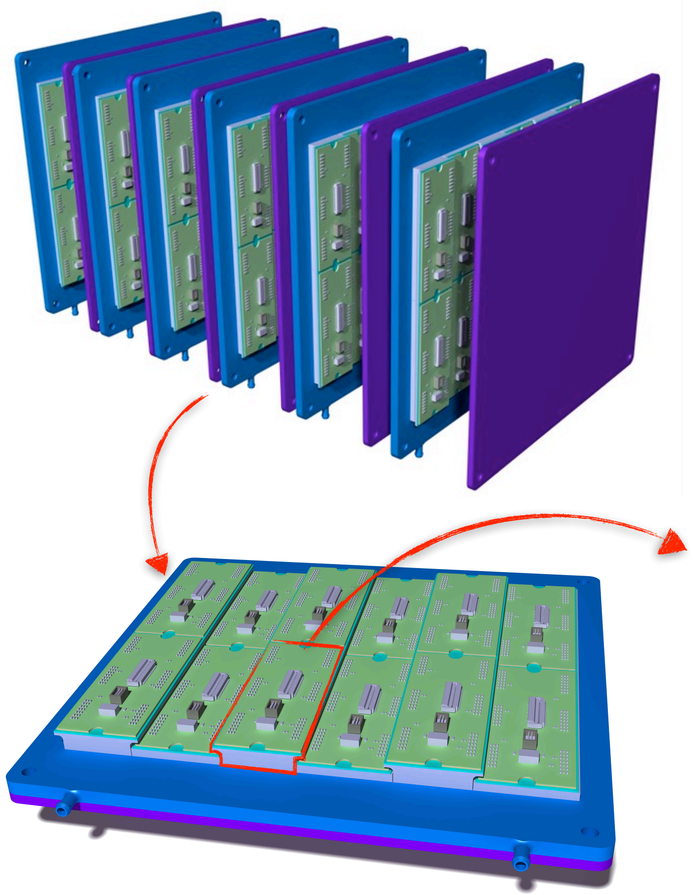
- 6 detector planes + 2 scintillators
  - each plane: 1 X_0 tungsten + monolithic Si pixel sensors
- project approved by CERN: CERN-LHCC-2022-006
- targeting installation in 2024, during LHC Run 3





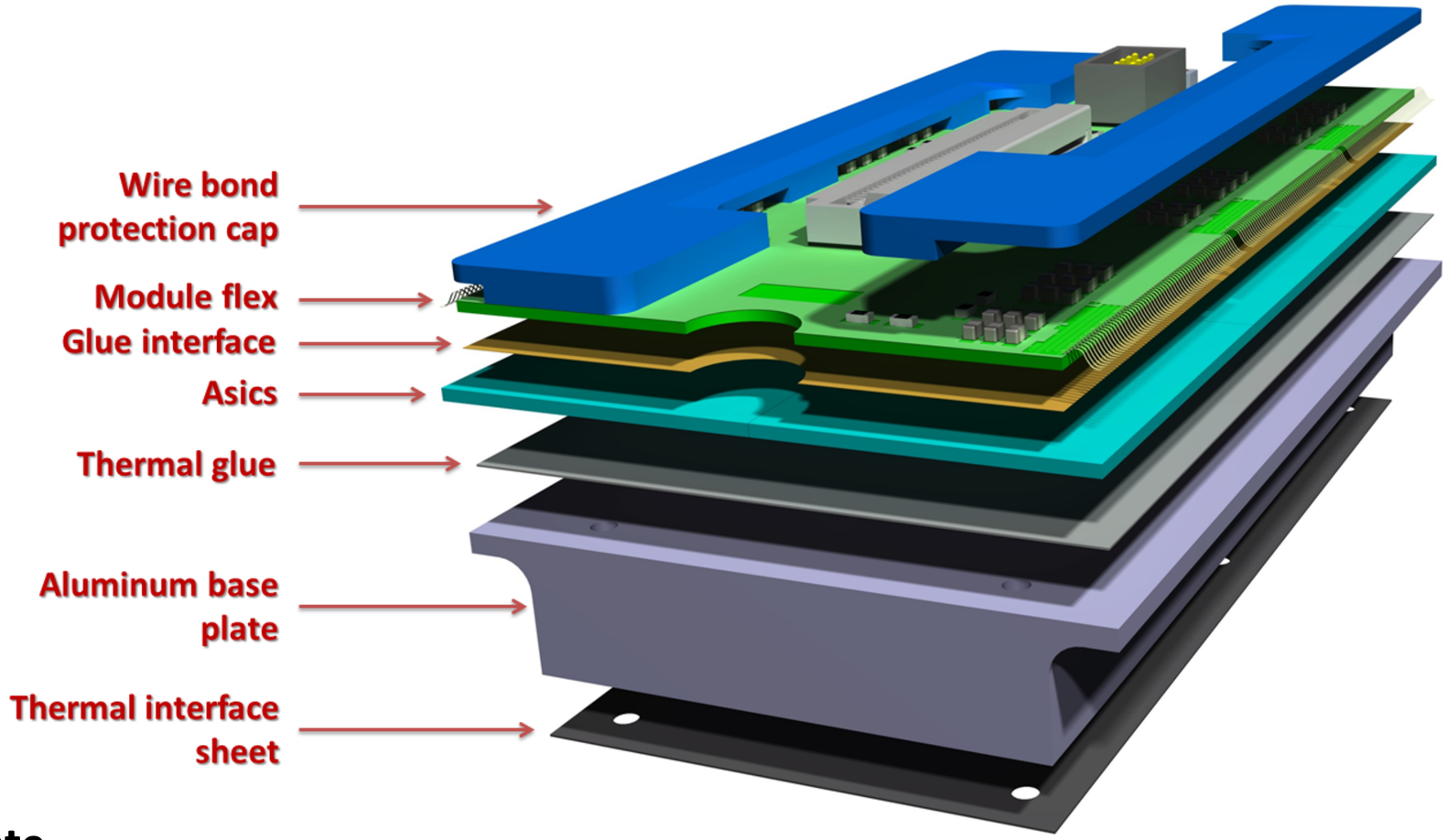
New Preshower Detector [II]

6 planes in total (silicon detector + W plate)



12 modules per plane, on cooling plate

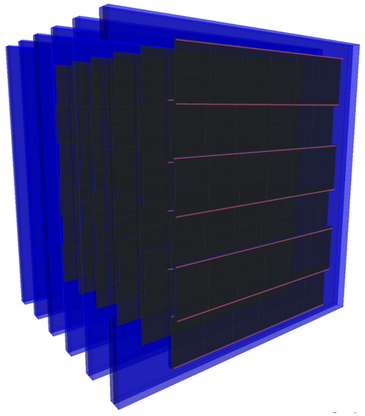
6 ASICs per module, 208x128 pixels each

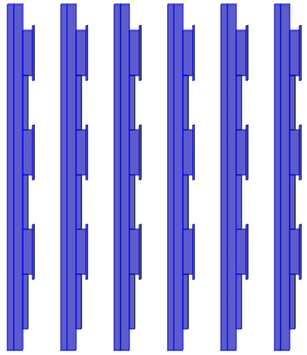


Detailed Preshower Simulation

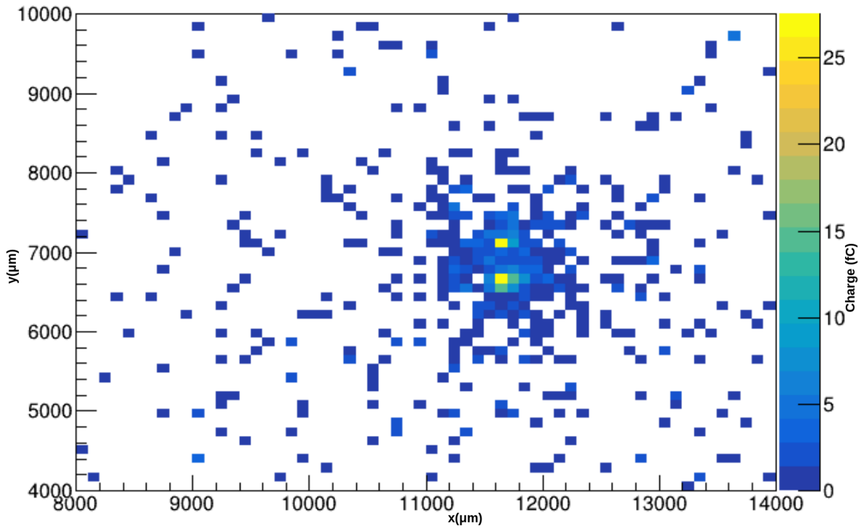
Two photons

E=1 TeV, ΔR=0.5 mm

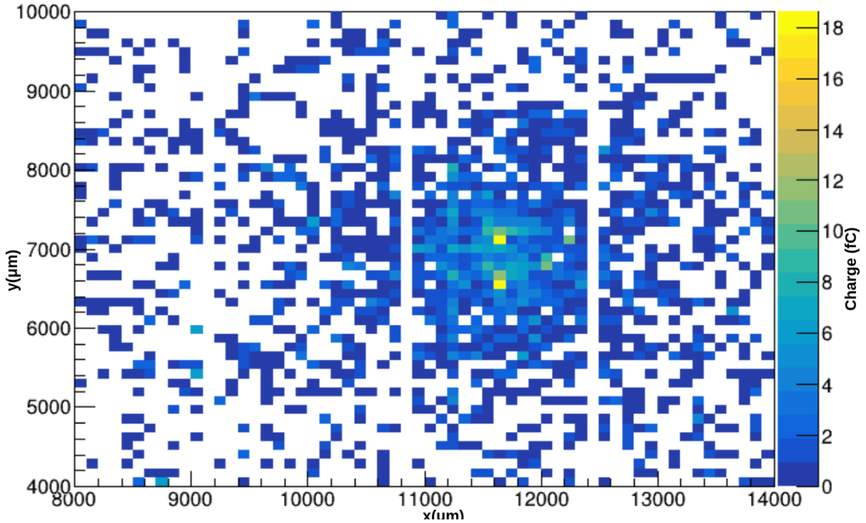




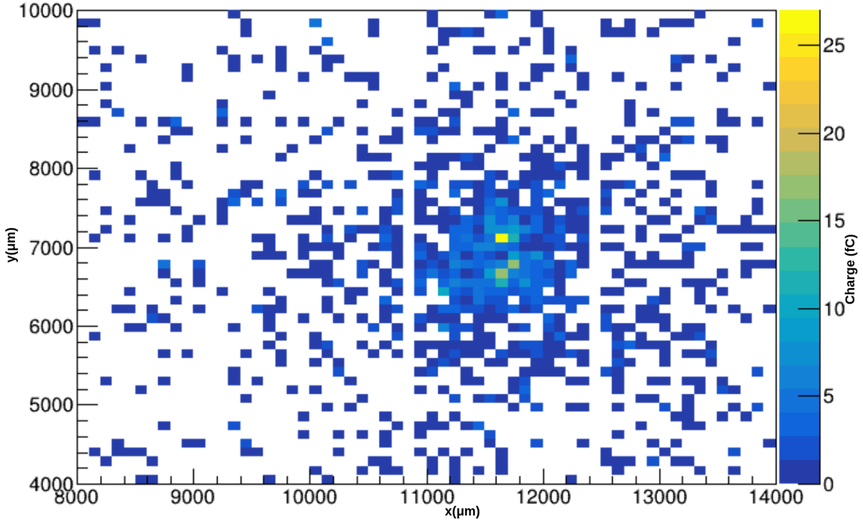
Plane 3



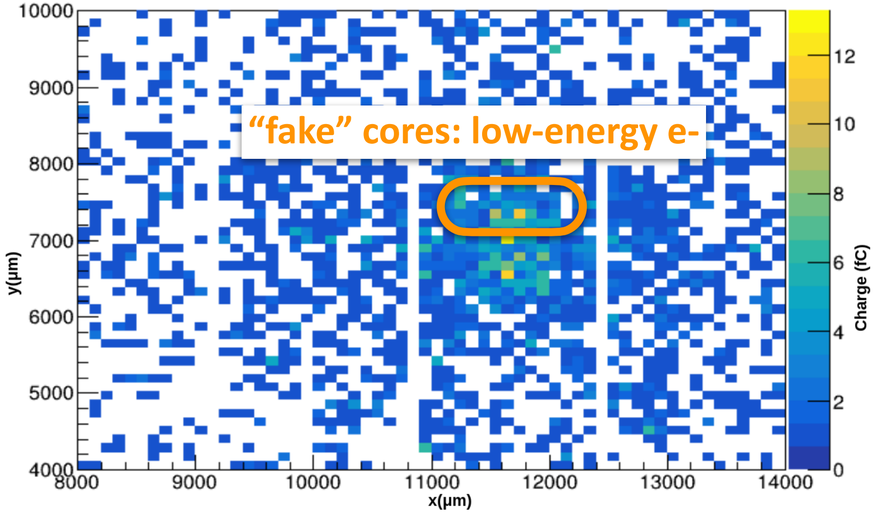
Plane 5



Plane 4



Plane 6

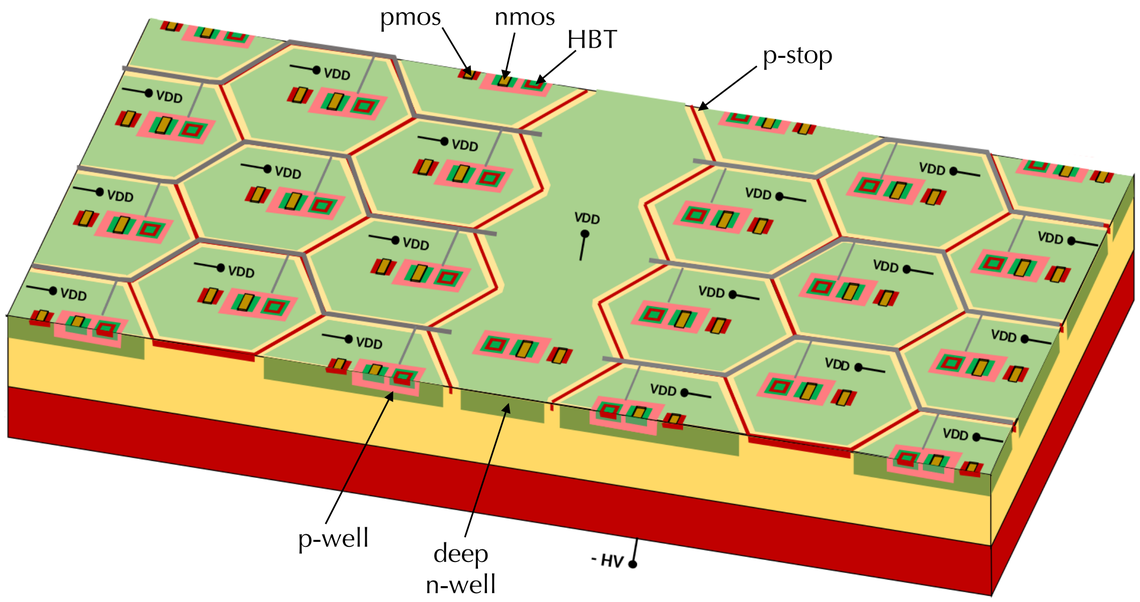


Monolithic Pixel ASIC: Sensor

Monolithic active pixel sensor

130 nm SiGe BiCMOS technology (IHP SG13G2)

- High-resistivity (220 Ω·cm) substrate, about 130 µm thickness
- Hexagonal pixels integrated as triple wells; pixel capacitance of 80 fF



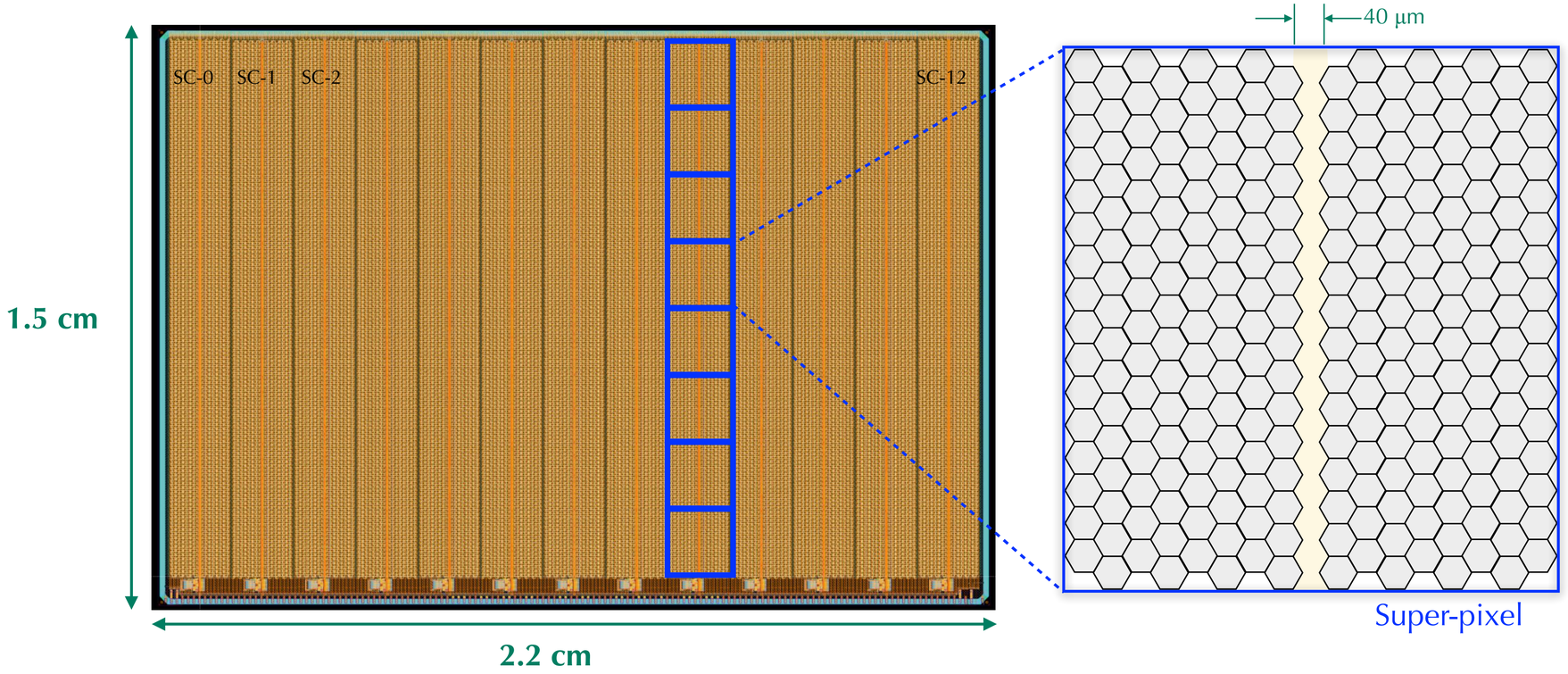
Main specifications	
Pixel Size	65 µm side (hexagonal)
Pixel dynamic range	0.5 ÷ 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 µs
Power consuption	< 150 mW/cm^2
Time resolution	< 300 ps

Monolithic Pixel ASIC: Chip Structure

Chip organized in 13 “*super-columns*”, each with:

- ⇒ active region, subdivided into 8 “*super-pixels*” of 16x16 pixel each
- ⇒ digital column (40 µm) in the middle: sharing of digital electronics

Digital periphery on the bottom, and multiple guard-ring structure



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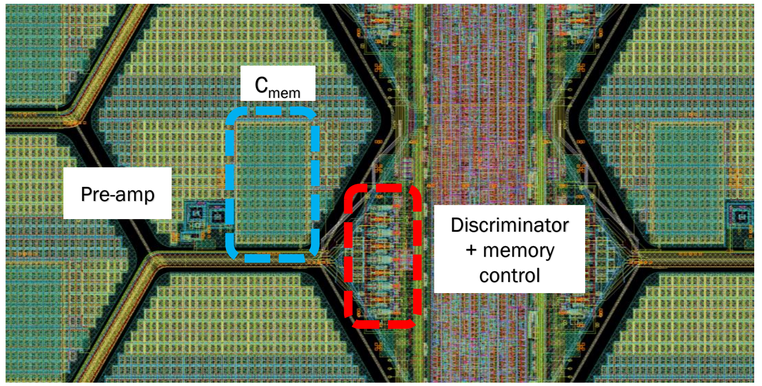
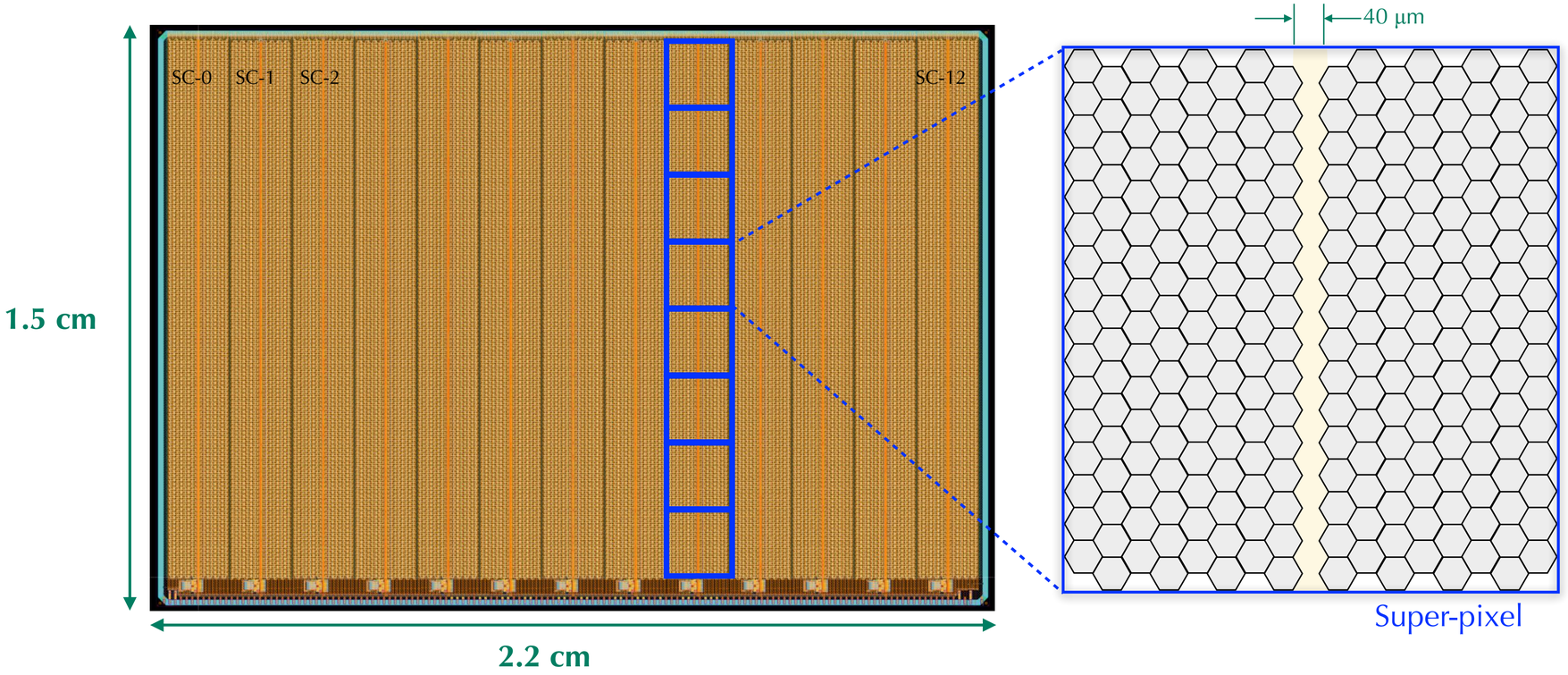




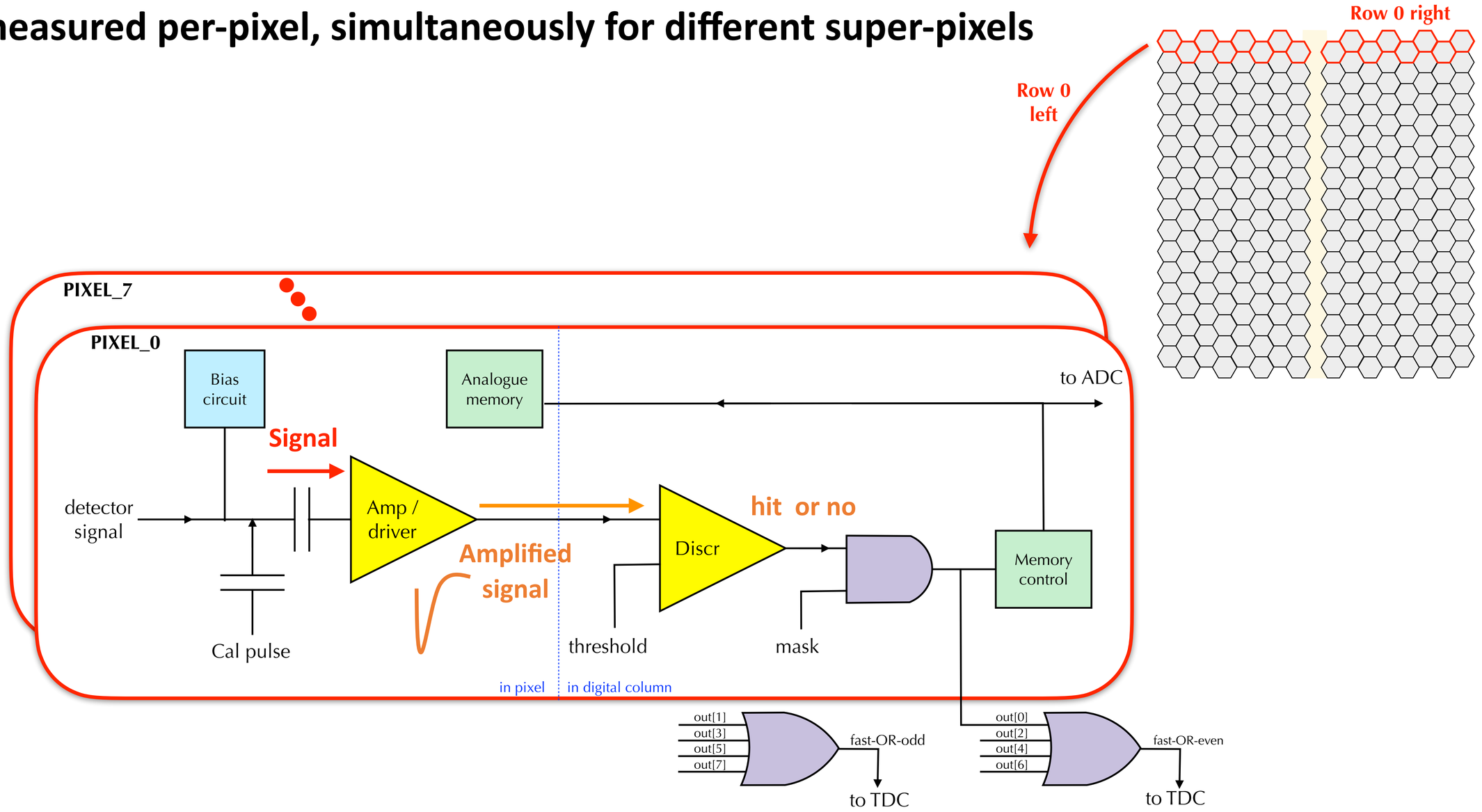
Super pixel:

- ↳ 16 rows of 8+8 pixels
- ↳ analog multiplexer
- ↳ 4-bit flash ADC
- ↳ 3 fast-OR lines
- ↳ local bias circuit
- ↳ programming logic to mask pixels

Dead area <5%

Monolithic Pixel ASIC: Pixel Circuitry

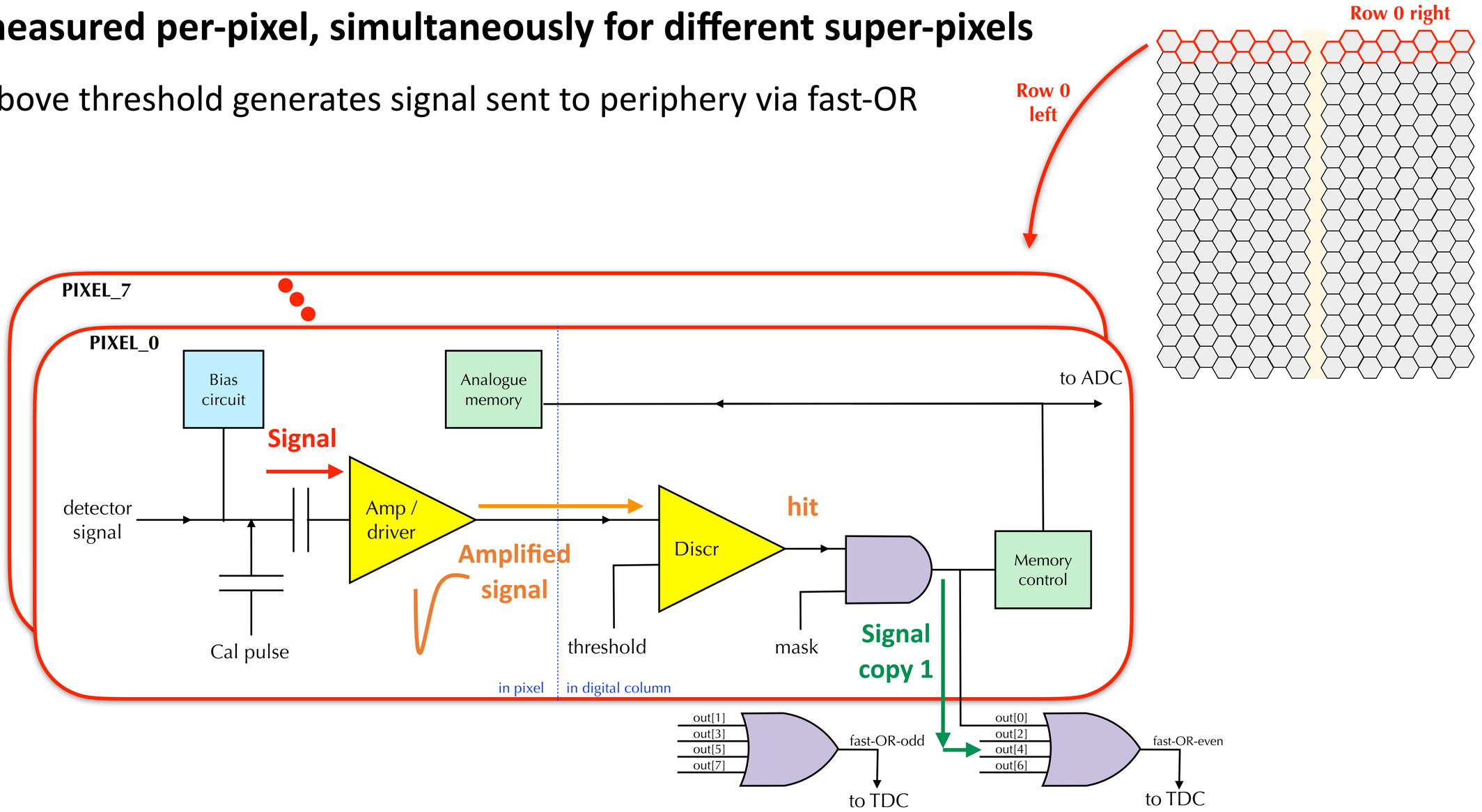
Charge measured per-pixel, simultaneously for different super-pixels



Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

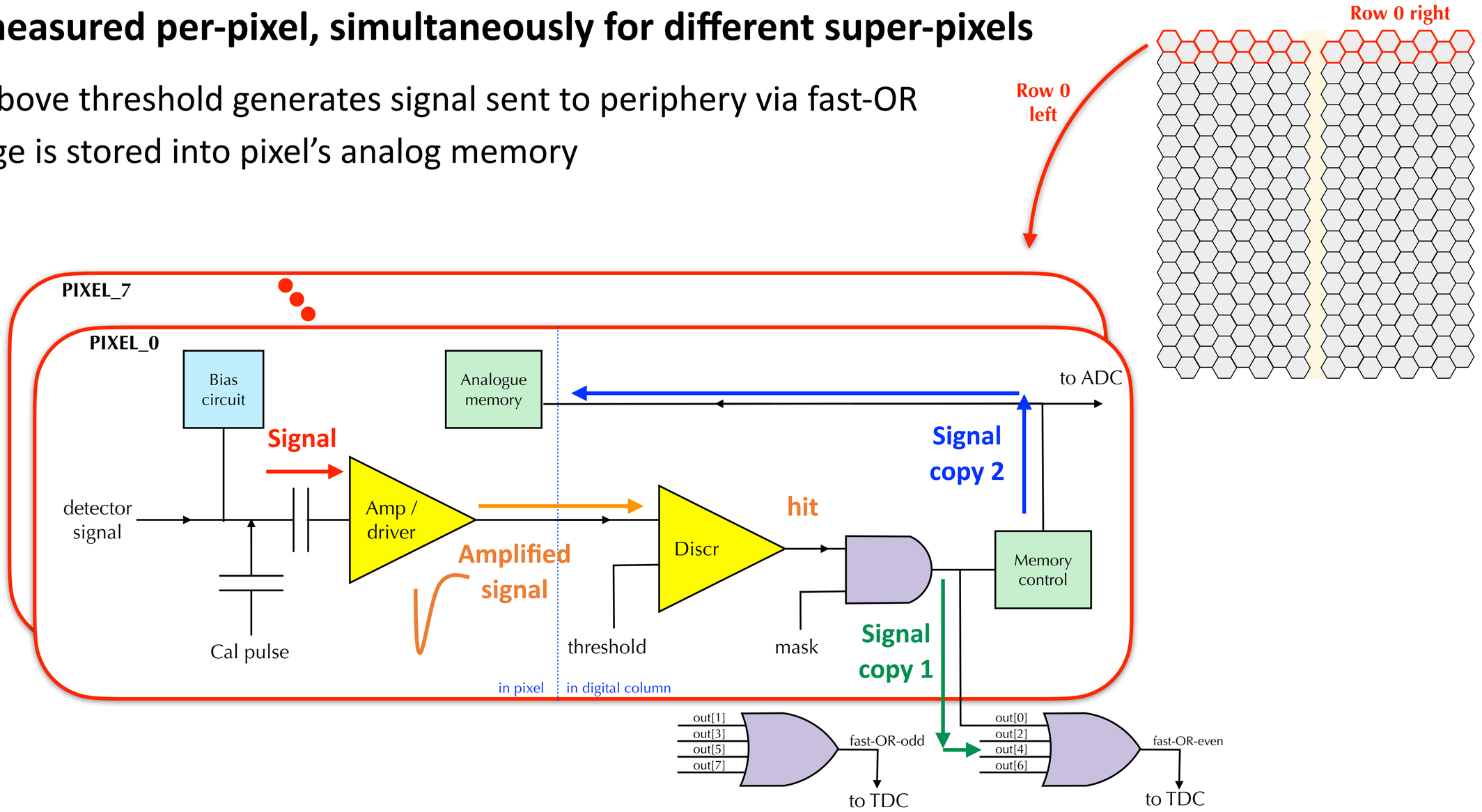
=▶ hit above threshold generates signal sent to periphery via fast-OR



Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

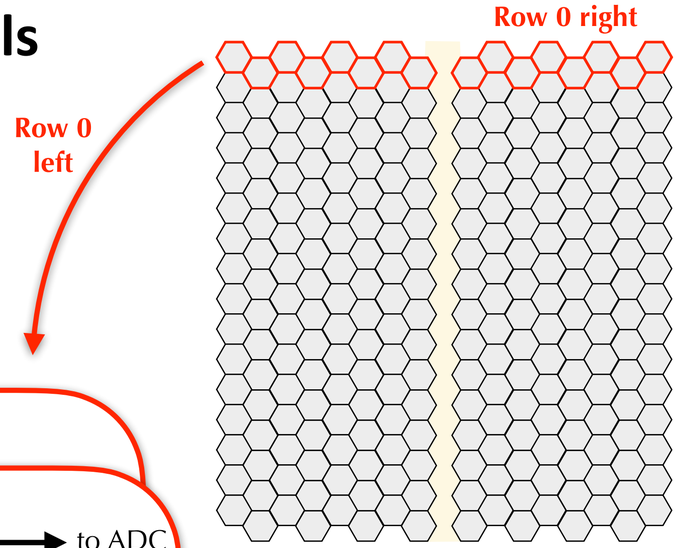
- ⇒ hit above threshold generates signal sent to periphery via fast-OR
- ⇒ charge is stored into pixel's analog memory

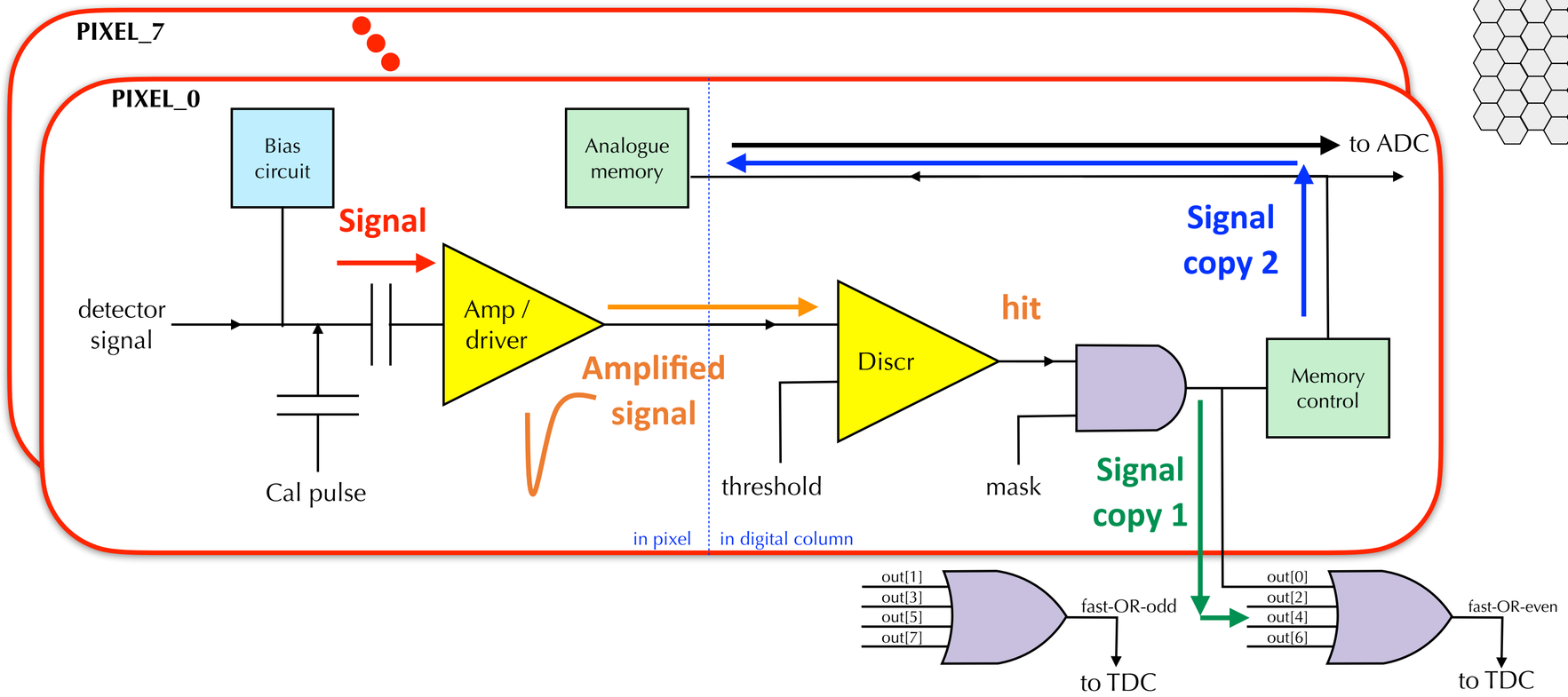


Monolithic Pixel ASIC: Pixel Circuitry

Charge measured per-pixel, simultaneously for different super-pixels

- ⇒ hit above threshold generates signal sent to periphery via fast-OR
- ⇒ charge is stored into pixel's analog memory
- ⇒ after some delay, readout starts super-column after super-column





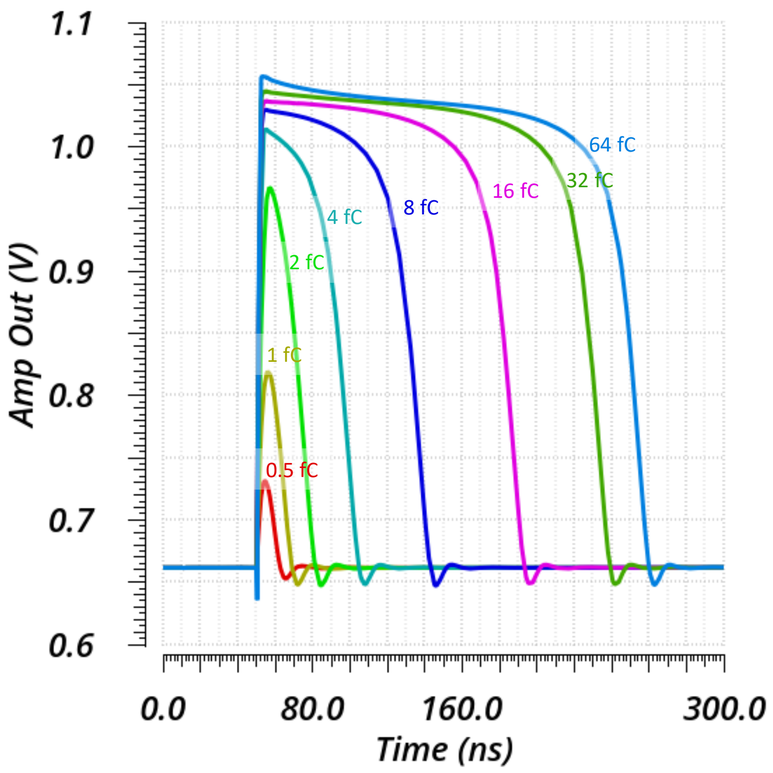
Monolithic Pixel ASIC: Charge Measurement

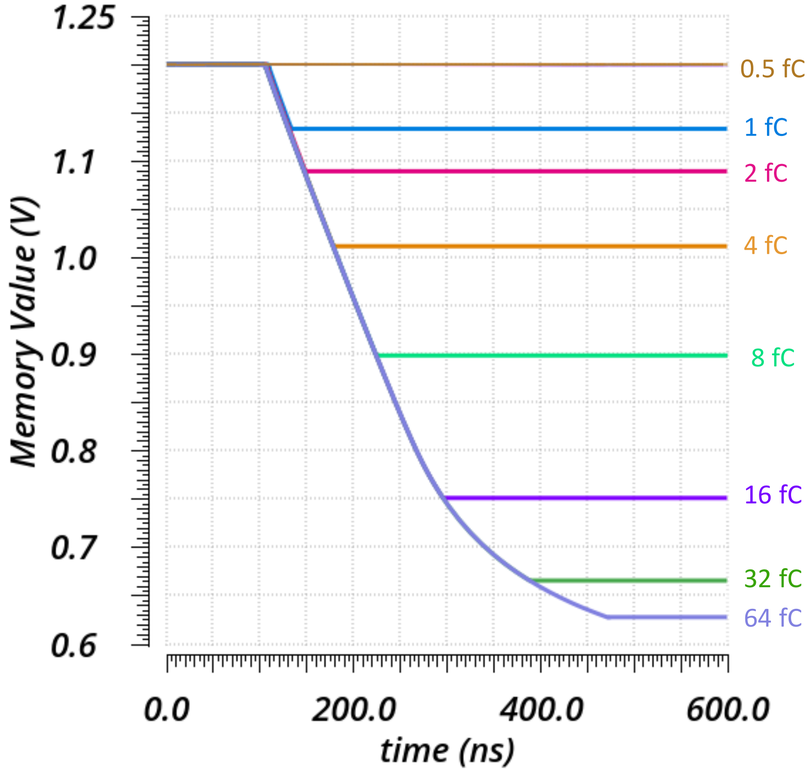
Analog memories: capacitors inside each pixel charged with const current during ToT

=▶ when signal returns below threshold, memory is disconnected and left floating until read by flash ADC

=▶ preamplifier designed to produce a signal proportional to the *log* of input charge

Simulation data





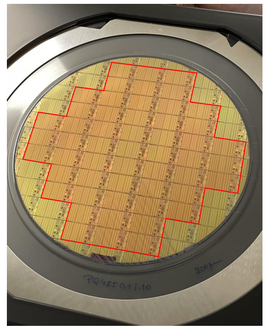
Pre-production Chip (2022)

Engineering run (IHP Microelectronics)

Reticle: 2.4 x 1.5 cm^2

53 reticles per wafer

Thickness 300 µm



=▶ In each reticle, three pixel matrices

FASER_v1 (baseline)

↳ 128 x 64 pixels, 4 super-columns

↳ in-pixel pre-amp and driver

↳ discriminator outside

FASER_v2

↳ 128 x 48 pixels, 3 super-columns

↳ in-pixel pre-amp, driver, and discriminator

FASER_ALT

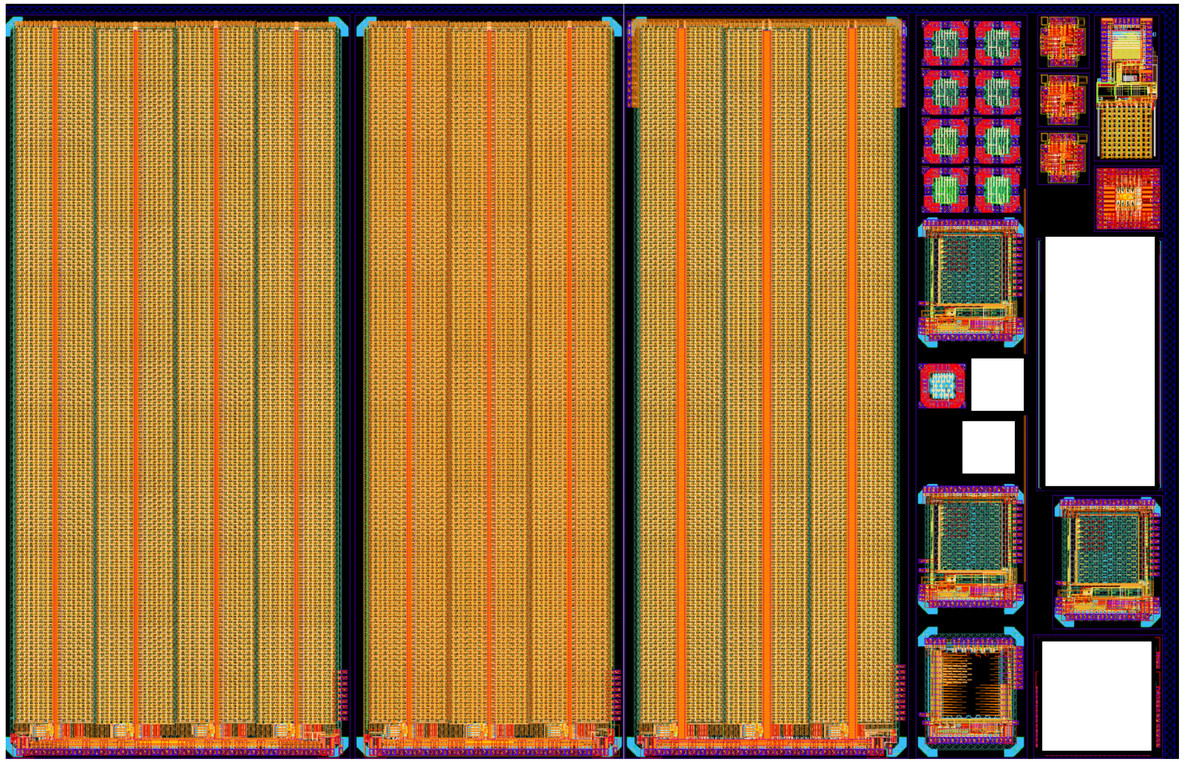
↳ 128 x 48 pixels, 3 super-columns

↳ no analog memories

↳ counter for charge measurement

=▶ Several test structures (TDC, etc…)

FASER_v2 *FASER_v1* *FASER_ALT*



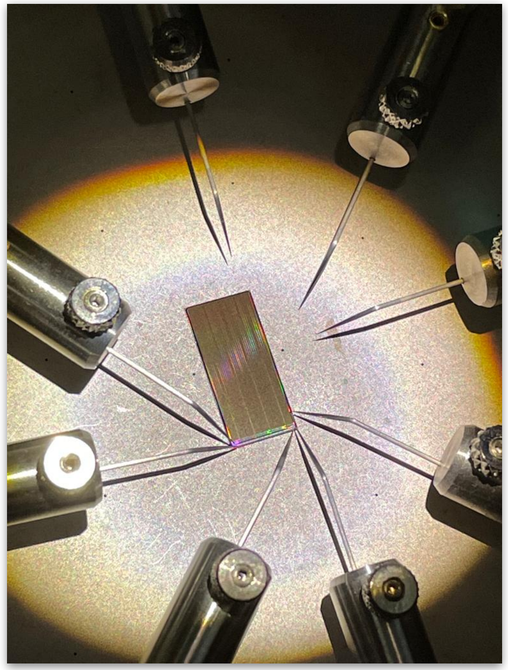
Pre-production Chip: I-V Characteristic [I]

Wafers with pre-production prototype chips received on Jun 13th, 2022

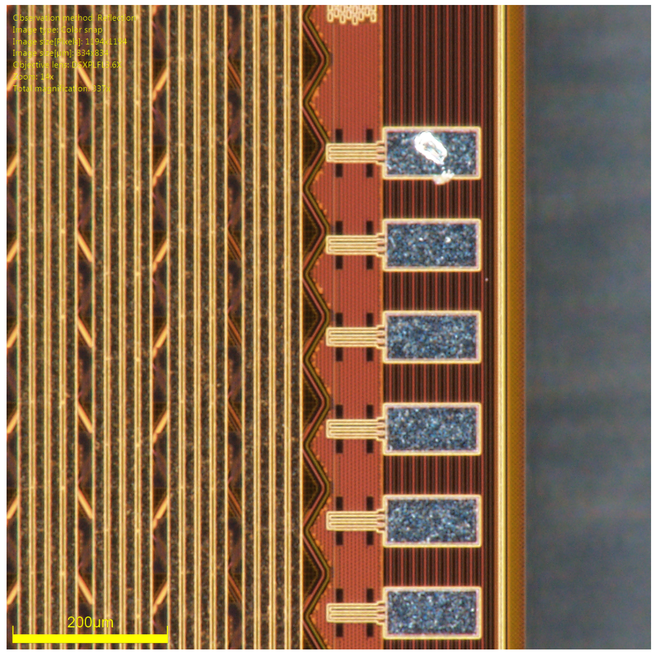
=▶ 3 standard wafers (50 Ω·cm w/o EPI), 3 EPI wafers (1 Ω·cm substrate + 350 Ω·cm EPI layer)

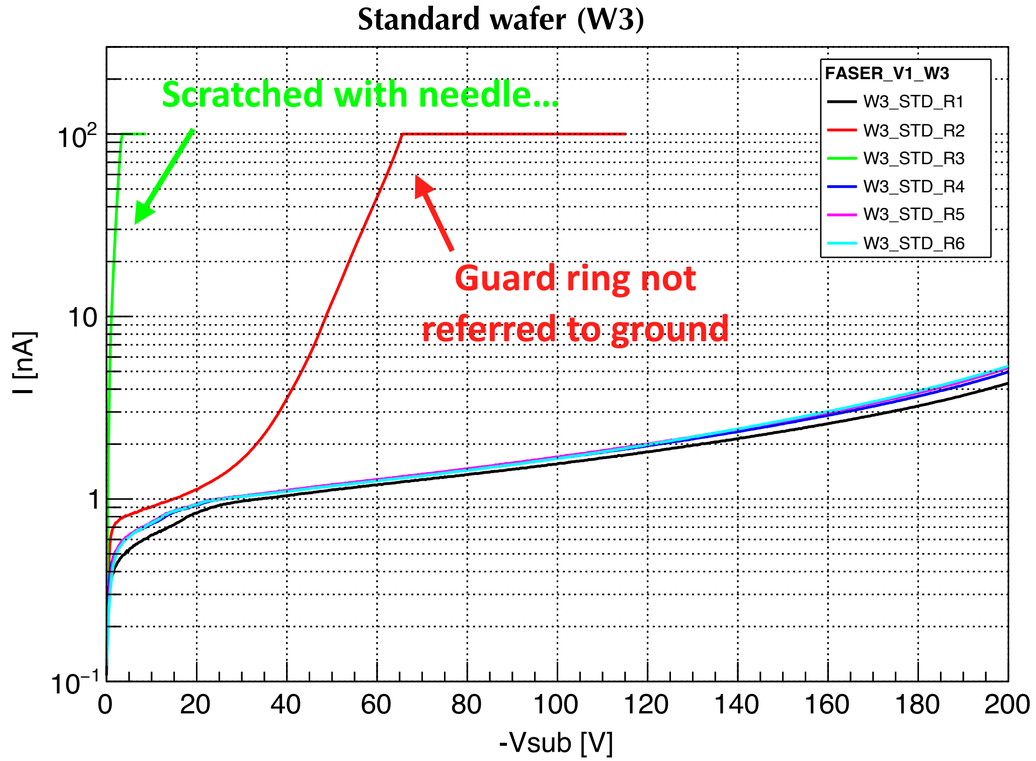
Good results from I-V characterizations at probe station

=▶ reaching 200 V with guard ring connected to ground, 170 V otherwise

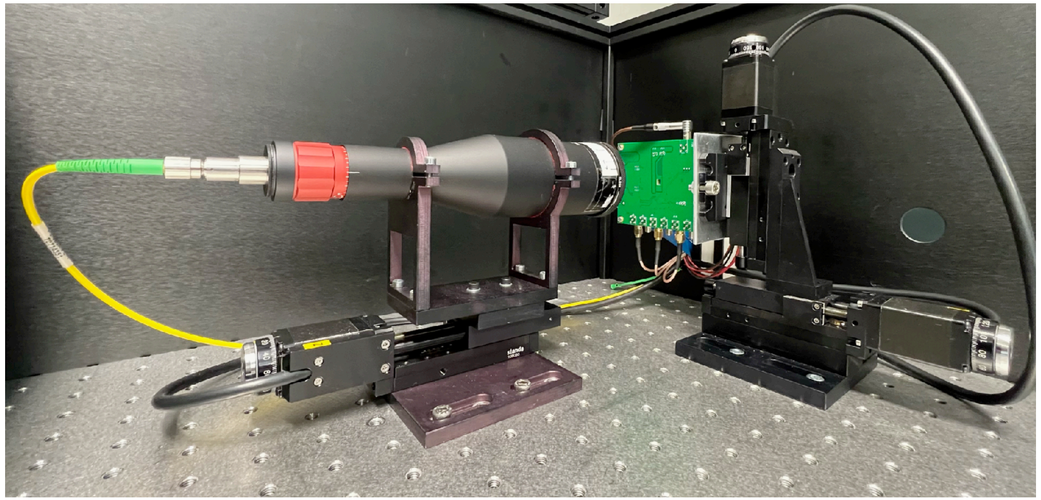


FASER_MAIN chip



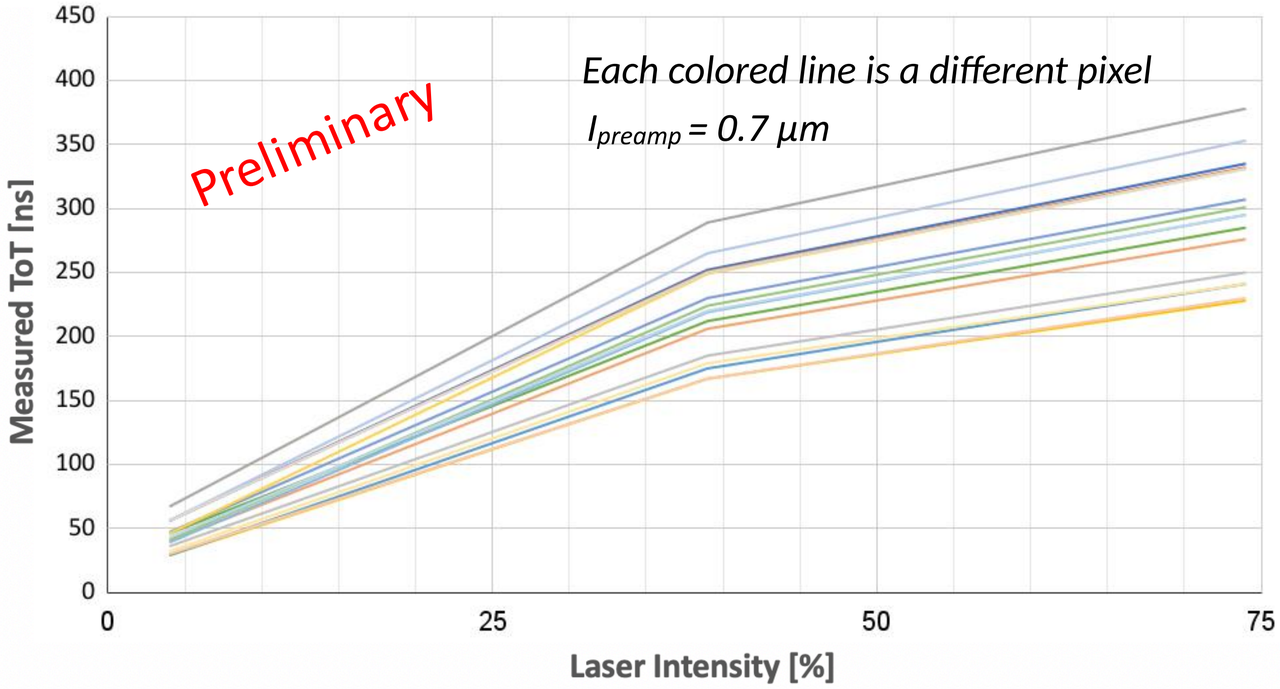


Pre-production Chip: TOT (Charge) Mismatch [I]



Evaluating charge response with infrared laser

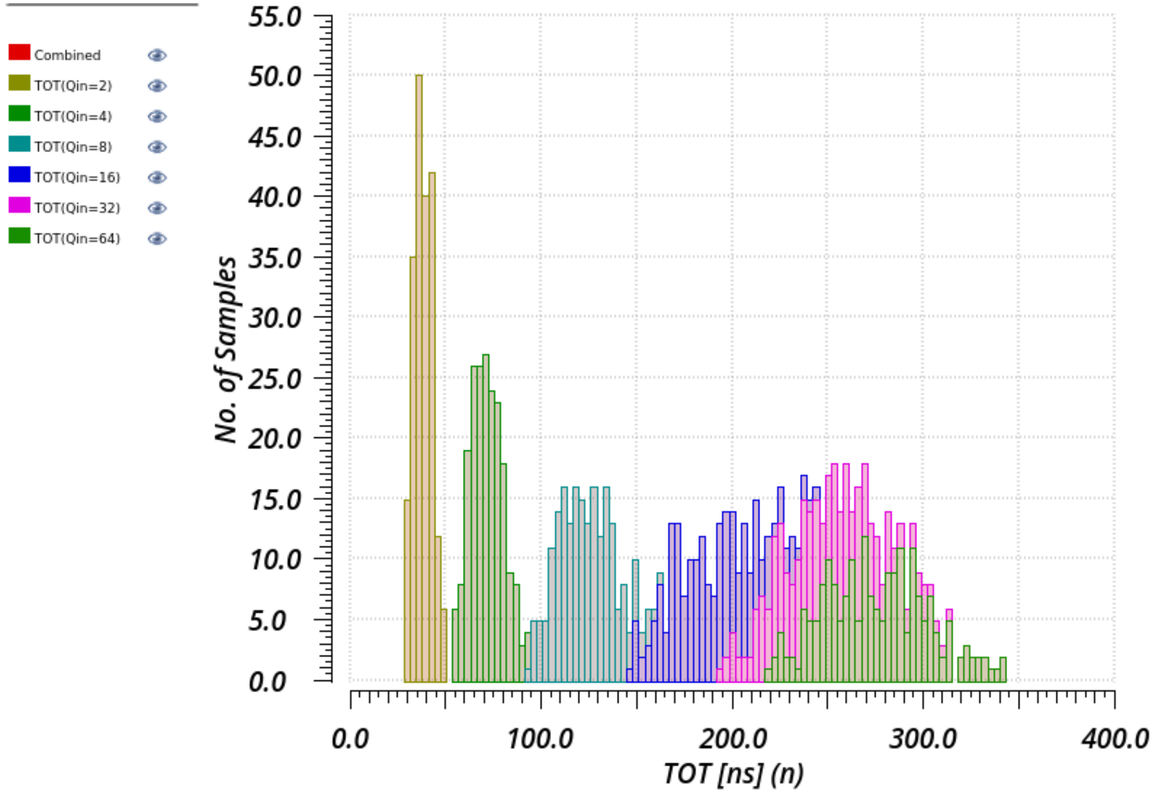
- measuring ToT via fast-OR signal on the scope
- varying per-pixel injected charge via laser attenuator
- measurement repeated at different I_{preamp}



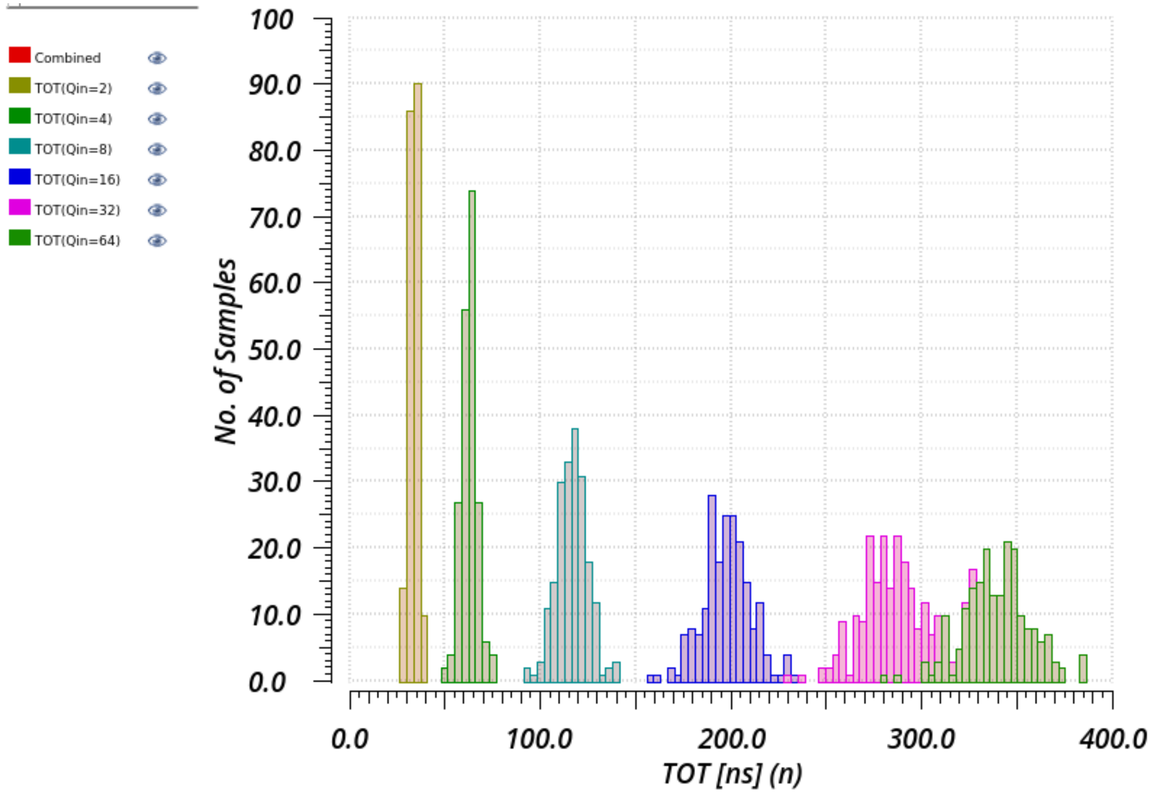
Pre-production Chip: TOT (Charge) Mismatch [II]

Expect improvement of front-end uniformity in production ASIC thanks to bigger transistors

Cadence Spectre Simulation:
front-end mismatch in pre-reduction prototype



Cadence Spectre Simulation:
front-end mismatch in production ASIC



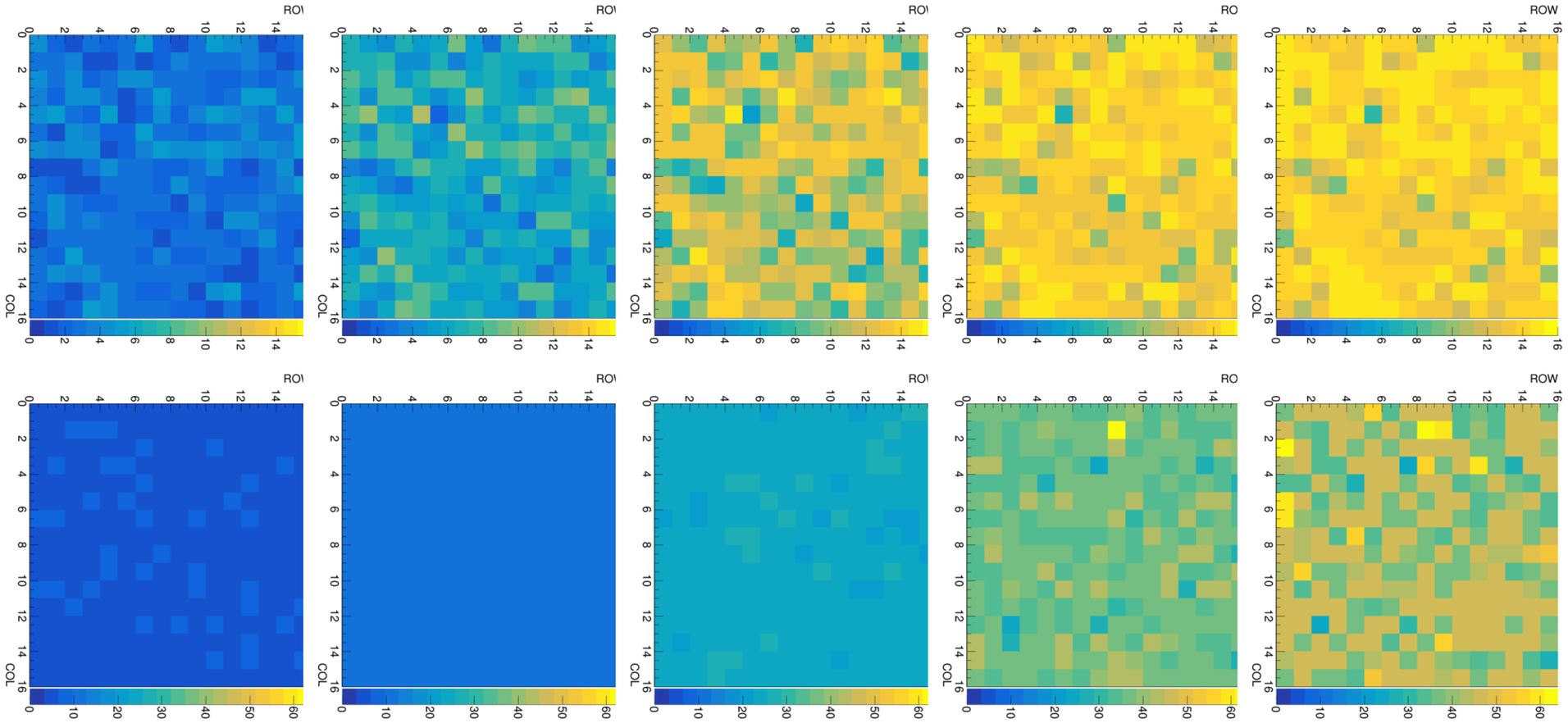
Test With Full Readout: Charge Calibration

One super pixel:
16x16 pixels

Increasing injected charge via testpulse

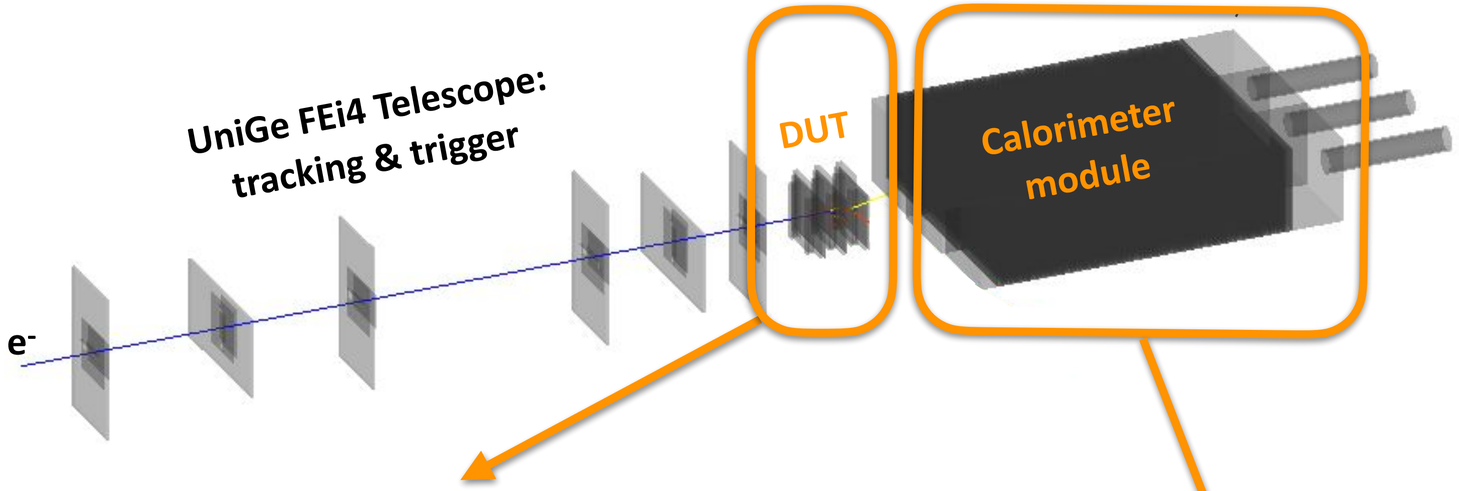
Before calibration

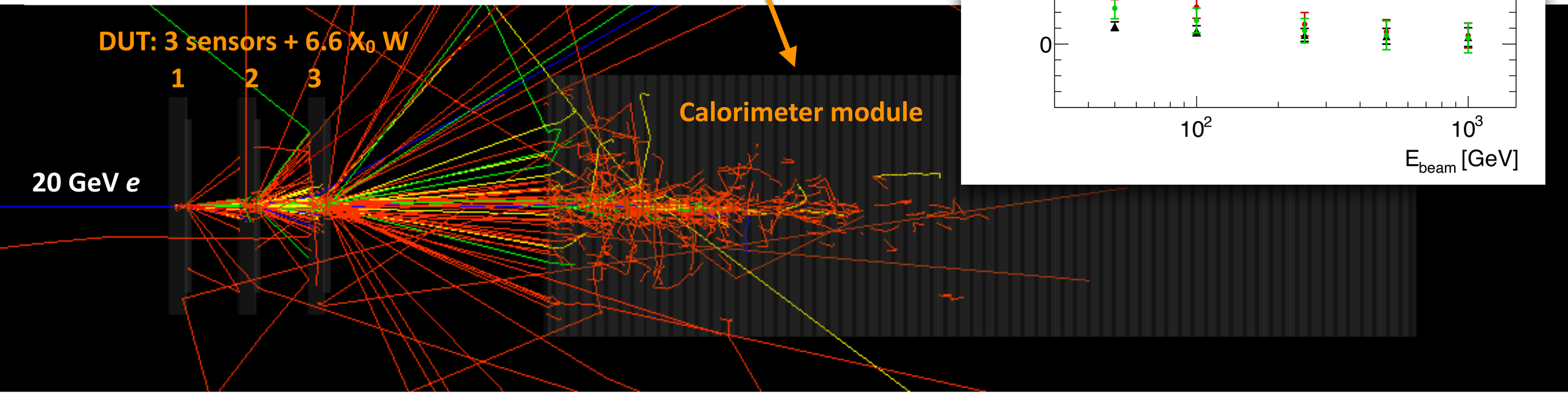
After calibration

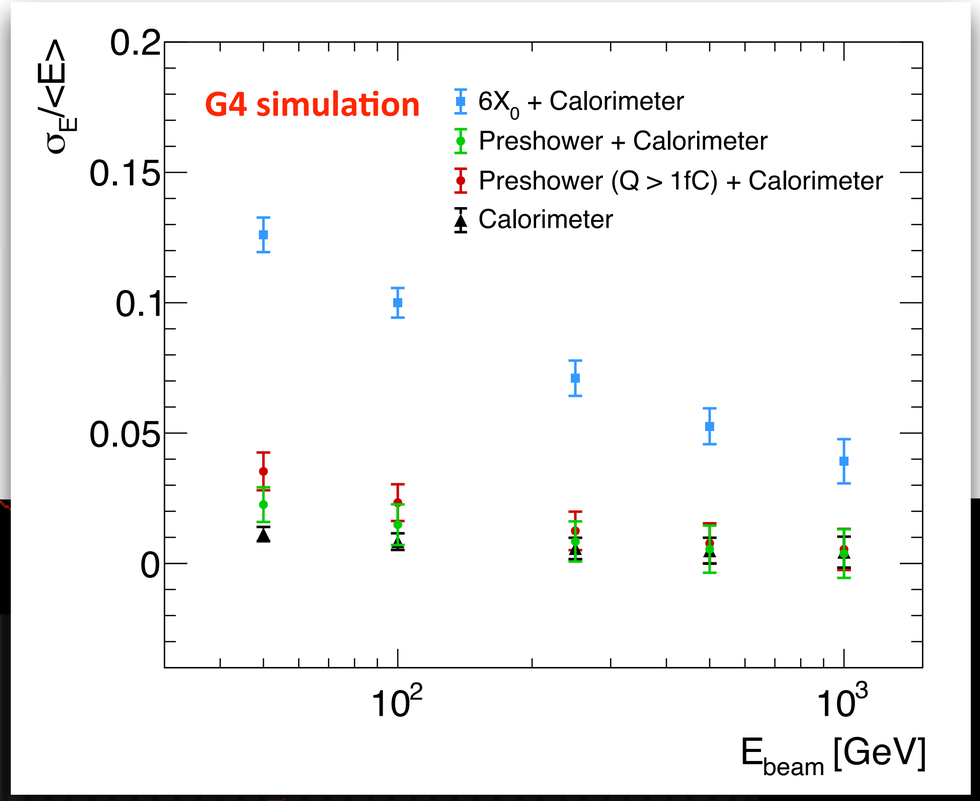


Color map ⇒ ADC response: [0-15] before calibration, [0fC-65fC] after calibration

September 2022: CERN SPS Test Beam (20-150 GeV e^-)







Summary & Outlook

A new preshower detector is being developed for the FASER experiment at the LHC

- ⇒ enabling discrimination of ultra-collimated multi-TeV diphoton events from LLP decays
- ⇒ chosen technology: SiGe MAPS designed and developed at UniGe
- ⇒ targeting installation in 2024, for data taking during LHC Run 3

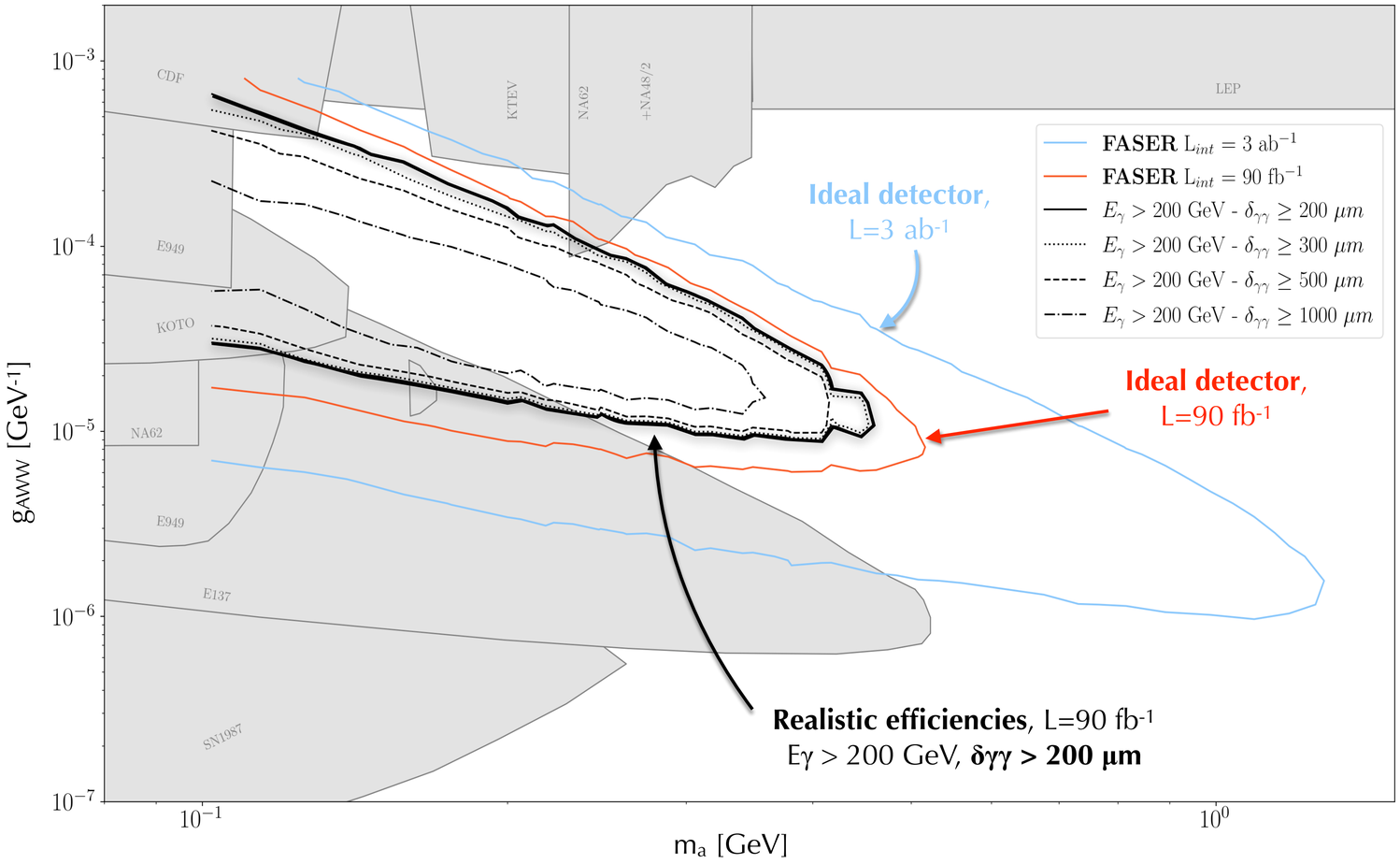
Pre-production chips received in June 2022, tests ongoing

- ⇒ I-V characteristics OK up to 200 V, charge measurement and readout also OK
- ⇒ possible improvements (e.g. TOT mismatch) individuated and planned
- ⇒ further tests on single chips and first assembled modules currently ongoing

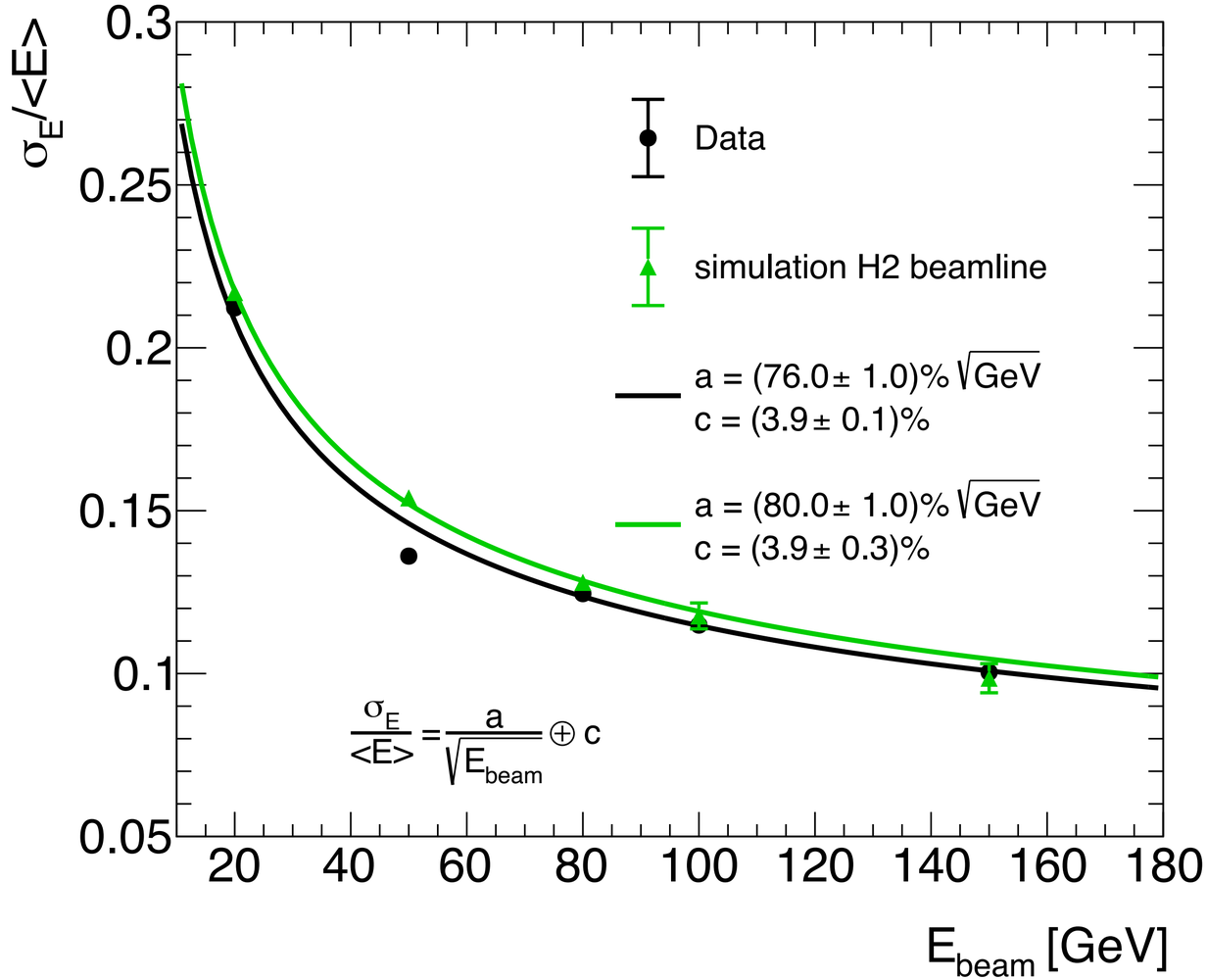
Submission of final chip design in May 2023

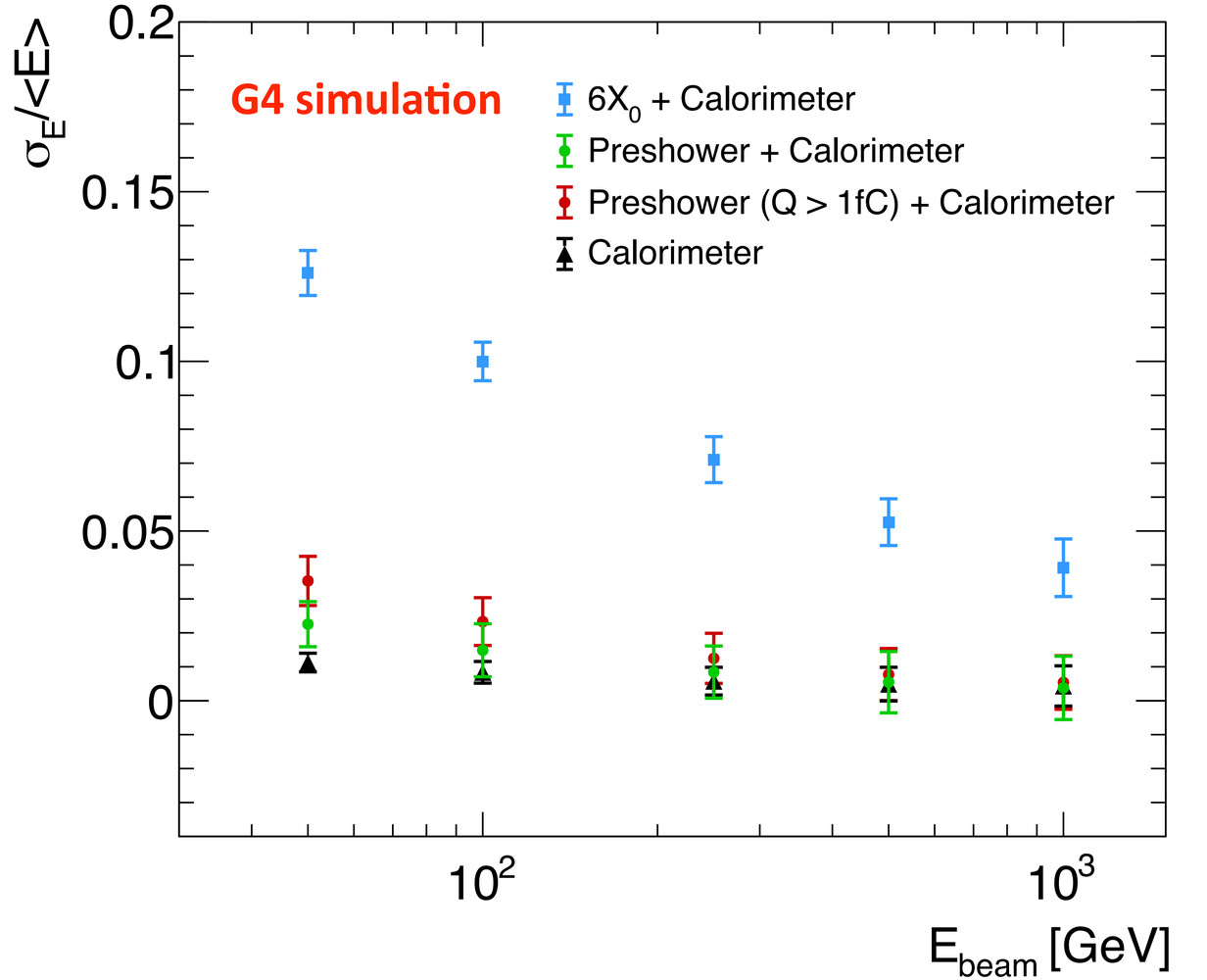
Spares

The development and construction of the W-Si pre-shower of the FASER experiment was funded by the **Swiss National Science Foundation (SNSF)** under the **FLARE grant 20FL21-201474** at the University of Geneva. Additional financial contributions from **KEK**, **Kyushu University**, **Mainz University**, **Tsinghua University** and the **Heising-Simons Foundation** are also acknowledged.



CERN SPS Test Beam: Simulation Vs Data



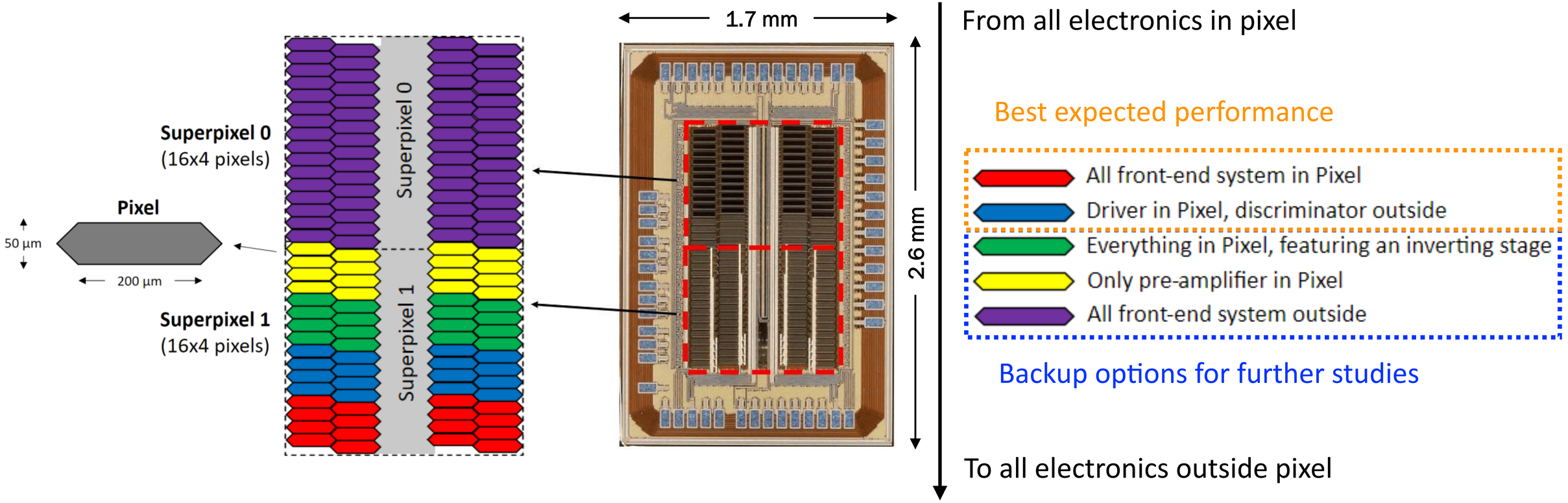


Small Prototype Chip (2021)

First chip prototype tested in 2021

F. Martinelli et al.
2021 *J. Inst.* **16** P12038
https://doi.org/10.1088/1748-0221/16/12/P12038

- designed to study different levels of integration of front-end electronics
- simultaneous goals: minimize dead area and routing capacitance, maximize stability



Small Prototype Chip (2021)

First chip prototype tested in 2021

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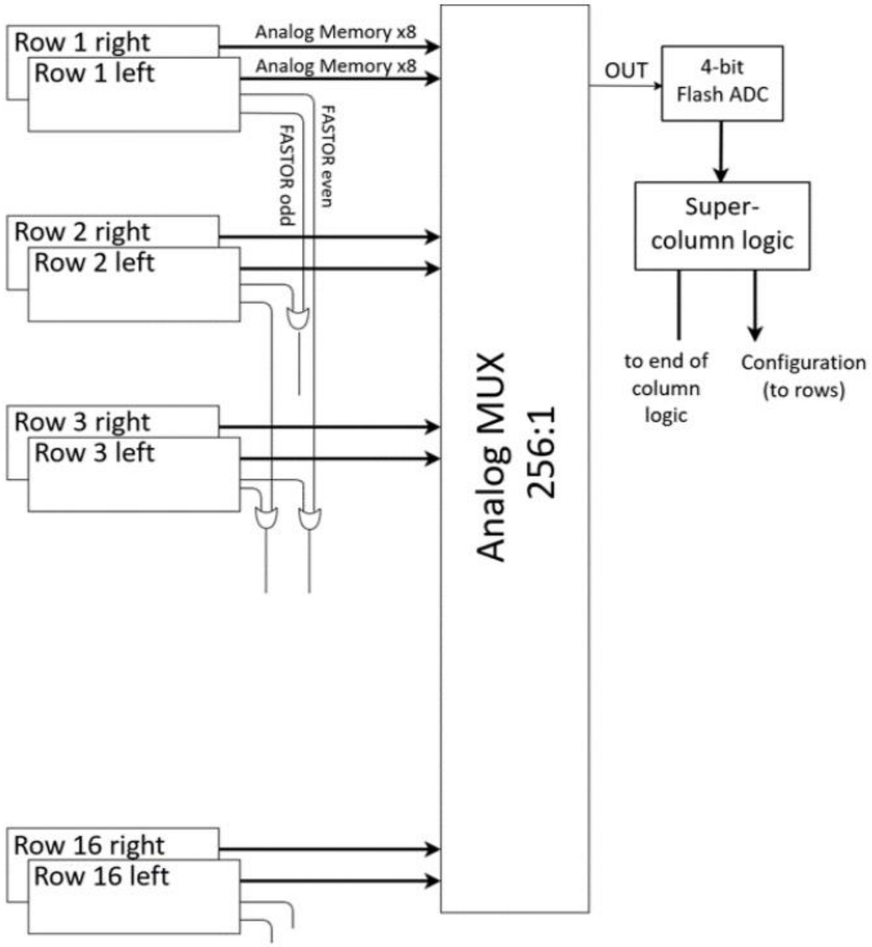
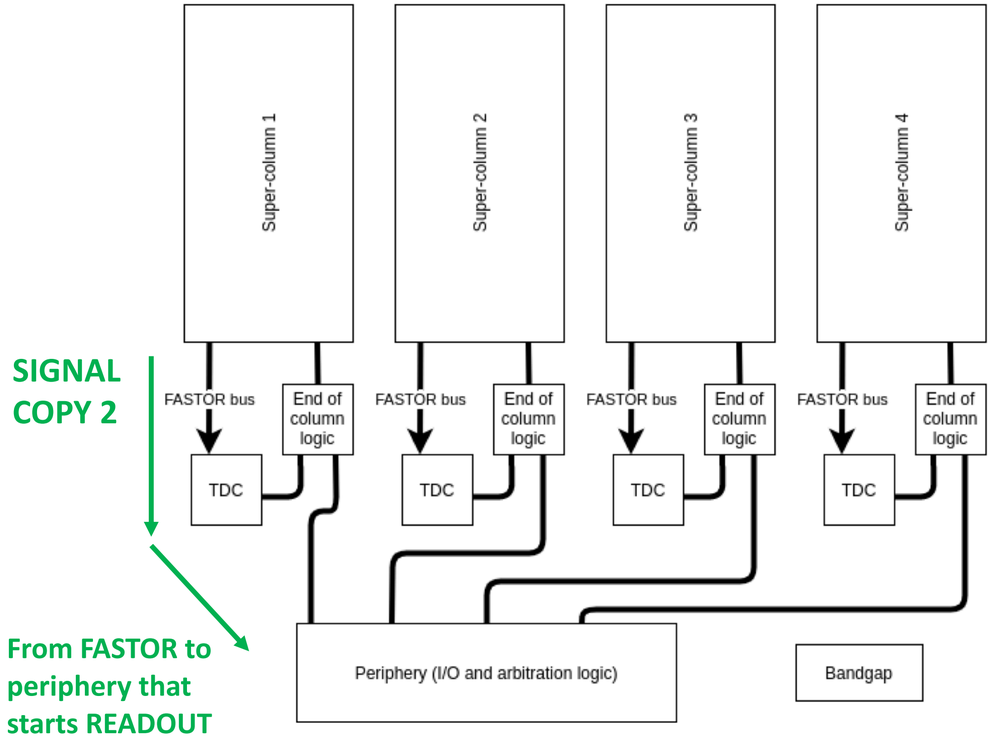
- ⇒ designed to study different levels of integration of front-end electronics
- ⇒ simultaneous goals: minimize dead area and routing capacitance, maximize stability

Configuration	σ_v [mV]	G_c [mV/fC]	ENC [e$^-$]	$\sigma_{V_{th}}$ [mV]
All f.e. outside pixel	4.2 ± 0.2	159 ± 1.0	165 ± 9	32.3
Only pre-amp. in pixel	2.5 ± 0.1	96.8 ± 0.5	161 ± 9	26.9
All f.e. in pixel, inv. stage	6.9 ± 0.5	179 ± 1.0	241 ± 19	30.8
Pre-amp. and driver in pixel	3.8 ± 0.2	133.7 ± 0.6	178 ± 9	23.4
All f.e. in pixel	5.4 ± 0.4	148 ± 1.0	228 ± 20	27.1

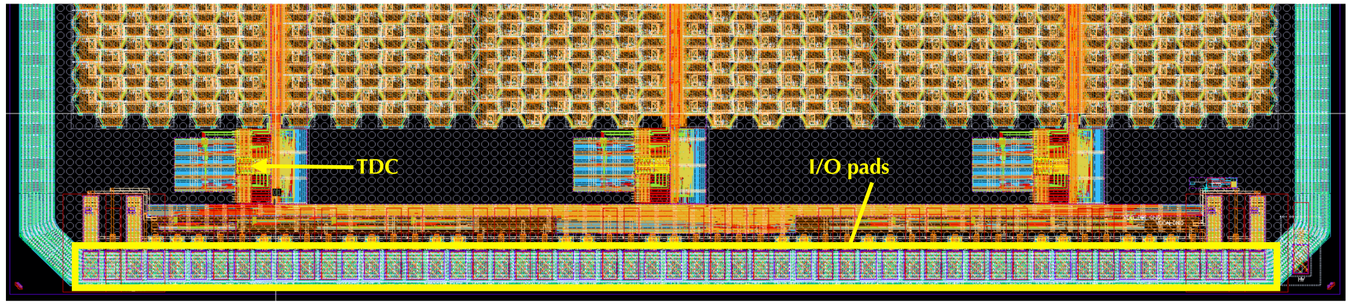
Last two configurations are good compromise between *compactness* and *performance*:
adopted for pre-production prototype

Monolithic Pixel ASIC: Charge Digitization & Readout





Periphery of matrix with three super-columns (from pre-production ASIC)



Pre-production Chip: I-V Characteristic [II]

Probed several chips from different wafers, at room temperature (22 °C)

- ⇒ good I-V characteristics, similar results for standard and EPI wafers
- ⇒ two chips going to early breakdown, under investigation (scratched by probe needle…)