Serial powering for the CMS Inner Tracker detector at High Luminosity LHC

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on behalf of the CMS Tracker Group

TREDI: 18th Trento Workshop on Advanced Silicon Radiation Detectors
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Trento - Italy

Outline

- Short introduction of HL-LHC
- Pills of Serial Powering in CMS Inner Tracker
- Laboratory tests on Serial Powering

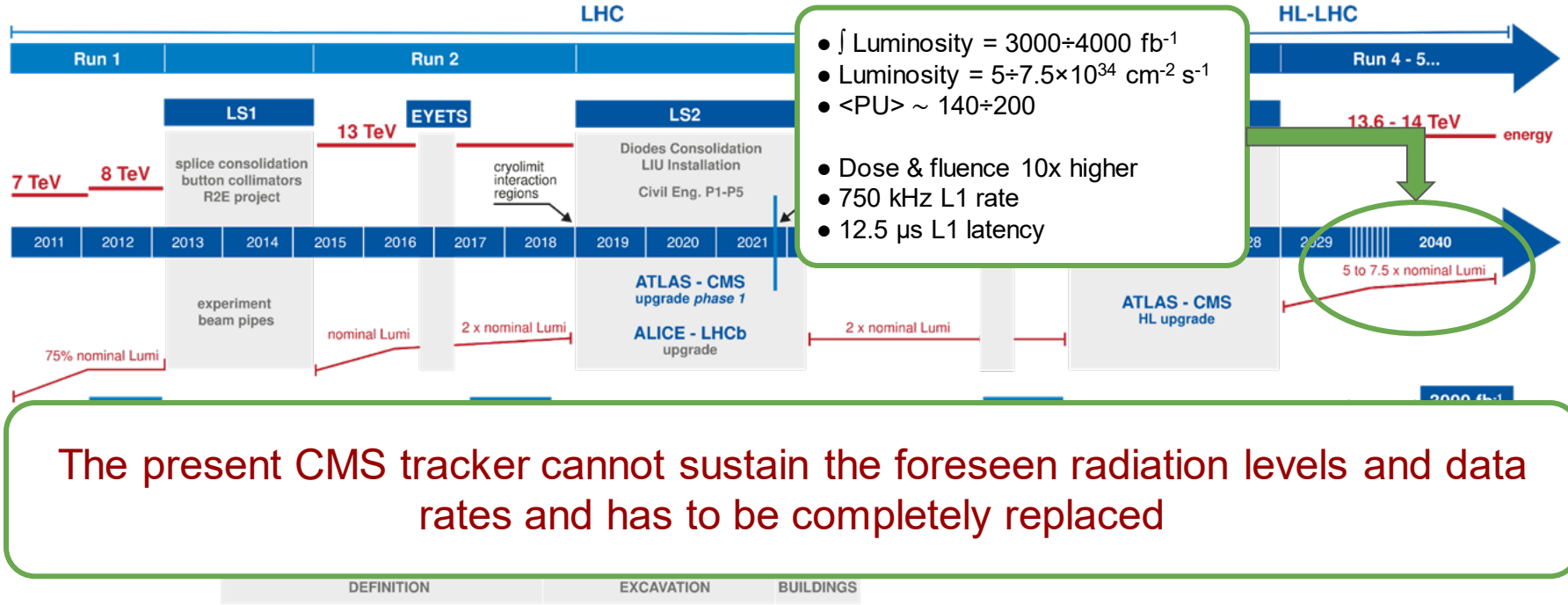
Report on planar sensor studies in talk
"First test beam results of HPK planar pixel sensors with the CROC readout chip for the CMS Phase 2 Upgrade"
Massimiliano Antonello - 28/02 at 14:25 (link)

Report on plan quad module and 3D spatial resolution studies in talk
"Test beam results of planar pixel quad modules and spatial resolution of 3D pixels for the phase-2 CMS tracker"
Martina Manoni - 28/02 at 15:05 (link)

Report on 3D sensor studies in talk
"Test Beam Results of 3D pixel sensors for the Phase-2 CMS Tracker with the RD53A and CROC readout chips"
Clara Lasaosa García - 01/03 at 11:10 (link)

CMS Phase-2 tracker @ HL-LHC

LHC / HL-LHC Plan

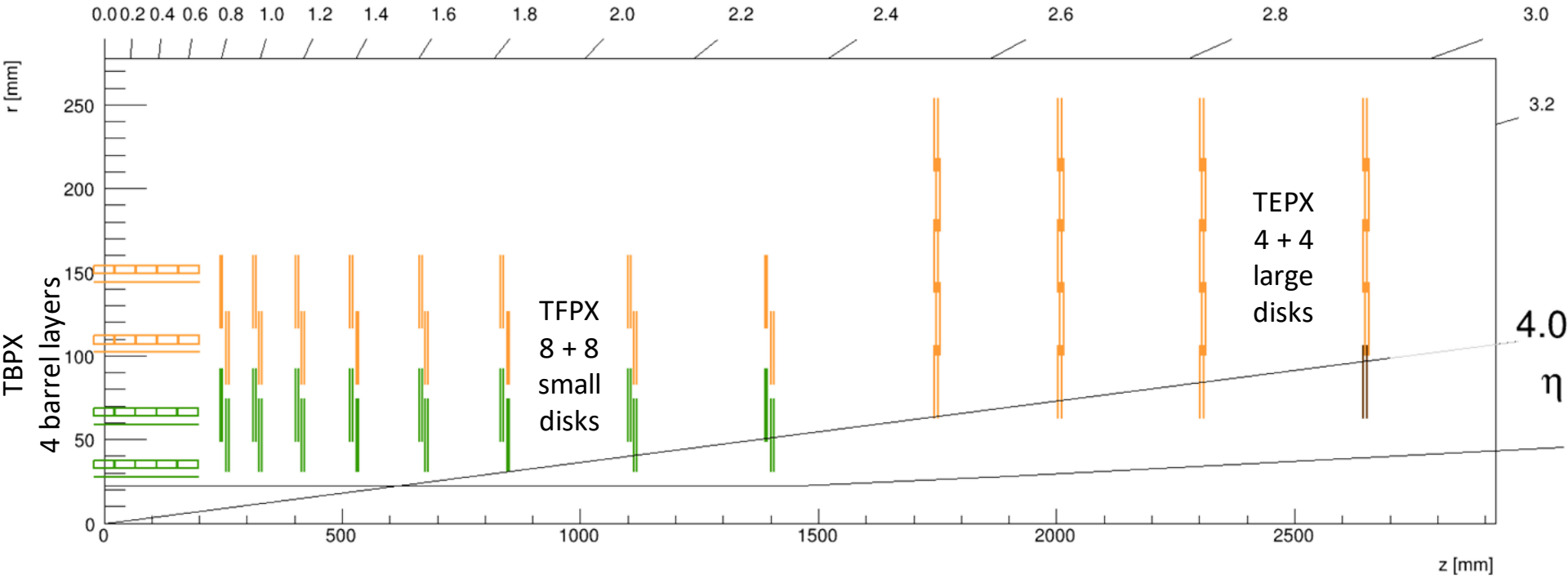


- ∫ Luminosity = 3000÷4000 fb^{-1}
- Luminosity = 5÷7.5×10^{34} cm^{-2} s^{-1}
- <PU> ~ 140÷200

- Dose & fluence 10x higher
- 750 kHz L1 rate
- 12.5 μs L1 latency

The present CMS tracker cannot sustain the foreseen radiation levels and data rates and has to be completely replaced

The CMS Inner Tracker for HL-LHC



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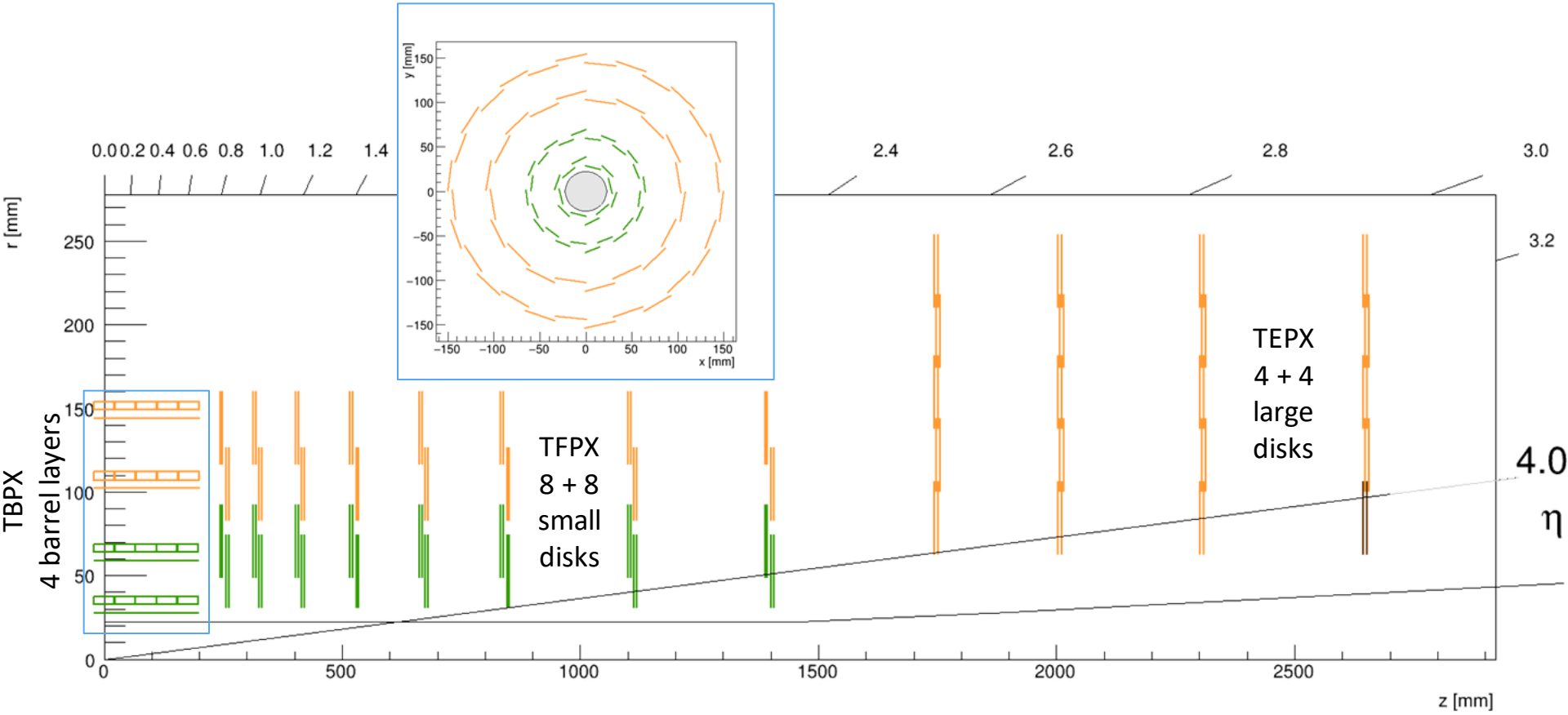

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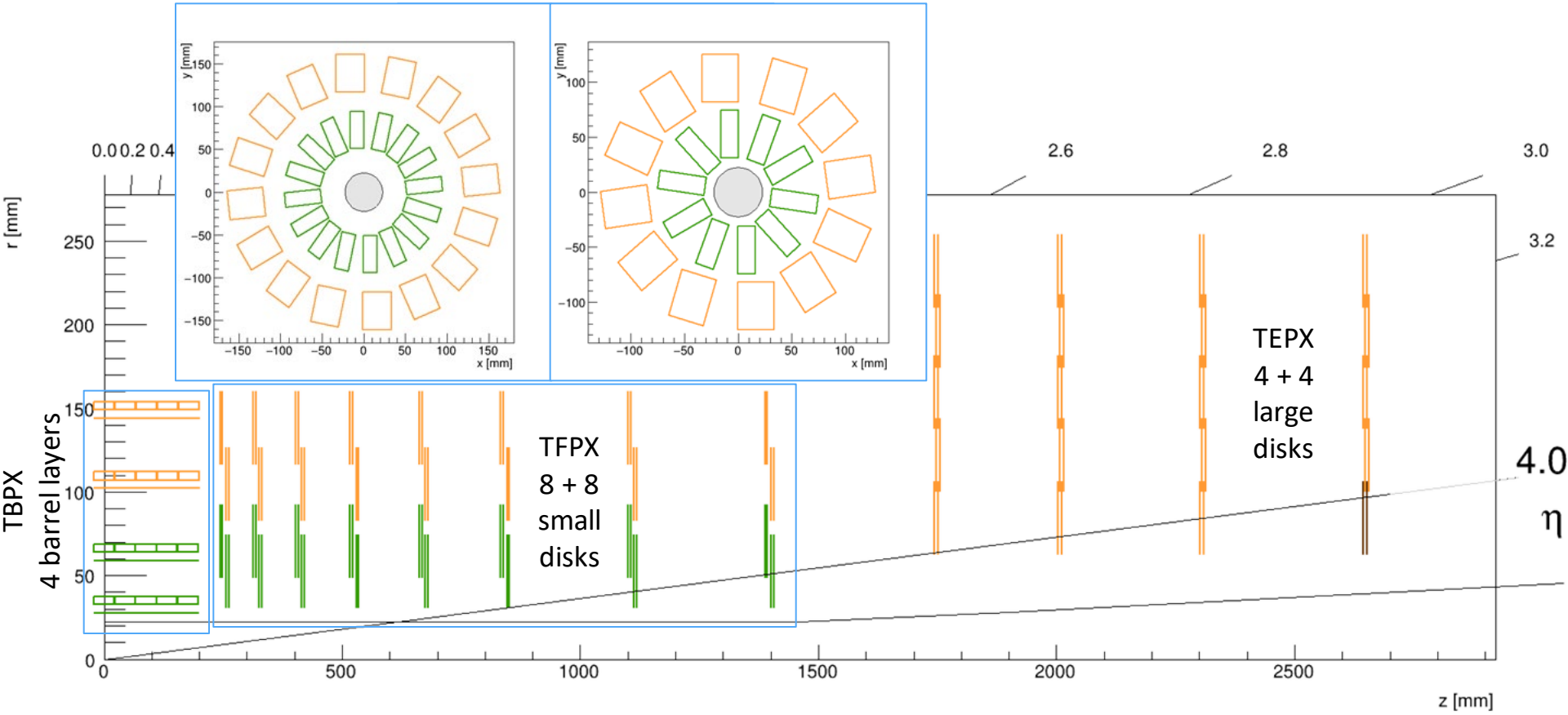

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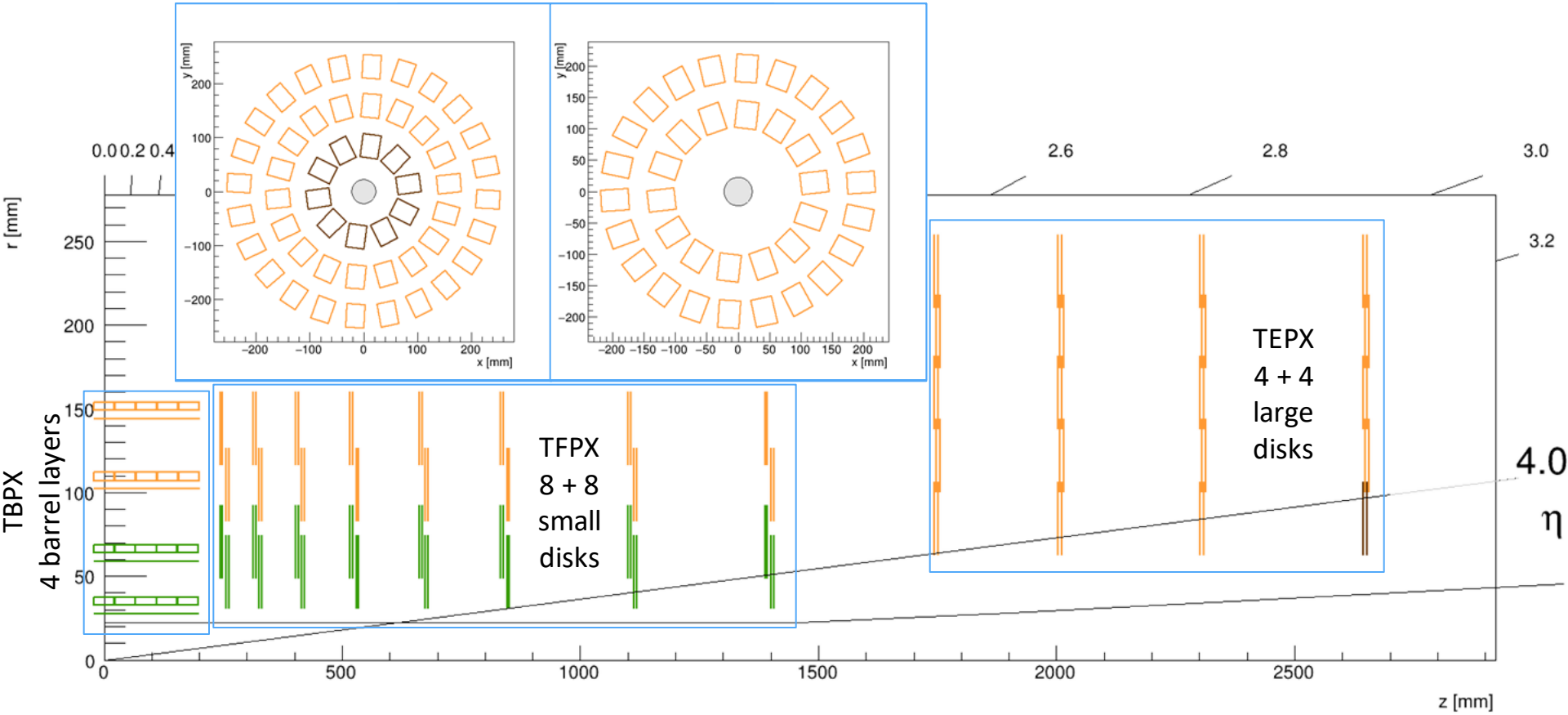
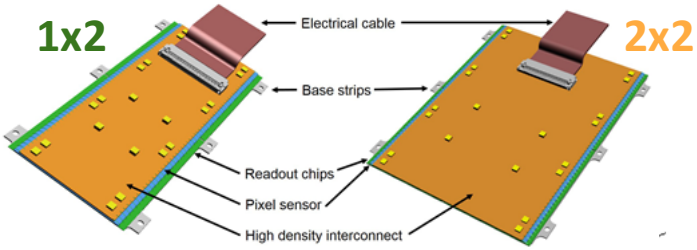


The CMS Inner Tracker for HL-LHC

Electronics main requests and innovations

- **High radiation tolerance:**
  - 2.3×10^{16} n_{eq}/cm^2, fluence
  - 1.2 Grad, TID
- **Improve tracks separation:**
  - High granularity
  - High bandwidth (up to 3.5 GHz/cm^2 occupancy)
  - Low material budget
- **Stringent space constraints**
- Thin n-in-p silicon sensors
- **Innovative power scheme**



- **3900 modules**
- **2×10^9 pixels** (124×10^6 in Phase-1)
- 4.9 m^2
- Hybrid modules with **2 (1×2)** or **4 (2×2)** readout chips
- **1156 modules**, **2736 modules**
- Occupancy < 0.1%
- Simple mechanics:
  - Can be removed for maintenance
  - Barrel splits in half at z ~ 0
  - Disks with planar geometry

Power distribution strategies

- Large area + granularity → large number of channels
- Thin sensors → low signal → low thresholds and low noise analog circuits
- High data bandwidth + long L1 latency → high digital activity

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High power budget

More than 3 times the Phase-1 tracker

- Almost same available total cable cross section
- Keep low material budget
- Delivered at ~ 1 ÷ 1.2 V

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Outer tracker 1

100 kW

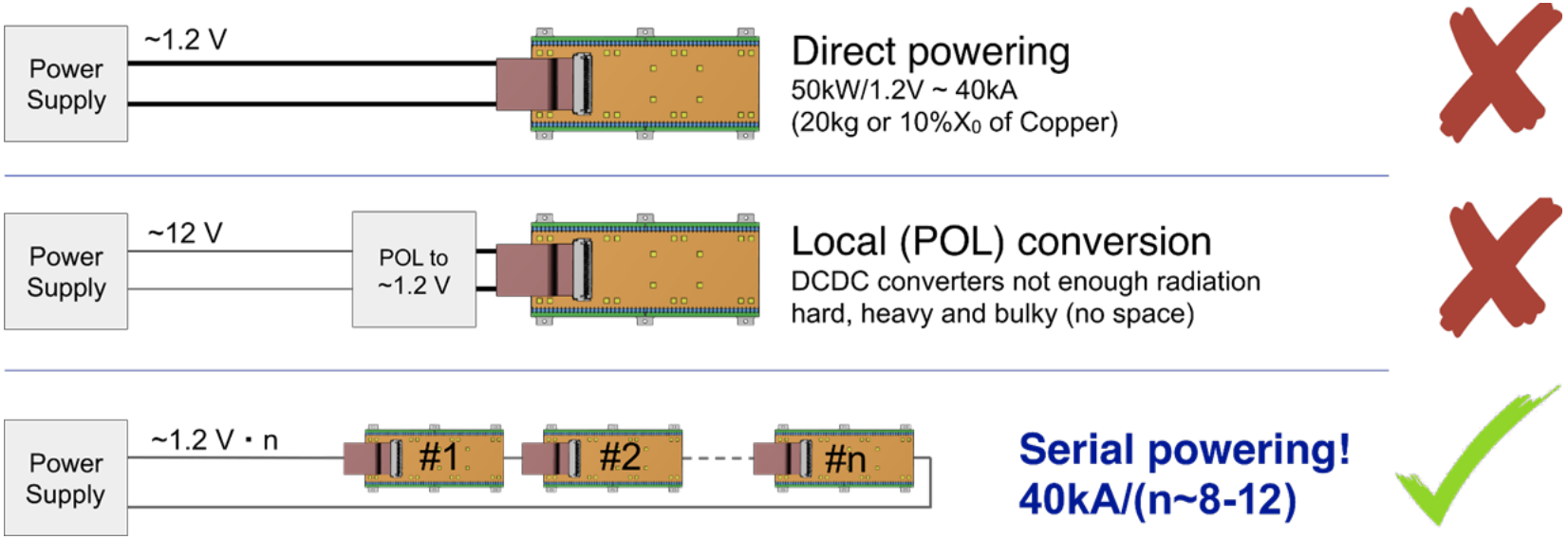
- Parallel powering
- 6 - 11V
- In-situ conversion
- DC/DC converters
  - Radiation hard
  - Work inside magnetic fields

Inner tracker 2

50 kW

- Serial powering
- Up to 12 modules per chain
- Radiation hard
- Magnetic fields
- Regulators integrated on the FE chip

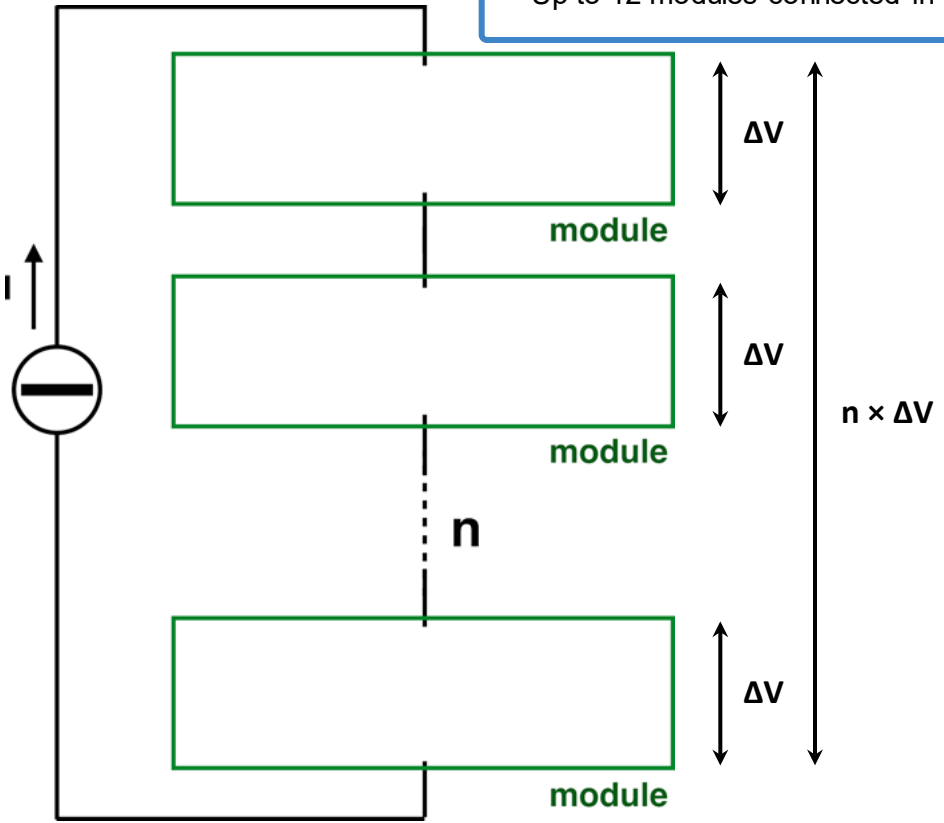
Inner tracker serial powering: why?



- The serial powering is the unique scheme compatible with HL-LHC physics
- It is a major technological challenge since it has never been used on large scale
- All the elements in a chain see the same current (by construction) while the voltage is equally shared if all elements represent the very same and constant load
- This is the task of the ShuntLDO, an IP block of the CMS ROC (CROC) developed by the RD53 Collaboration: no additional ancillary components are needed

Power distribution scheme

Up to 12 modules connected in one serial chain



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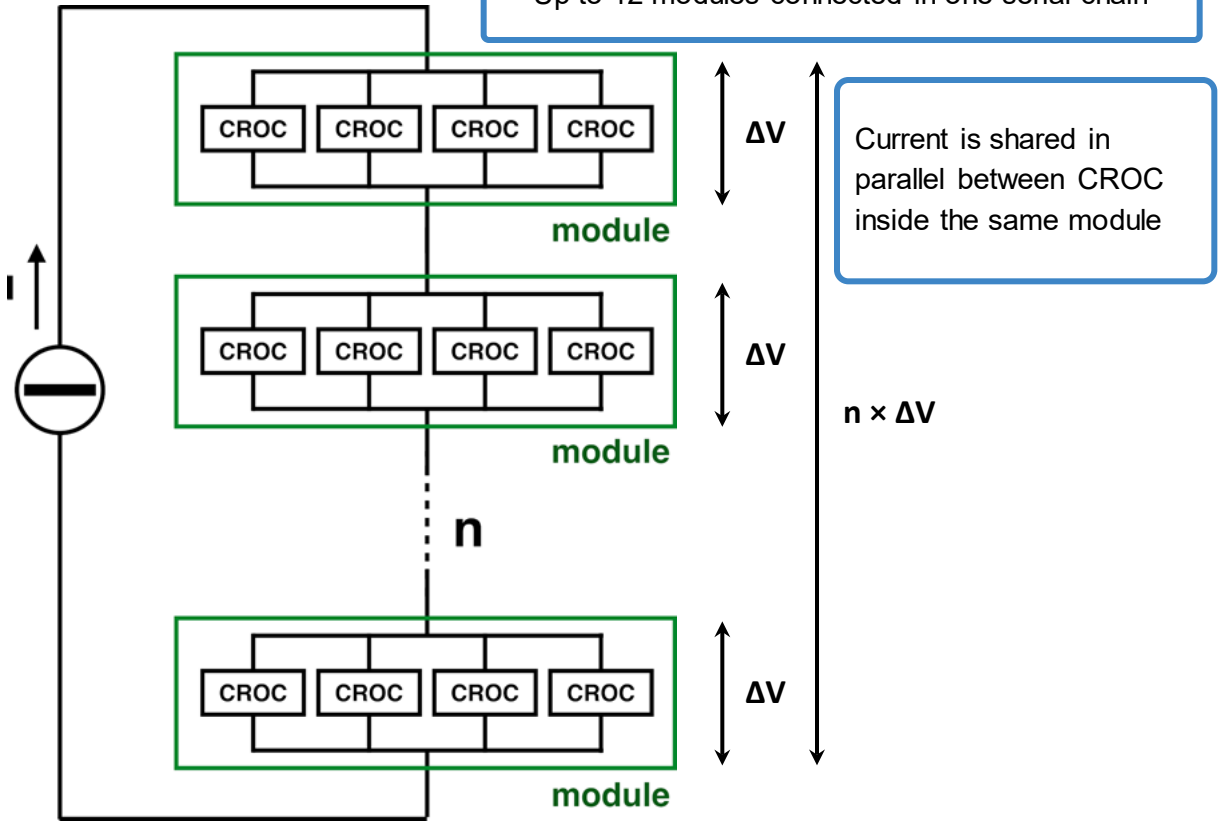

Current is shared in parallel between CROC inside the same module

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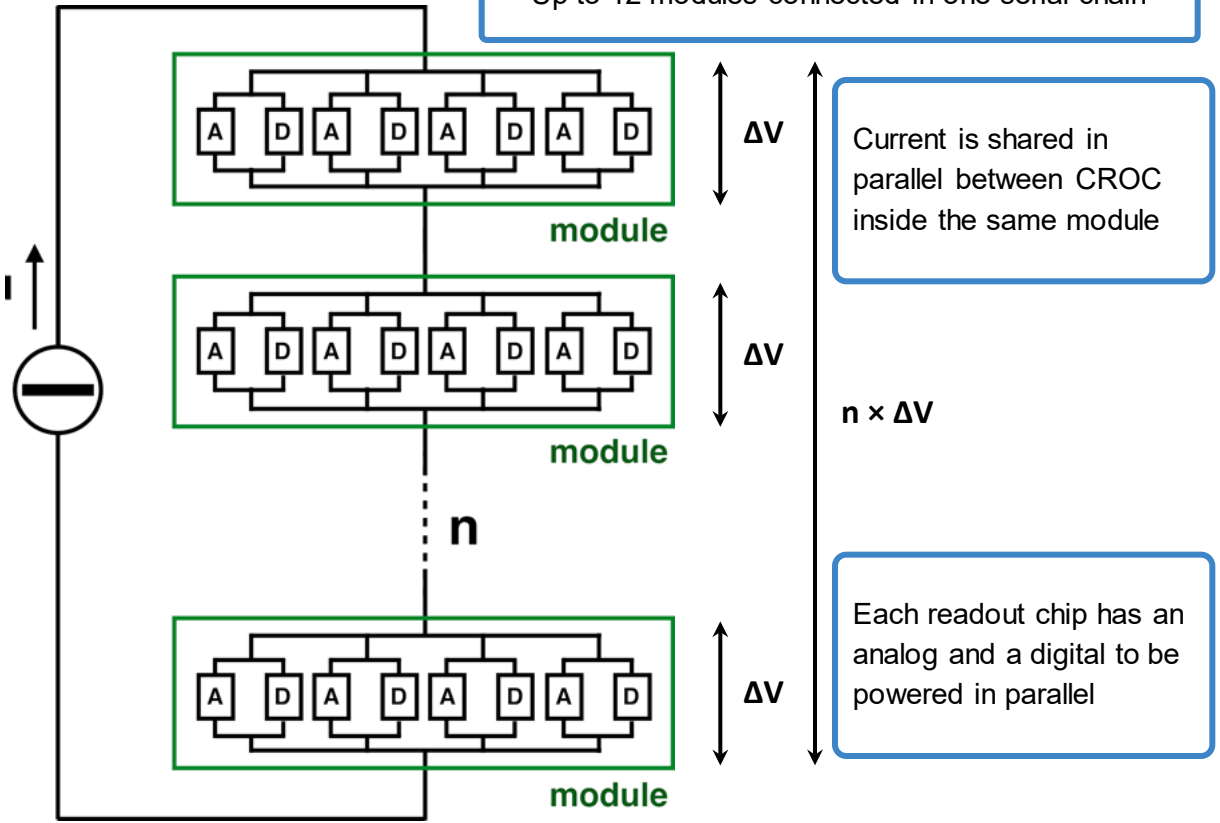

Current is shared in parallel between CROC inside the same module

Each readout chip has an analog and a digital to be powered in parallel

Power distribution scheme

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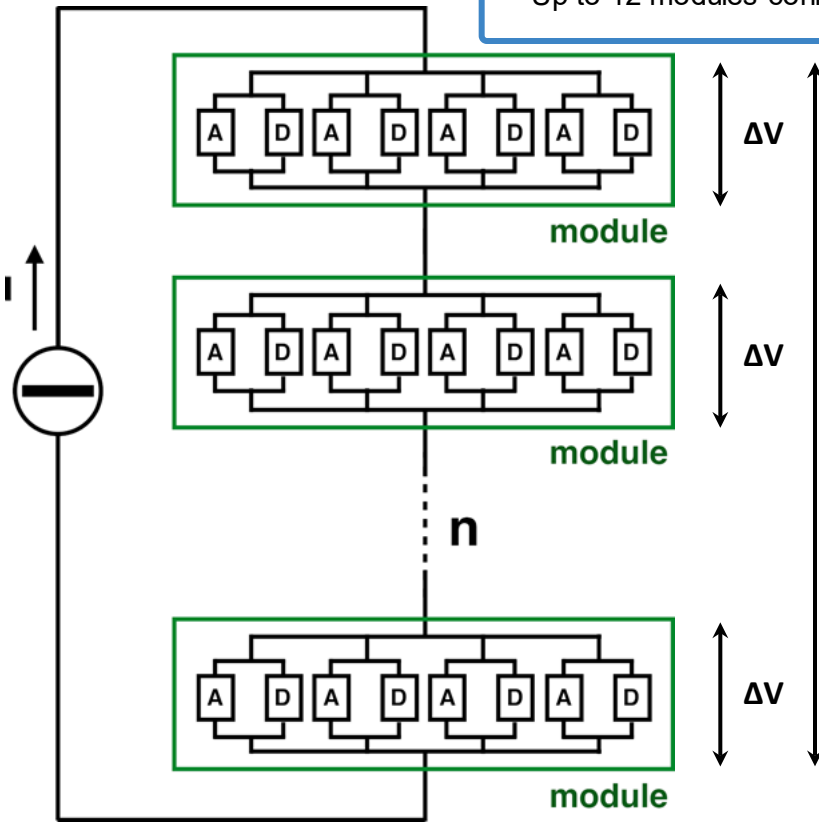

Current is shared in parallel between CROC inside the same module

500 serial chains power the full IT

164 - 4 A chains for 2-chips modules

336 - 8 A chains for 4-chips modules

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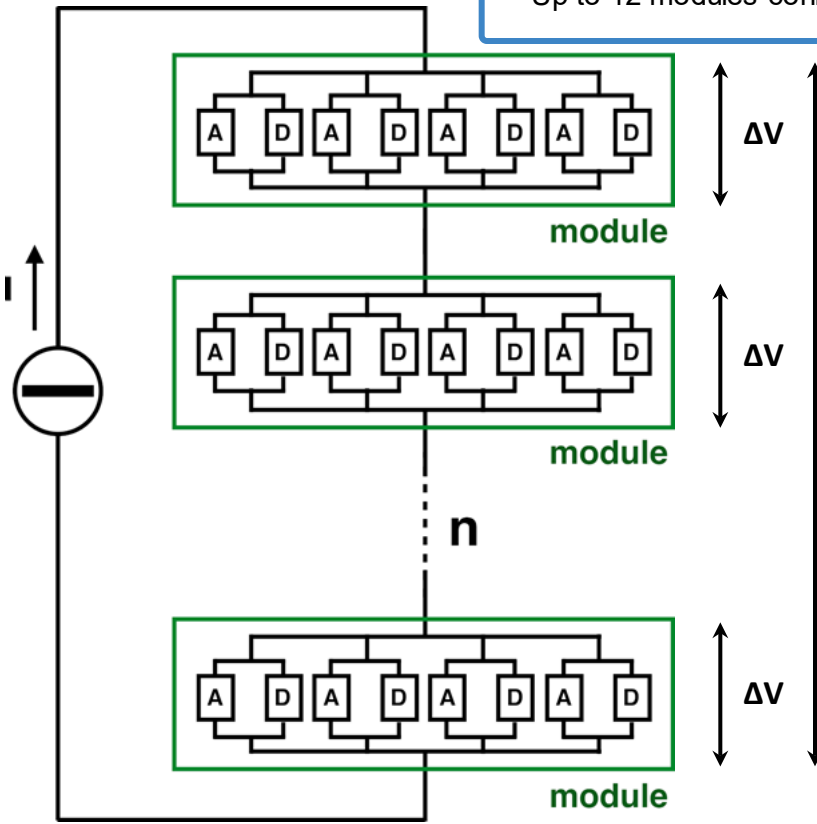

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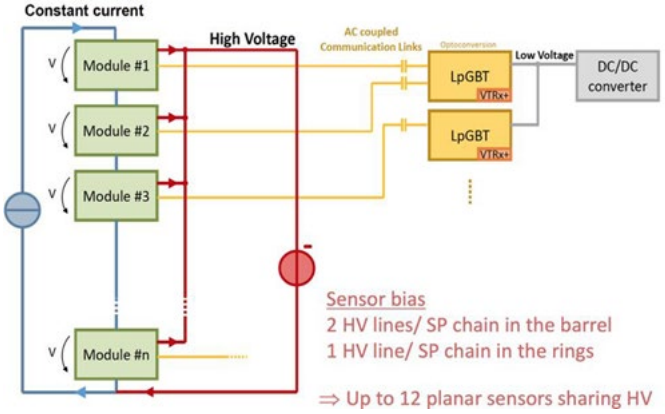

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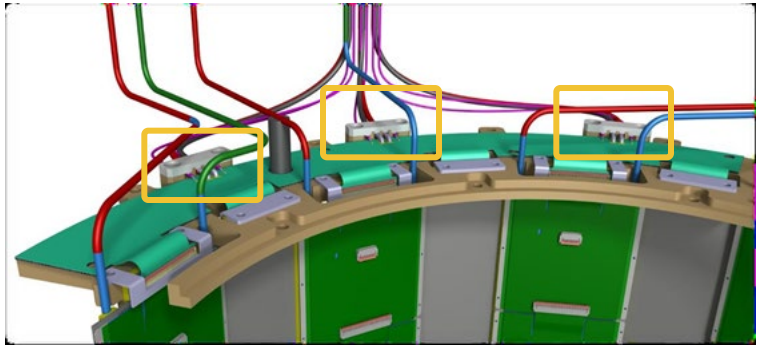
HV distributed in parallel

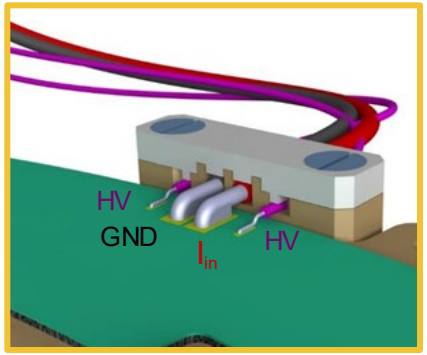
Each readout chip has an analog and a digital to be powered in parallel

Sensor bias following the serial power chains with single return line

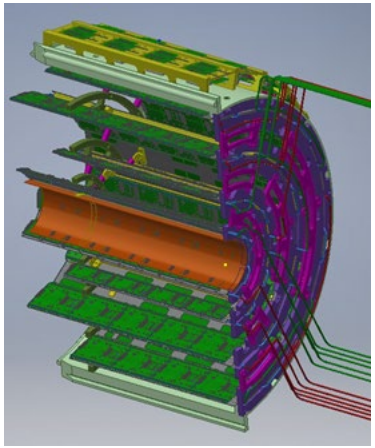
Serial power distribution

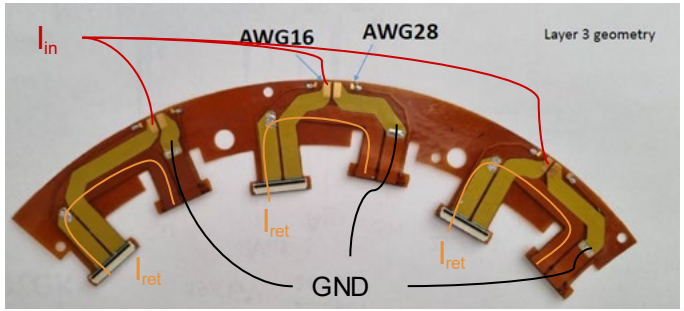
Barrel

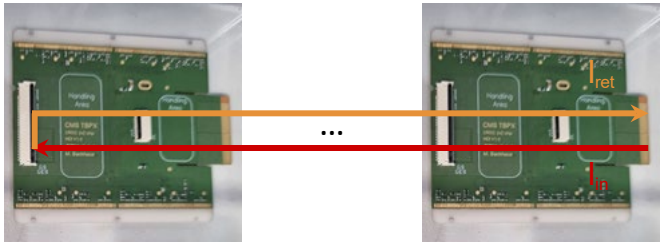


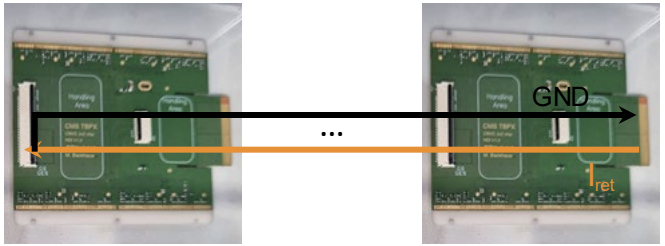


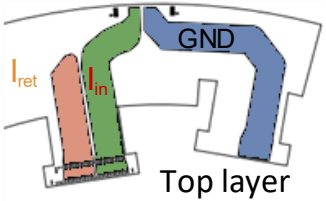
8 modules/chain
or
10 modules/chain

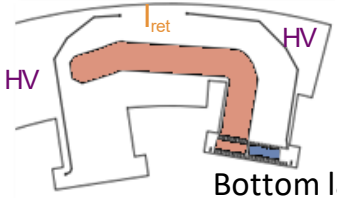






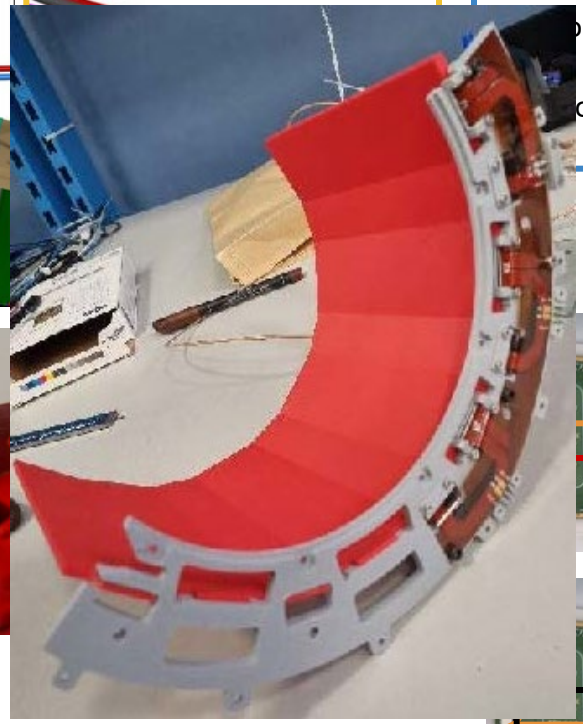


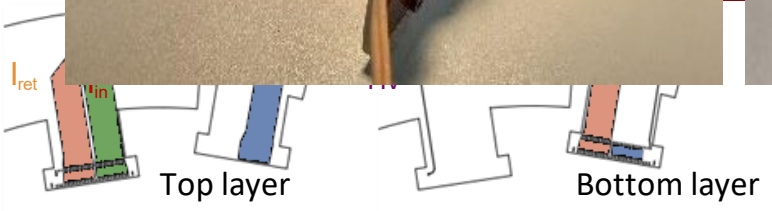




Serial power distribution

Barrel





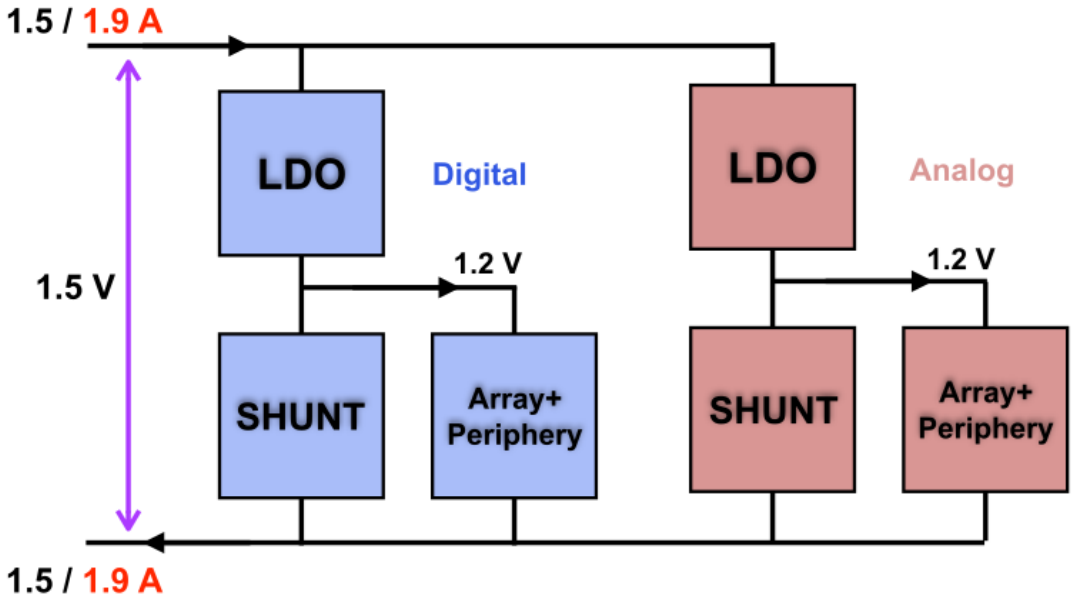
The Shunt-LDO and the serial powering (1)

Serial powering is supported by the readout chip via the Shunt-LDO IP block

- Integrated **on-chip solution**
  - Low mass, radiation hard and no extra ASICs

Shunt-LDO

- **Shunt** functionality needed to implement the serial scheme
- **LDO regulation** needed to ensure the correct voltage to the electronics, i.e. ~ 1.2 V
- Aiming at ΔV ~ 1.5 V (1.2 V + 0.3 V for LDO)



The Shunt-LDO and the serial powering (2)

Serial powering is supported by the readout chip via the Shunt-LDO IP block

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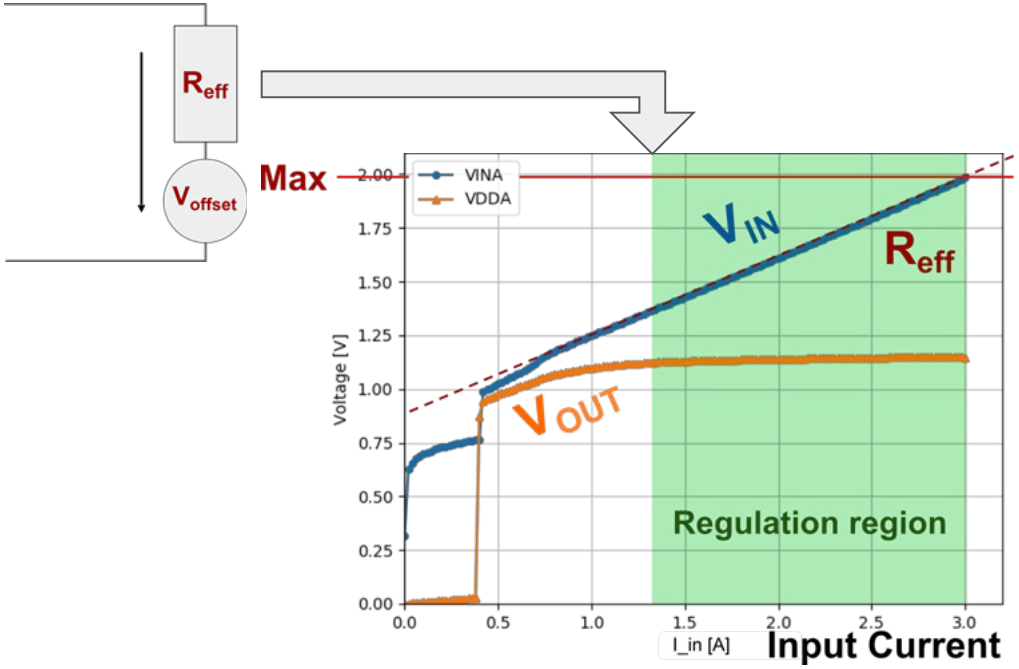
Shunt-LDO

- Equivalent to a resistor in series with a voltage source (**ΔV = f(I)**)
  - Healthy behaviour in **parallel applications**
- Each module has **its own local ground**
  - I/O in AC
  - Not trivial bias distribution to sensors
- The chain has to provide enough power for transients: 20-25% current headroom ⇒ Intrinsically **not efficient**
- A brand-new world of **failure modes**



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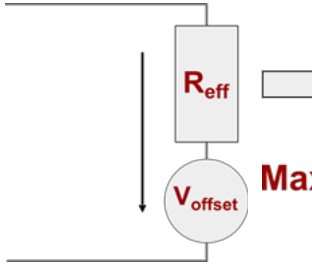
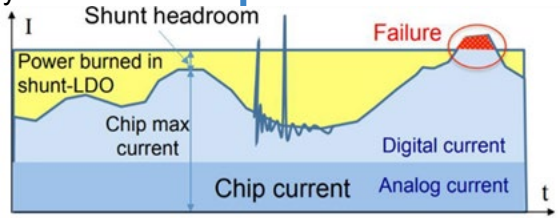
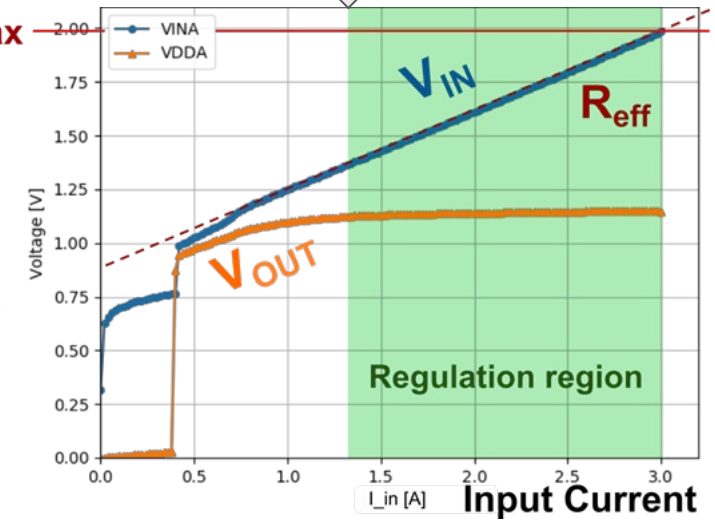


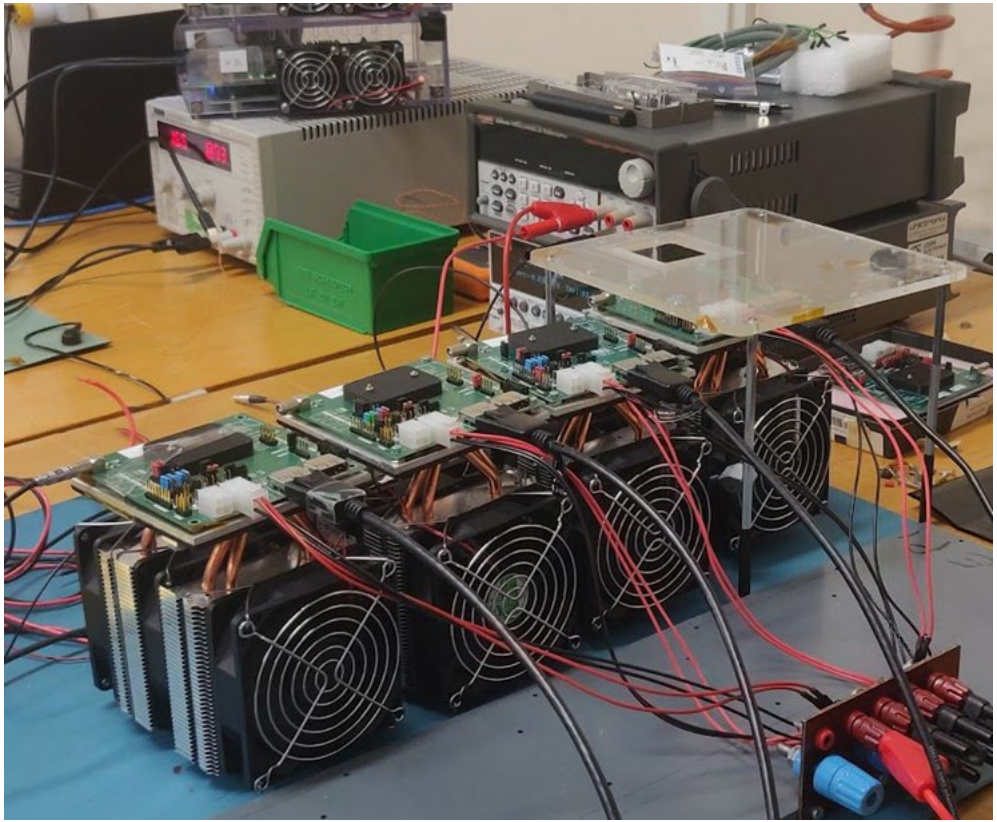




Laboratory tests

Serial power and 3D pixel module

- 4 3D RD53A modules in series
  - Peltier based cooling
- Same 3D module tested at the beginning and at the end of the powering chain
  - Beta source
  - Look for possible different behaviours (cluster size)
- Same bias voltage at HV power supply
  - “Effective” voltage 30V at the beginning of the chain
  - “Effective” voltage 36V at the end of the chain
  - Comparable leakage current in the two positions



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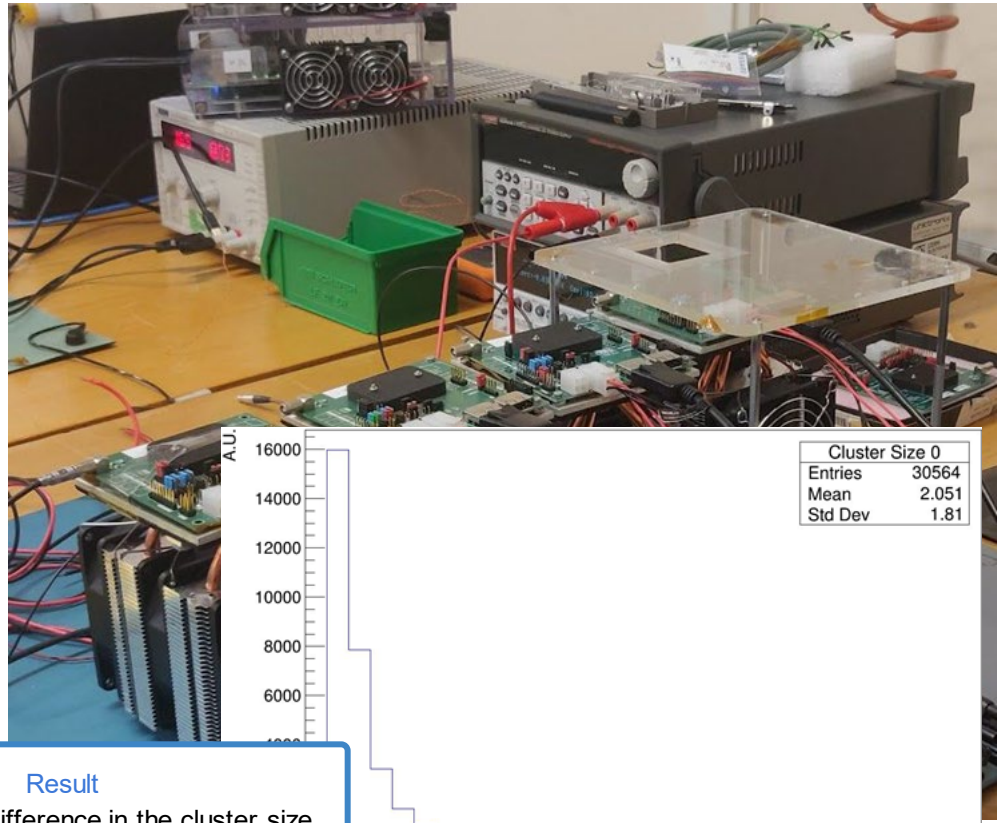

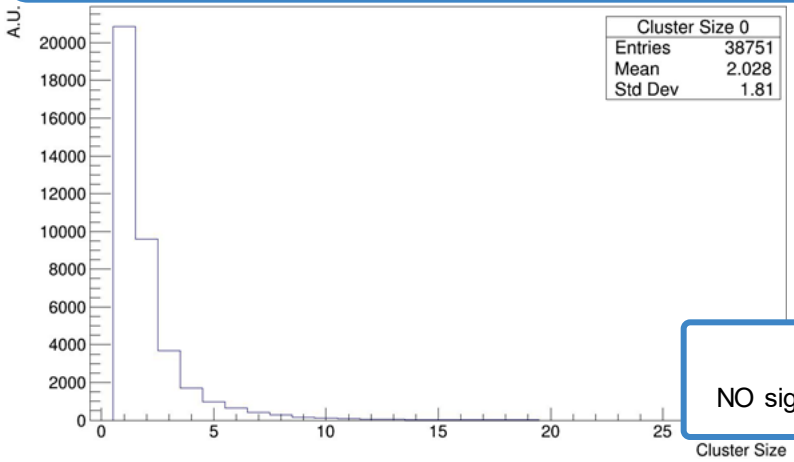

Result

NO significant difference in the cluster size

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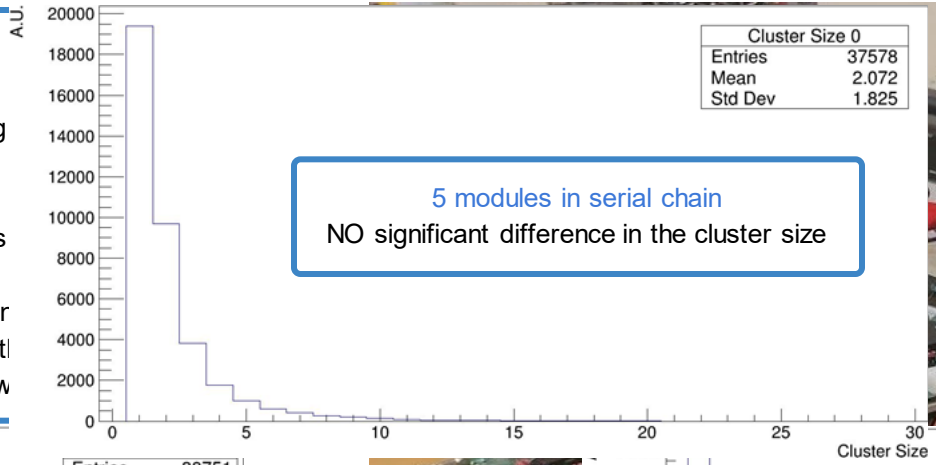
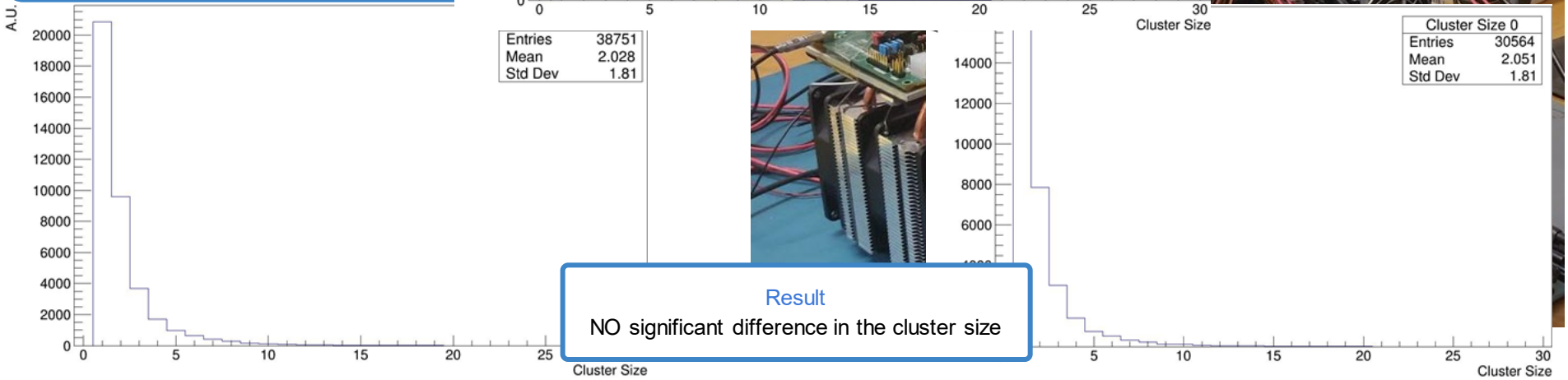


5 modules in serial chain
NO significant difference in the cluster size



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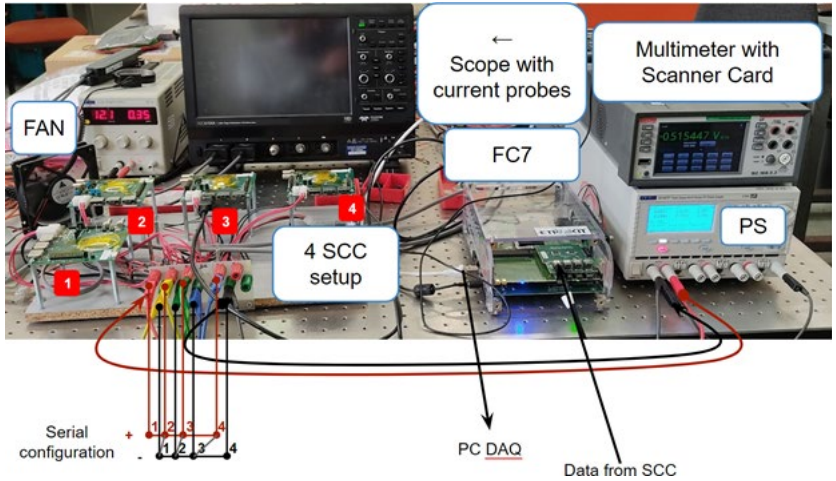
Bare CROC serial powering tests



- 4 CMS ROC (CROC) Single Chip Card
  - FAN cooling
- Multimeter with scanner card for monitoring
- Multimeter and power supply remotely controlled using a high level C++ library developed for laboratory instruments control
  - Interacts with Ph2_ACF (DAQ software) via a TCP socket

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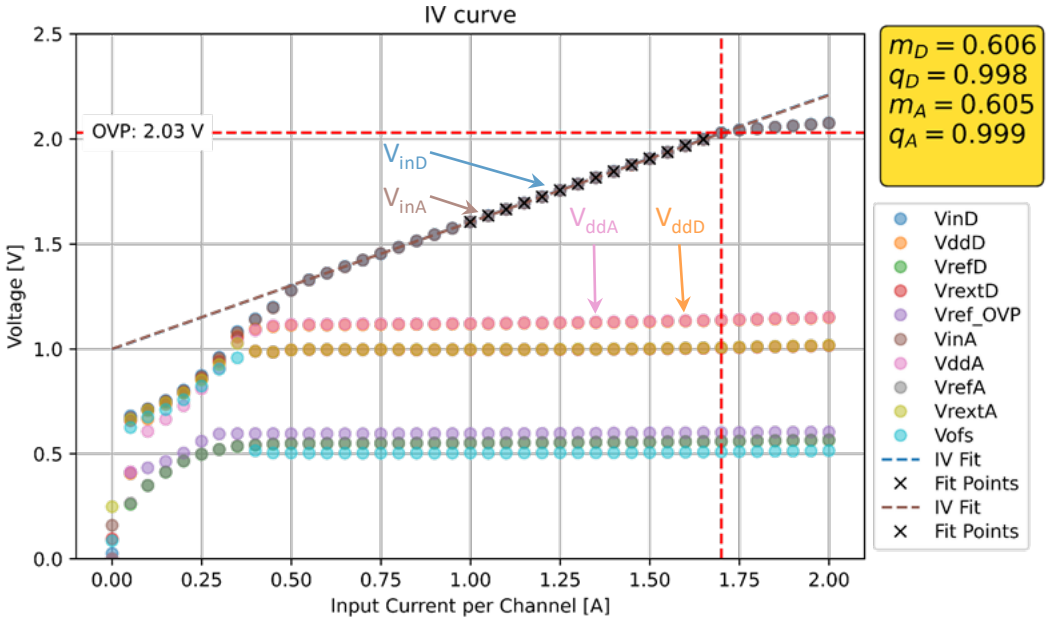

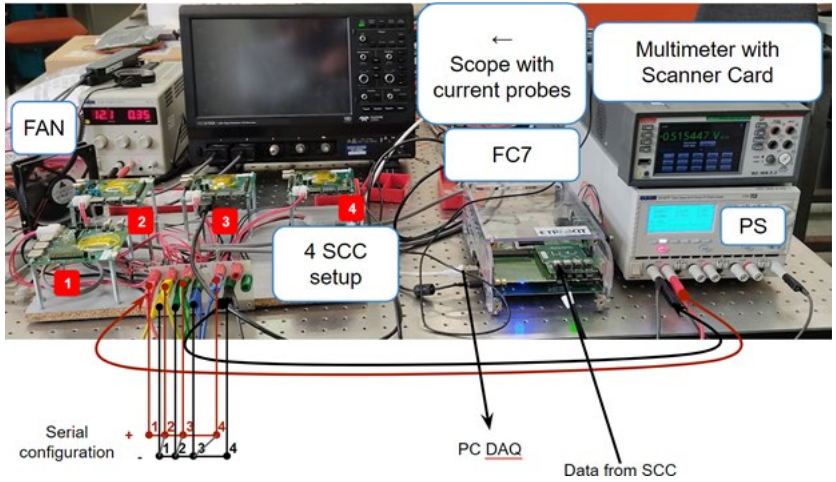

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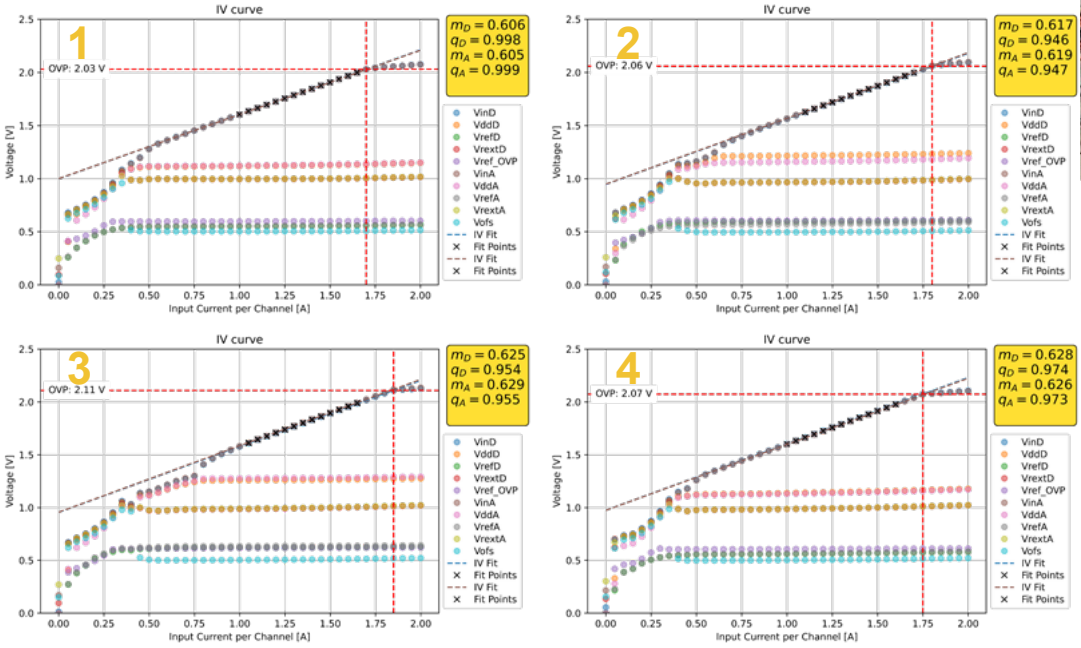

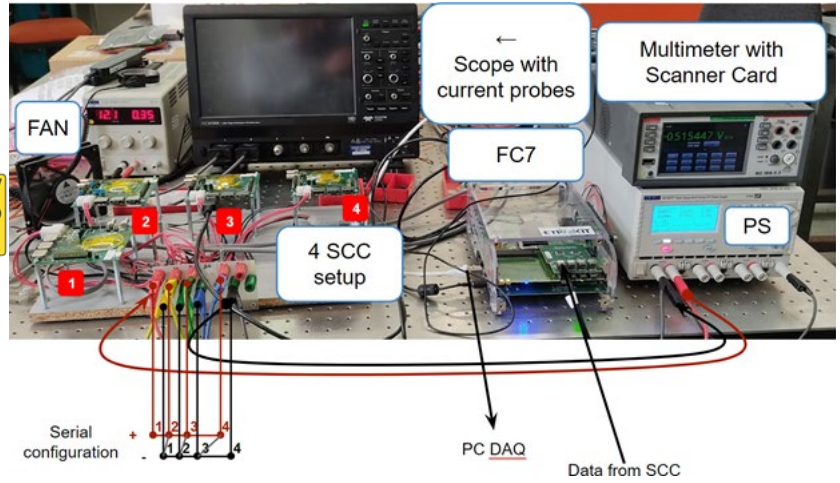

- Overall expected behaviour in the chain
- Same fitted V_{off} (namely $q_{A/D}$) in the same SCC
- Slight different $q_{A/D}$ between SCCs

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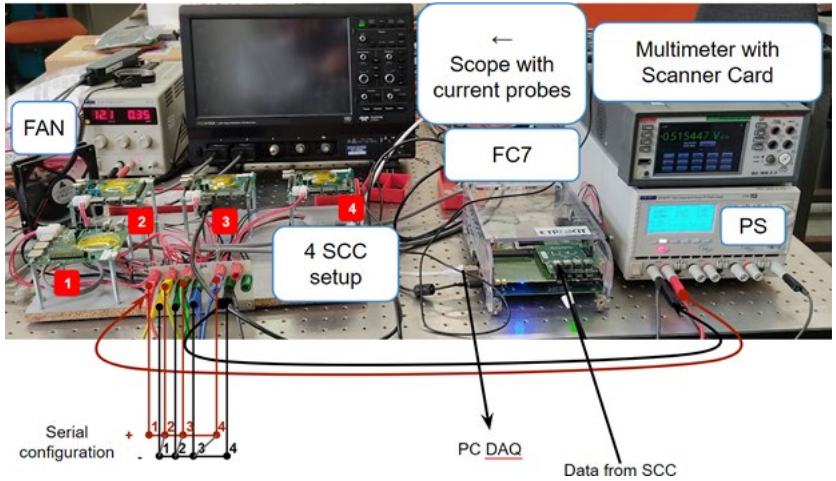

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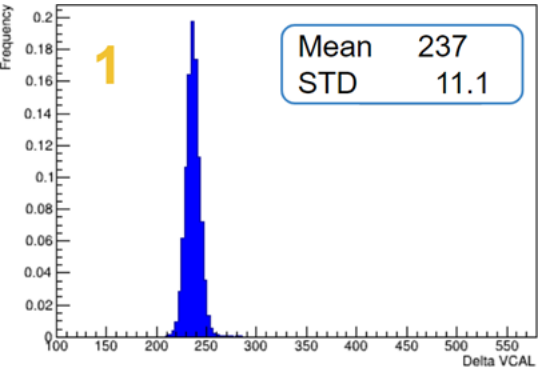
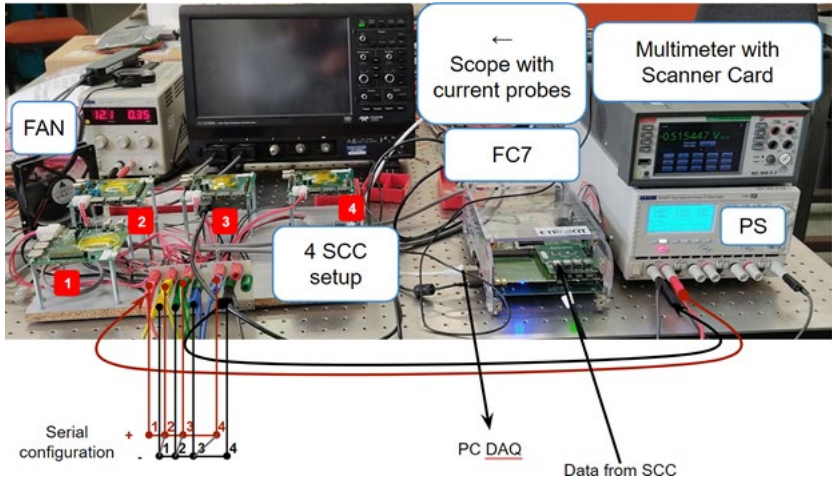
The channels were tuned to an average threshold ~1250e^-

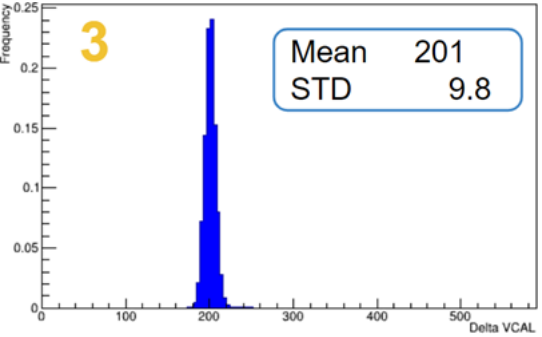
- Threshold distribution in the chain
- Noise distribution in the chain

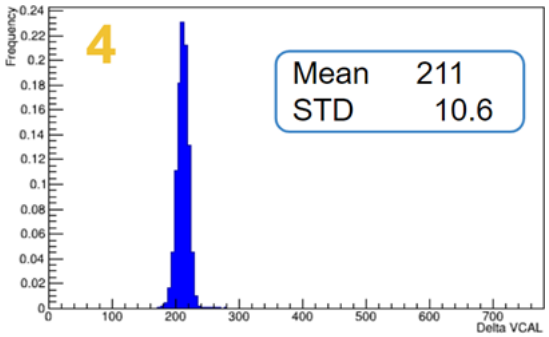
Bare CROC serial powering tests



1 ΔVCal ~ 5 e⁻





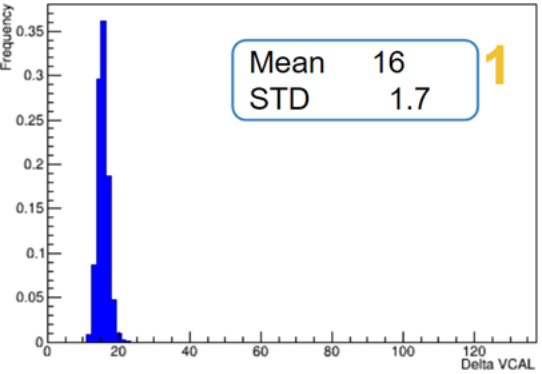


The channels were tuned to an average threshold ~1250e⁻

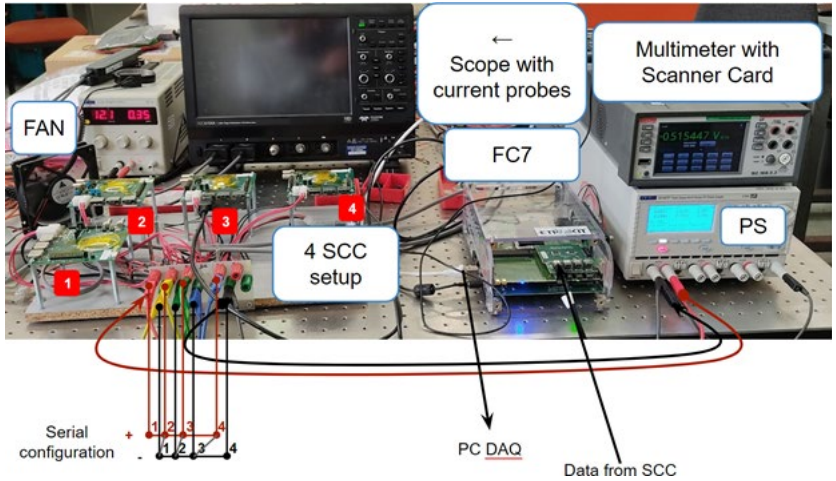
- Threshold distribution in the chain
- Noise distribution in the chain

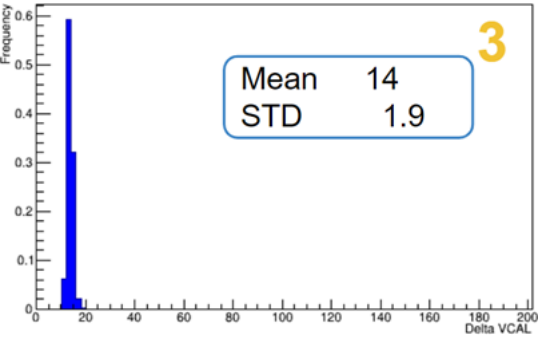
- 4 CMS ROC (CROC) Single Chip Card
  - FAN cooling
- Multimeter with scanner card for monitoring
- Multimeter and power supply remotely controlled using a high level C++ library developed for laboratory instruments control
  - Interacts with Ph2_ACF (DAQ software) via a TCP socket

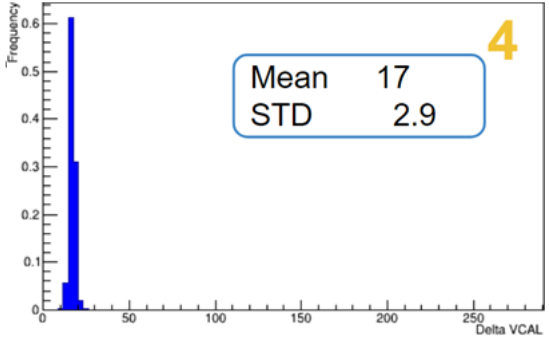
Bare CROC serial powering tests



1 ΔVCal ~ 5 e⁻







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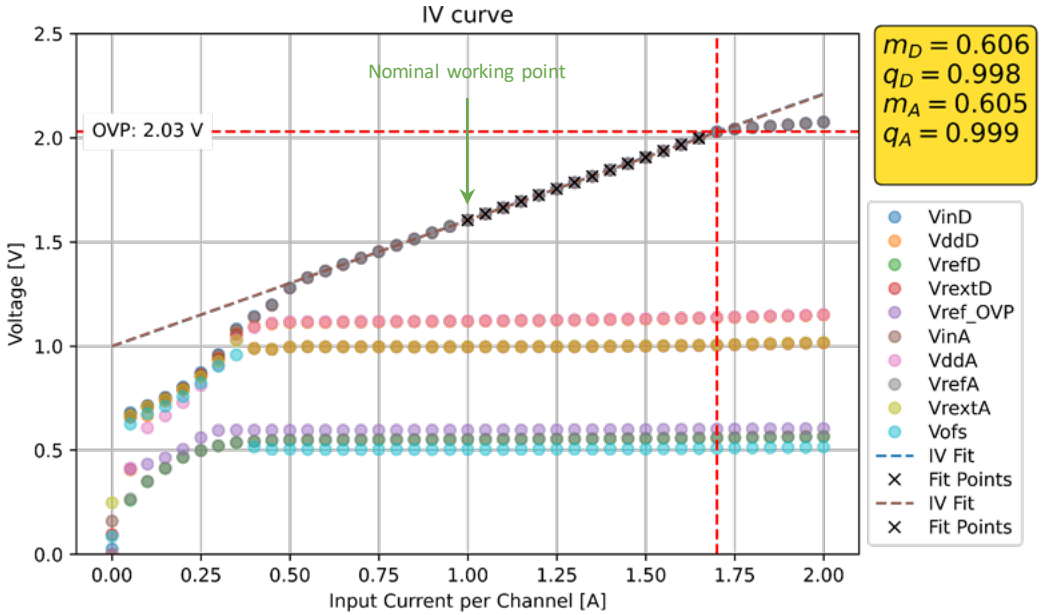
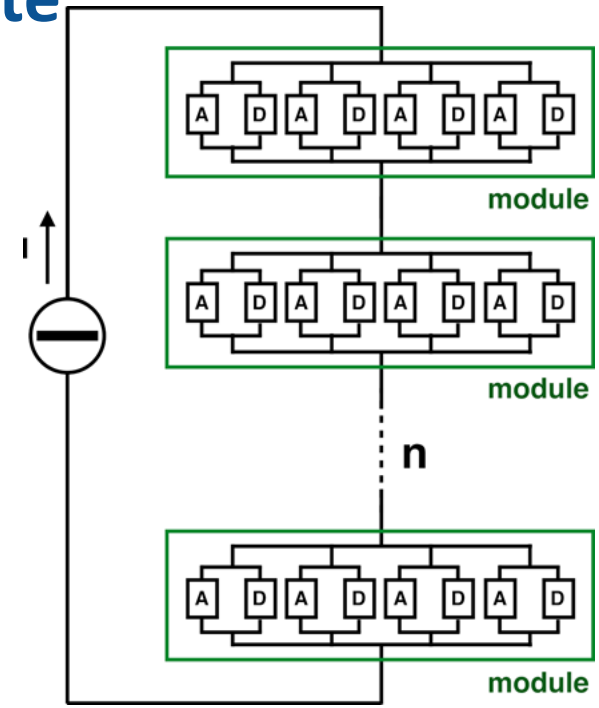
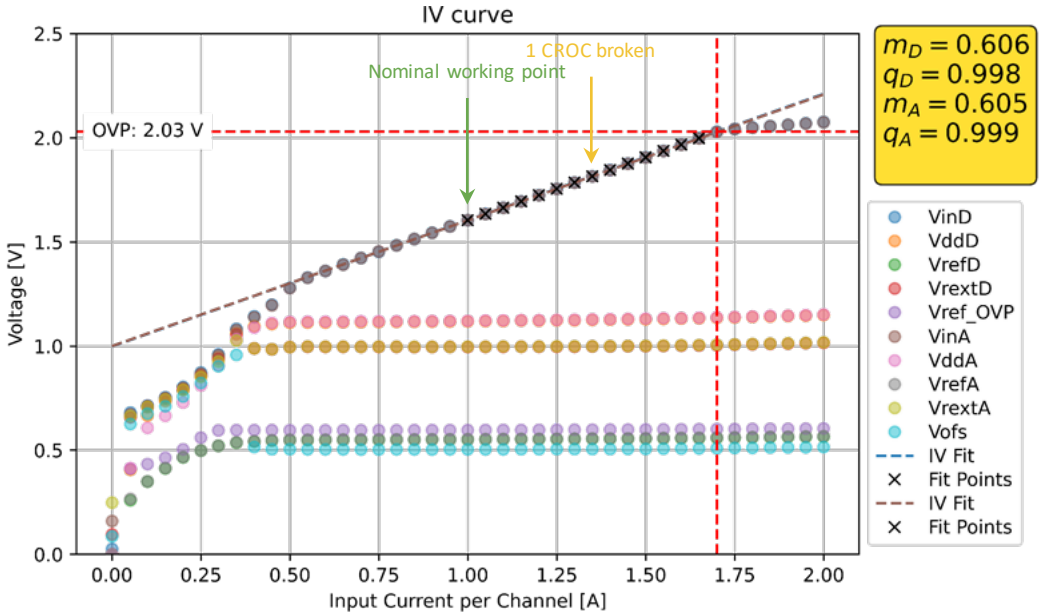
- Noise distribution in the chain

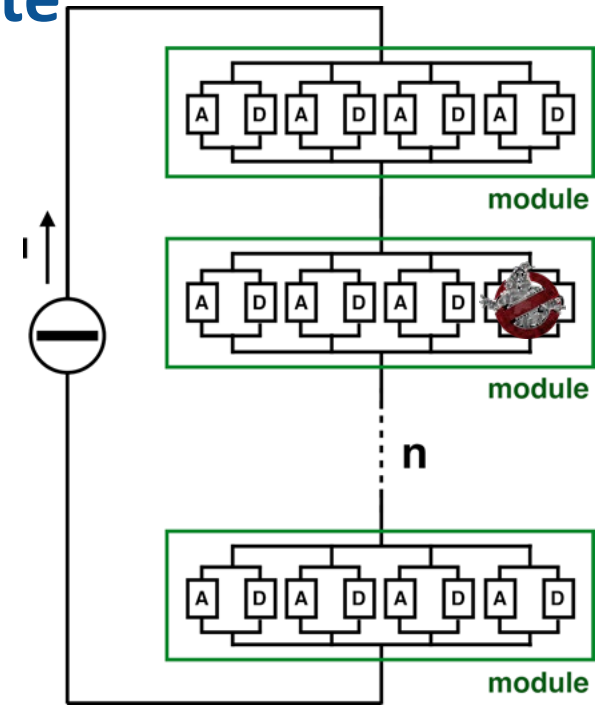
Single CROC Overvoltage Protection state



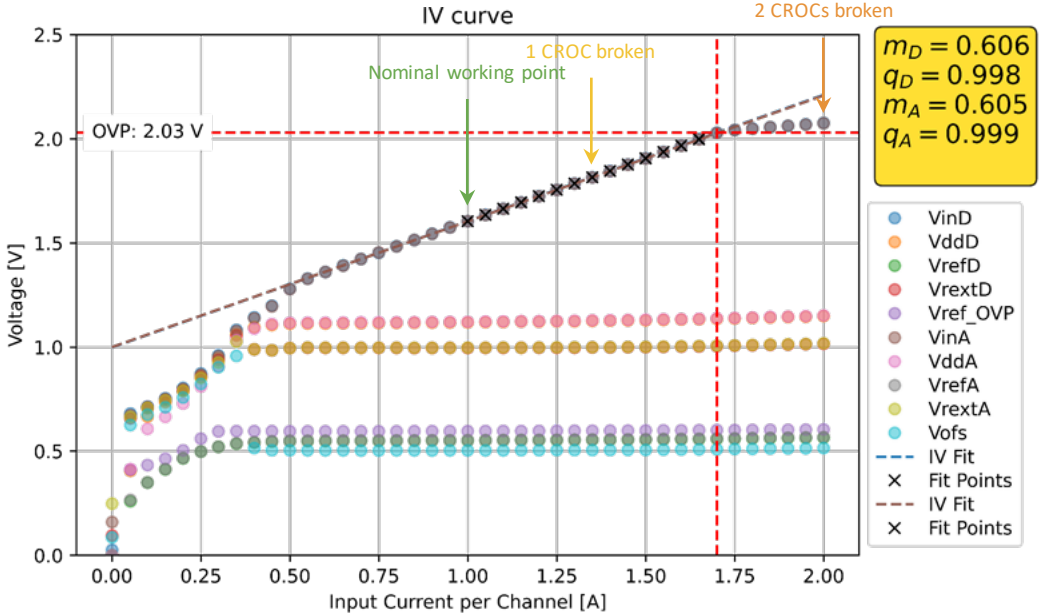


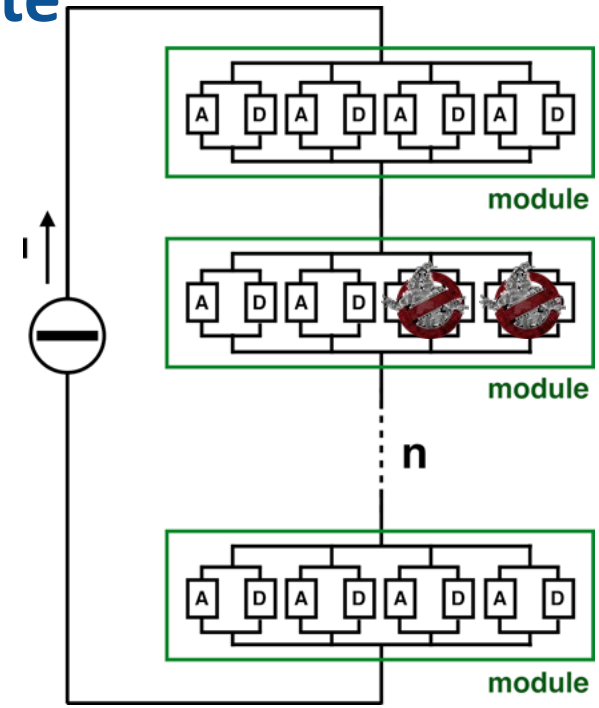
Single CROC Overvoltage Protection state



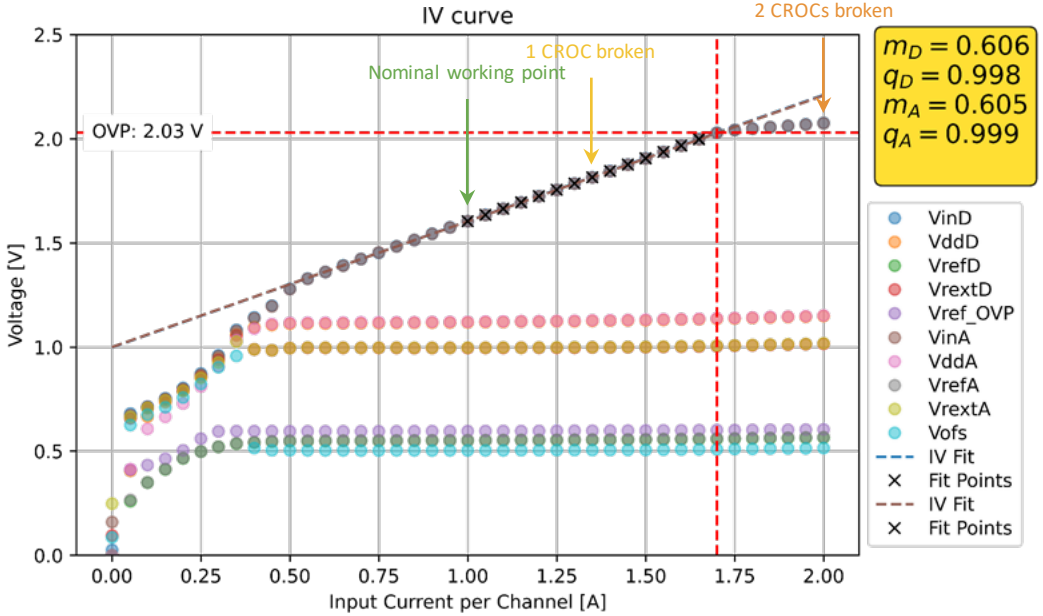


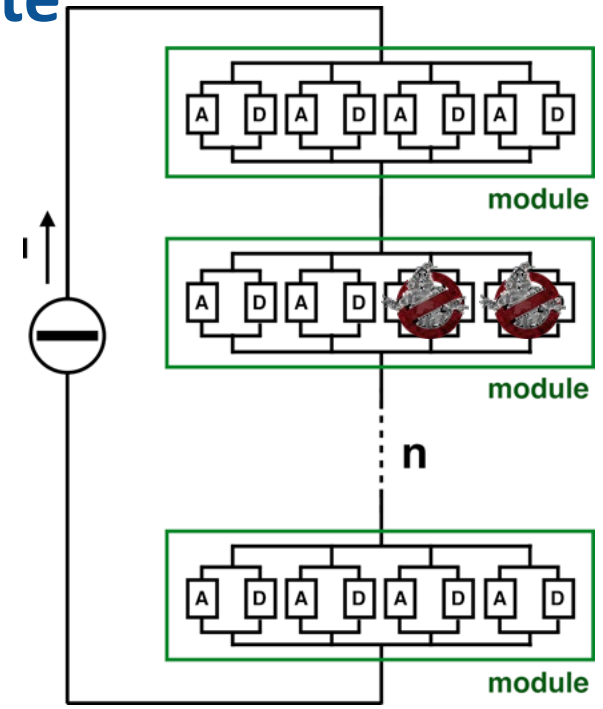
Single CROC Overvoltage Protection state





Single CROC Overvoltage Protection state

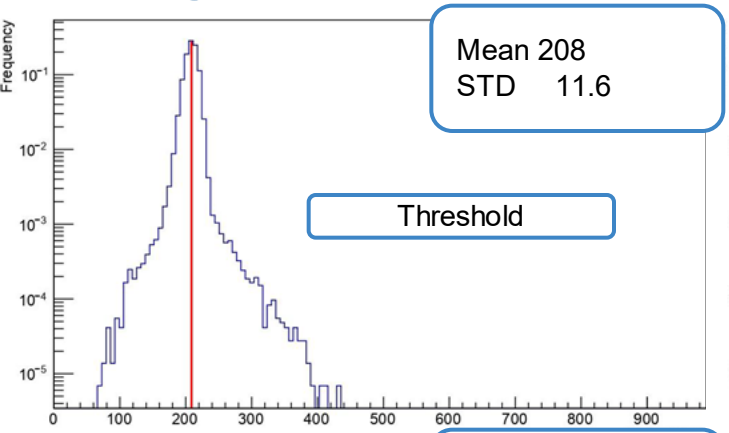


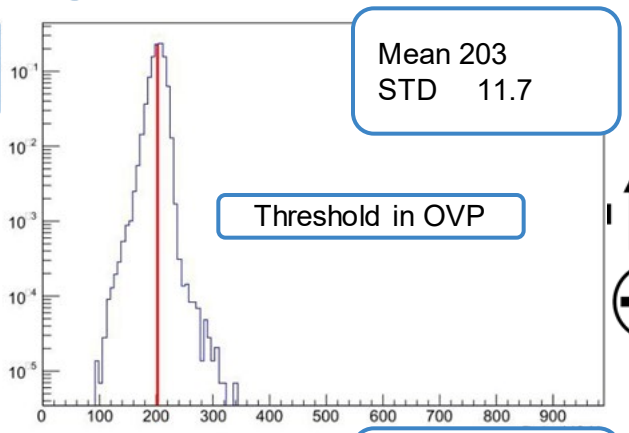


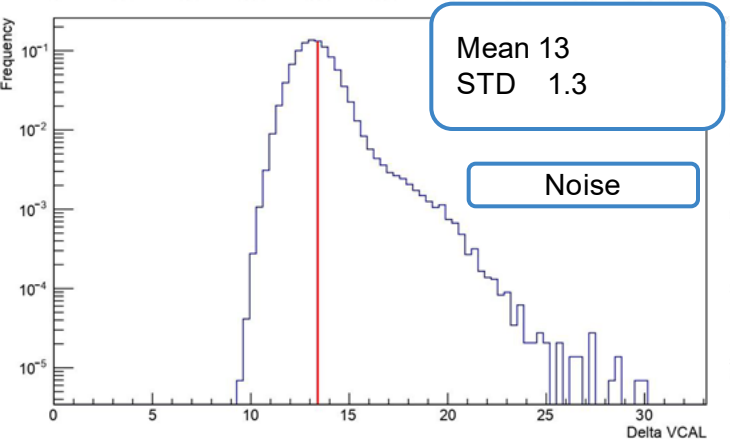
Checking the chip behaviour when in OVP conditions

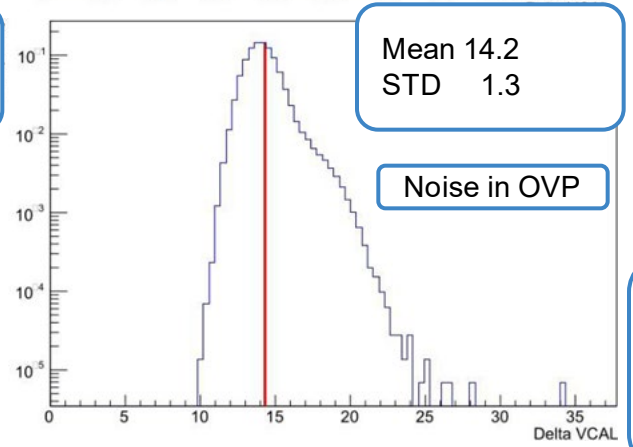
- Threshold distribution
- Noise distribution

Single CROC Overvoltage Protection state

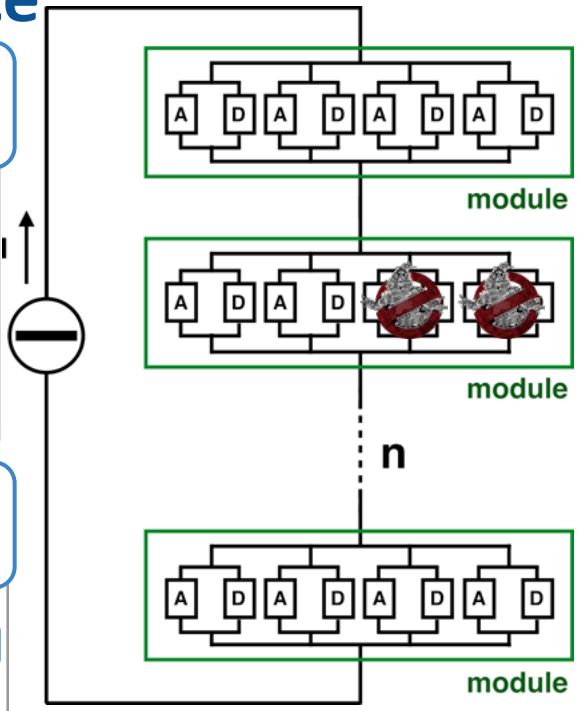








1 ΔVCal ~ 5 e⁻



Checking the chip behaviour when in OVP conditions

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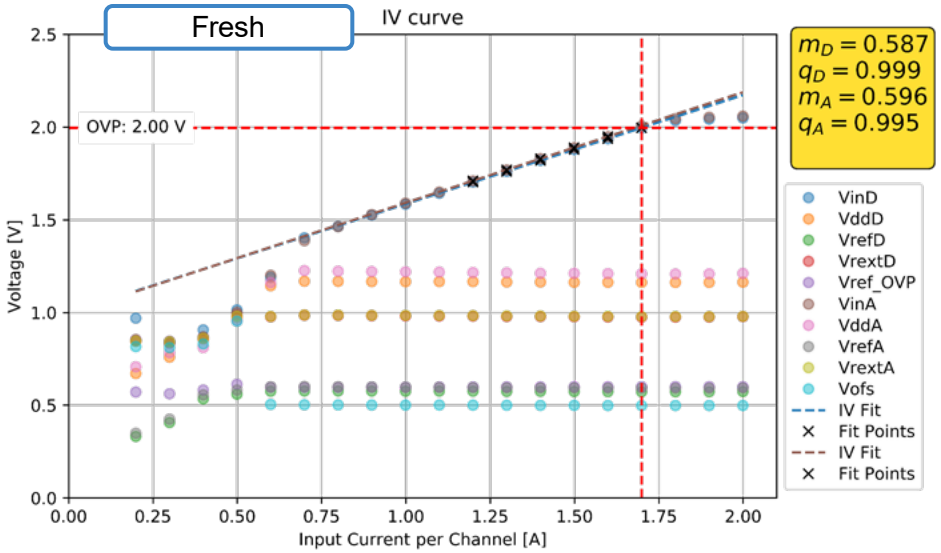
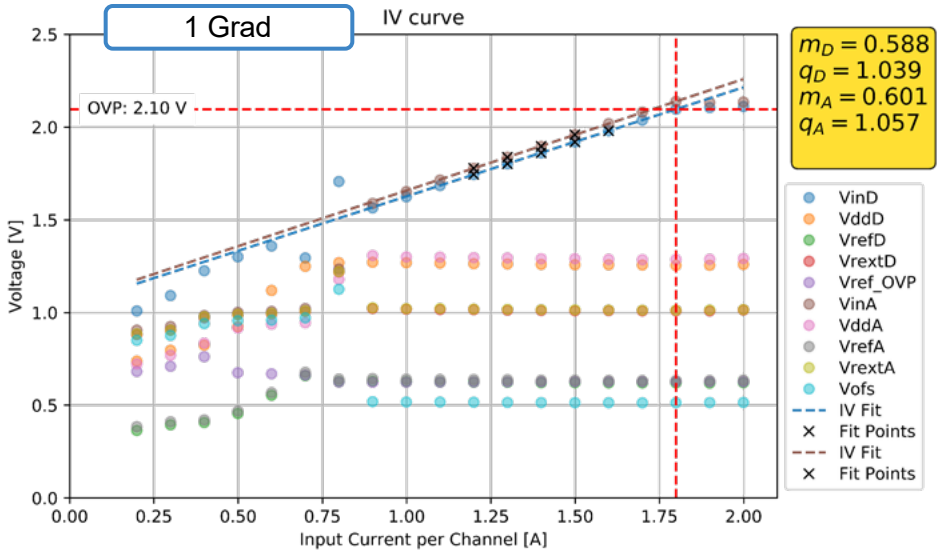
- Noise distribution

CROC SLDO irradiation studies





- Small shift of V_{off} towards higher values with the irradiation
- $V_{ddD/A}$ shift towards higher values with irradiation (lead to the choice of default $V_{ddD/A}$ to be 1.2V)
- OVP shift towards higher values

Summary

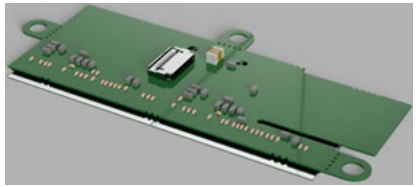
- The upgraded CMS Tracker is an extremely challenging project
- Innovative powering schemes that represent a technological challenge due to:
  - ✓ Low material budget
  - ✓ Mechanical constraints
  - ✓ High level of radiation
  - ✓ High segmentation of detector
  - ✓ High power requests
- Advanced status of serial powering studies
- Some other system studies are foreseen

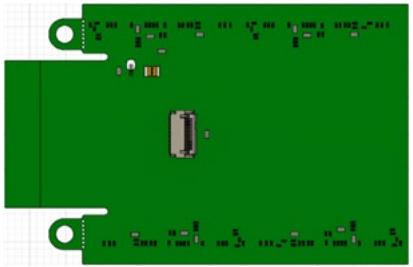
Thank you for your attention

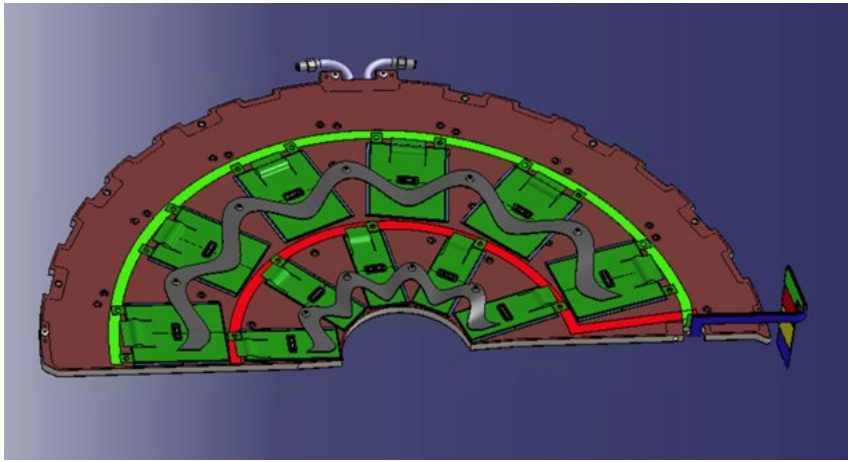
Backup

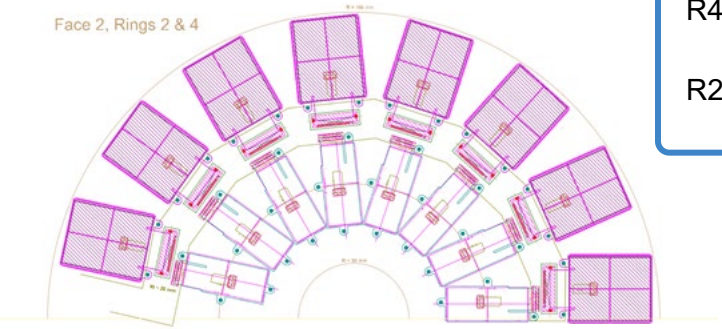
Serial power distribution

TFPX



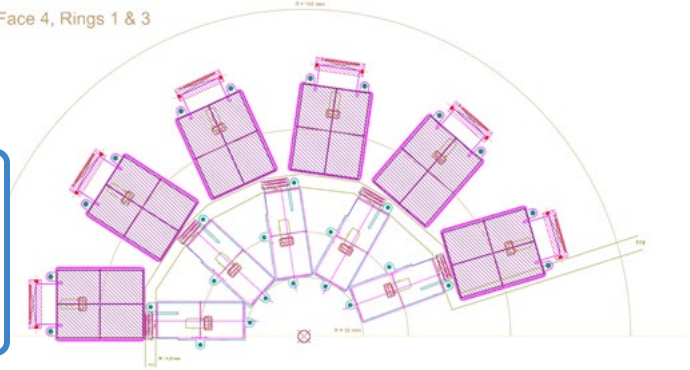






R4: 8 modules/chain

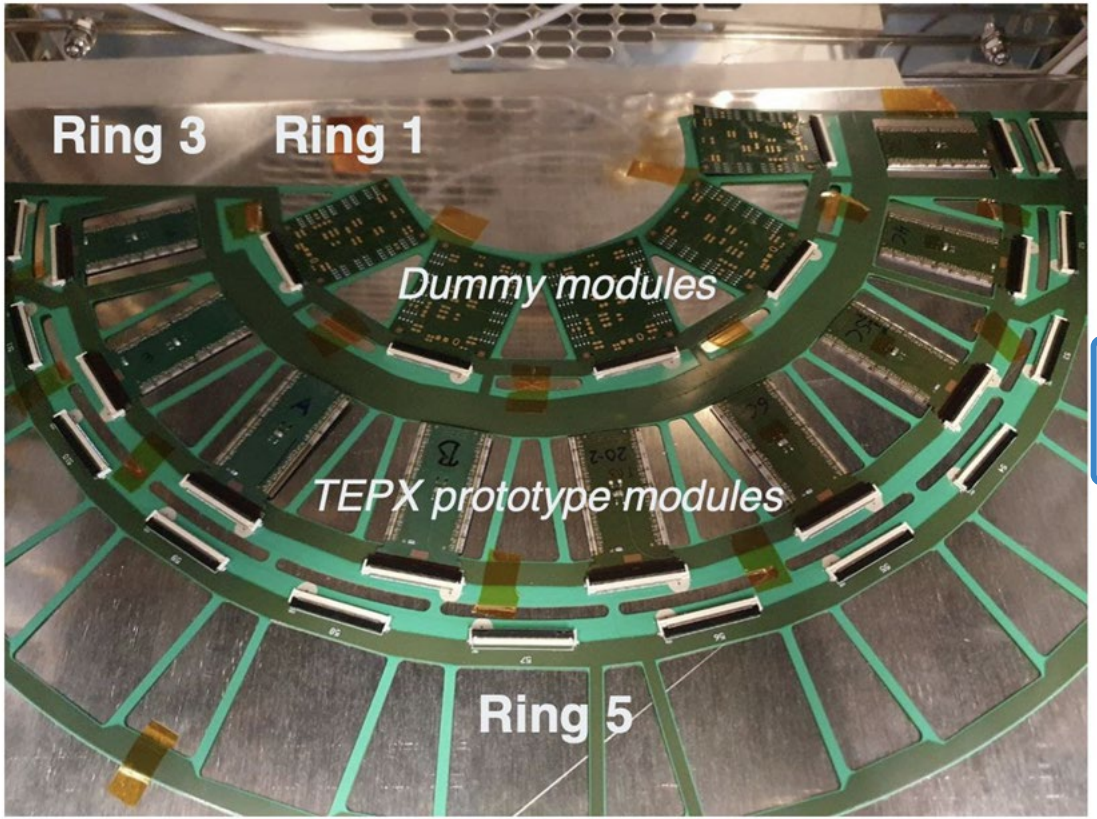
R2: 8 modules/chain



R3: 6 modules/chain

R1: 5 modules/chain

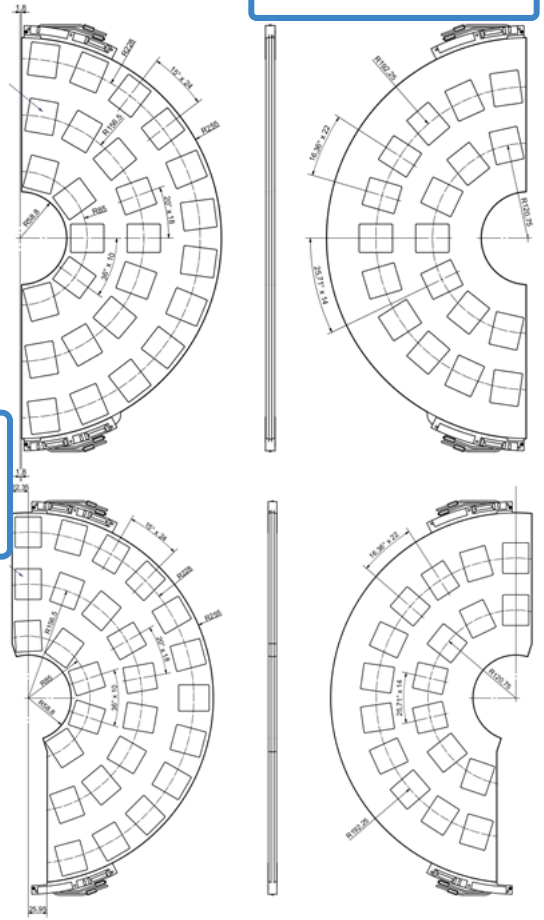
Serial power distribution



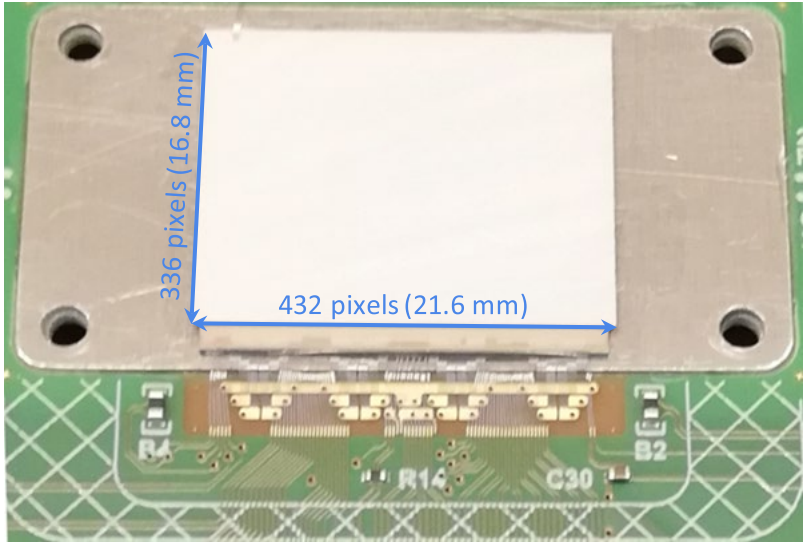
TEPX

R4: 11 modules/chain
R2: 7 modules/chain

R5: 12 modules/chain
R3: 9 modules/chain
R1: 5 modules/chain



CMS Read Out Chip (C-ROC)



- CMS chip size (16.8×21.6 mm^2, 336×432 cells)
- 65 nm CMOS technology
- Dead time ≤1% @3.2 GHz/cm^2
- 1 Grad TID (Total Ionizing Dose) resistant
- Strongly protected against SEU effects
- 50×50 μm^2 cell
- Linear analog FE
- Low threshold (≤ 1000 e^-)
- High hit and trigger rate (up to 4×1.28 Gb/s output links)
- Serial powering capabilities
- First wafer level test of the new chip has been performed
- Irradiation campaigns and full C-ROC characterization ongoing

RD53: the inner tracker readout chip

RD53 ROC

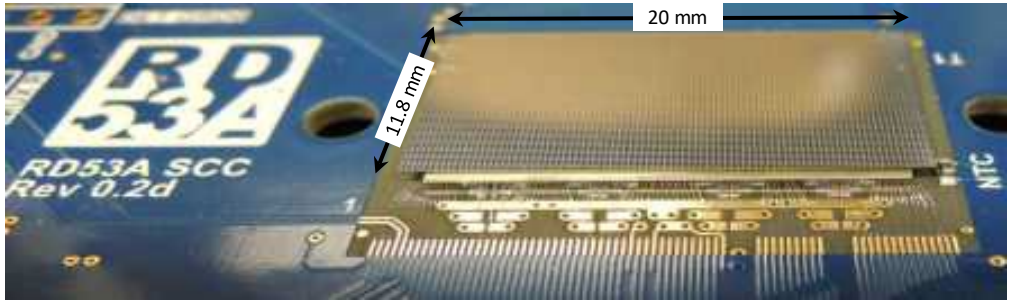
RD53 collaboration is developing an ROC with:

- Dead time ≤1% @3.2 GHz/cm^2
- 0.5 Grad TID resistant
- 65 nm technology
- 50×50 μm^2 cell
- low threshold (≤ 1000 e$^-$)
- High hit and trigger rate (up to 4×1.28 Gb/s output links)
- Serial powering capabilities
- CMS chip size (16.8×21.6 mm^2, 336×432 cells)

RD53: the inner tracker readout chip

RD53A first prototype

- ½ total size (50×50 μm^2 cell, 65 nm technology)
- Used for R&D
- Radiation hard up to 0.5 Grad
- Low threshold and high hit and rate capabilities (160 Mbps input and 1.28 Gbps output links)



RD53 ROC

RD53 collaboration is developing an ROC with:

- Dead time ≤1% @3.2 GHz/cm^2
- 0.5 Grad TID resistant
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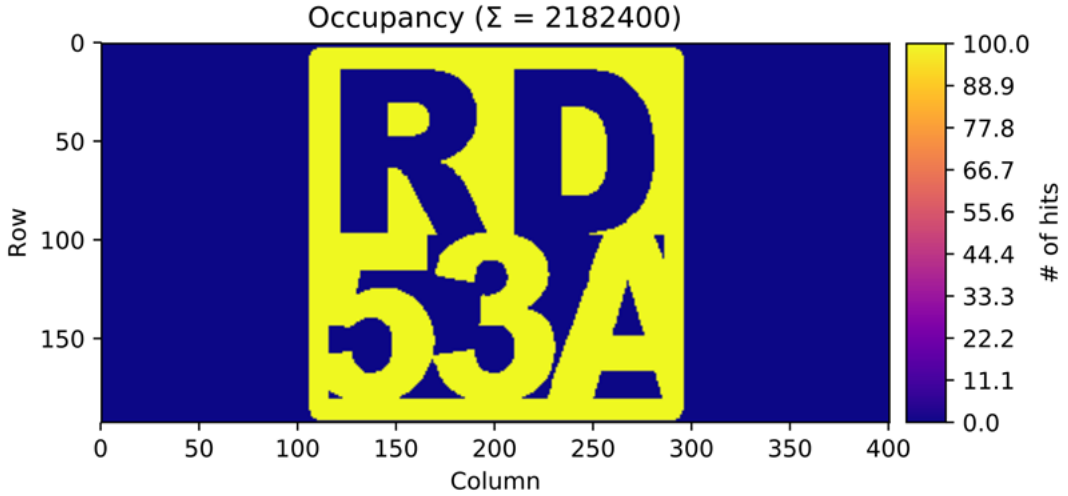
- Serial powering capabilities
- CMS chip size (16.8×21.6 mm^2, 336×432 cells)



R&D and tests

Active R&D ongoing in ATLAS, CMS and RD53 with tests and simulations

- First failure mitigation in CMS: the Inner Tracker can be accessed and any part replaced by design
- Current sharing investigations
- Turn on procedure studies
- Failure modes investigations are currently under study (shunt failure, regulator failure, serial chain failure, …)
- HV distribution in parallel to modules within the same serial chain
- ...

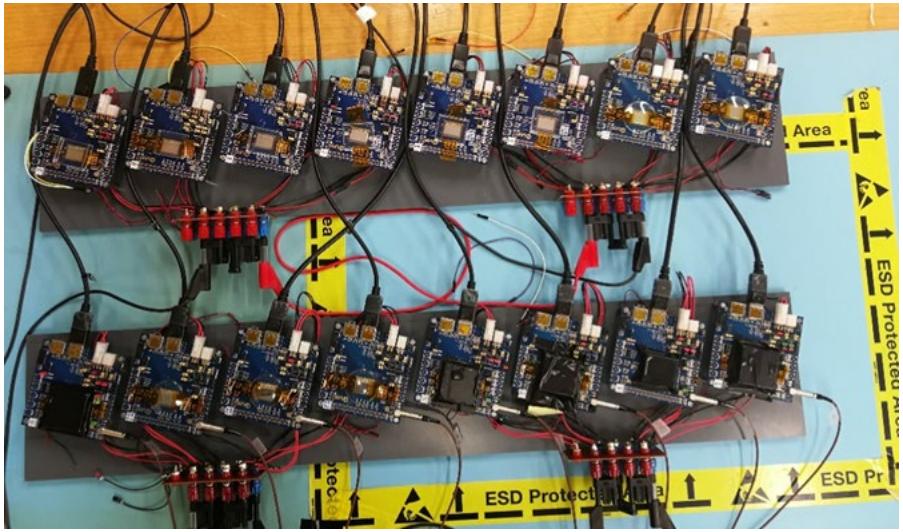
R&D and tests

Serial Powering concept established

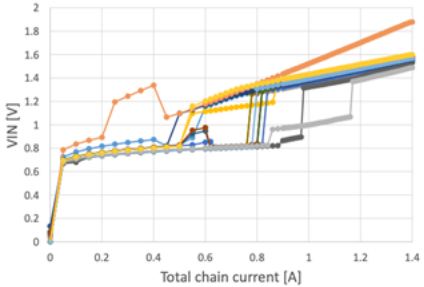
- Serial chains with up to 16 RD53A chips were successfully operated in lab

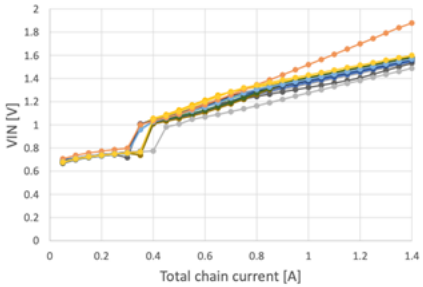
CROC will be final CMS ROC

- Further tests undergoing in collaboration of RD53, Atlas and CMS

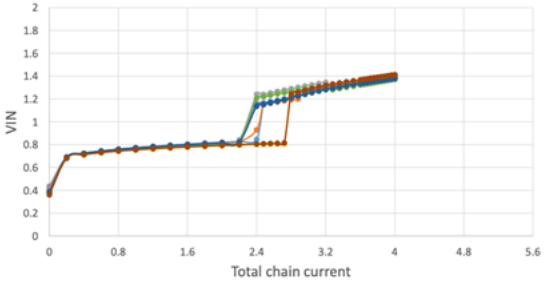


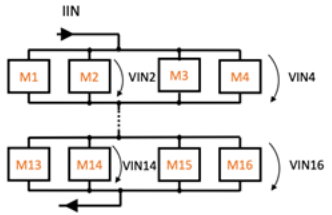
IV curves for 16x1: Ramp up and ramp down





IV curves for 4x4





- Measured two VIN per four chips on same level in chain
- Reached PS voltage limitation (6V) at 4A
- Small differences between VINs on the same level:
  - Combination of current sharing variations and current path impedance mismatches

HV distribution in parallel vs Serial power for LV

HV on / LV off state forbidden

- When LV off, the path for the sensor leakage currents might not be established to the readout chip, resulting in a damage
- For operation LV has to be switched on first and then the HV
- HV off / LV on status is also potentially dangerous

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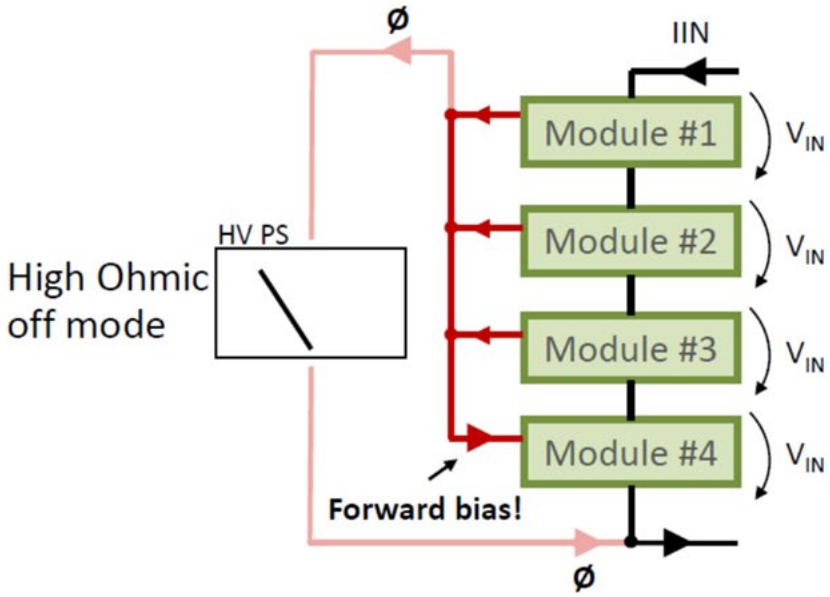
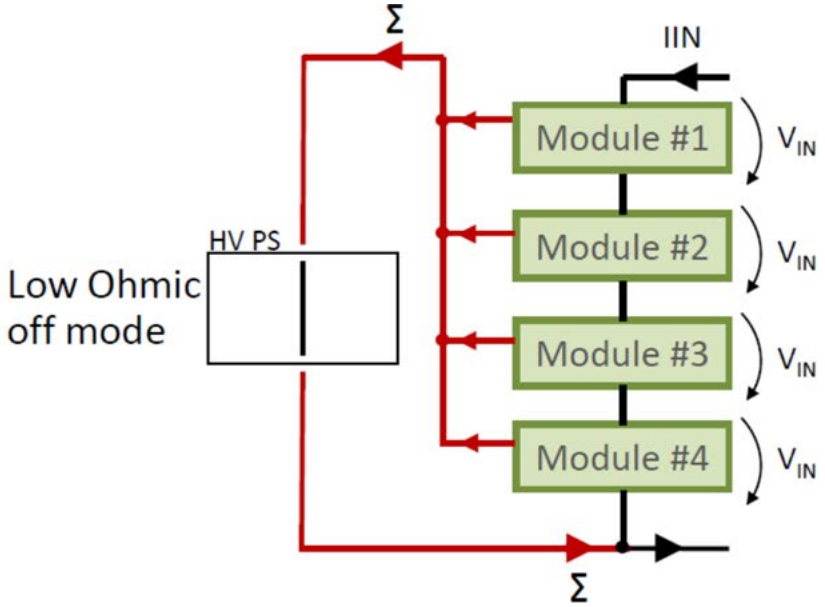
HV power supply off modes

- High/low ohmic mode
- Important for leakage current path
- Different local ground for each module
  - HV off not necessarily means 0 V on sensors (LV on)
  - Biased sensor and leakage current in off mode possible





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arily means 0 V on sensors (LV on)
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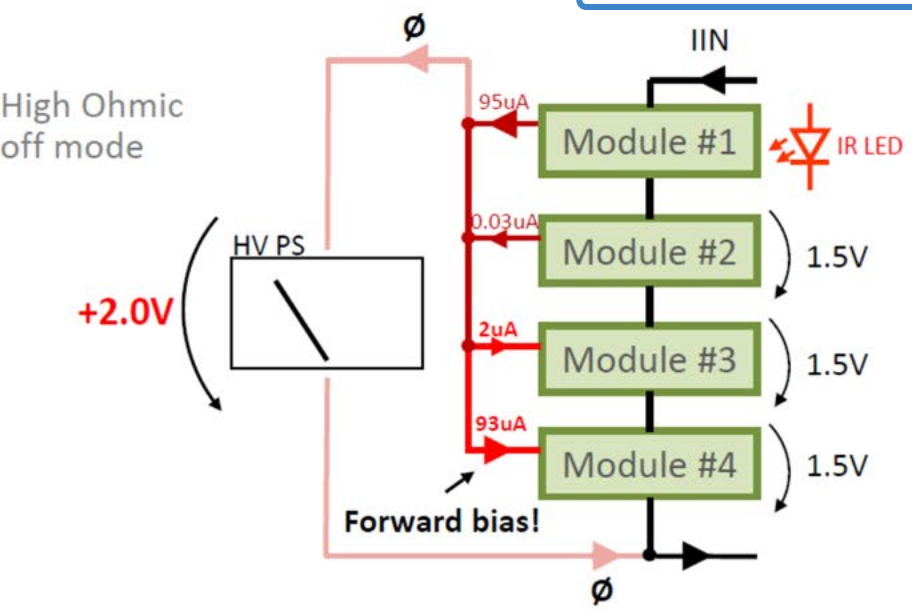
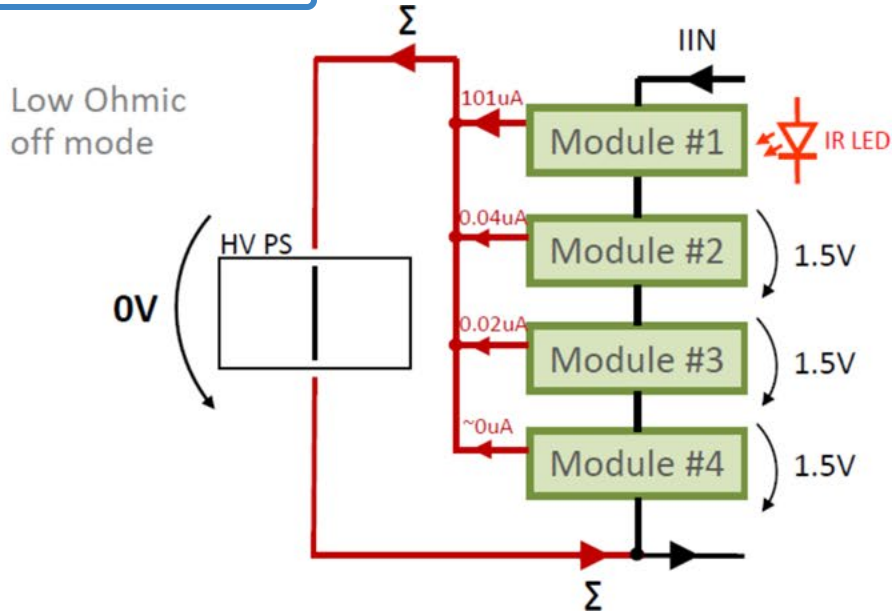
Experimental example using 4 modules





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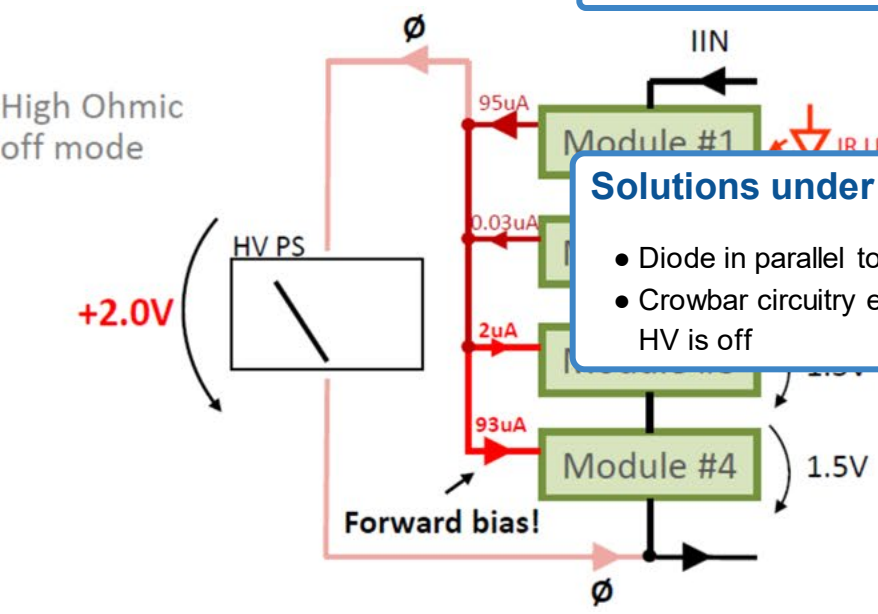
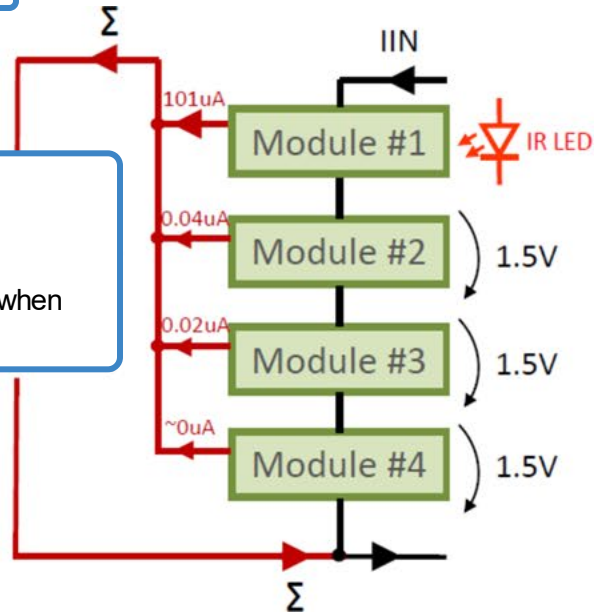


Solutions under investigation include:

- Diode in parallel to HV regulator
- Crowbar circuitry ensuring low impedance to ground when HV is off



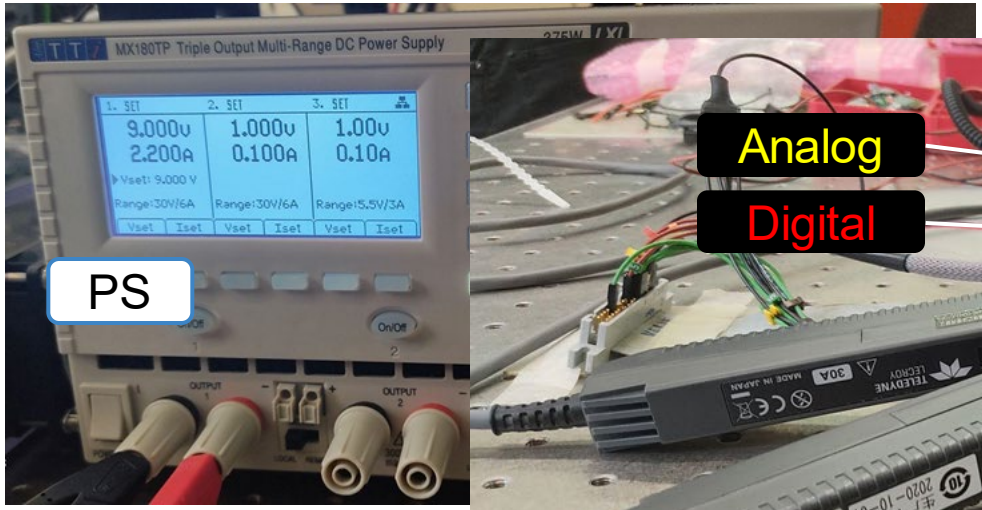
Test setup

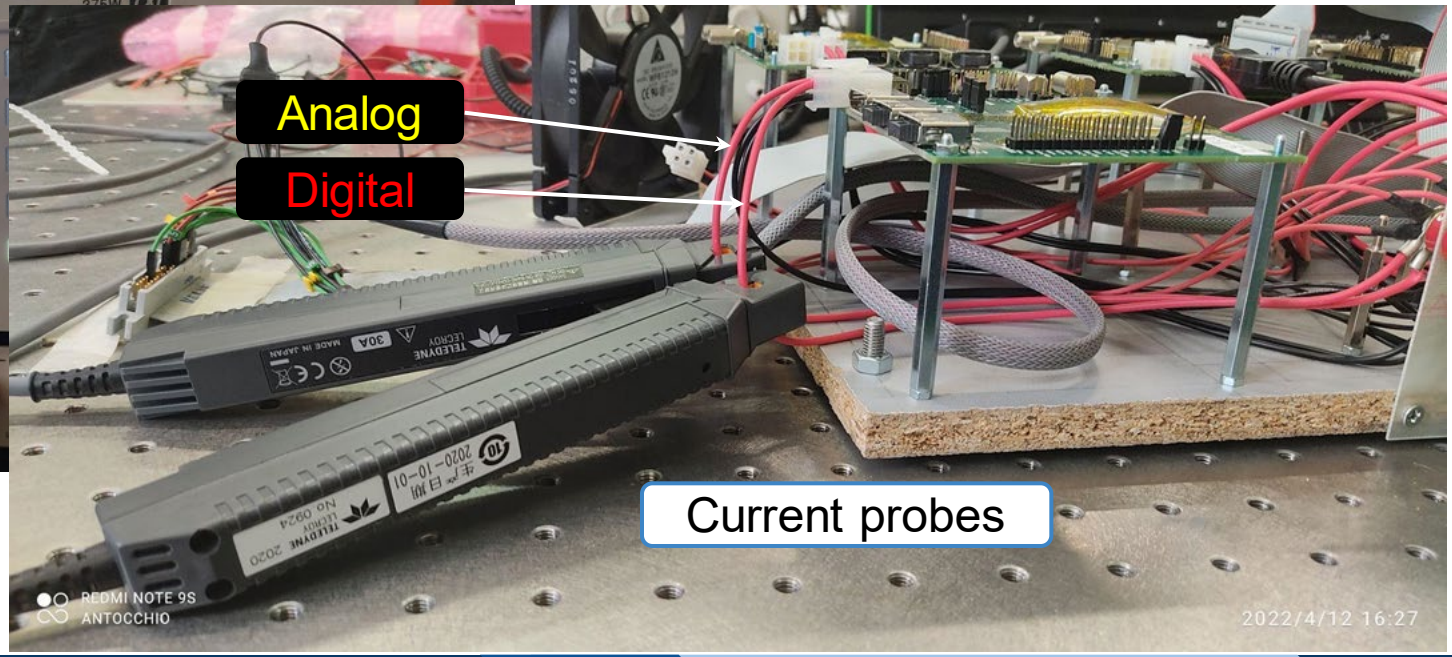
- Single power supply channel for both Analog and Digital
- I_{ref} tuned such that V_{OFS} = 0.50 ± 0.01 V
- Reading of MONITOR header through Scanner card:
  - V_{inA}, V_{ddA}, V_{rextA}, V_{refA}, V_{OFS} → GNDA
  - V_{inD}, V_{ddD}, V_{rextD}, V_{refD}, V_{ref_ovp} → GNDD

- The tested CROCs are mounted on Bonn SCC
- SCC local ground configuration modified for serial powering chain:
  - ✓ Remove: R_GND_BDAQ, R_VDDD_SNS, R_GND_SNS, R_SCAN
  - ✓ Open PMTM on DEBUG jumper

Current sharing

- Bench commercial standard PS (ramps not configurable)
- Single power channel for both analog and digital domain
- Current probe to verify proper current sharing





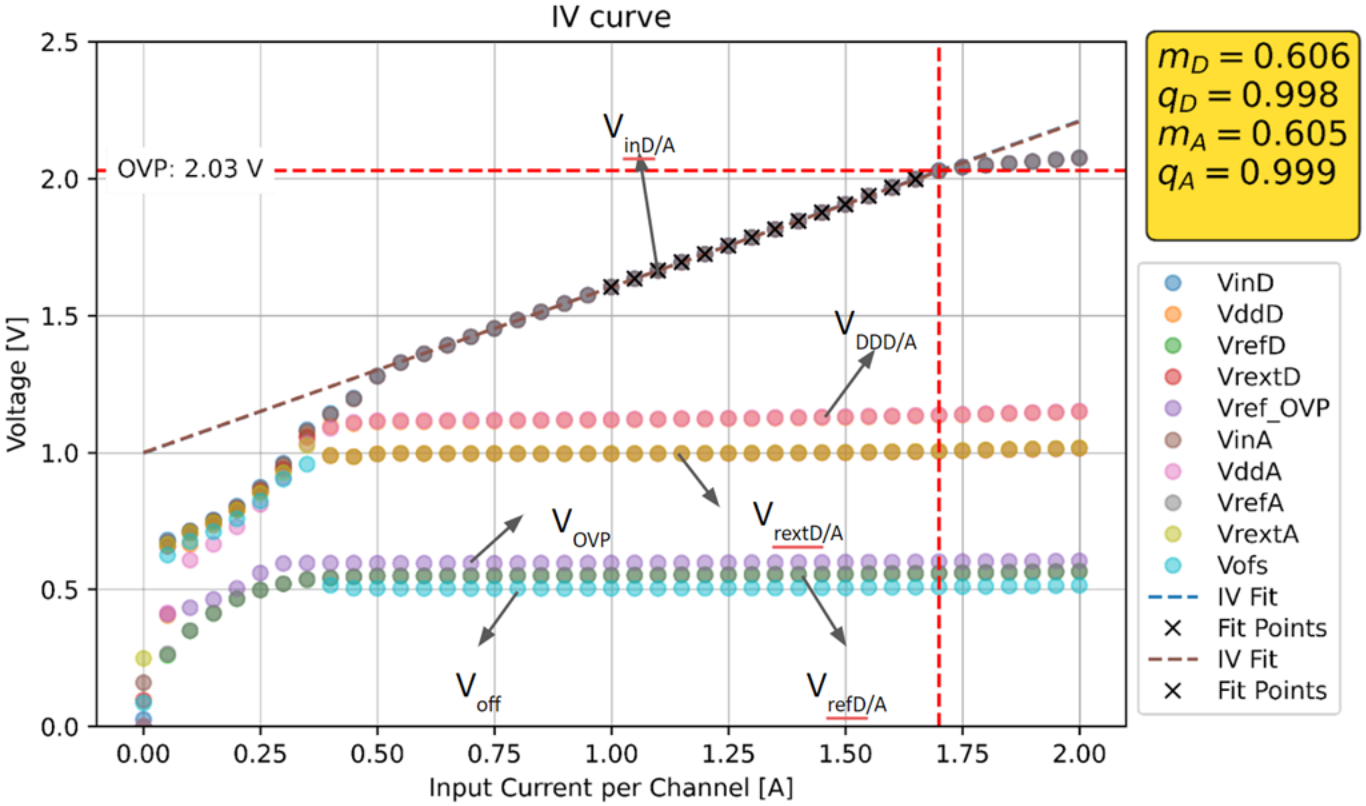
IV Curve Strategy

$V_{ofs} \times 2 \sim V_{rextD/A} \sim q_{D/A}$

$V_{refD/A} \times 2 \sim V_{DDD/A}$

$V_{OVP} \times 3 \sim OVP$

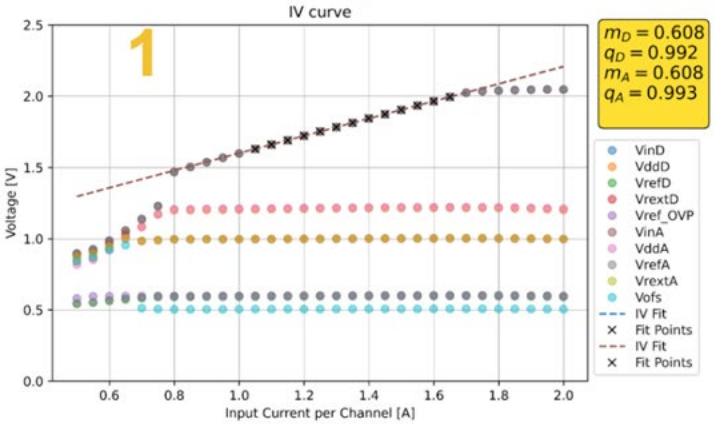
- Assume 50/50 current sharing

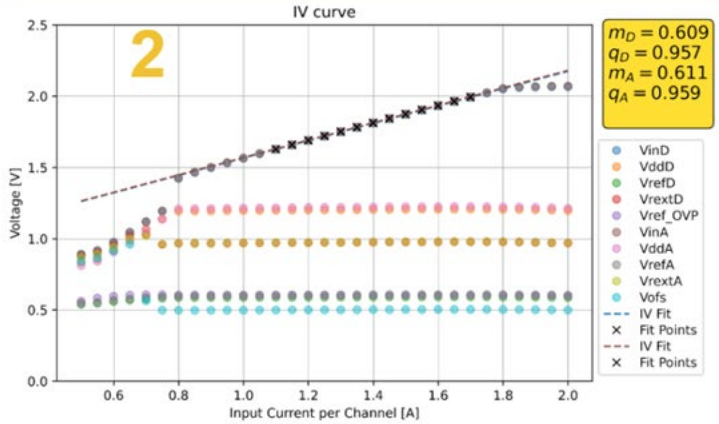


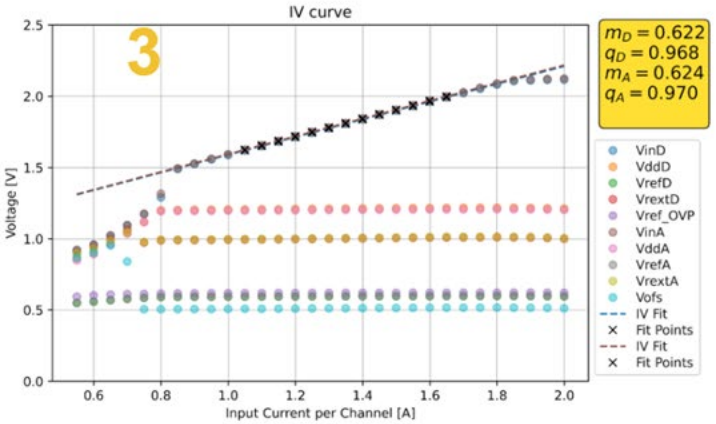
IV Curve

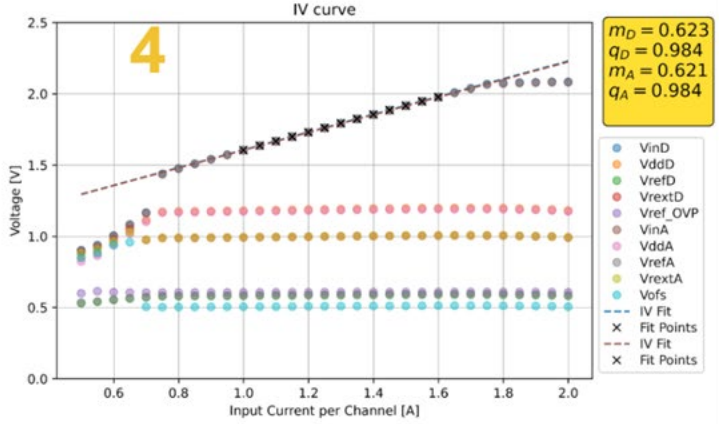
Ramp-down: 4 → 0 A
Chip configured
(Trimmed VDDD/A)

- Overall expected behaviour in the chain
- Same fitted V_{off} (namely $q_{A/D}$) in the same SCC
- Slight different $q_{A/D}$ between SCCs

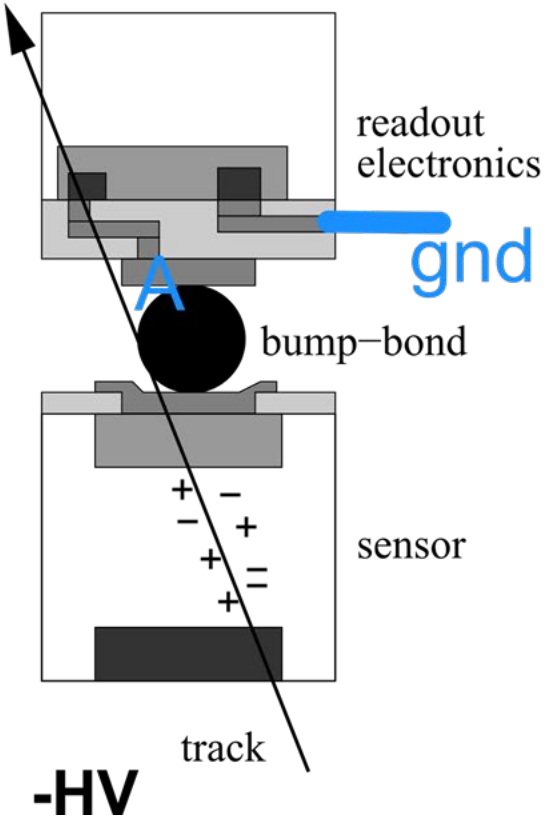








Avoid HV on LV off



Point A to virtual GND only when FE is powered.

In Serial Powering GND here is just a “local” GND