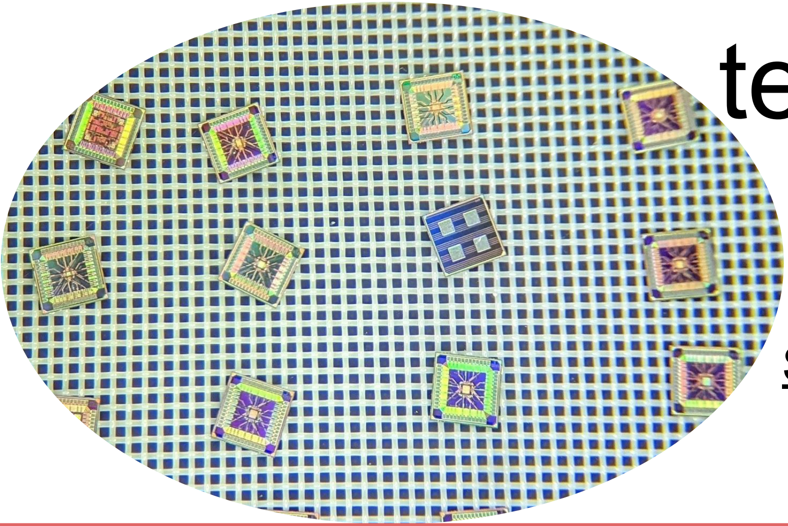
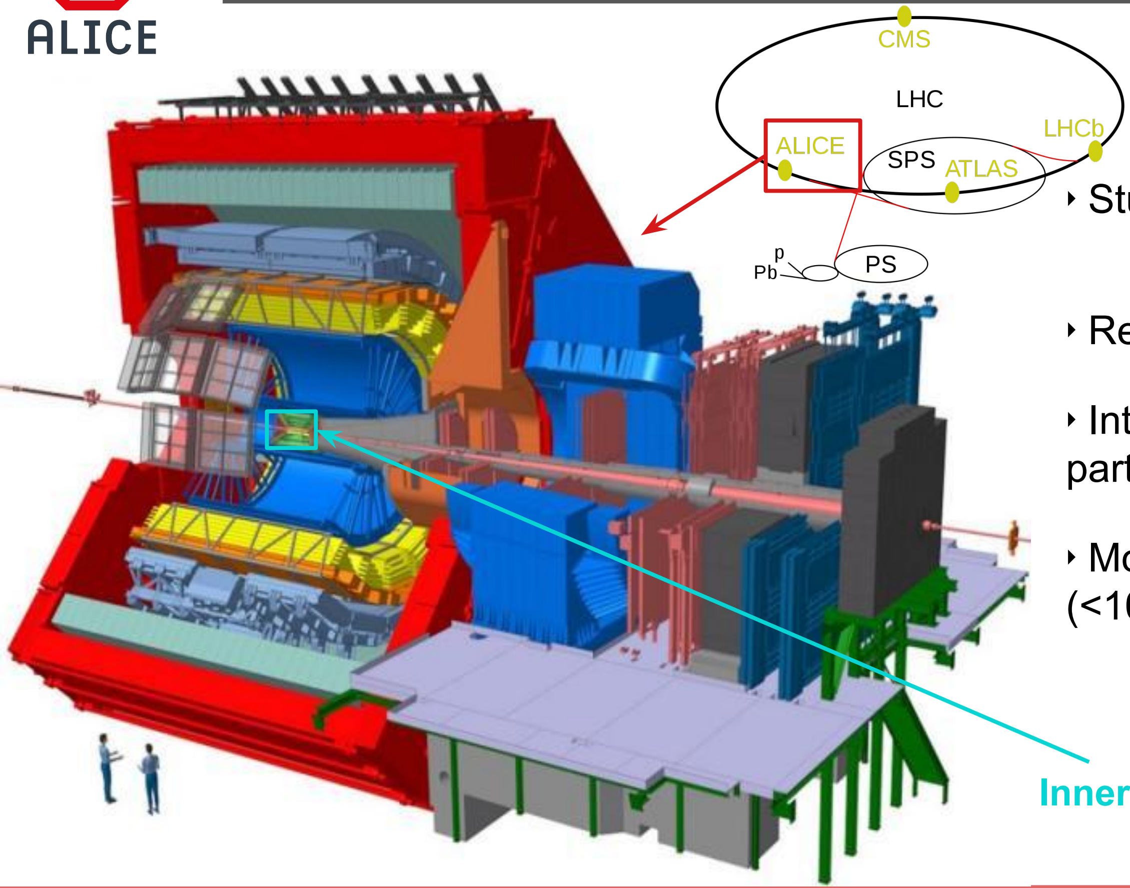
First results on monolithic pixel sensors test structures in the 65 nm technology



Stefania Perciballi, stefania.perciballi@unito.it,
on behalf of the ALICE Collaboration

The ALICE experiment

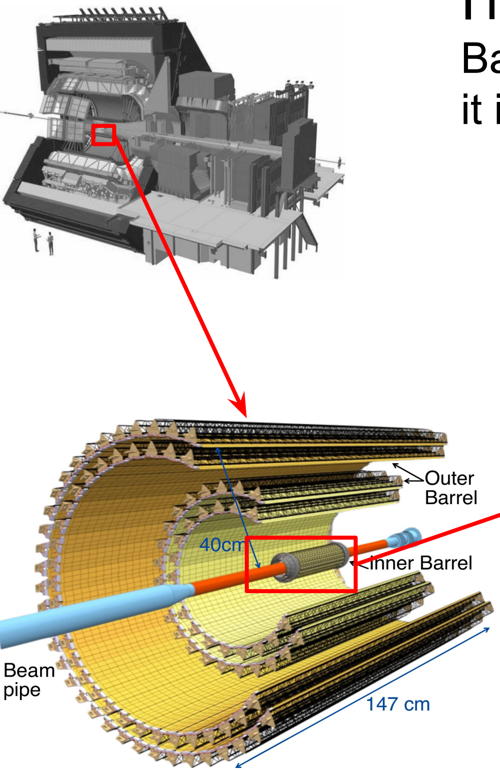


- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
  - requires **precise inner tracker**
- Interest in low momentum ($\lesssim$1 GeV/c) particle reconstruction
  - requires **low material budgets**
- Moderate radiation environment ($<10^{14}$ 1MeV neq/cm^2 NIEL)

Inner Tracking System (ITS2)

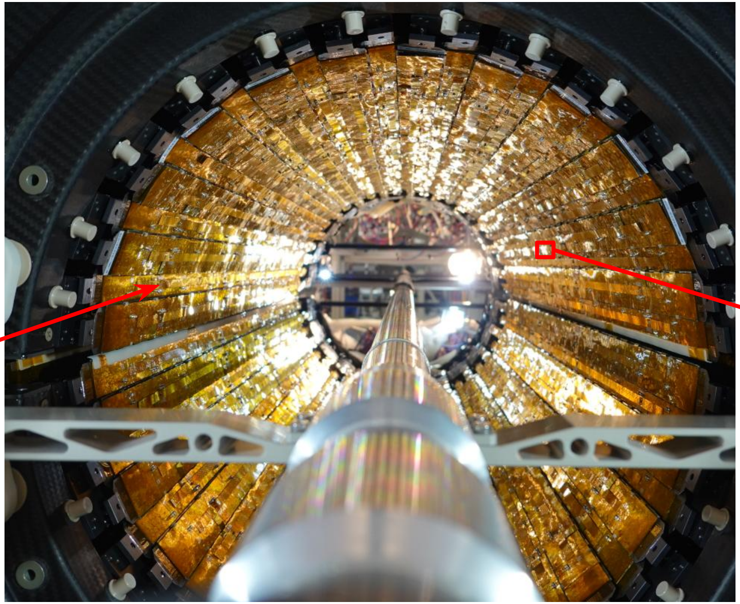
The ALICE Inner Tracking System 2

ALICE



ITS2:

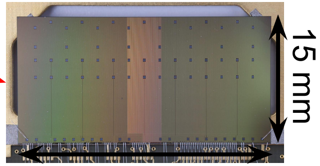
Based on Monolithic Active Pixel Sensors (**MAPS**)
it is the **largest pixel detector** ever built



ALice PIxel DEtector (ALPIDE)
→ developed for ALICE ITS 2

- technology: TowerJazz 180 nm
- sensor area: 15x30 mm^2
- 1024x512 MAP matrix

ALPIDE

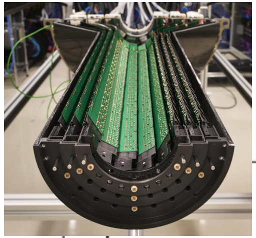


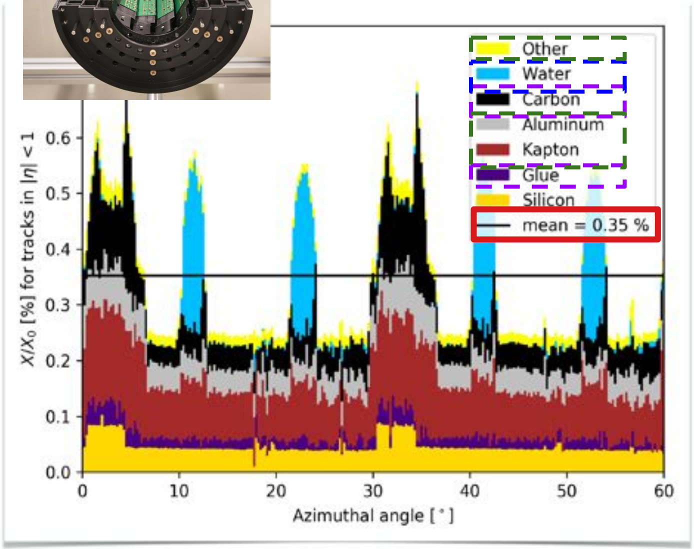
Further improvements?

ALICE ITS upgrade for LS3

ALICE

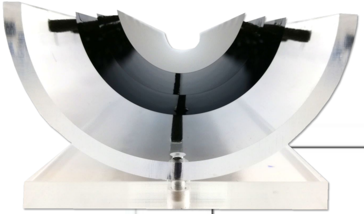
ITS2

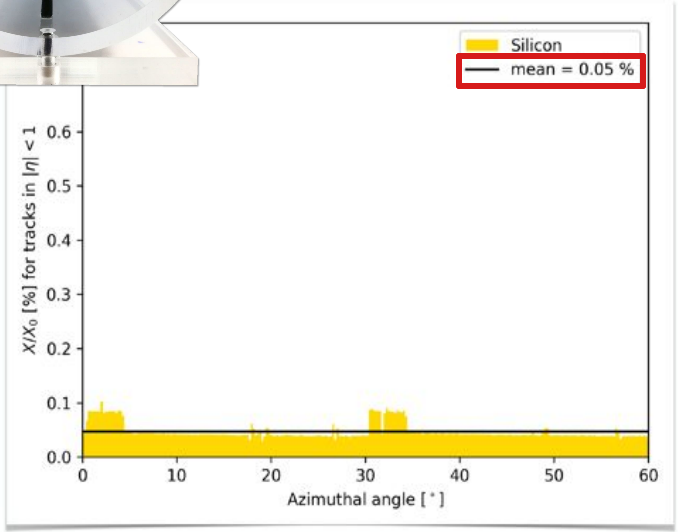




x 1/7

ITS3

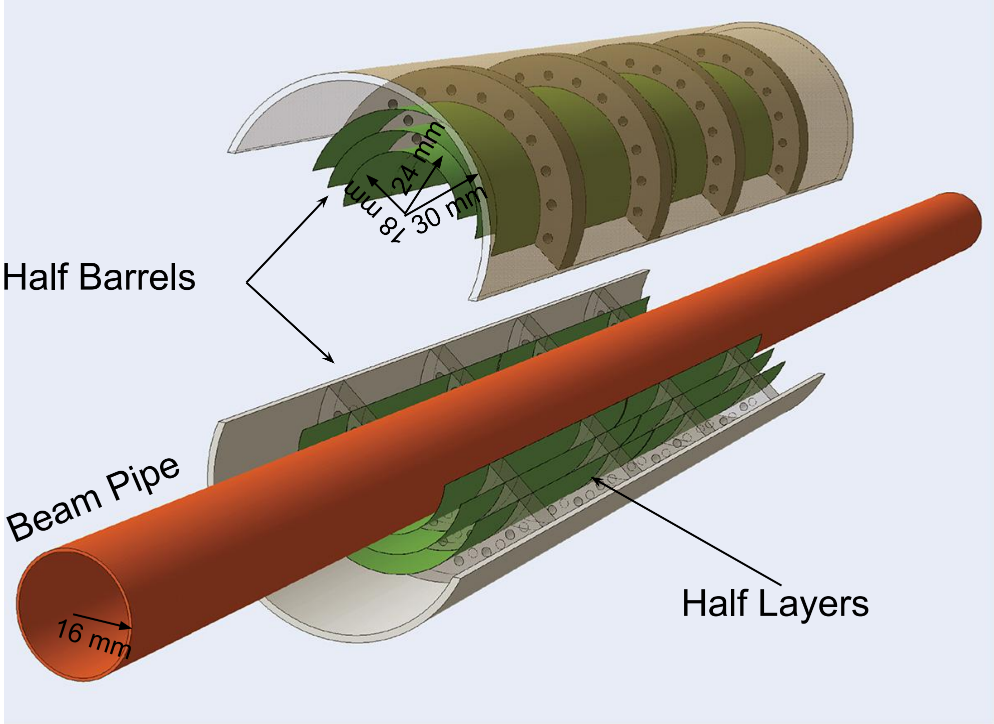




- **circuit board** → not required if integrated in circuit (stitching)
- **water cooling** → not required if the power consumption is < 20 mW/cm^2
- **mechanical support** → not required if self supporting arched structure

Letter of Intent for an ALICE ITS Upgrade in LS3 https://cds.cern.ch/record/2703140

ITS3: 6 truly cylindrical wafer-scale MAPS

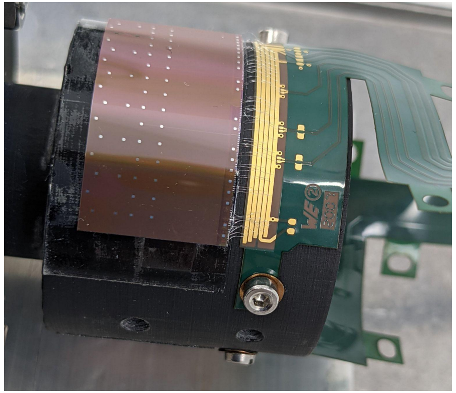


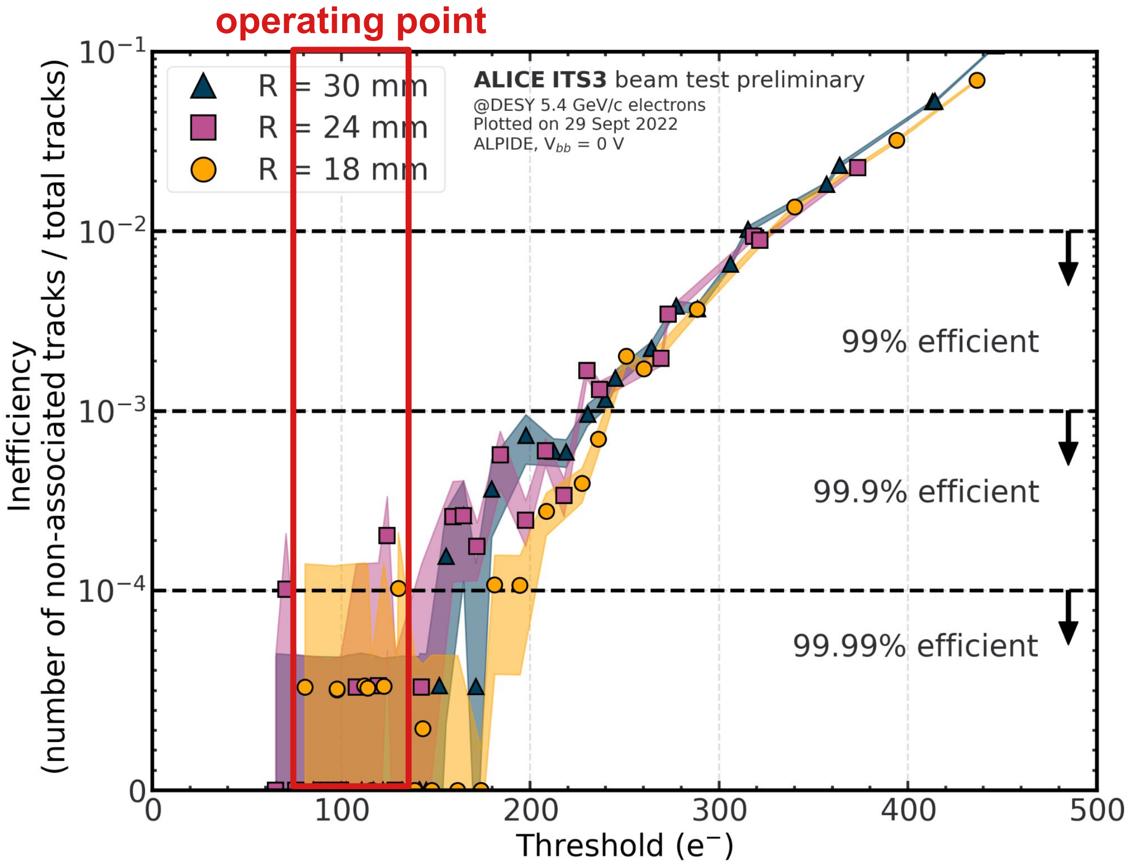
- **300 mm wafer-scale MAPS sensors**, fabricated using **stitching** (→ requires to move from the 180 nm ⇒ 65 nm)
- **thinned down to 20-40 µm** making them flexible
- **bent** to target radii (L_0: 23 mm→18 mm, **closer** to the interaction point thanks to the new beampipe at 16 mm)
- mechanically held in place by carbon foam ribs

Letter of Intent for an ALICE ITS upgrade in LS3: https://cds.cern.ch/record/2703140?ln=it

Silicon flexibility and bending of ALPIDEs

- **Chip performance doesn't change after bending**
- **Efficiency above 99.99%** at a threshold of 100 e$^-$ (normal operating point), consistent with flat ALPIDE



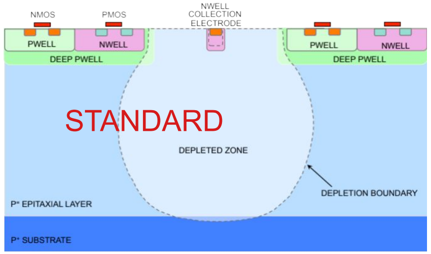


MAPS in the 65 nm CMOS process

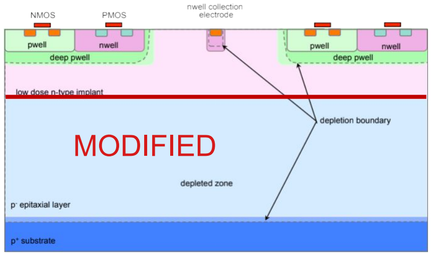
First submission in the Tower Partners Semiconductor (TPSCo) 65 nm technology

Verification of the technology for charge collection efficiency, detection efficiency, radiation hardness:

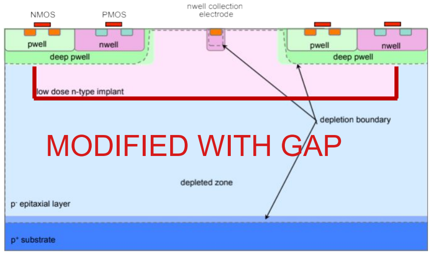
- ❖ Process modification for fully depleted sensor:
  - ➢ standard → increase depletion region until epitaxial layer
  - ➢ modified
  - ➢ modified with gap → increase the lateral field to speed up the charge collection process



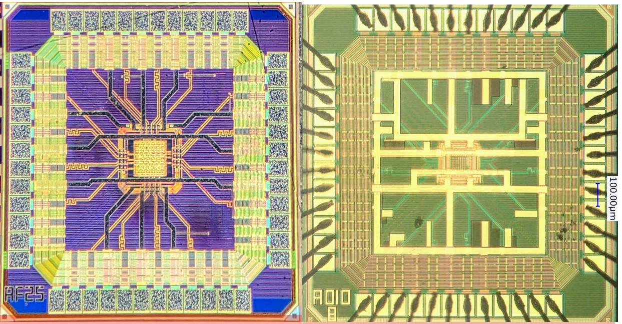
https://doi.org/10.1016/j.nima.2017.07.046



http://dx.doi.org/10.1088/1748-0221/14/05/C05013



MLR1 Test Structures

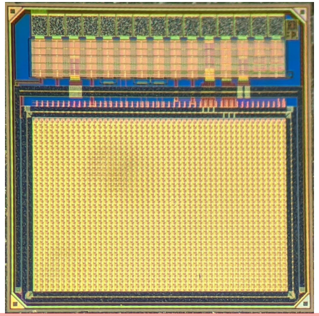


Analogue Pixel Test Structure (APTS)

- **aim:** explore different pixel designs
- **matrix sizes:** 4×4
- **pixel pitch:** 10, 15, 20, 25 µm

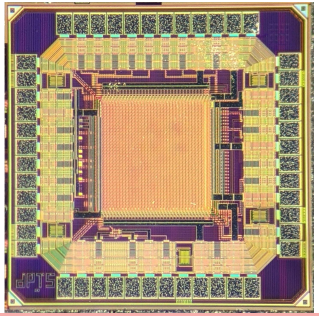
Two types of output drivers:

- Source follower (APTS-SF)
- OpAmp (APTS-OA) → timing



Circuit Exploratoire (CE65)

- **aim:** study pixel matrix uniformity
- **matrix sizes:** 64x32, 48x32
- **pixel pitch:** 25, 15 µm



Digital Pixel Test Structure (DPTS)

- **aim:** study in-pixel discrimination
- **matrix sizes:** 32×32
- **pixel pitch:** 15 µm

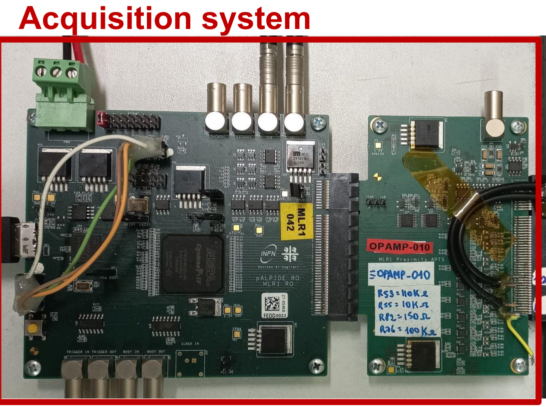
Chip Characterization

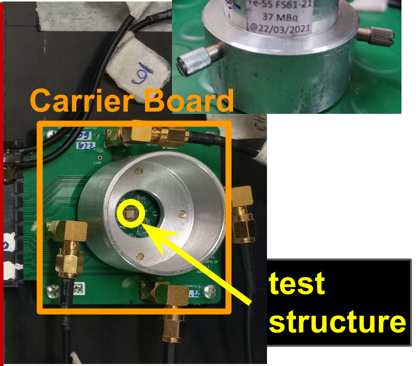
In Lab measurements:

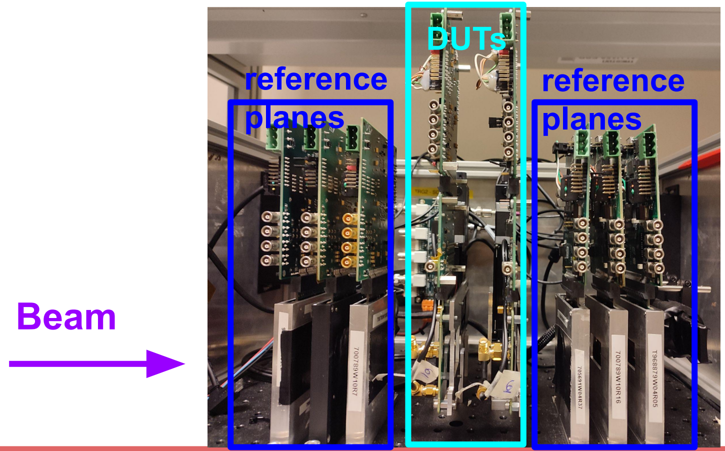
- Pulse and noise measurements
- Measurements with an X-rays source (^{55}Fe)
  - Tuning of operational parameters
  - Signal calibration
  - Charge collection efficiency study

At Test Beam facilities:

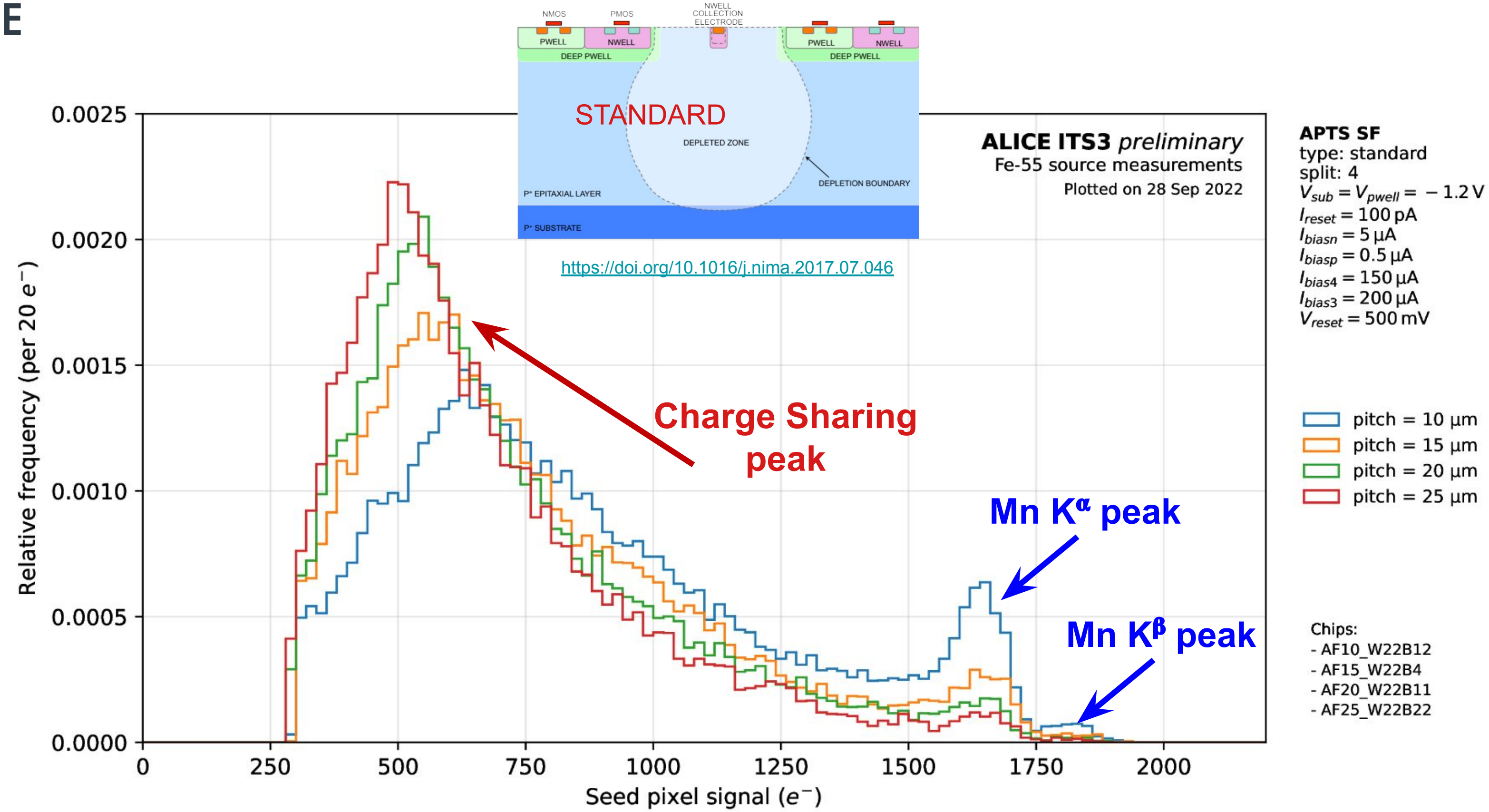
- Particle tracks reconstructed by telescope
- Association of clusters in DUT with tracks
- Efficiency/Fake Hit Rate vs. discriminator threshold for digital chips
- Energy straggling for analogue chips
- Spatial and temporal resolution



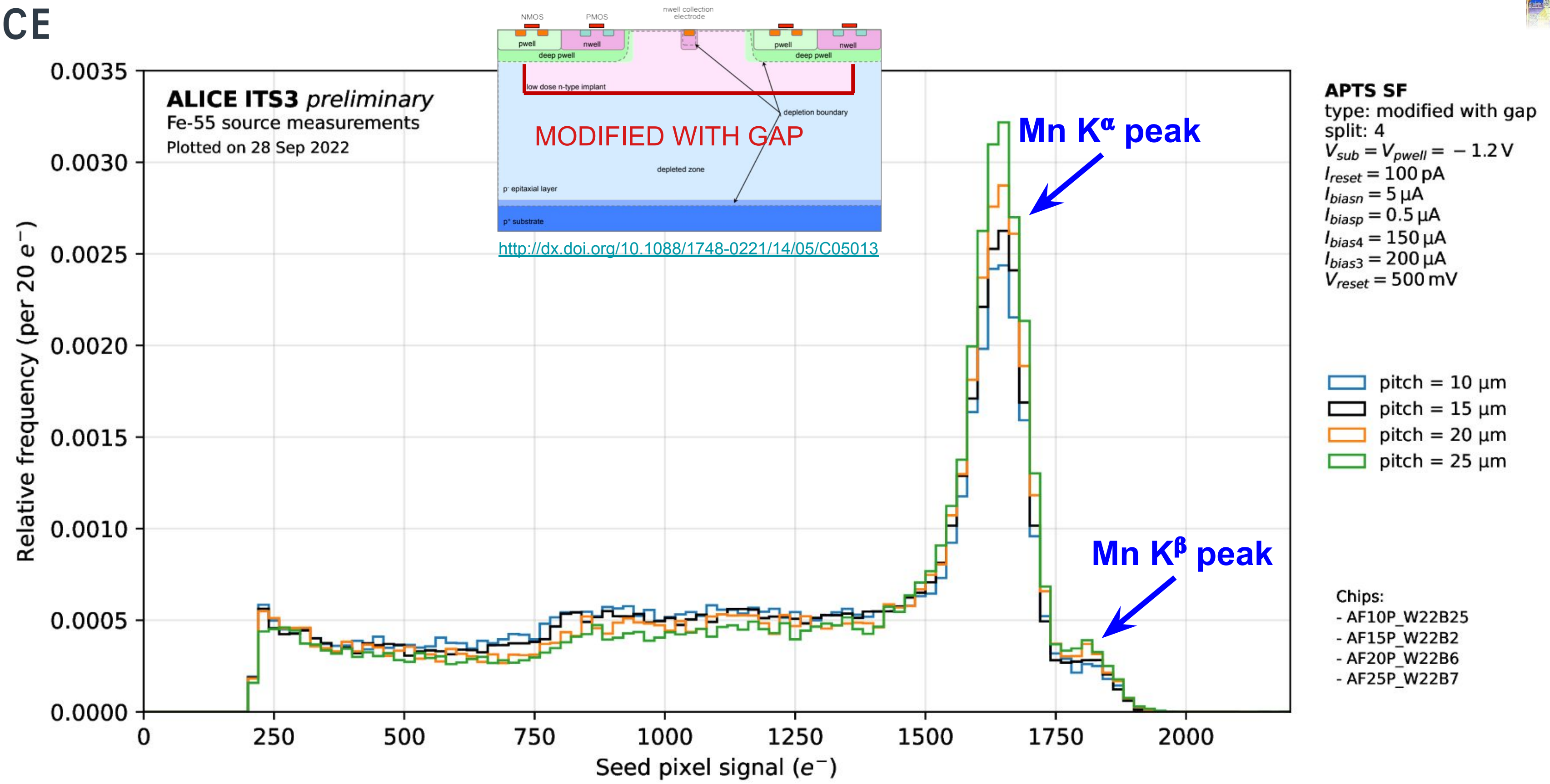




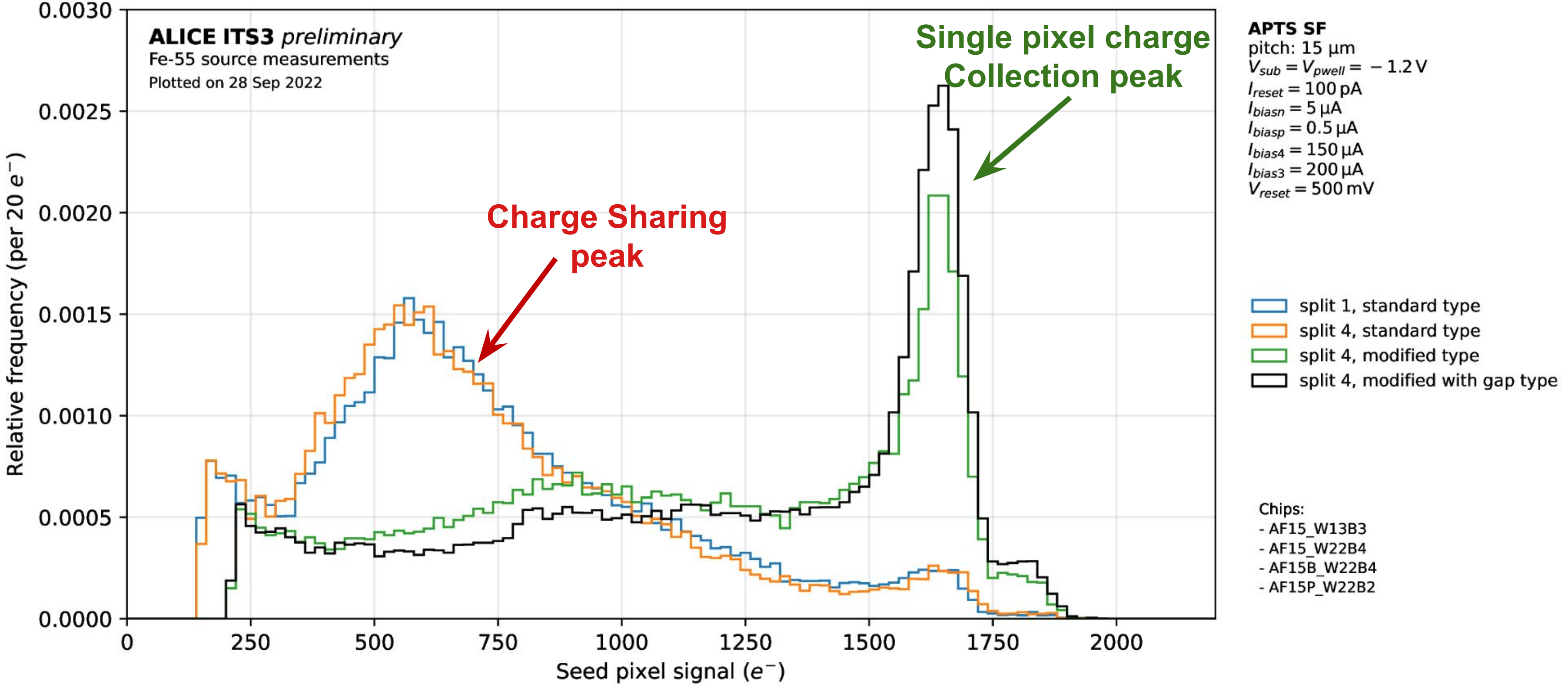
APTS-SF - ^{55}Fe Results



APTS-SF - ^{55}Fe Results

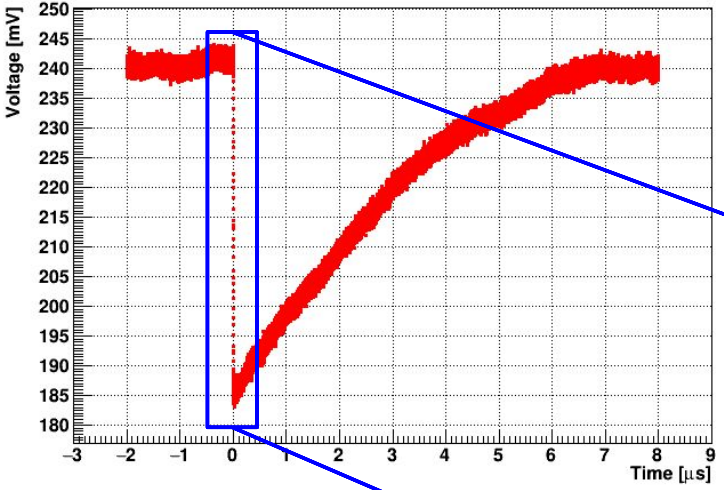


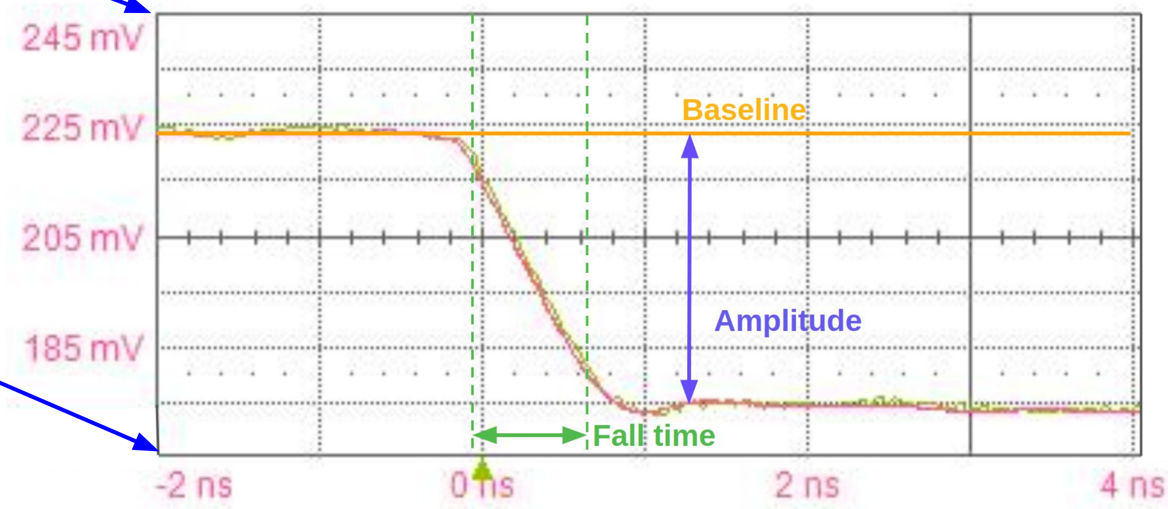
APTS-SF - ^{55}Fe Results



APTS-OPAMP - Signal Parameters

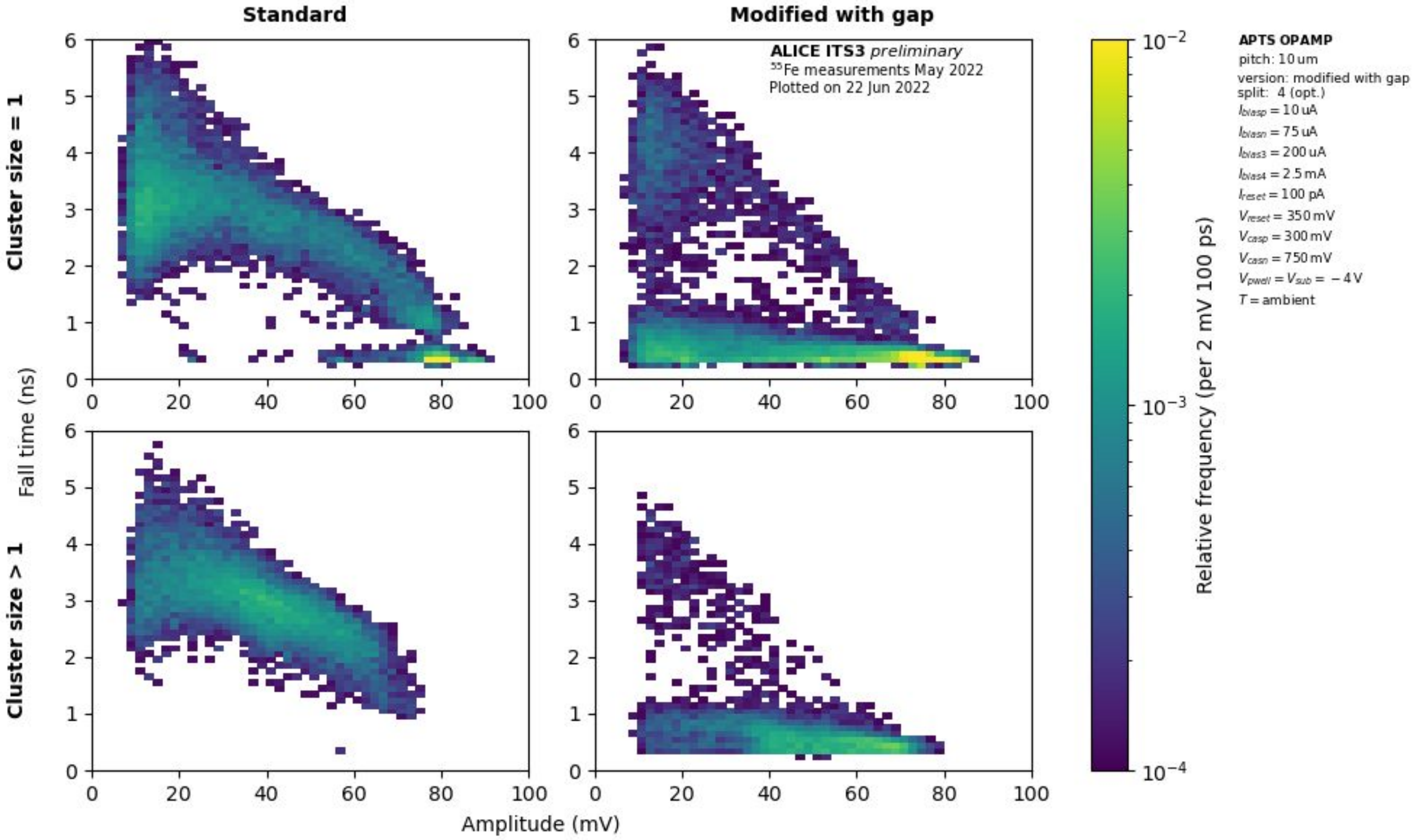
- **Baseline:** reference voltage level
- **Amplitude:** difference between the baseline and the minimum voltage reached by the signal
- **Fall Time:** time difference between 10% and 90% of signal amplitude



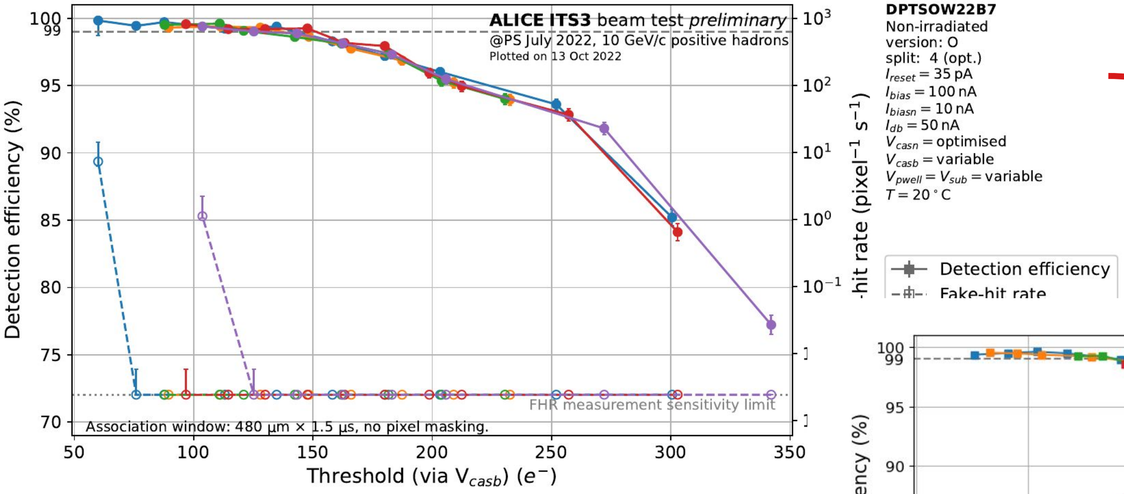


APTS-OPAMP - ^{55}Fe Results

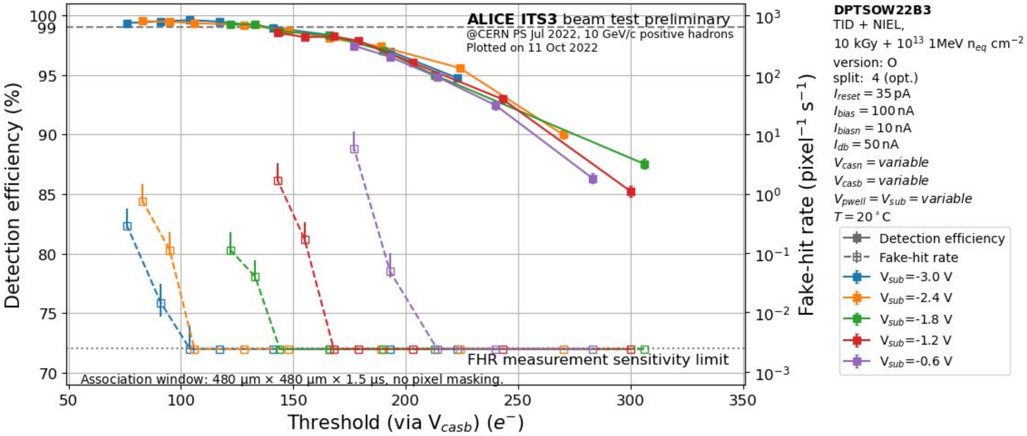
Fast readout allows to estimate the charge collection time via signal fall time



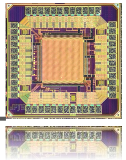
DPTS - Test Beam Results

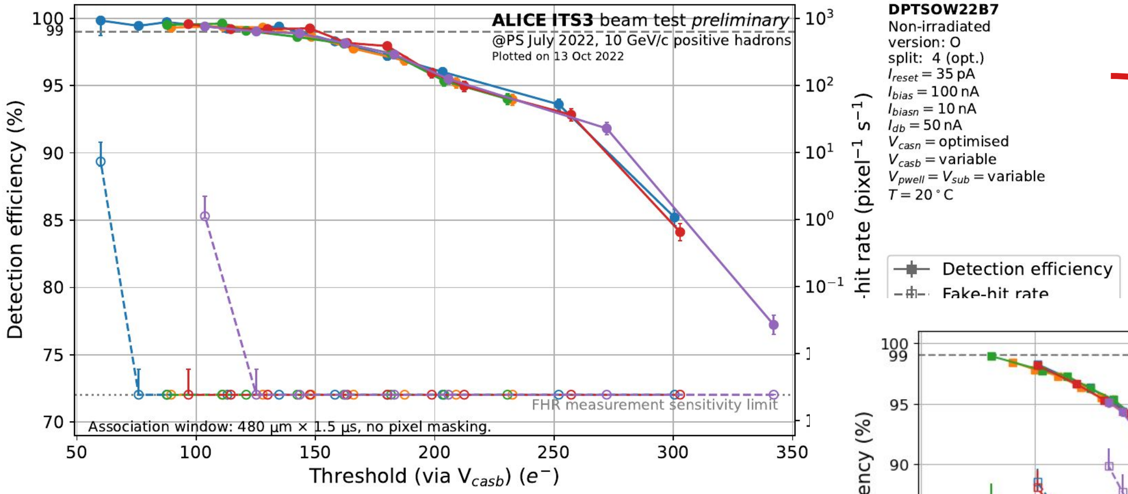


After Irradiation:
TID (10 kGy) + NIEL (10^{13} 1MeV n_{eq} cm^{-2})

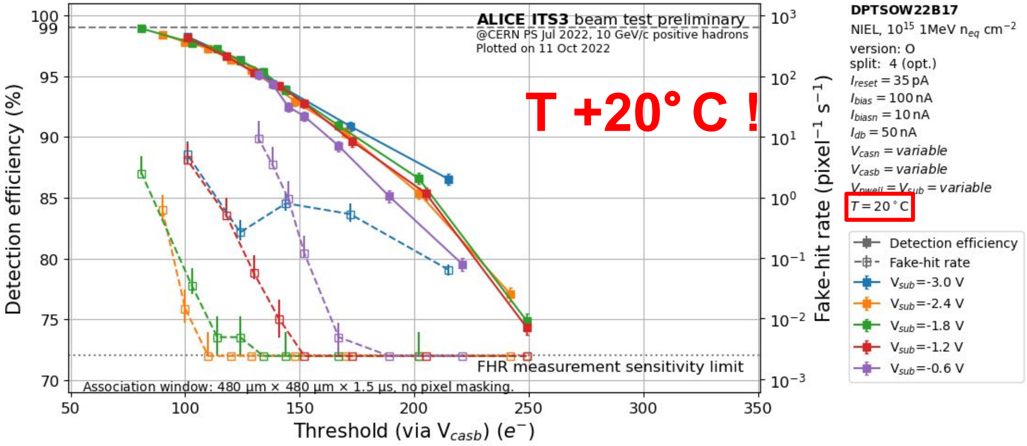


DPTS - Test Beam Results



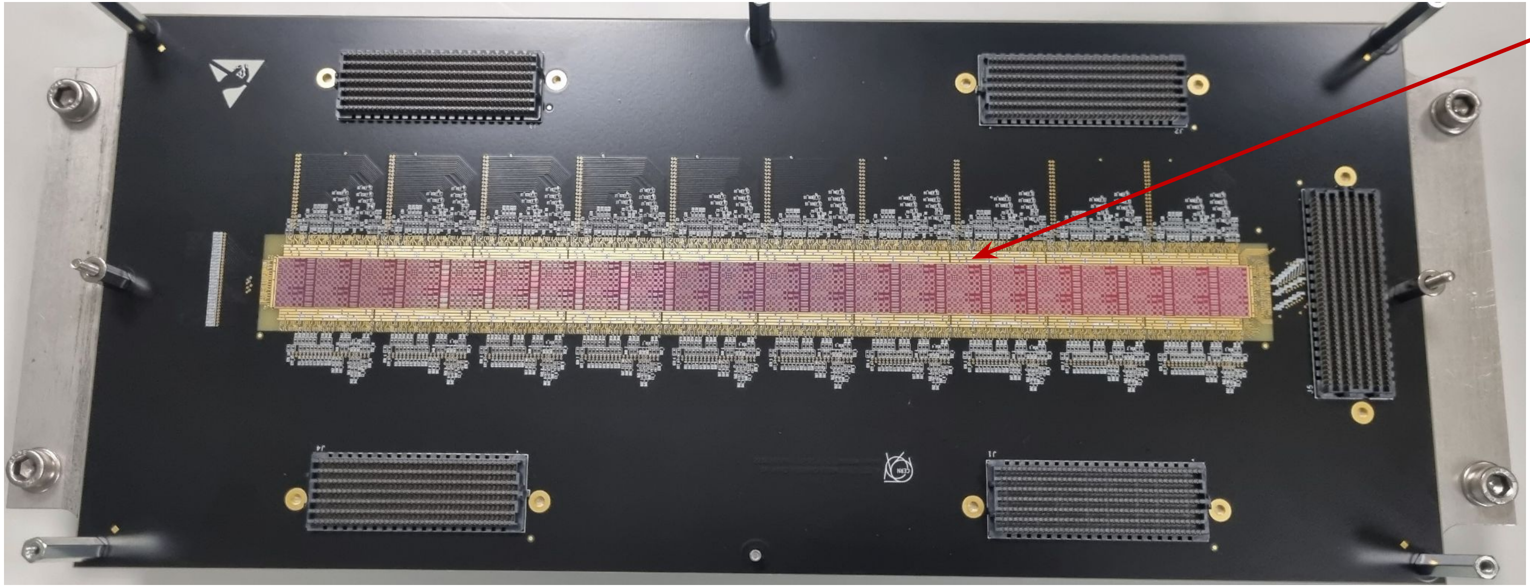


After Irradiation:
NIEL (10^{15} 1MeV $n_{eq}cm^{-2}$)



Next Steps

- Submitted the first stitched sensors
- the setup for testing is being prepared



wafer-scale dummy sensor

Conclusions

- ITS3 replaces the 3 innermost layers of ALICE ITS2 by a bent, wafer scale MAPS detector which reduces material budget by factor of 7 compared to ITS2
- The TPSCo 65 nm technology is chosen and is being characterized
- results on small scale prototypes are promising and meet the requirements of ITS3 and beyond
- stitched sensors will be ready for testing in spring
- TDR under preparation

ALICE

Thank you!

Back-up Slides

CE65 - Test Beam Results

All submatrices in standard and modified processes collect the same total charge