MightyPix: A HV-CMOS Pixel Chip for LHCb's Mighty Tracker

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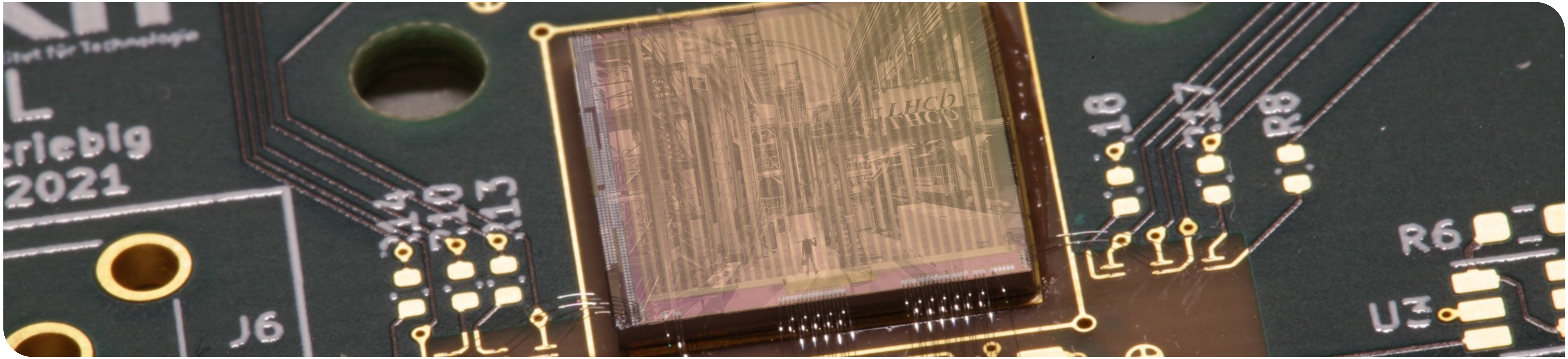
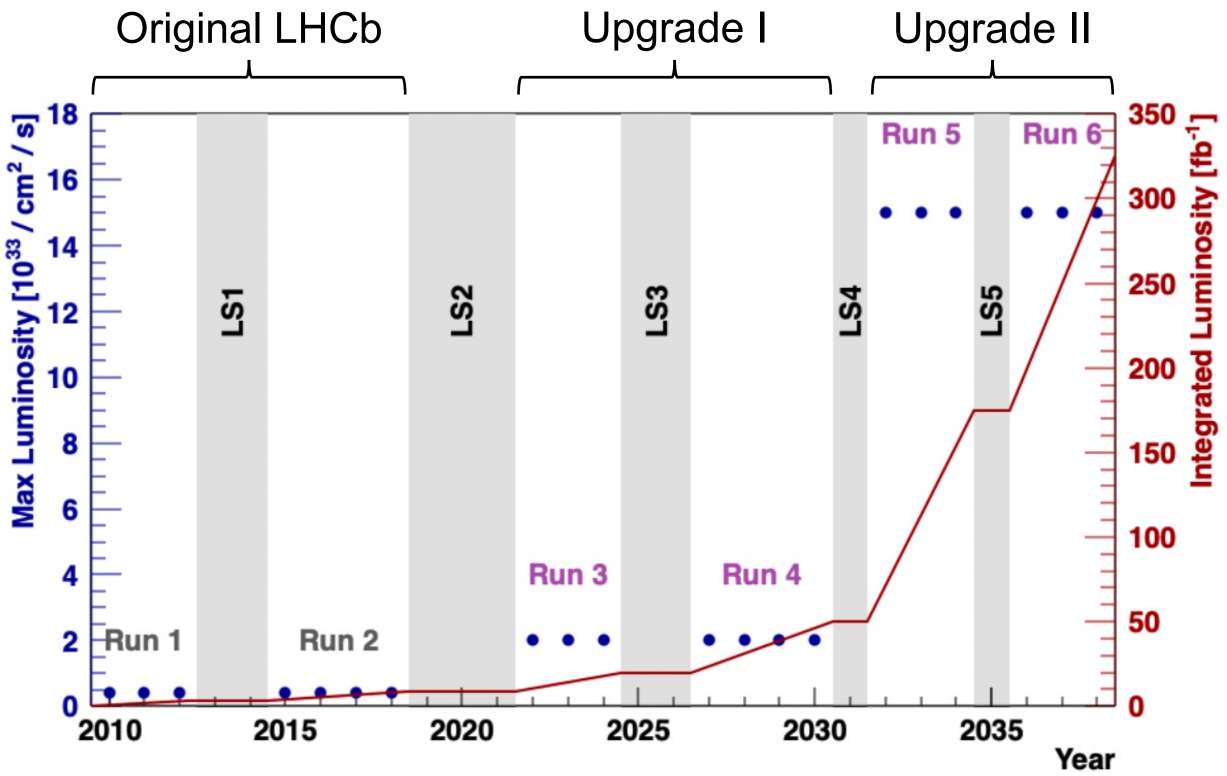


LHCb at the HL-LHC

- Upgrade towards High-Luminosity LHC
- Luminosities[1] for LHCb:
  - Upgrade I: $\mathcal{L}_{\max} = 2 \times 10^{33} \mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - Upgrade II: $\mathcal{L}_{\max} = 1.5 \times 10^{34} \mathrm{cm}^{-2}\mathrm{s}^{-1}$
  - Leading to at least $\int \mathcal{L} = 300\ \mathrm{fb}^{-1}$ of collected data[2]
- Increased readout speed of 40 MHz bunch-crossing (BX) rate
- New software-only trigger

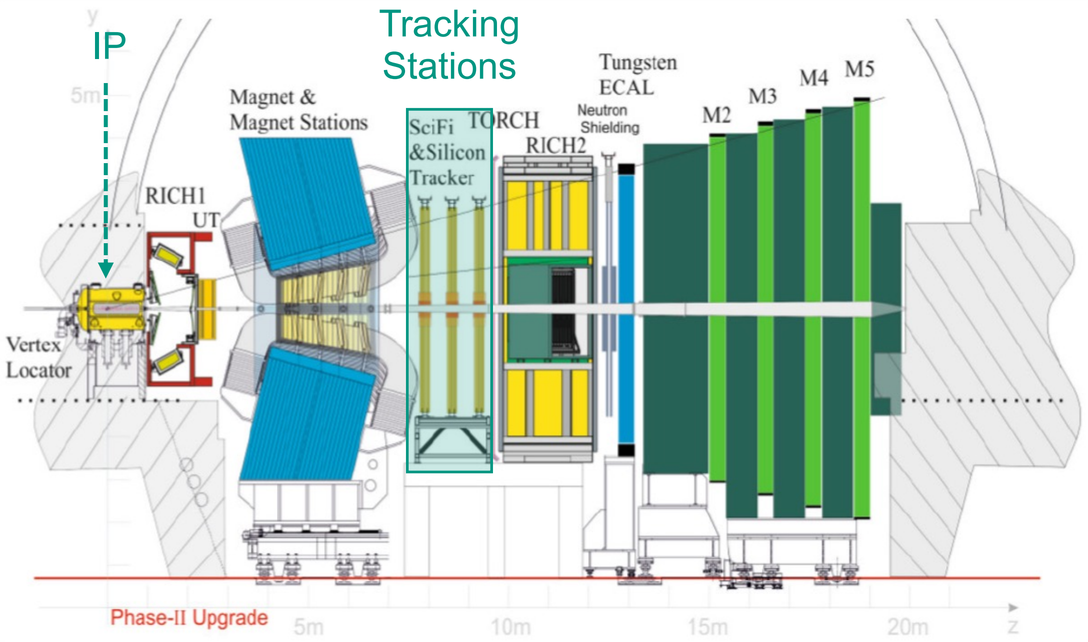


Luminosity profile for the LHCb detector. [1]

[1] Luminosity = detected events per area and time
[2] $1\ \mathrm{fb}^{-1} = 10^{-28}\ \mathrm{m}^2$ ($100\ \mathrm{fm}^2$)

Upgraded LHCb Detector

- Proposed hybrid tracker **Mighty Tracker**
- Composed of…
  - SciFi Tracker
  - Inner Tracker
  - Middle Tracker



Schematic side view of the Upgrade II LHCb detector. [1]

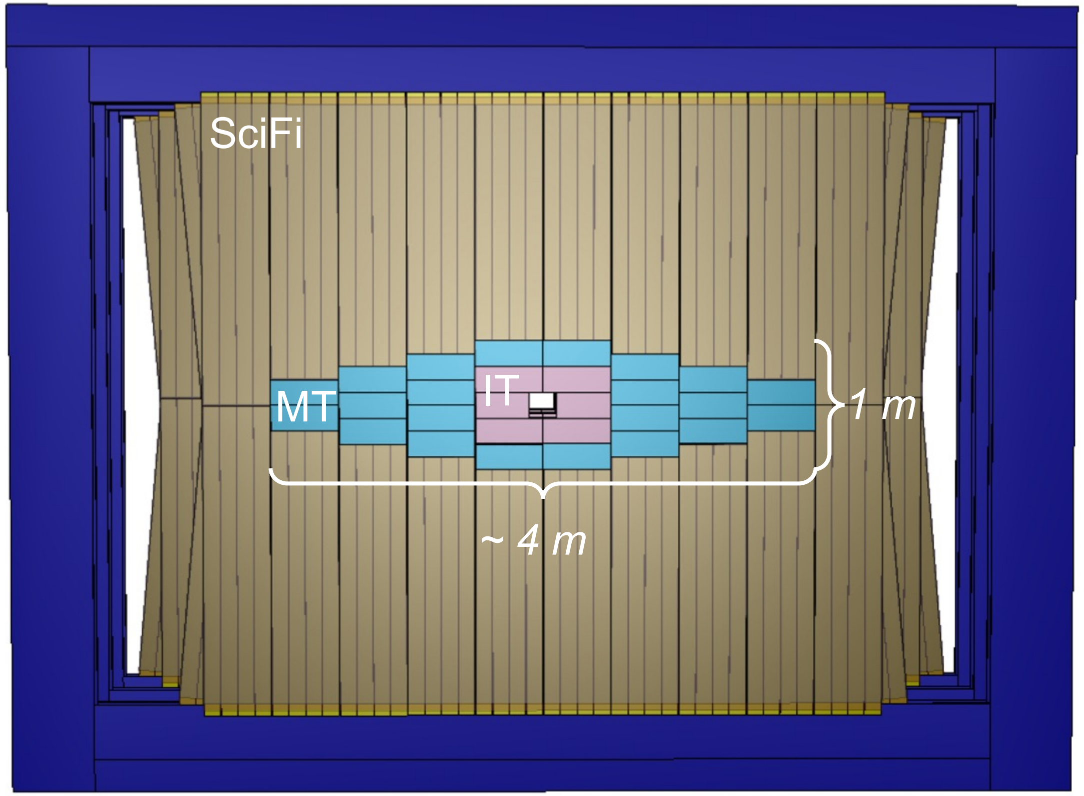
Schedule from January 2022. [2]

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
LS2	**Run 3**				**LS3** (Long Shutdown 3)			**Run 4**				**LS4**	

- LS2: Installation of SciFi
- LS3: Replacements for SciFi, Installation of Inner Tracker
- LS4: Installation of Middle Tracker

Mighty Tracker

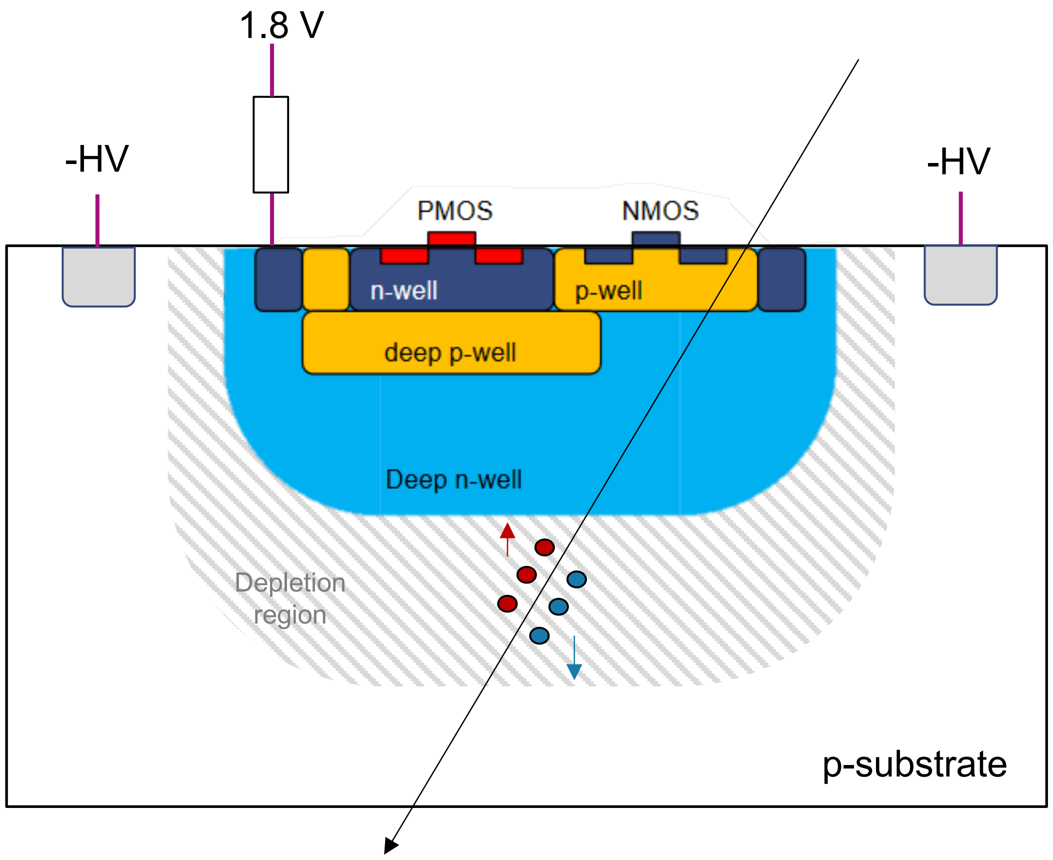
- SciFi Tracker
  - Scintillating fibres with SiPM readout
- Inner Tracker and Middle Tracker
  - Silicon sensors meet requirements of radiation hardness and granularity
  - Baseline technology:
    HV-CMOS pixel chip **MightyPix**
  - In total over 46000 silicon sensors to cover area of 18 m^2 (minus beam-pipe hole)



Schematic of one layer of the Mighty Tracker. [1]

HV-CMOS

- Sensing element and readout circuit on same chip
- n-well/p-substrate diode acts as sensor
- Readout electronics isolated from high voltage by deep n-well
- High reverse bias creates thick depletion region between deep n-well and p-substrate
- Photons and ionising particles create electron/hole pairs, collected via drift



Working principle of HV-CMOS sensors.

MightyPix

Karlsruhe Institute of Technology

- Based on knowledge from ATLASPix[1] and MuPix[2]
- Final design parameters and requirements:

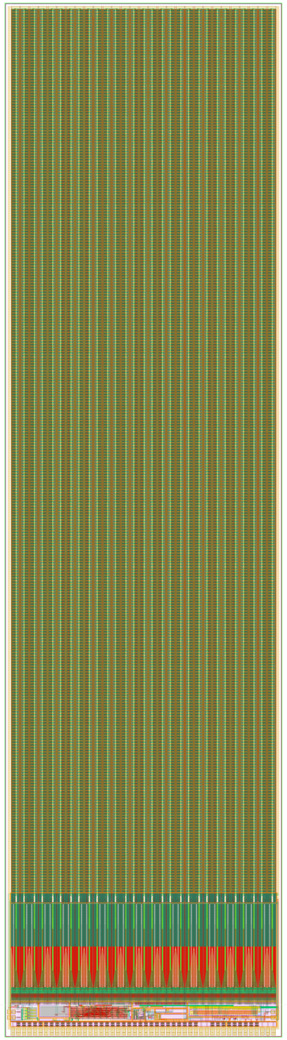
Parameter	Required Value	Notes
Chip size	$\sim 2\ \mathrm{cm} \times 2\ \mathrm{cm}$	
Pixel size	$\sim 50\ \mu\mathrm{m} \times 150\ \mu\mathrm{m}$	
Time resolution	$< 3\ \mathrm{ns}$	Hit assigned to right BX
Power consumption	$< 0.15\ \mathrm{W/cm^2}$	
NIEL[3]	$6 \times 10^{14}\ 1\ \mathrm{MeV}\ \mathrm{n_{eq}/cm^2}$	Includes safety factor of 2
Cooling	$< 0°\mathrm{C}$	Test beam studies

- First prototype: **MightyPix1**

[1] HV-CMOS pixel chip for the ATLAS experiment at CERN
[2] HV-CMOS pixel chip for the Mu3e experiment at PSI
[3] Non Ionising Energy Loss

MightyPix1: Overview

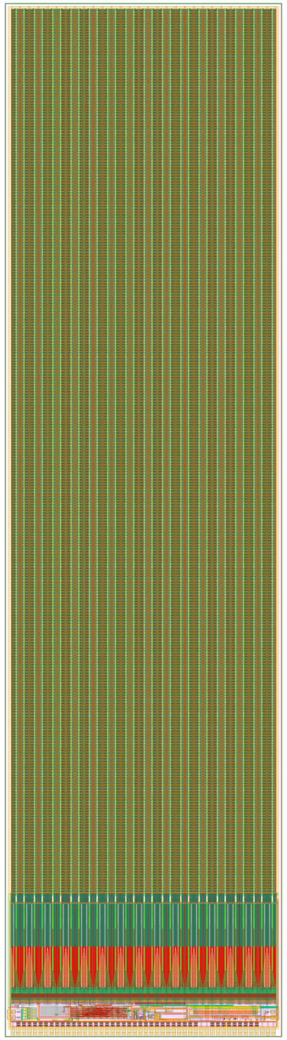
- Implemented in TSI 180 nm process
- Submitted in May 2022
- Chip size: ~ 2 cm × 0.5 cm → full column length, ¼ width
- Pixel matrix: 29 columns, 320 rows
- Pixel:
  - 165 µm × 55 µm
  - CMOS amplifier and CMOS comparator
- Data format: 2 × 32 bit words per hit
- Data output rate: 1.28 Gbit/s going to lpGBT



The first prototype: MightyPix1

MightyPix1: Overview

- Digital interfaces:
  - Timing and Fast Control (TFC)
  - Slow Control (I2C)
  - Configuration shift register (SR) interface
- Clock generation:
  - External: 40 MHz and 640 MHz coming from lpGBT
  - Internal: CML and CMOS PLL with 40 MHz reference clock
- Bias voltages:
  - Integrated 10 bit voltage DACs
  - Can be supplied externally

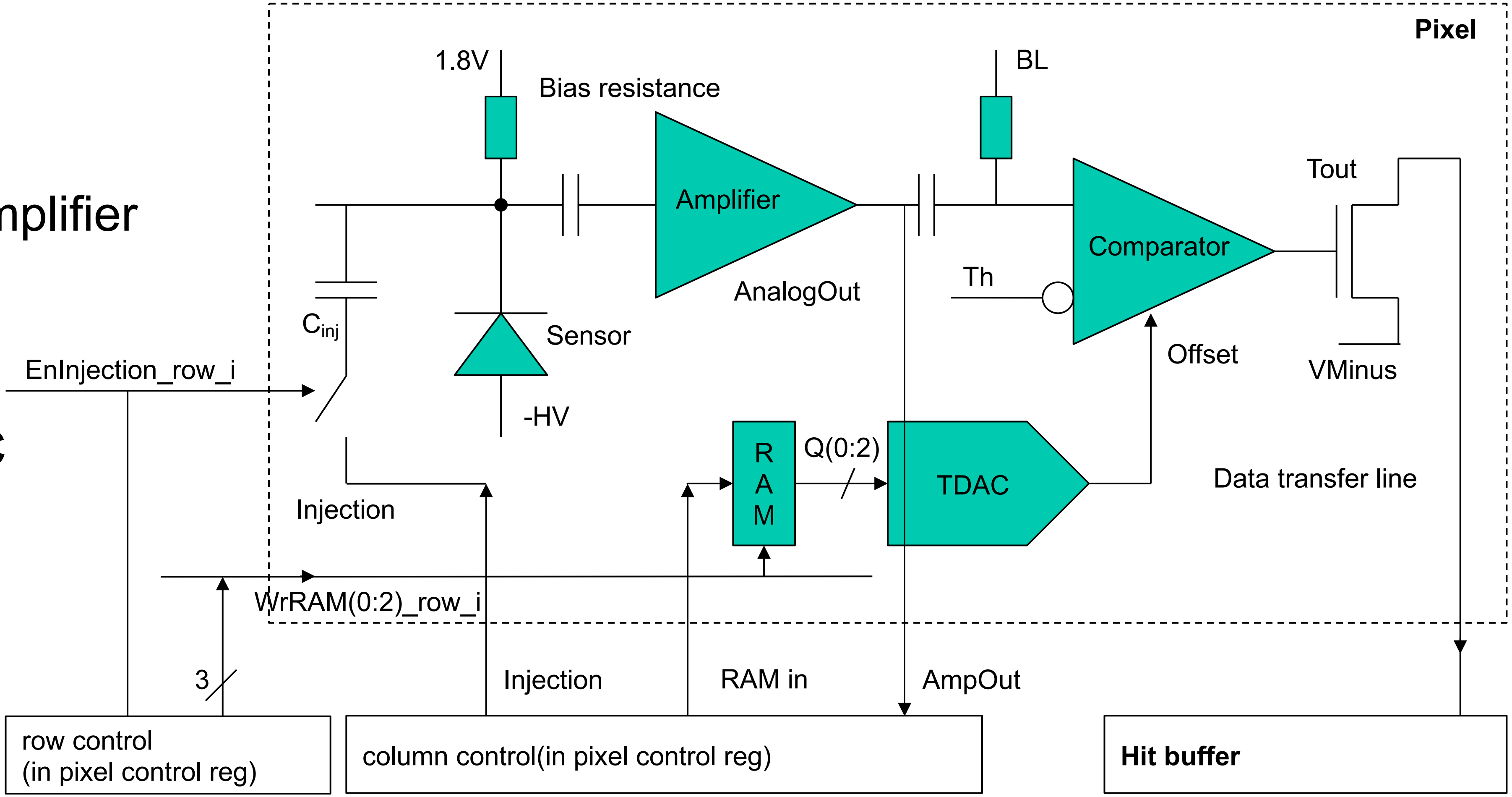


The first prototype: MightyPix1

MightyPix1: Analogue Part

Pixel contains:

- Sensor diode
- Charge Sensitive Amplifier (CSA)
- Comparator
- Threshold tune DAC
- RAM for tune bits

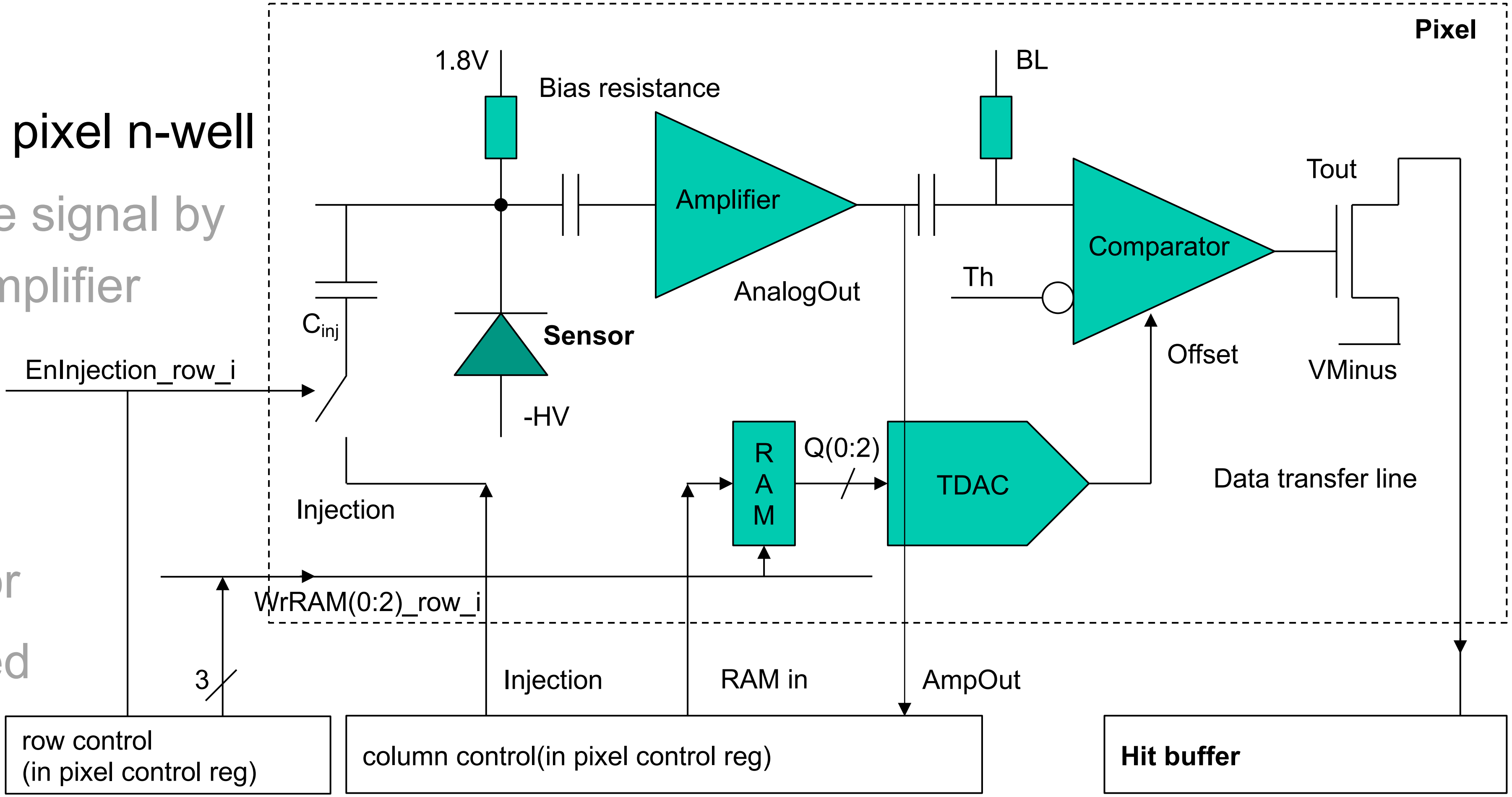


Source: Ivan Perić

MightyPix1: Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer



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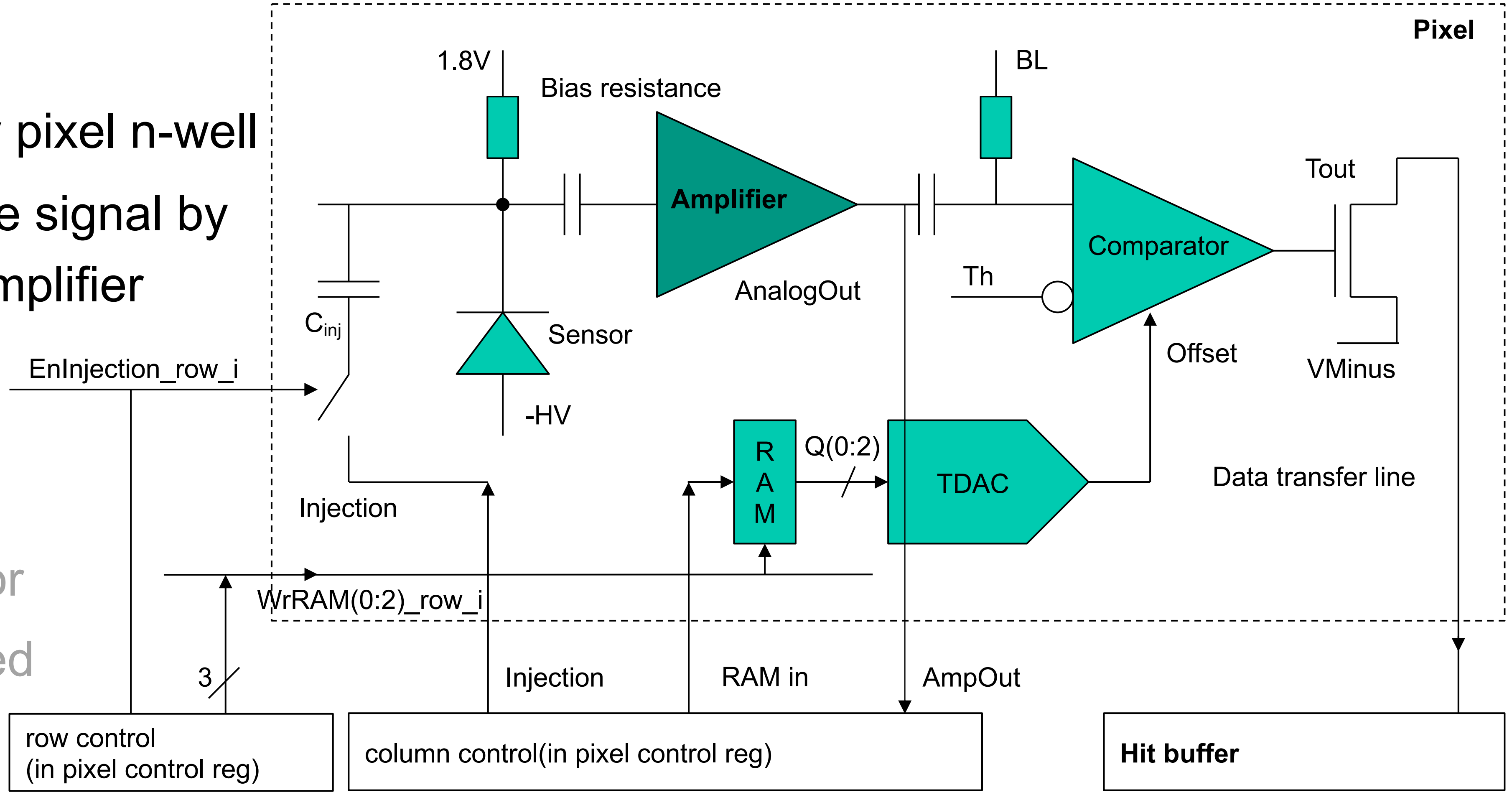

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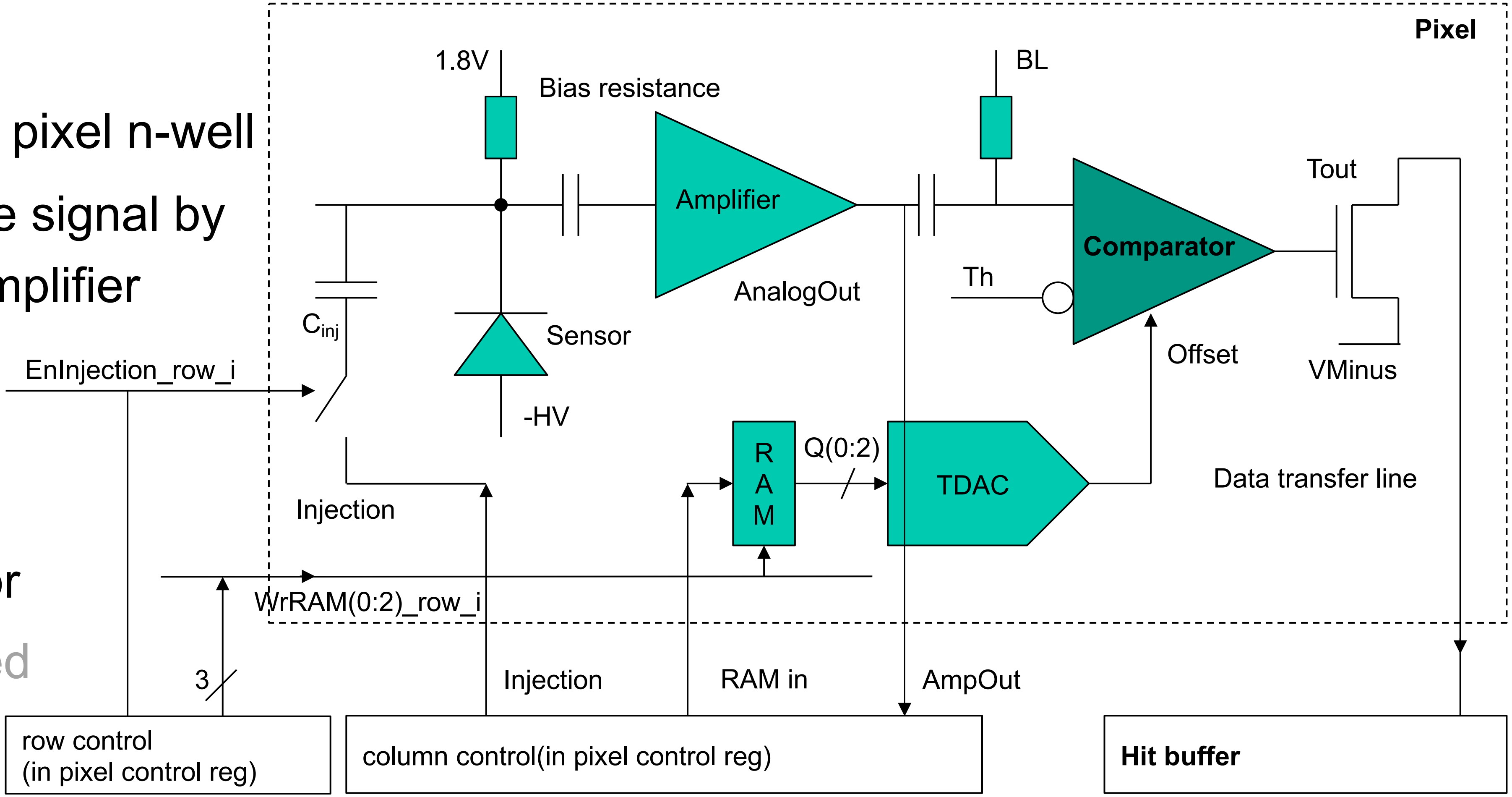

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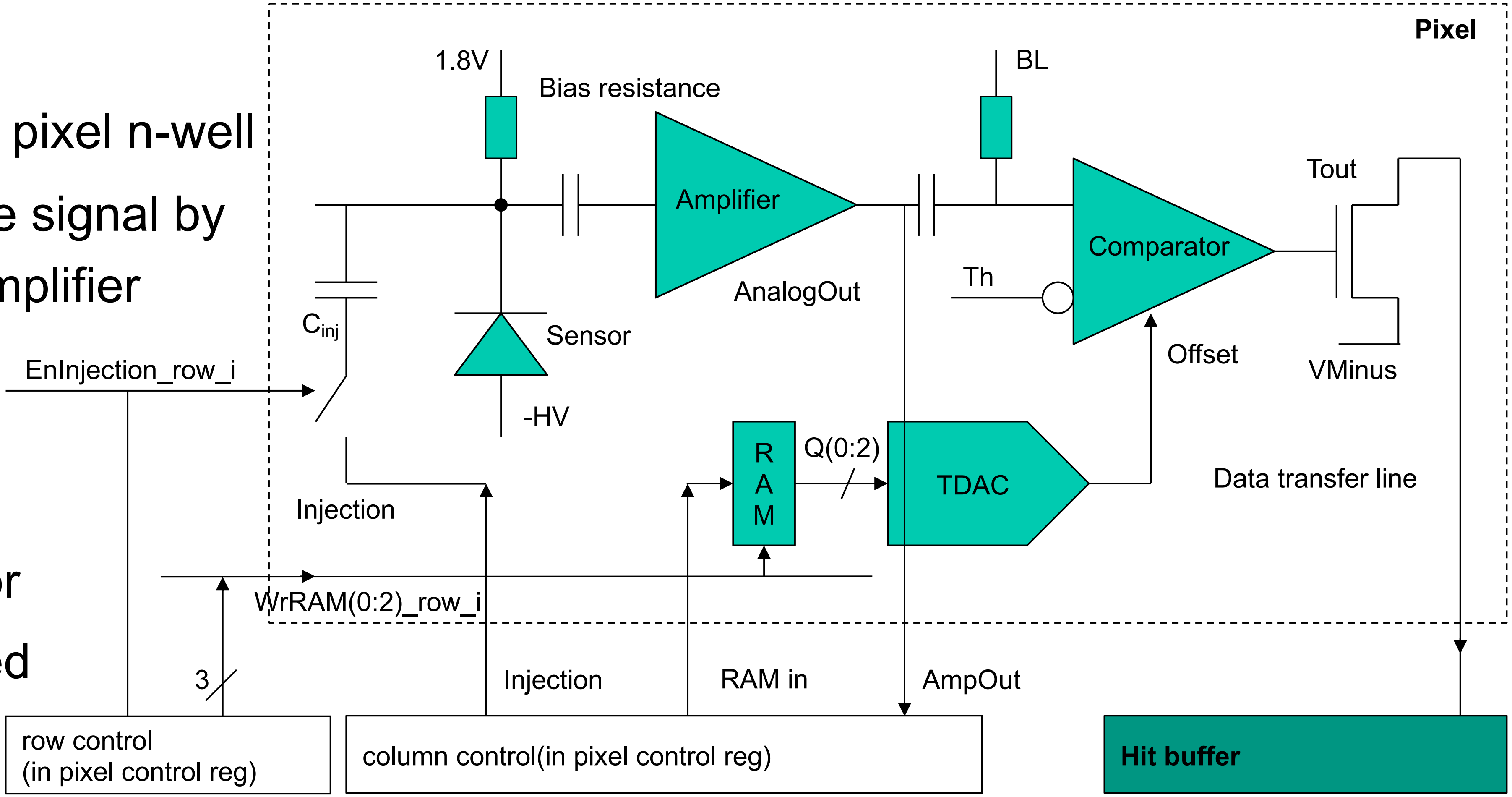
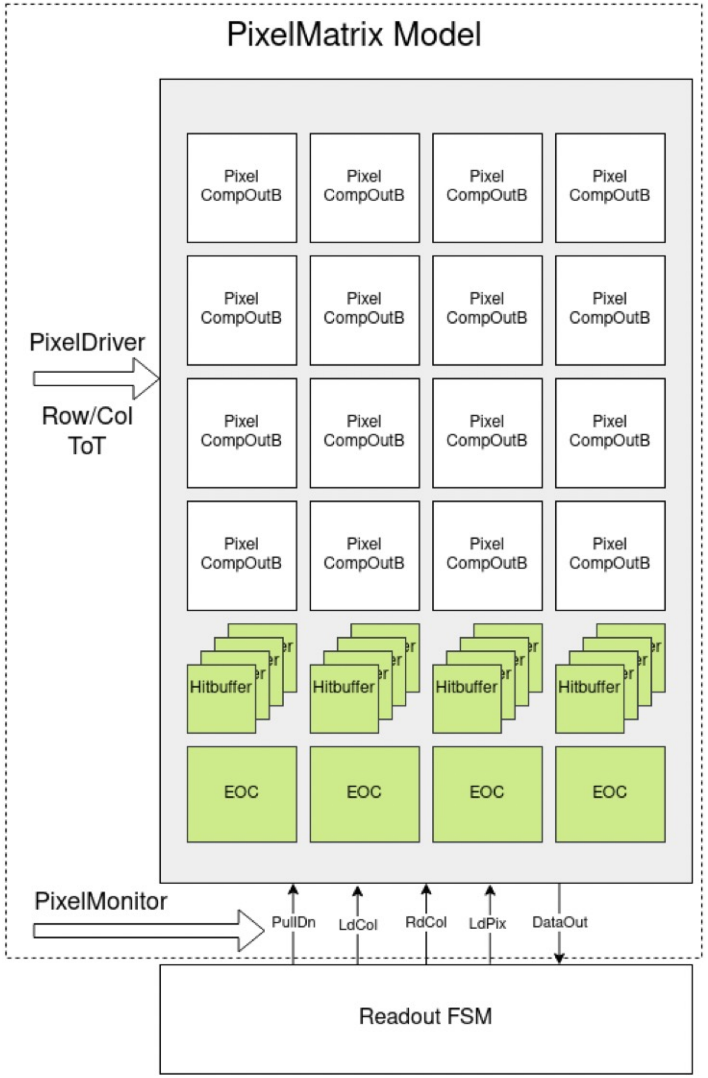


Source: Ivan Perić

MightyPix1: Digital Readout

- Readout Control Unit (RCU) FSM
- Working principle:
  - Data busses discharged
  - Data loaded from highest active hit buffer to EoC buffer, go on to next one
  - Read data from EoC
  - For every hit 2 × 32 bit data words
  - Parallel scrambler analogue to VELOPix
  - Data sent into serializer tree and sent out



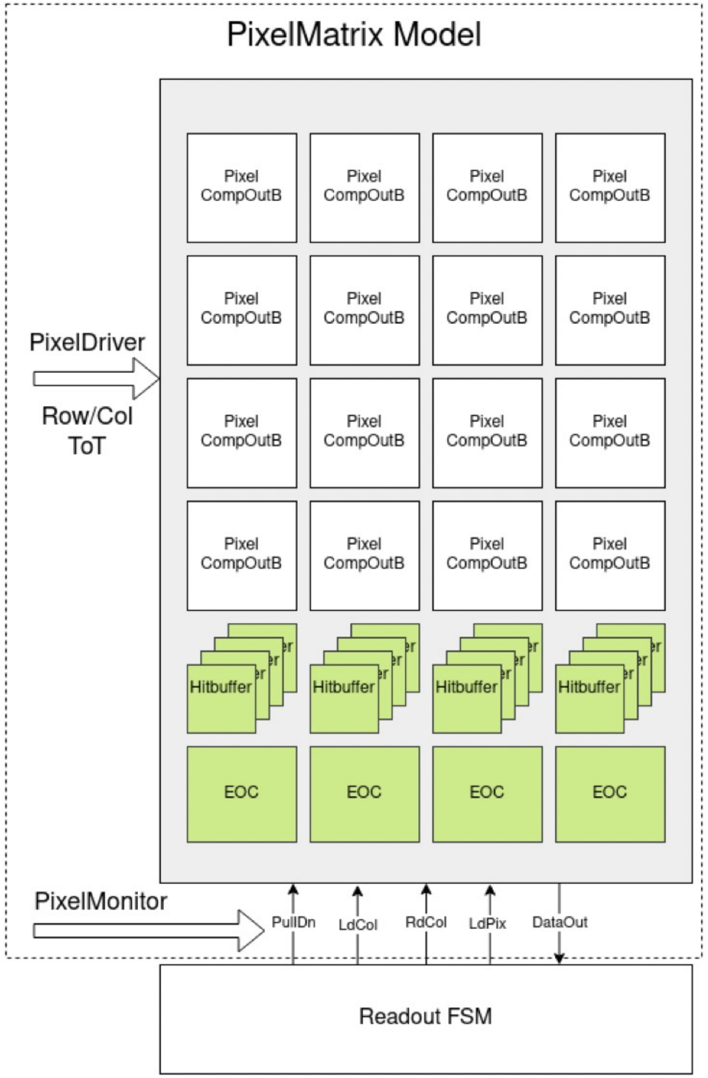
Source: Nicolas Striebig

MightyPix1: Efficiency Simulation

Can MightyPix handle the hit rate at LHCb?

- Detector performance quantified by efficiency
  → Ratio of detected to total events
- Maximum expected rate at Mighty Tracker ~ 17 MHz/cm^2
- Additionally 5% of clusters where two pixels are hit

- Parametrizable model of pixel matrix
  - Send simulation data to model
  - Comparison of input data with data seen at RCU
  - Check if model correctly detects all hits that are sent in



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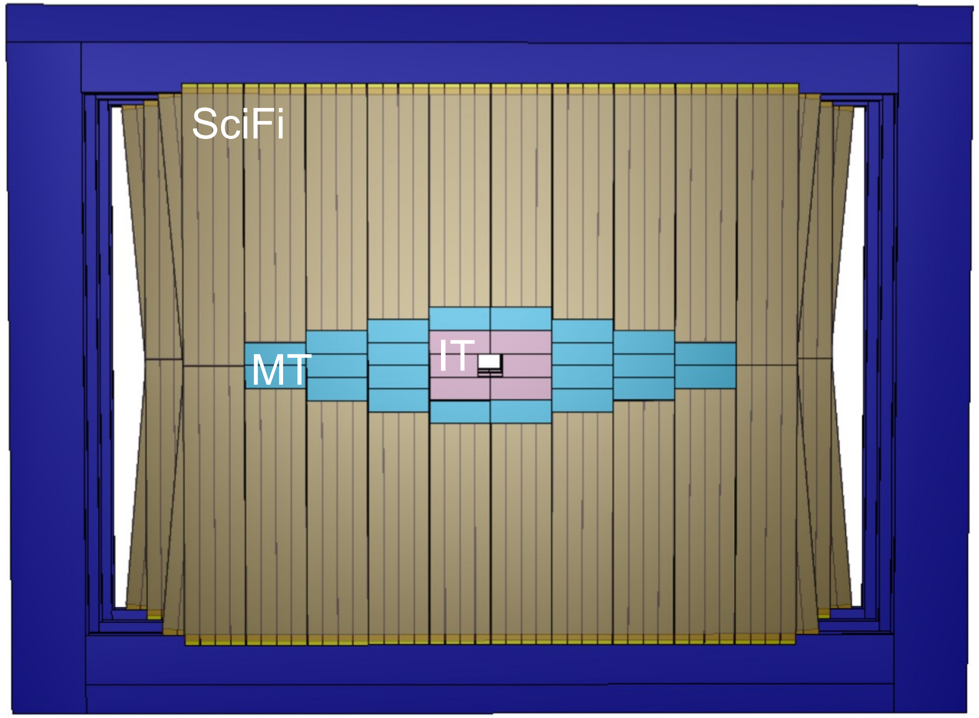
MightyPix1: Efficiency Simulation

- Data from *Occupancy studies for the LHCb Run4 Mighty Tracker [3]*, by T. Hume, V. Bellee, O. Steinkamp



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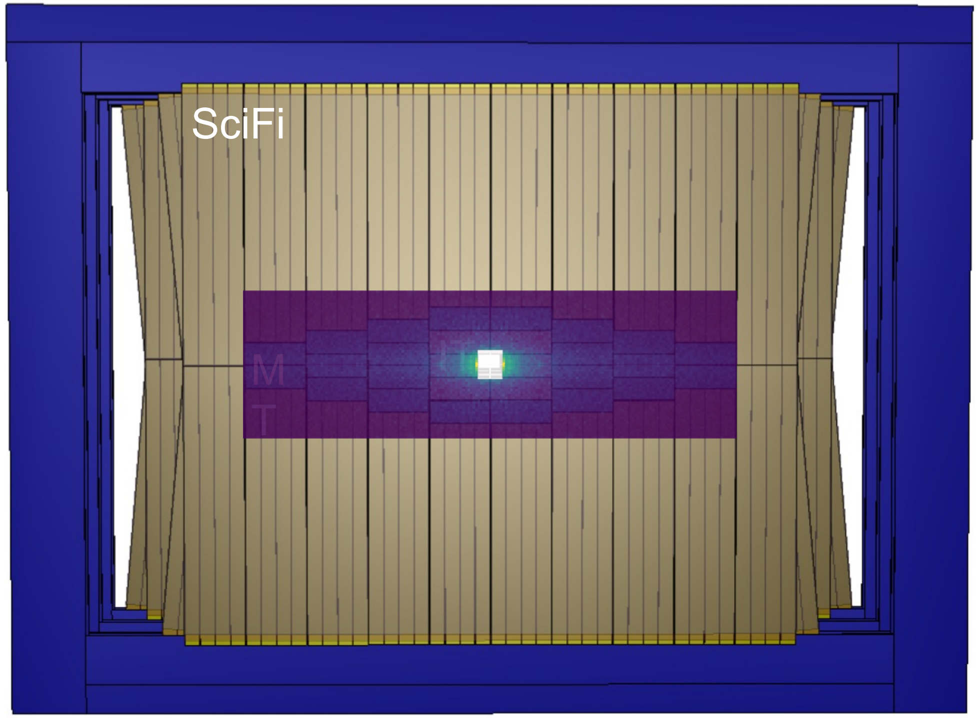

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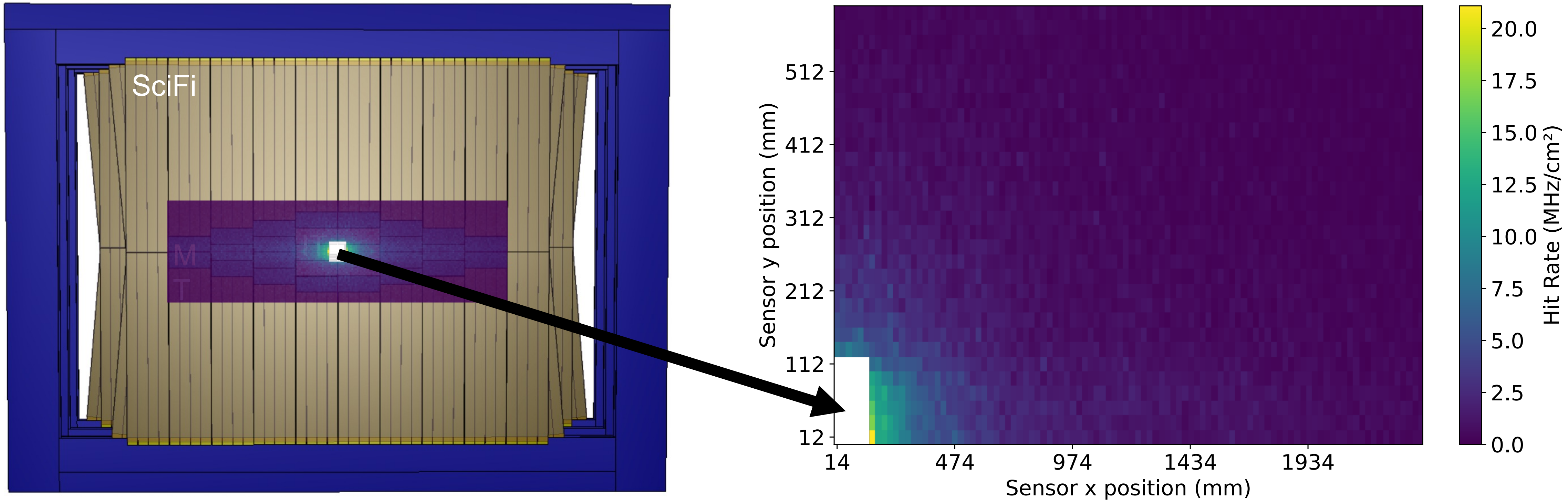
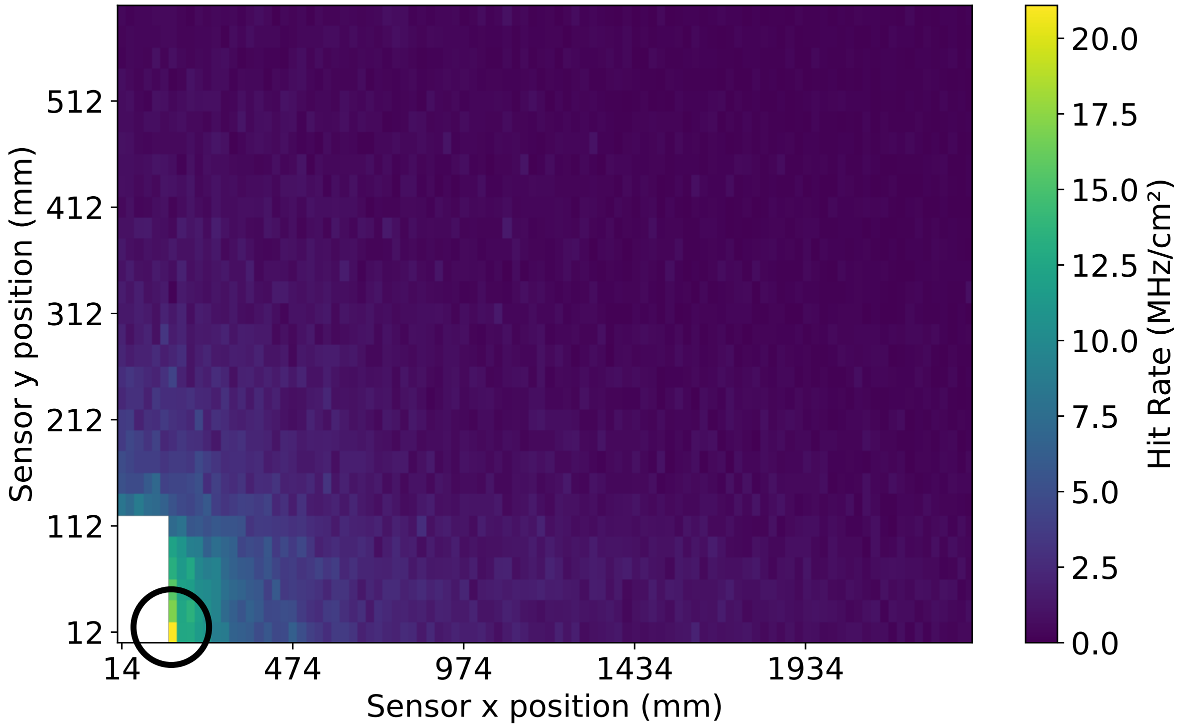


MightyPix1: Efficiency Simulation

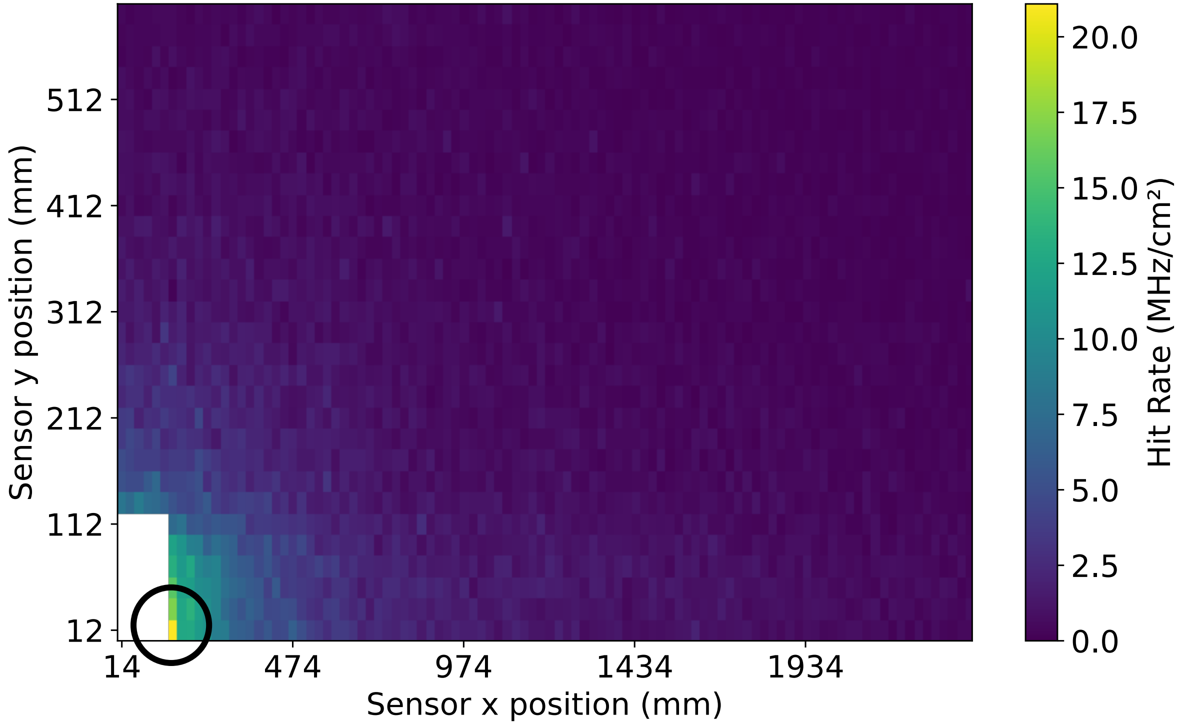
- Data from *Occupancy studies for the LHCb Run4 Mighty Tracker [3]*, by T. Hume, V. Bellee, O. Steinkamp
- Focus on “hottest” sensor



MightyPix1: Efficiency Simulation

- Data from *Occupancy studies for the LHCb Run4 Mighty Tracker [3]*, by T. Hume, V. Bellee, O. Steinkamp
- Focus on “hottest” sensor

Hottest Sensor	
Hit Rate	*Max.*
ToT	*2 us*
Clusters	*No*
Total Hits	*1183*
Missing Hits	*9*
Efficiency	*99.24%*



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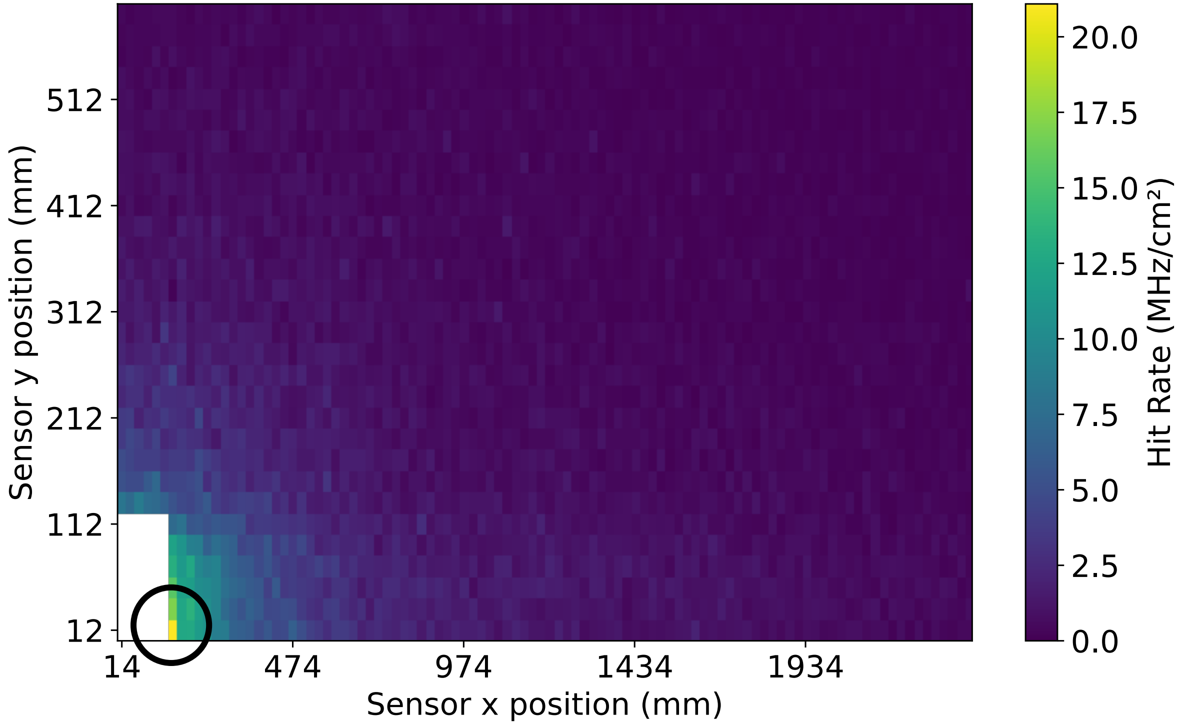
- Focus on “hottest” sensor

Hottest Sensor		
Hit Rate	*Max.*	
ToT	*2 us*	
Clusters	*No*	*5%*
Total Hits	*1183*	*1242*
Missing Hits	*9*	*9*
Efficiency	*99.24%*	*99.28%*



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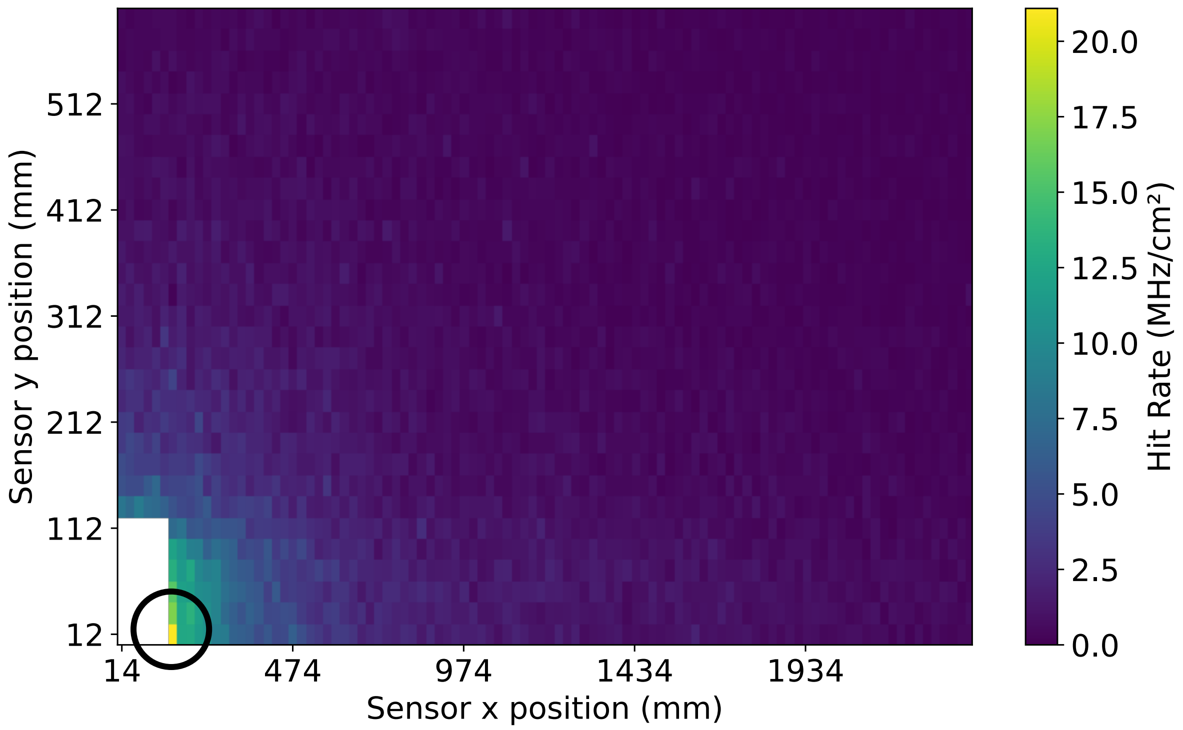
- Focus on "hottest" sensor

Hottest Sensor			
Hit Rate	*Max.*		
ToT	*2 us*		*5 us*
Clusters	*No*	*5%*	*No*
Total Hits	*1183*	*1242*	*1183*
Missing Hits	*9*	*9*	*14*
Efficiency	*99.24%*	*99.28%*	*98.82%*



Summary

- Proposed new tracker for LHCb: **Mighty Tracker**
  - → To be instrumented with 18 m^2 of silicon sensors
- First prototype **MightyPix1**
  - → Submitted in May 2022
  - → Compatible with LHCb readout
- Efficiency simulations
  - → MightyPix1 is able to handle highest expected hit rates
  - → Further studies to inform decisions on electronics

References

[1] CERN/LHCC 2021-012
(*https://cds.cern.ch/record/2776420*)

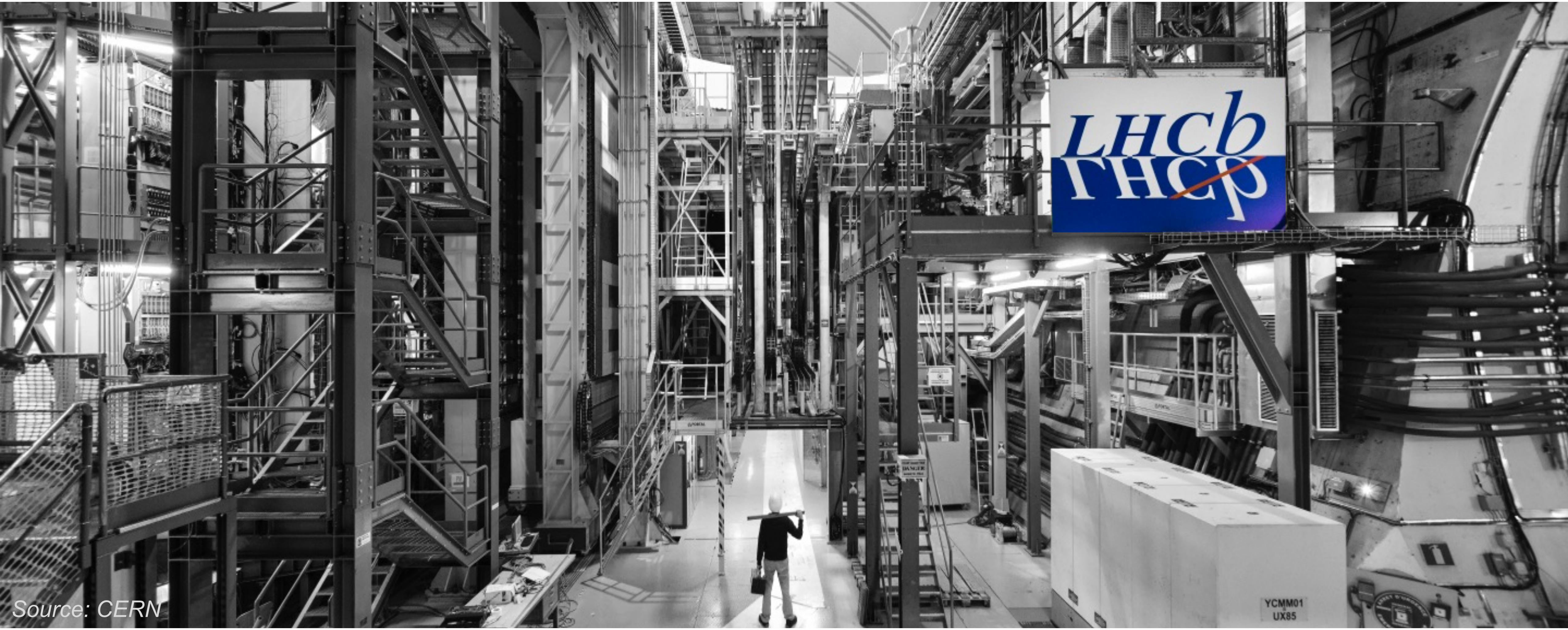
[2] https://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm
(*Accessed 23/9/2022*)

[3] CERN-LHCb-PUB-2022-003
(*https://cds.cern.ch/record/2800986?ln=en, publication pending*)

[4] H. Augustin et al. *The MuPix sensor for the Mu3e experiment.* Nucl. Instrum. Meth. A, 979:164441, 2020.

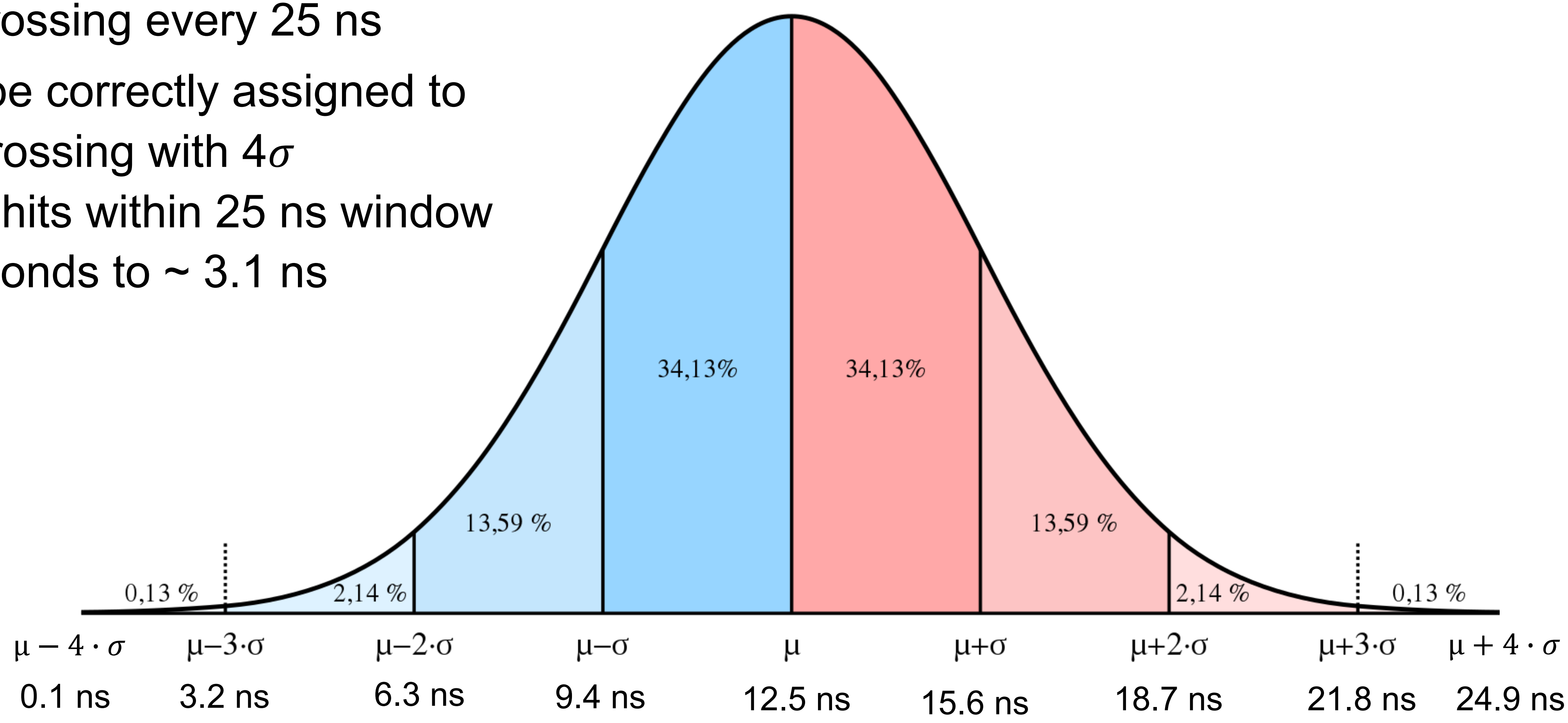
[5] https://commons.wikimedia.org/wiki/File:Normal_Distribution_Sigma.svg

Backup



Why do we need a time resolution of < 3 ns?

- One bunch crossing every 25 ns
- Hits need to be correctly assigned to right bunch crossing with 4σ
  → 99.99% of hits within 25 ns window
  → 1σ corresponds to ~ 3.1 ns



Normal distribution. [5]

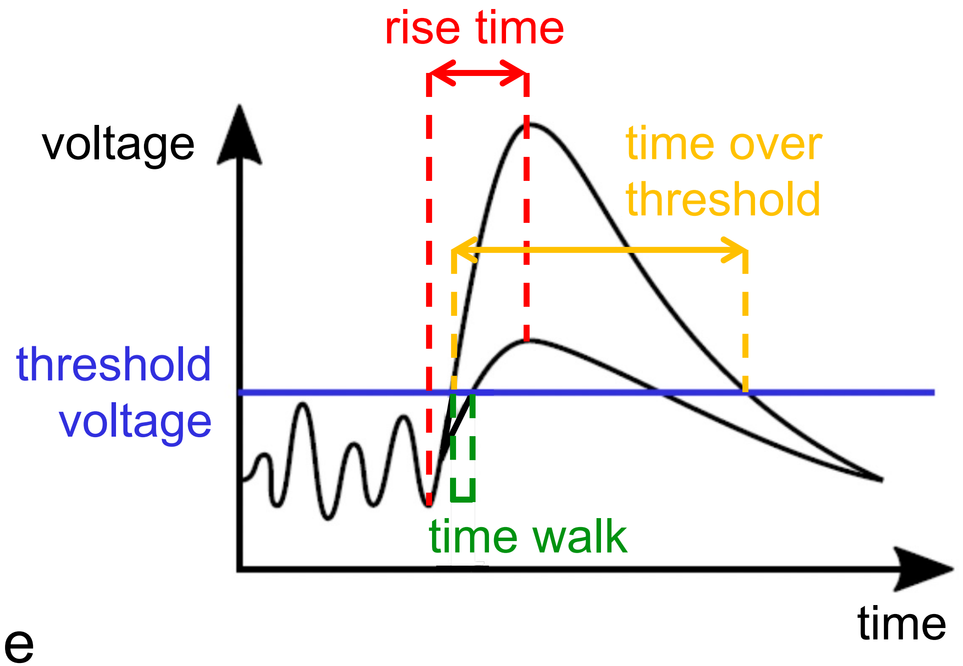
MightyPix1: TFC Signals

- LHCb sends Timing and Fast Control (TFC) signals to all FE modules

- **BXReset:** Reset internal BXcounter to synchronise chips to same BX
- **Snapshot:** Capture number of received TFC commands *(partially implem.)*
- **FEReset:** Reset all modules except for TFC receiver, BXcounter and chip configuration registers
- **Cal:** Could be used to control an on-chip injection circuit *(not yet implem.)*
- **Sync:** Chip outputs sync pattern, configurable via configuration register

MightyPix1: Time Walk and ToT

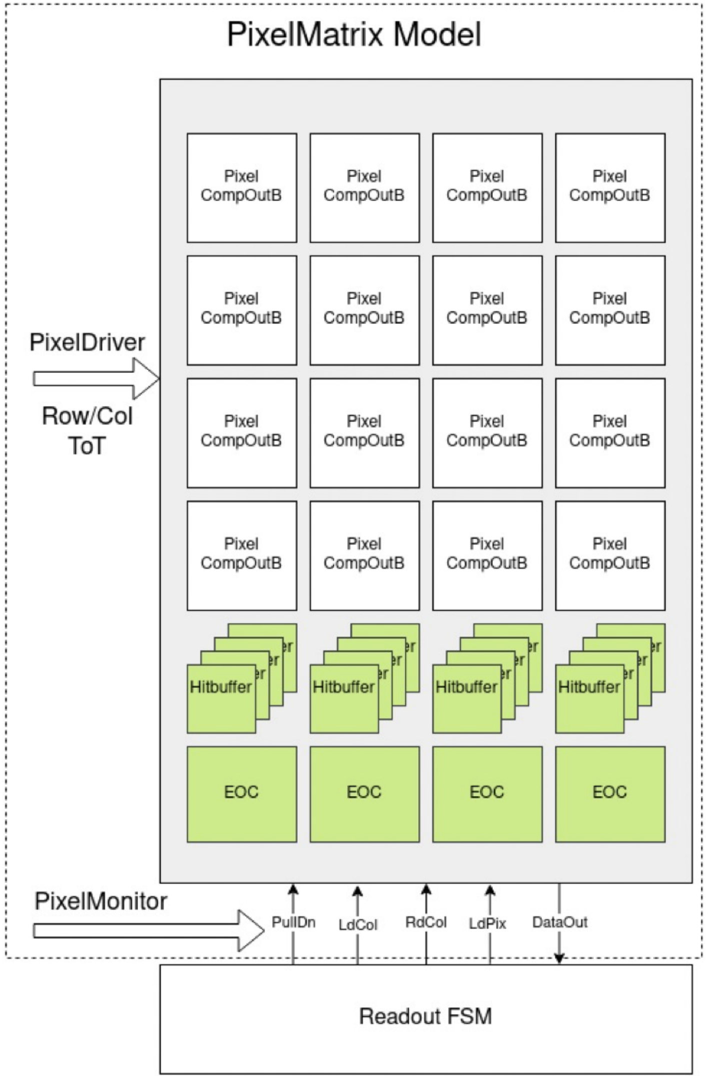
- **Time walk:**
  - Rise time same for all signals
  - Difference in time at which threshold is crossed is called time walk
  - Time walk ~ 2.5 ns for signals of 2500 e^- and 25000 e^-
- **Time over Threshold:**
  - 1.5 µs to 2 µs
  - Simulations show impact of resulting dead time negligible (*See slides on Efficiency Simulation)*



Schematic description of time walk, rise time, and time over threshold. Adapted from [4].

MightyPix1: Efficiency Simulation

- ***Why do hits go missing?***
  - Each pixel has one hit buffer
  - Columns scanned left to right
  - Hit info loaded to EoC for each hit buffer
  - Lower rows have priority
  - If readout takes too long and next hit already occurs before readout it will be missed



Source: Nicolas Striebig

MightyPix1: Efficiency Simulation

Readout Speed	40 MHz				160 MHz	
Clusters	*No*	*No*	*Yes*	*Yes*	*No*	*No*
Hit Rate	*Expected*[1]	*Twice exp.*[2]	*Expected*[1]	*Twice exp.*[2]	*Expected*[1]	*Twice exp.*[2]
Simulated Hits	1166 *100%*	2322 *100%*	1223 *100%*	2437 *100%*	1166 *100%*	2322 *100%*
Missing Hits	9 *0.77%*	105 *4.52%*	9 *0.74%*	122 *5.01%*	7 *0.60%*	16 *0.69%*

[1]Expected hit rate: 1.7 hits per 25 ns and 2 cm x 2 cm chip
[2]Twice the expected hit rate: 3.4 hits per 25 ns and 2 cm x 2 cm chip