Characterization of a digital SiPM in 150 nm CMOS Imaging Technology

First Characterization & Results

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Overview

dSiPM ongoing studies





Sensor & DAQ

- DESY dSiPM Specifications
- Pixel Design & Readout
- DAQ Chain



Laboratory Characterization

- IV Curves & Dark Count Rate
- Quenching & Pixel Masking





Test Beam studies

- DESY-II TB Setup
- First Results

Introduction

What is a Silicon PhotoMultiplier

- Solid state single photon detectors
- Array of Single Photon Avalanche Diodes (SPADs) with pitches in the range 10-100 µm
- **High Internal Gain (~10⁶)** thanks to High doped amplification region
- Signal **proportional** to the number of photons that hit the sensor
- High quantum efficiency
- Low power consumption
- Insensitive to magnetic fields



Photomultipliers



Schematic structure of SPAD (Fraunhofer IMS)



SiPMs



Typical SiPM design (KETEK)

Introduction

Analog vs Digital SiPMs

Project Goals

- Investigate CMOS SPADs performances & possibilities
- Possible Applications:
 - Optical Fibre Read-Out
 - 4D-Tracking

Why digital?

- Small quenching circuitry
- Inverter as event discriminator
- In-pixel/in-Chip Hit counting
- Masking & Hit map readout

Commercial CMOS processes

- Sensor & electronics in the same Chip
- Direct photon detection (Monolithic: no backside processing)
- Low-cost R&D (Available in Multi Project Wafer)
- High volume production



Schematic representation of the readout chain of an Analog SiPM



Schematic representation of the readout chain of a Digital SiPM

DESY dSiPM Specifications

ASIC in LF 150 nm CMOS

Layout

- In LFoundry 150 nm CMOS Technology
- Main matrix: 32 x 32 pixels
- Sensor area: 2230 x 2430 μm²
- Test structures in the Chip periphery

Features

- Full hit matrix readout and timing measurements
- 4 x 12-bit TDCs with <100 ps timing resolution
- Pixel masking
- 2-bit in-pixel hit counting
- Validation logic whit adjustable settings
- Readout is Frame based (3 MHz frame rate)



ASIC Design of the DESY dSiPM

Pixel Design & Readout

4 SPAD Layout

Pixel Layout & electronics

- 4 SPADs sharing one Frontend and additional readout electronics
- Fill factor ~30% (limited by SPAD dimension available)
- Quenching Transistor (V_{Quench})
- Masking Circuitry
- In-pixel Hit counter

Readout concept

- The ASIC is divided into four identical quadrants (16 x 16 pixel units)
- Outputs of all pixels are combined in a wired-OR
- The fastest pixel signal triggers a running 12-bit TDC
- Validation logic to discard undesirable events
- The Hit matrix is readout via a 16-to-1 multiplexer



Microscope picture of a pixel



Microscope picture of the Chip



Readout concept of a 16-by-16 pixel unit (Quadrant)

DAQ Chain

Caribou System

Junit

Caribou

- Versatile readout system developed by CERN, BNL, DESY and University of Geneva
- Allows fast, simple and Low-cost implementation & tests of sensors
- Already used for: ATLASPix, CLICTD, DPTS, FASTPIX, etc.

SoC Board

- An embedded CPU runs DAQ and control software
- An FPGA runs custom hardware for data handling and detector control

Control and Readout (CaR) Interface Board

- Provides physical interface from the SoC to the detector chip
- Contains all peripherals needed to interface and run the chip: power supplies, ADCs, voltage/current references, LVDS links, etc.

Chip Board

- Passive & detector-specific components only
- DSiPM here glued & bonded
- Enclosed in Aluminum case that acts as heat sink and light shield

http://dx.doi.org/10.22323/1.370.0100 https://gitlab.cern.ch/Caribou/







Chip Board

Chip Glued & Bonded

IV Curves & Dark Count Rate

Chip Characterization

- Detailed characterization performed on several samples
 (Chip4 shown in figures)
- IV & Dark Count Rate studies performed whit controlled temperature (from -25 to 20 °C) and humidity (~ 0 %) in a dark environment
- Measurements compatible with expectations





10

Allows in-depth characterization of SPAD arrays

Quenching & Pixel Masking

Two Peculiar Features

Quenching

- The Pixel's quenching circuit consists of a single Transistor
- Acting on V_{Quench} is possible to tune the signal length
- Non-overlapping hits (up to 3) can be ٠ distinguished and counted within the frame (3MHz frame rate)

Pixel Masking

- Individual pixels can be disabled
- Allows deactivation of noisy/unused pixels (DCR & power consumption reduction)



IVs whit different masks

19.5

20

18.5 19

17 17.5

18

All ON

pixels OFF

Low noise

single pixel

20.5

21 V_{Bias} [V]

Page 9

dSiPM

pixel

Pixel

electronics





 V_{Bias}

 V_{Quench}

4 || SPADs

masking

Pixel Circuit

DESY-II TB Setup

May and Oct. 2022

- Two Test Beam campaigns with Caribou+dSiPM at DESY-II TB
- 4 GeV/c electron beam
- 6 beam telescope MIMOSA 26 planes used for track reconstruction (Spatial resolution 3.24 µm per plane)
- Scintillators + PMT (in May) and Pixelated timing plane (in October) used as **Trigger reference**
- Active cooling to allow stable conditions & Temperature Scans (down to ~0 °C on Chip)
- AIDA Trigger Logic Unit (TLU) allowed synchronous operation of the involved detector systems
- Mechanics, cooling system and optical isolation was optimized to maximize track resolution
- Particle Track & time was reconstructed using Telescope data, dSiPM response in **MIP detection** can be investigated





DESY II Test Beam Setup



Time Residuals

- Defined as the difference between the Track time stamp (TLU+trigger) and the Hit time stamp (dSiPMTDC)
- Time correlation between dSiPM Hit & tracks confirmed
- Width dominated by Trigger time resolution (~ 2ns)

Spatial Residuals

- Defined as the difference between hit position in DUT and interpolated track in the same z-position
- Double-peak structure due to inefficient regions inside the pixels
- Proves pixel scale resolution of the dSiPM

Efficiency

- The Efficient area can be associated to the SPAD position
- Track resolution at the DUT ~ 5 μm
- Chip Total efficency in MIP detection ~ O(Fill Factor)*

*Impact of noise & systematics to be studied



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Summary A promising R&D

Chips & Characterisations

- A digital SiPM was designed at DESY in LFoundry 150 nm CMOS
- CMOS circuits are implemented in-pixel and in Chip periphery
- All characterisations performed to date are in line with the expected performances

Results from Test Beam

- DESY dSiPM was successfully integrated in DESY-II TB setup
- 4D-Tracking performances of the prototype are currently being studied

Project Plans

- Next TB with focus on dSiPM timing in a few days (13-27 Mar.)
 - 2 aligned DUT: time resolution using TOA difference
- Pixel & Subpixel scale laser studies
- Ongoing research of possible applications



Dark Events Hitmap whit DESY logo Mask applied

Thank you.

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Additional characterizations

Validation Logic & Dead Time

Validation logic

- A 4-step validation logic is implemented in every quadrant
- Every step can be configured to be an AND or OR gate
- A flag bit is generated for event validation within 2 ns
- Successfully validated using laser pulses and masking

Quenching & Dead Time

- In 2-bit mode is it possible to count laser pulses within the frame
- Consecutive pulses can be distinguished only if the discriminator threshold is crossed (non-overlapping pulses)
- Pulse length can be tuned by acting on Vquench Transistor (Global Setting)





Schematic representation of the Validation Logic





Pixel Circuit

Dead Time vs V_{Quench} (chip4)

Laser Studies

At sub pixel level

Setup

- DUT placed on an x-y stage ٠
- Laser Optical System on a z-stage ٠
- 1064 nm pulsed laser ٠
- Laser in sync with the DAQ Clock

Ongoing & future studies

- Characterize Chip functionality ٠
 - Tests on validation logic ٠
 - Dead time evaluation ٠
- Uniformity & delay of the array response ٠
- Study time resolution/efficiency with ٠ 2D scan, investigating sub-pixel structure









high light conditions (17-17)

DUT & Trigger Alignment

A Peculiar Approach

- High DCR of dSiPM makes alignment of DUT and the trigger reference complicated (DCR/MIP event distinction impossible before alignment)
- Used Corryvreckan Material Budget Imaging (MBI)
- The software reconstructs the tracks and evaluates the scattering angle at the DUT z-position (proportional to Material Budget)
- The MB is minimized at the position of the dSiPM, which is then easily located





https://gitlab.cern.ch/corryvreckan/corryvreckan/-/tree/master/src/modules/AnalysisMaterialBudget

Software used for the analysis

Corryvreckan

Corryvreckan use hit (pixels above threshold) and Clusters (groups of adjacent hits) to reconstruct particles trajectories



- Real Track Hit
- Cluster
- Cluster center
- Reconstructed Track
- Residuals





Data Decoding

Alignment & **DUT** Association

DUT Association & Analysis

- Raw Telescope & dSiPM data acquired in TB are decoded into a format accessible to Corryvreckan
- Hitmap and Timestamp is ٠ reconstructed event by event for each detector involved

- Cluster of hits in ٠ the reference telescope are identified and used in the reconstruction of the MIP Track.
- Spatial and temporal cuts ٠ are applied to associate clusters with Tracks

- Translations and rotations of the telescope and DUT planes are performed
- Multiple iterations maximize accuracy in tracks reconstruction

- DUT clusters are associated ٠ with the reconstructed tracks
- The response of dSiPM in MIP detection is analyzed. it is possible to determine spatial resolution, temporal resolution, efficiency, Cluster size, etc.

