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Design and performance of UKRI-MPW0: an HV-CMOS prototype with a novel sensor cross-section

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The High Voltage CMOS (HV-CMOS) technology is a promising candidate for future particle physics experiments. To meet the needs of future experiments, especially in terms of single point resolution ($50 \times 50 \mu\mathrm{m}^2$), time resolution (0.2 ns) and radiation tolerance ($10^{16} \mathrm{n_{eq}}/\mathrm{cm}^2$), the HV-CMOS pixel sensor performance needs to be further improved. The Liverpool HV-CMOS group has developed a prototype HV-CMOS chip, named UKRI-MPW0, which aims at addressing some of these challenges.
This chip is developed using the 150 nm HV-CMOS process from LFoundry. It implements a novel sensor cross-section optimised for backside biasing at unprecedented high voltages. Preliminary measurements have shown the chip is able to sustain high bias voltages (> 600 V) much beyond the state of the art, thus promising a large improvement in radiation tolerance. Pixel matrices with 20 rows and 29 columns (pixel size of $60 \times 60 \mu\mathrm{m}^2$) and several test structures are included in the chip.
This contribution will present the design details and evaluation of UKRI-MPW0, with focus on the performance characterisation of its pixel matrix. Initial characterisation results show pixels have Equivalent Noise Charge (ENC) $< 100 \mathrm{e}^-$ and gain $> 100 \mathrm{mV}/\mathrm{ke}^-$.

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