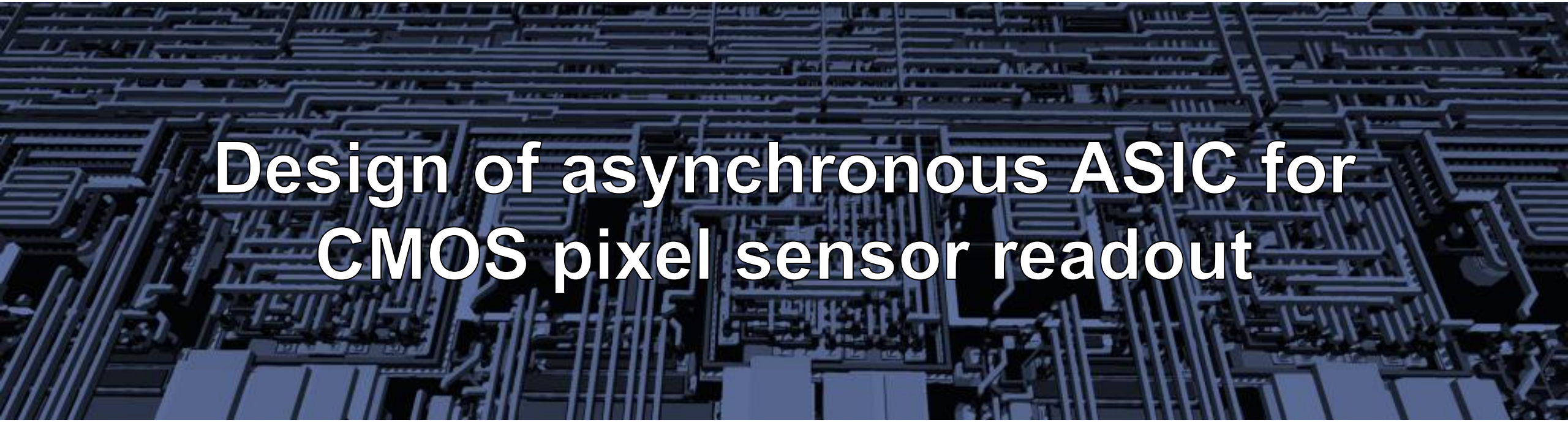


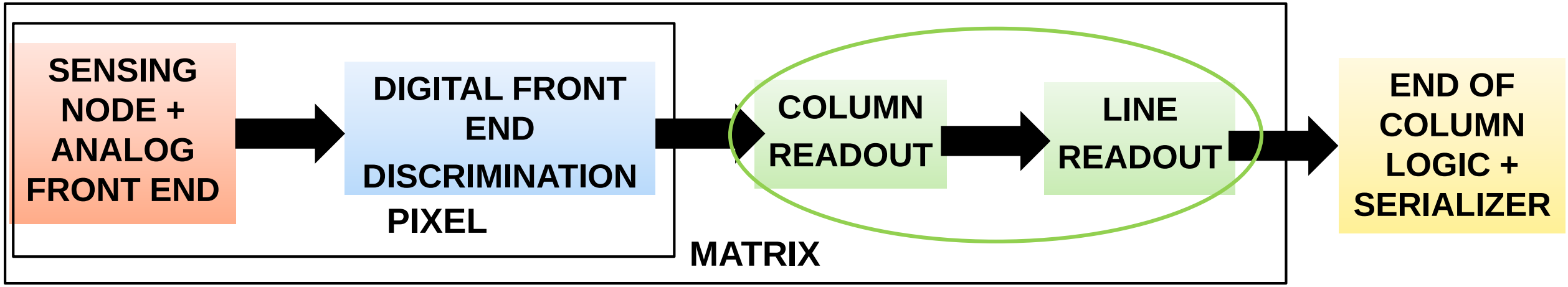
Design of asynchronous ASIC for CMOS pixel sensor readout

Jean Soudier

IPHC - Strasbourg

Foudil DADOUCHE (ICube), Frederic Morel (IPHC), Grégory Bertolone (IPHC), Isabelle Valin (IPHC), Jean-Baptiste KAMMERER (ICube), Jerome Baudot (IPHC), Thanh Hung PHAM (IPHC), Wilfried UHRING (ICube), Xiaochao Fang (IPHC), abdelkader HIMMI (IPHC)

Why designing asynchronous circuits for MAPS with sparse readout ?



↘ Reduce power consumption (working at the needs)

↗ Increase bandwidth (all the circuit is independent)

↘ Can lead to size reduction (no clock to route)

OUTLINE

I. Presentation in functionality of the priority encoder (current)

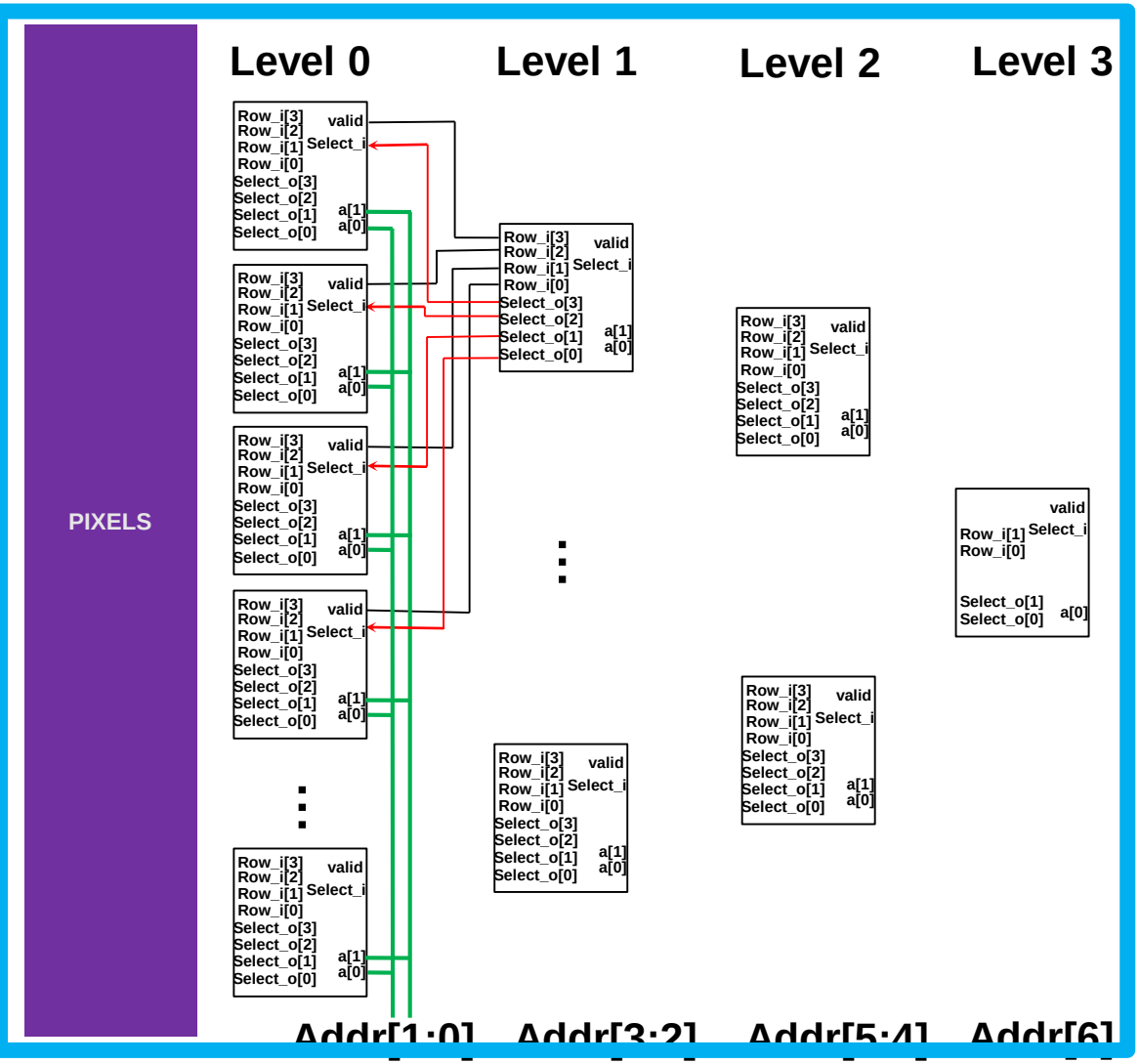
II. Global overview of the asynchronous design

III. First results

IV. Conclusion

The priority encoder

Symbolic view of the readout tree



- **Commonly used readout circuit (ALPIDE [a], MIMOSIS [b] and MOSS [c])**
- **Synchronous architecture (with global nets) so frequency dependant**

[a] G. Aglieri Rinella, 'The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System', *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 845, pp. 583–587, Feb. 2017, doi: 10.1016/j.nima.2016.05.016.

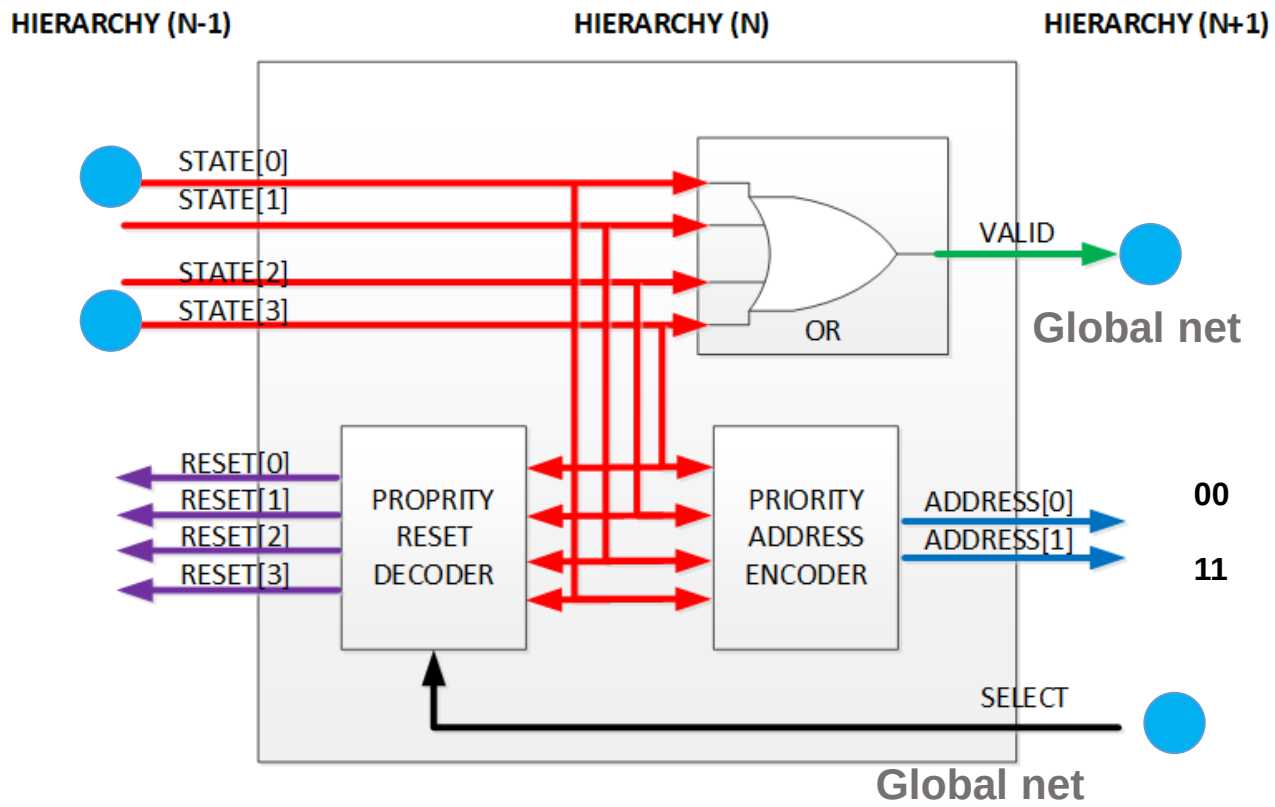
[b] « TIPP 2021 », *Indico*. https://indico.cern.ch/event/981823/contributions/4293566/ (consulté le 28 février 2023).

[c] P. Vicente Leitao *et al.*, « Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE Inner Tracking system », *J. Inst.*, vol. 18, nº 01, p. C01044, janv. 2023, doi: 10.1088/1748-0221/18/01/C01044.

[1] Extract from a presentation for the MOSS project

Zoom on a small block from the priority encoder

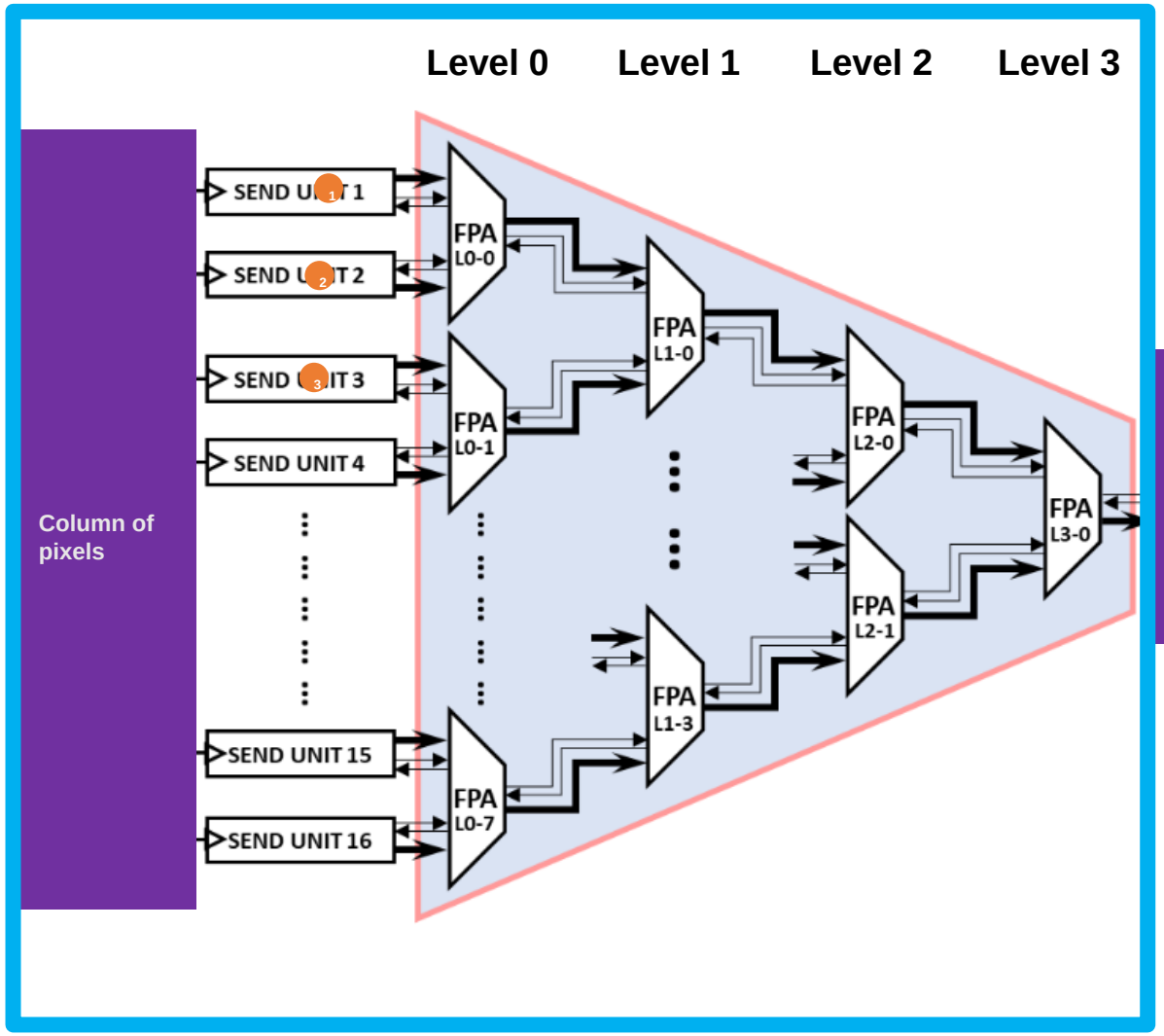
Block to set if there is a data (valid), decode the address with the highest priority and provide a way to reset the concern pixel

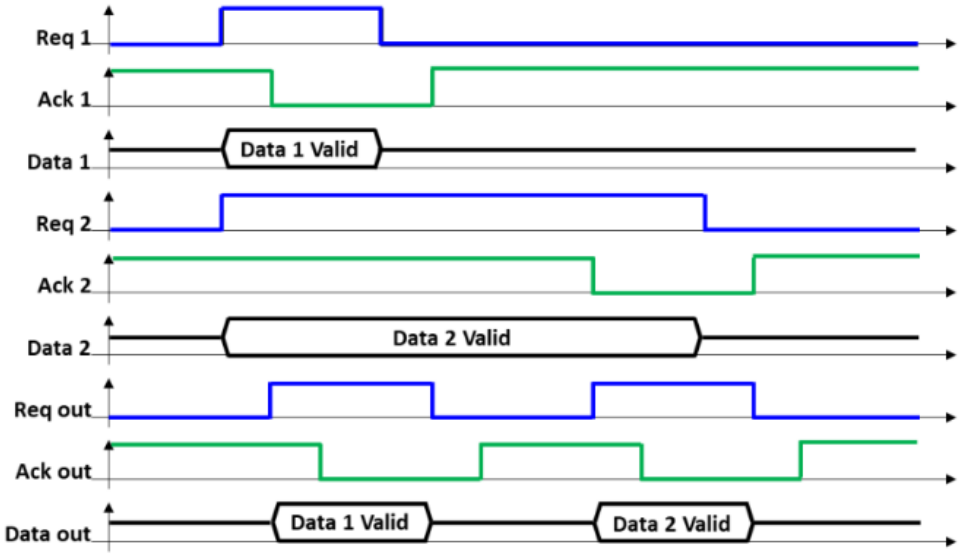


[1] Extract from a presentation of prototype sensor MOSS for ALICE ITS3

Asynchronous design: priority tree (MUX)

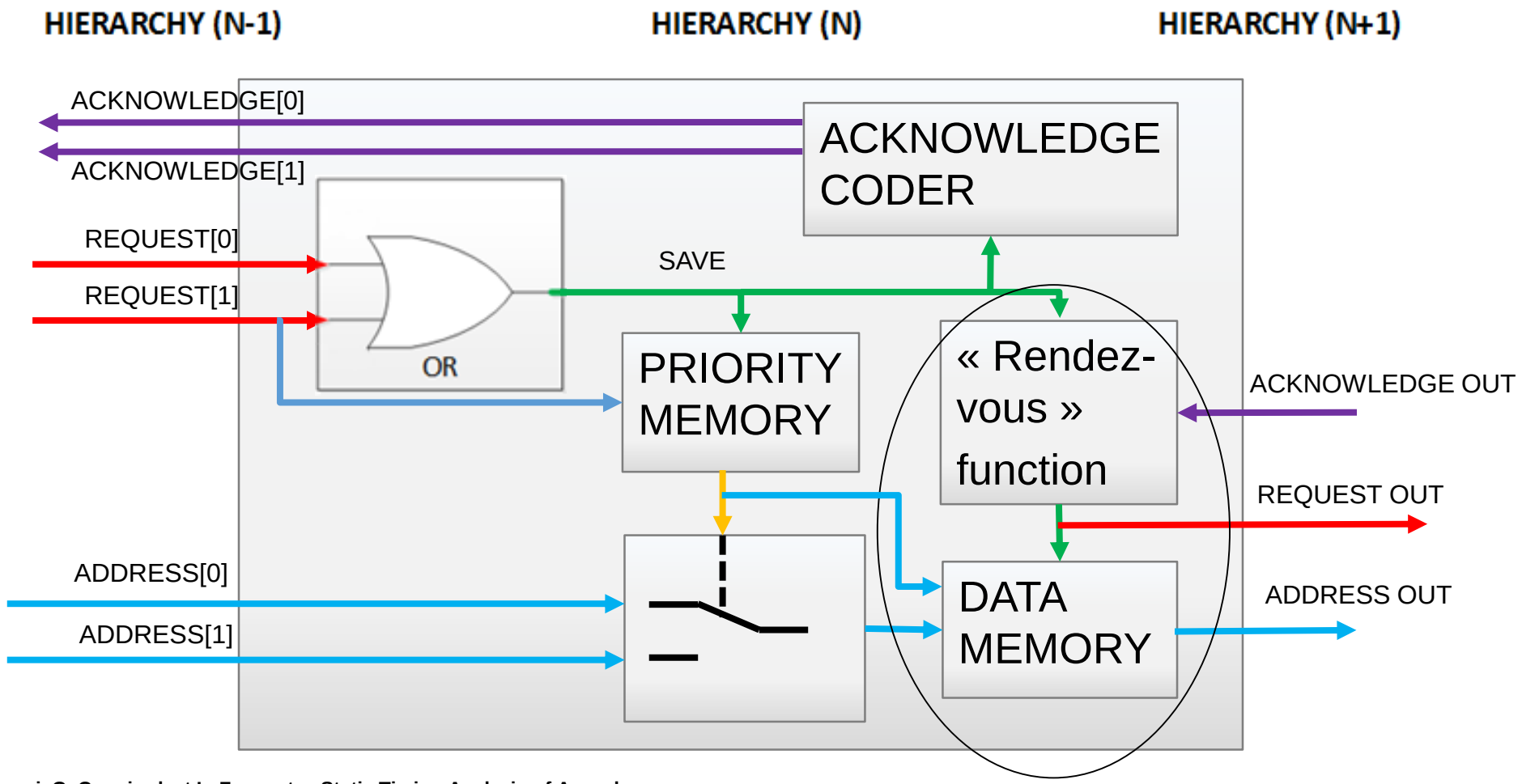
Symbolic view of the readout tree





[2] E. Aguénounon *et al.*, « Design and Characterization of an Asynchronous Fixed Priority Tree Arbiter for SPAD Array Readout », *Sensors*, vol. 21, juin 2021, doi: 10.3390/s21123949.

Inside a Fixed Priority Arbiter (MUX 2 to 1)

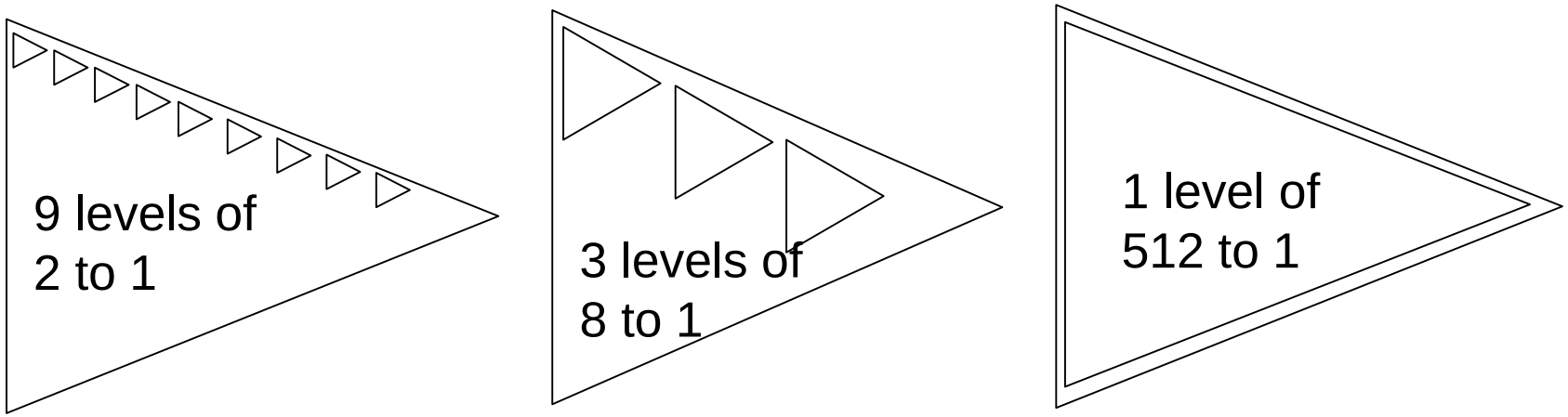


[3] G. Gimenez, A. Cherkaoui, G. Cogniard, et L. Fesquet, « Static Timing Analysis of Asynchronous Bundled-Data Circuits », in *2018 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, mai 2018, p. 110-118. doi: 10.1109/ASYNC.2018.00036.

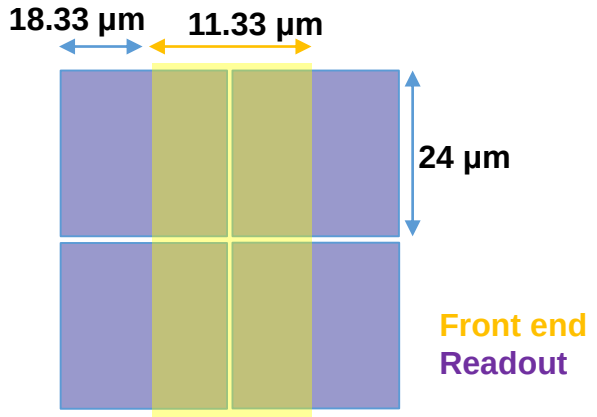
Current implementation in 65nm CMOS process

	Pixel pitch [µm]	Analog area [µm²]	Number of metal layers	Number of pixels (double column)	State
FPA controller size 1 *	24	136	6	512	Post-CTS
FPA controller size 3 *	24	136	6	512	Post-CTS
FPA controller size 3	20	180	4	512	Fit in area
FPA controller size 9 *	24	136	6	512	Post-CTS
PE (MOSS) *for matrix	18, 22.5	136	4	320 (simple column)	Production in progress
PE (MOSS2)	18	180	4	1024	Design in progress

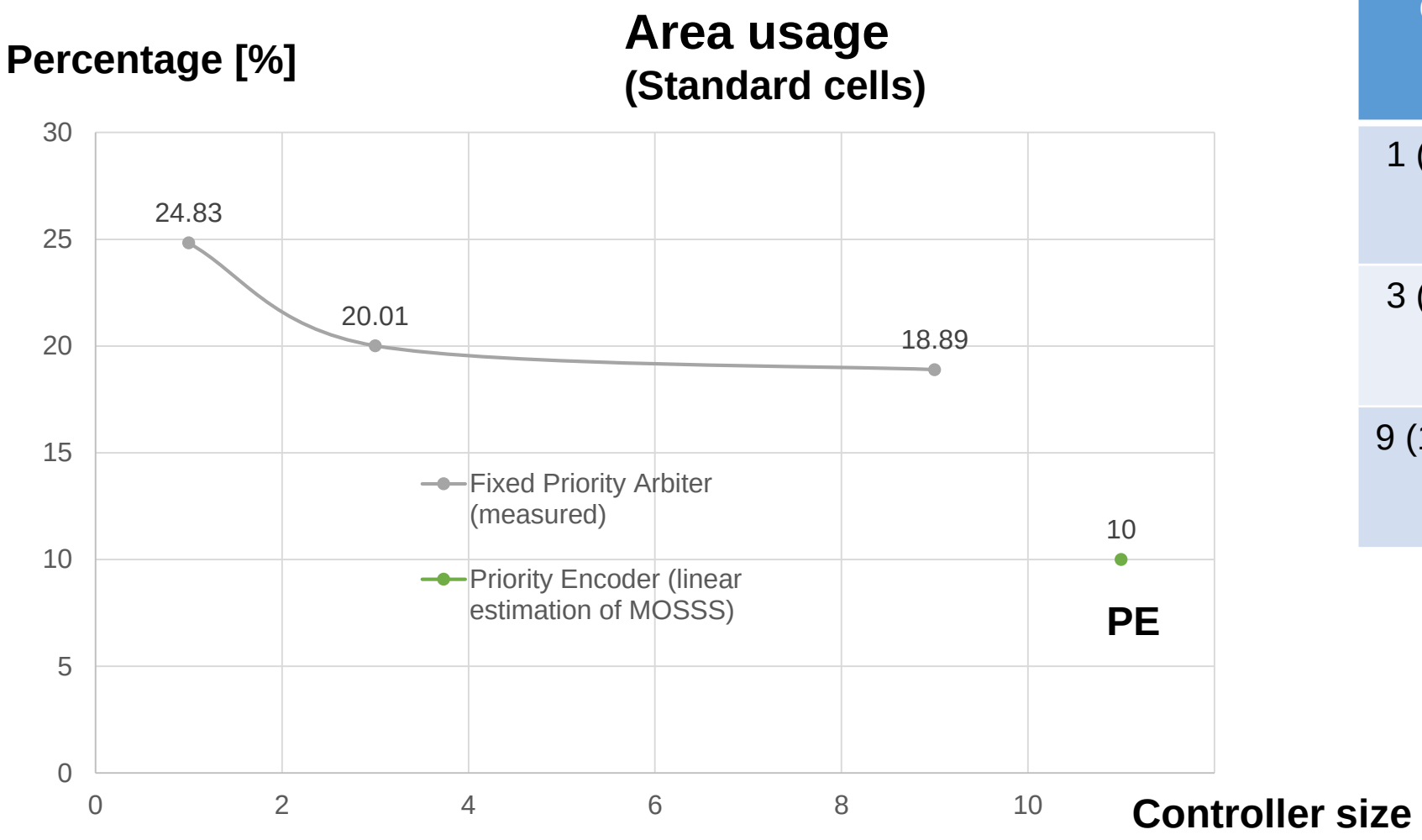
*** Circuit that being tested**



Zoom on a 2x2 pixels integration



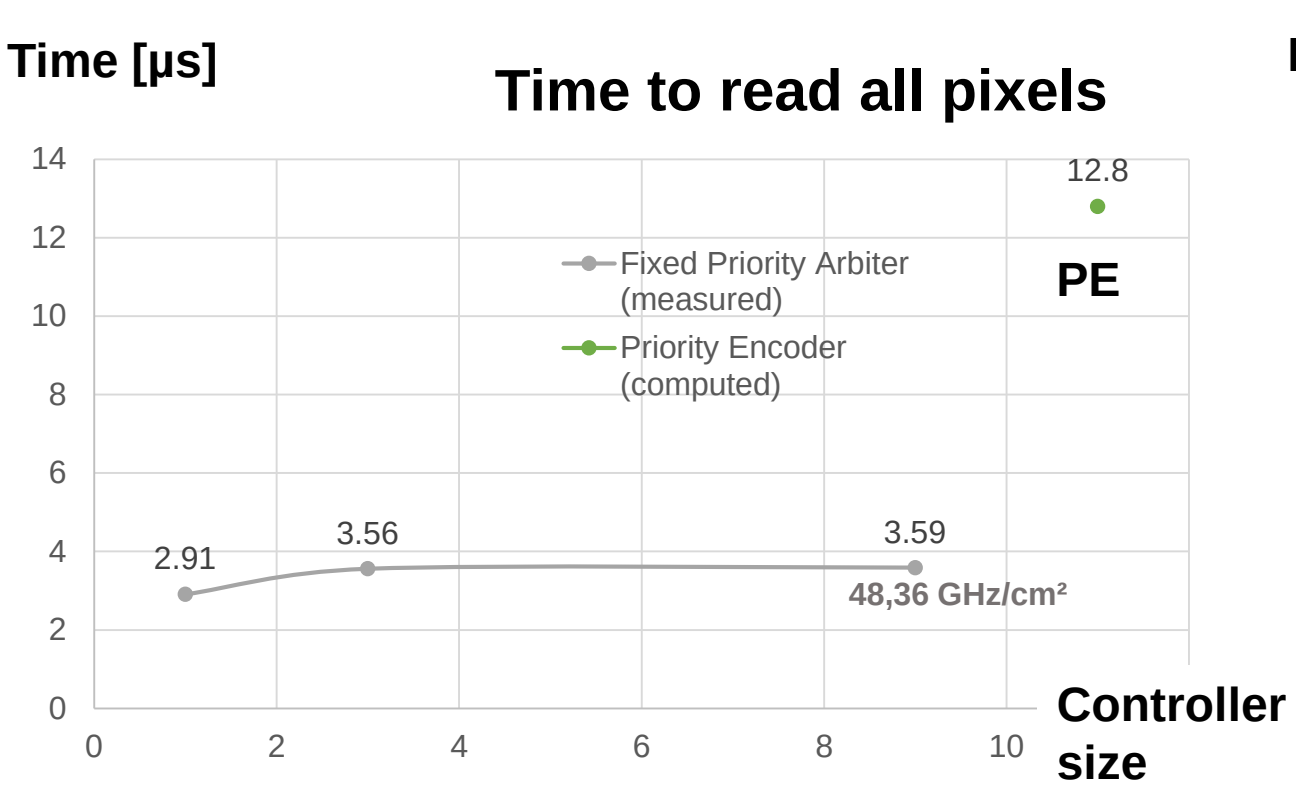
Results on area to fit in small pitch

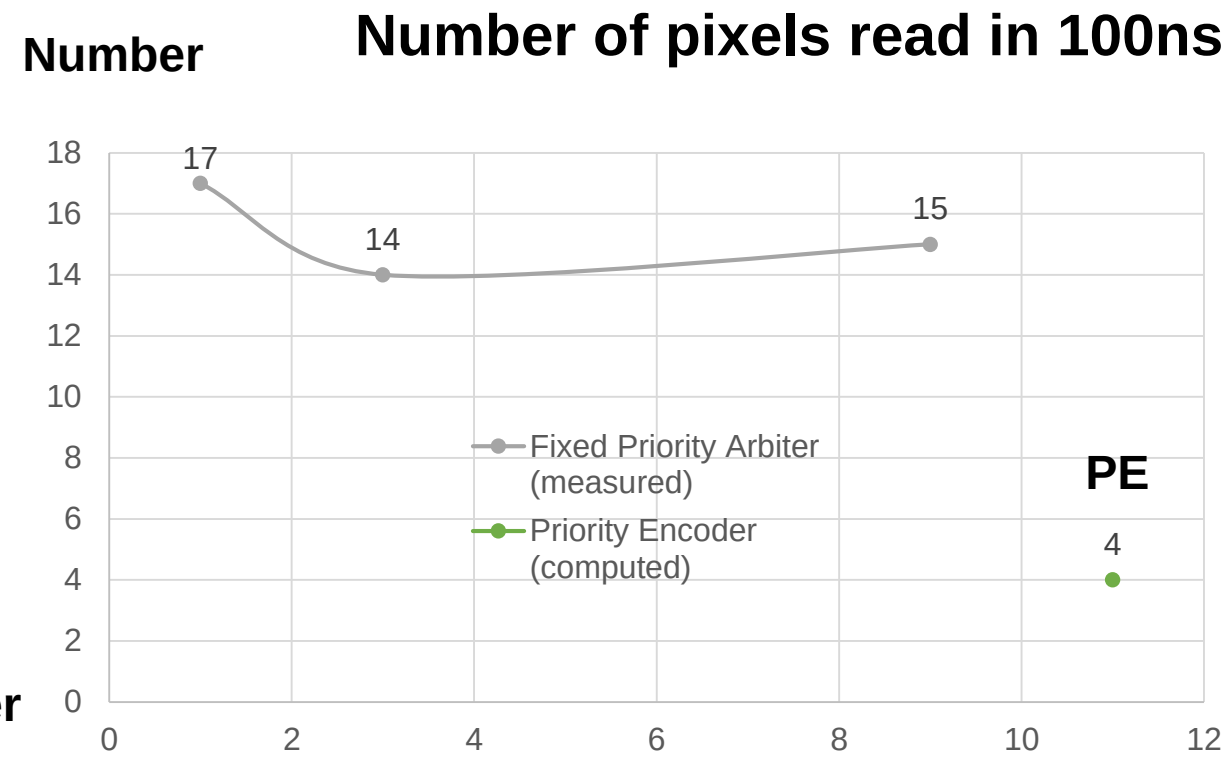


Controller size	Pourcentage of Gcells full (routing cells)
1 (9 levels of 2 to 1)	44,31% (limitation, huge congestion)
3 (3 levels of 8 to 1)	0%
9 (1 level of 512 to 1)	0%

Functional results for 512 pixels

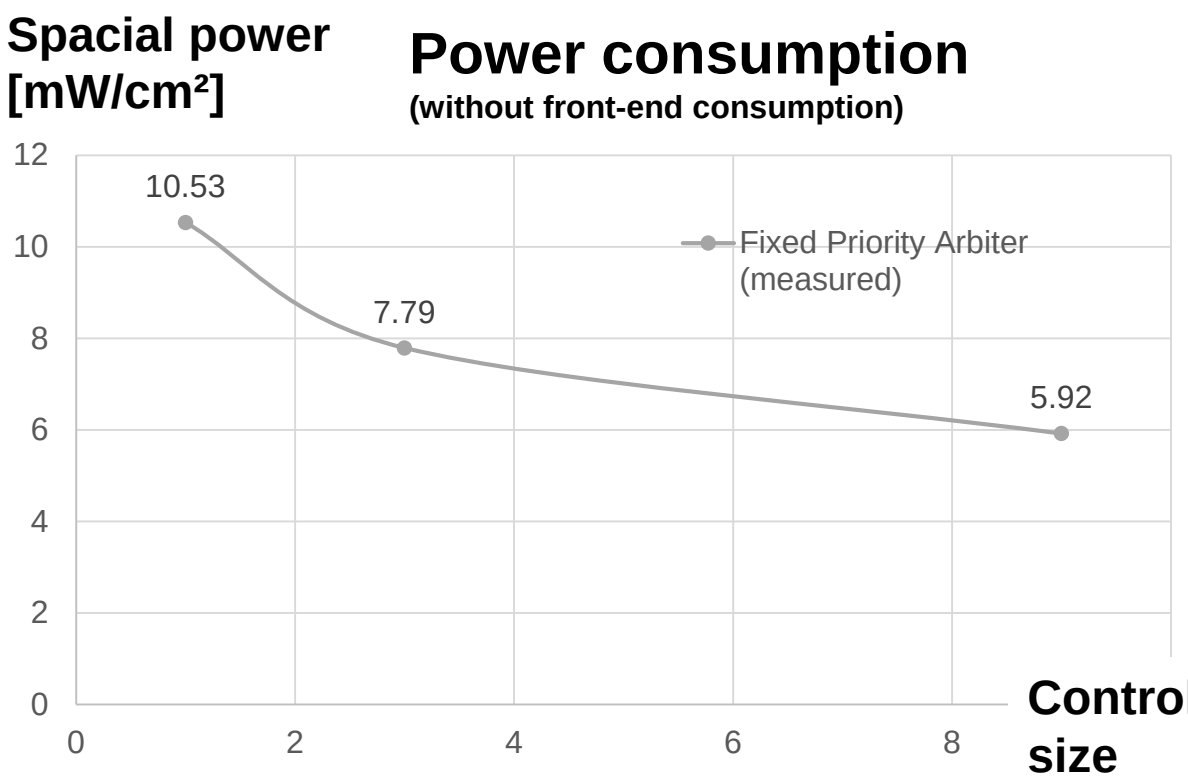
Test name	Description	Type of results
Functional	Firing every pixels to evaluate the bandwidth	Time to read all pixels and number of pixels read in 100ns

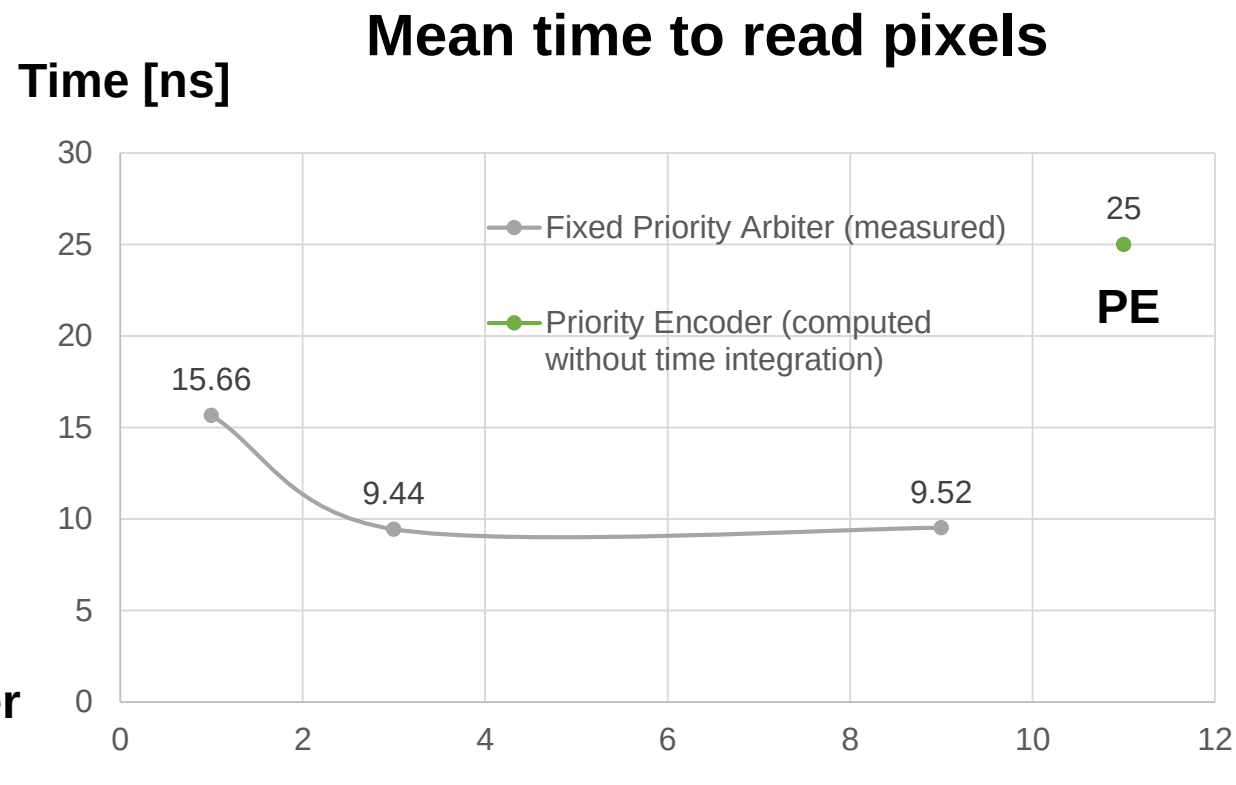




Exploitation results with 3,19 GHz/cm² hit rate

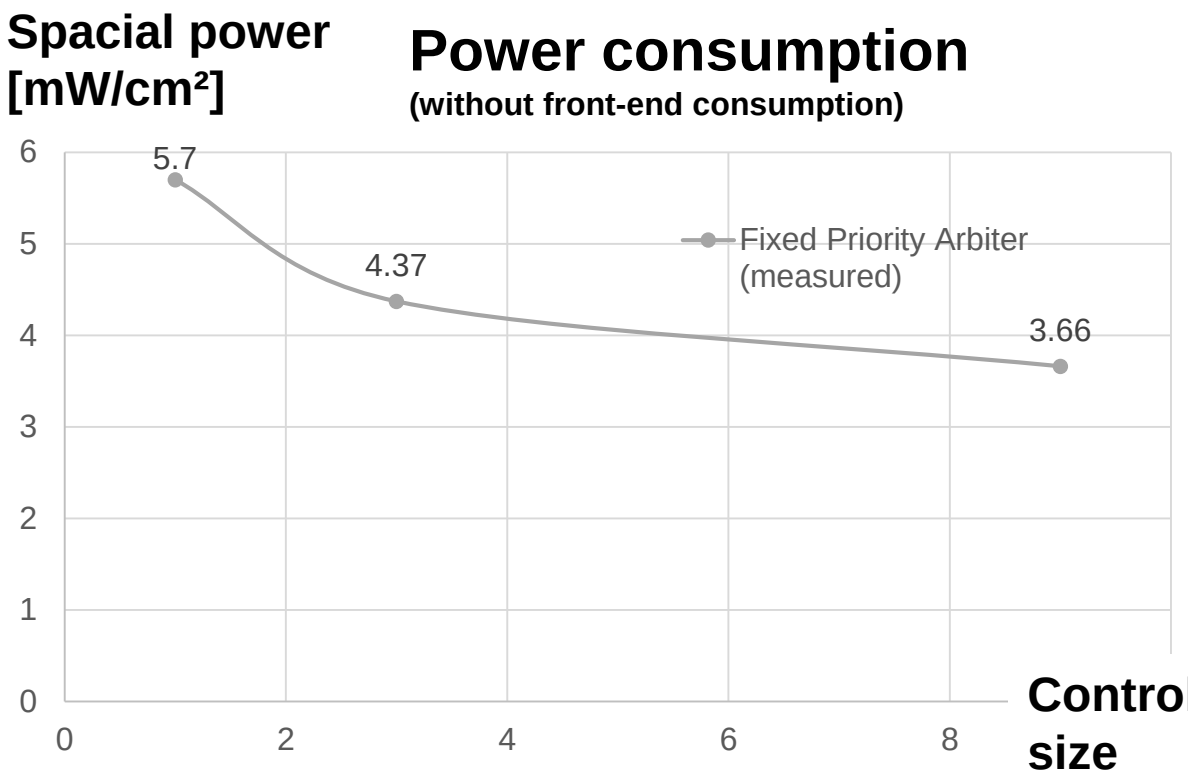
Test name	Description	Type of results
Classical usage	940 pixels firing during 100 µs	Power consumption and mean hit rate

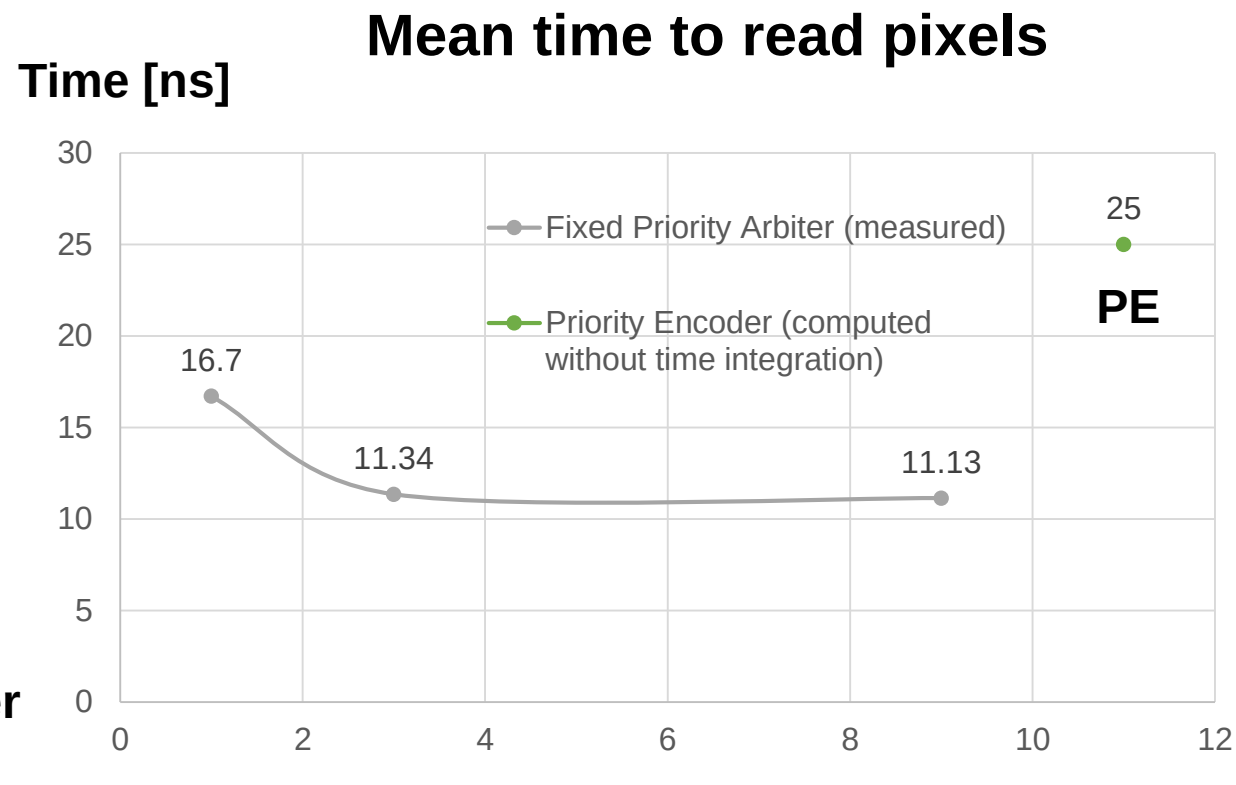




Exploitation results with 330 MHz/cm² hit rate

Test name	Description	Type of results
Classical usage	98 pixels firing during 100 µs	Power consumption and mean hit rate



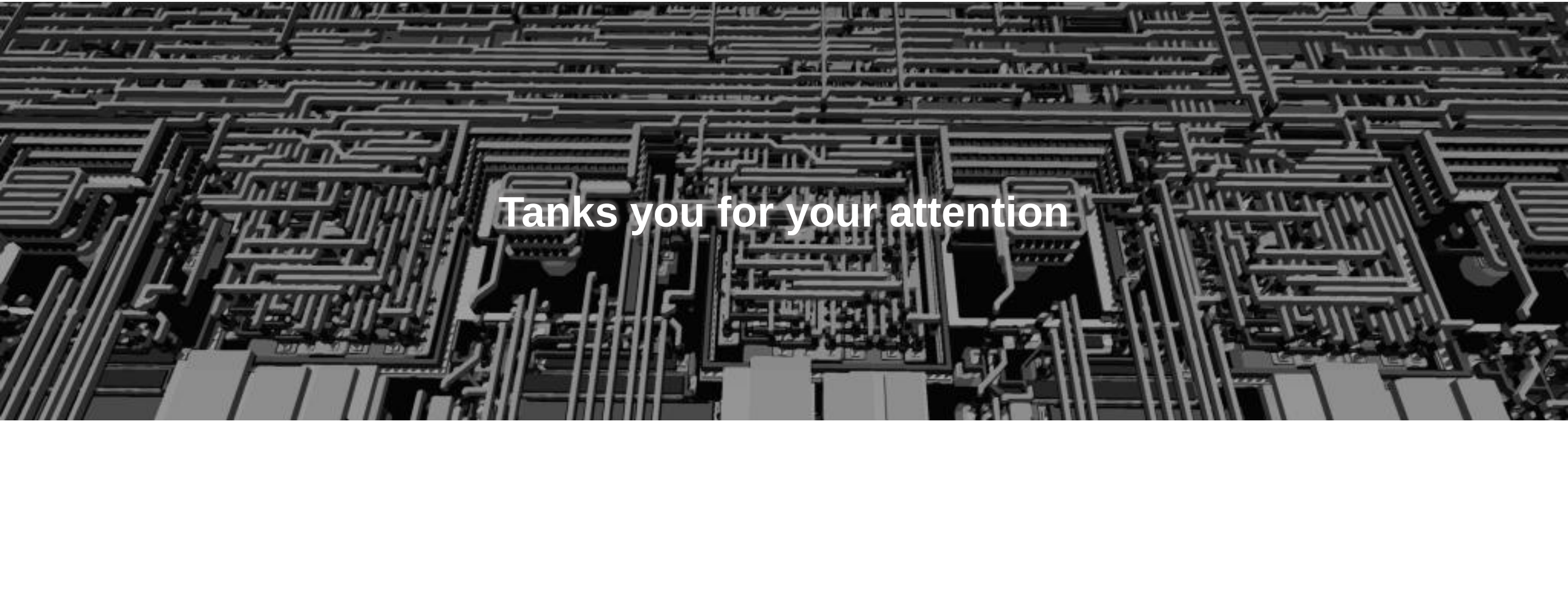


Conclusion

- **Pros:** reading speed **4x** better and provide timestamping at ns level
- **Cons:** area occupation, complex integration with standard digital tool

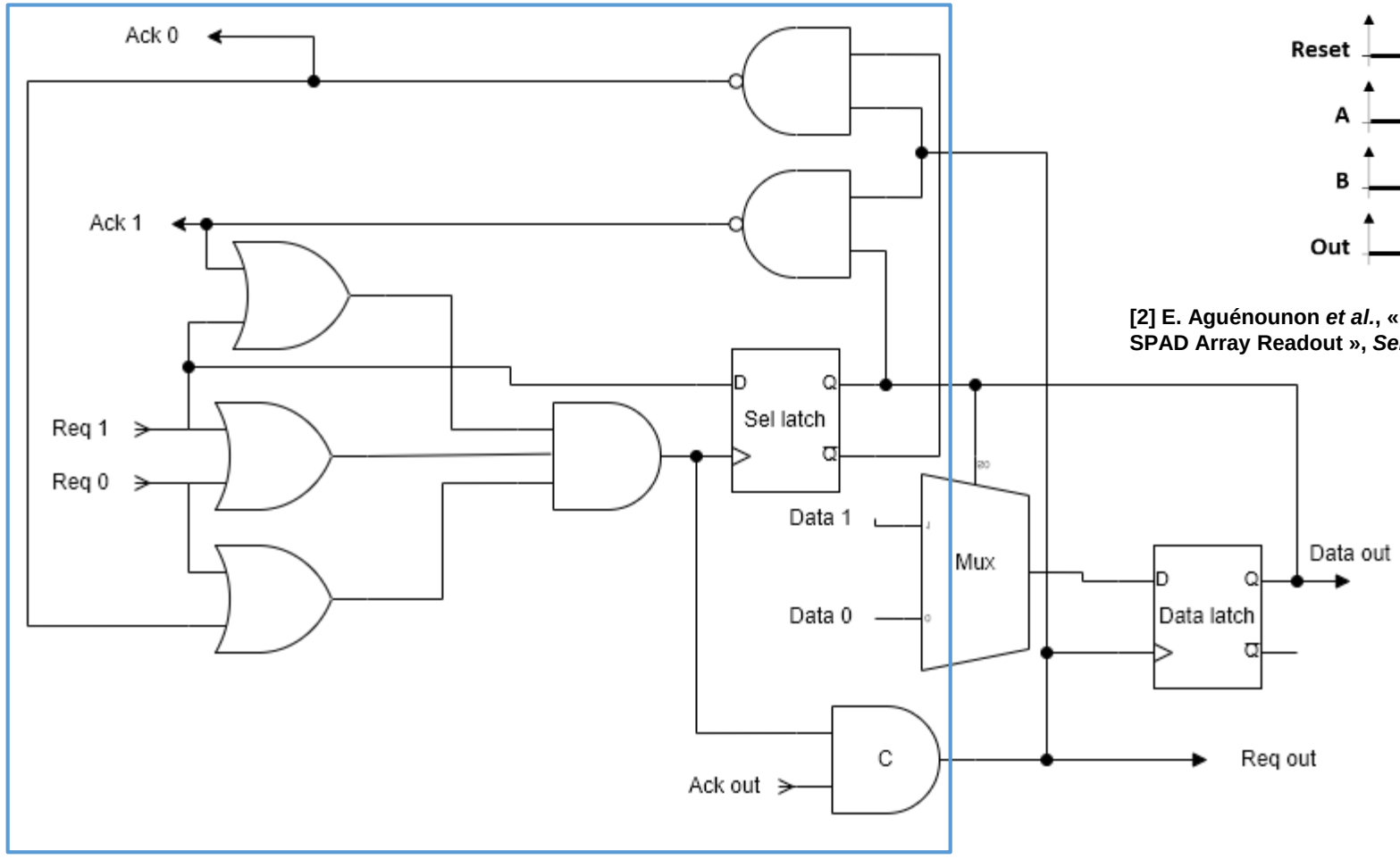
➢ Adapted to pixel detectors with high hit rate (GHz/cm²), air cooling (few tens mW/cm²) and allow small pitch (around 20µm)

- **Currently:** estimation for 512 pixels in 3 controller sizes (1, 3 and 9)
- **Next:** physical implementation on small prototype (optimization to be decided)

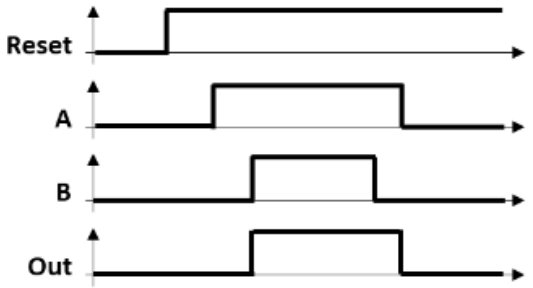

Tanks you for your attention

Working principle of FPA

Inside a basic block



C element

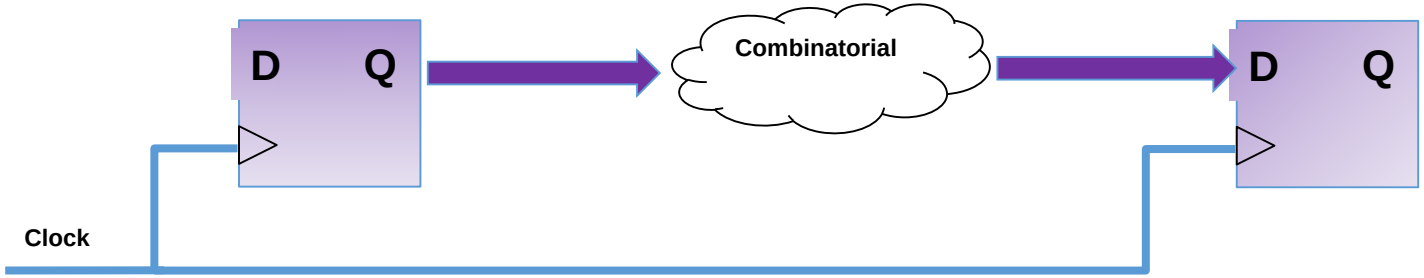


Reset	A	B	Out
1	0	0	0
1	0	1	Out^{-1}
1	1	0	Out^{-1}
1	1	1	1
0	X	X	0

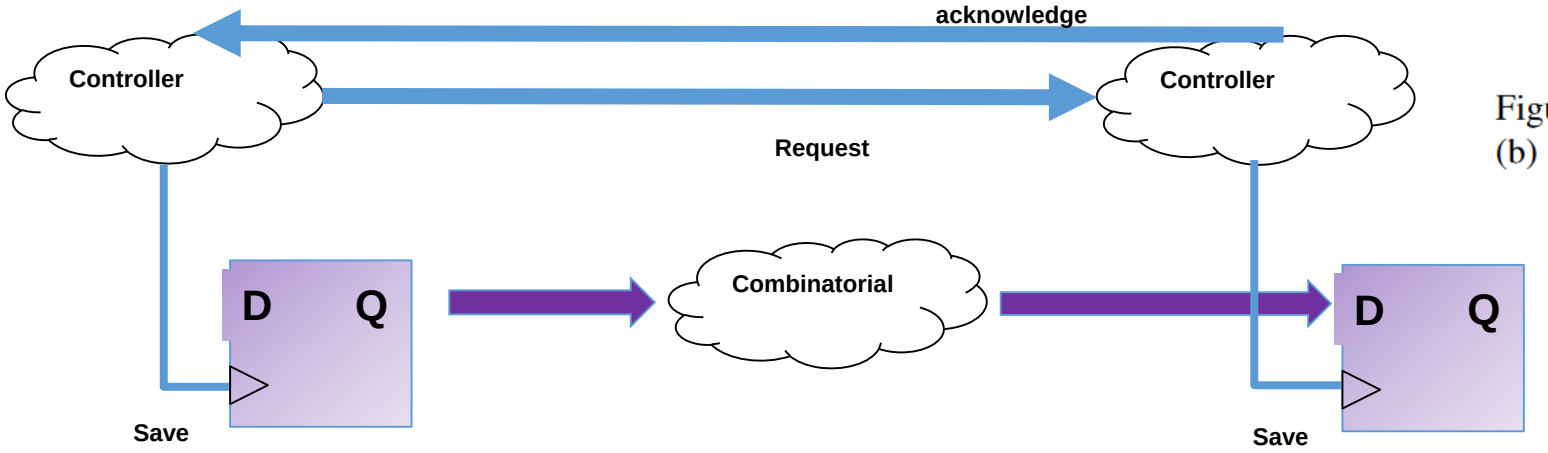
[2] E. Aguénounon *et al.*, « Design and Characterization of an Asynchronous Fixed Priority Tree Arbiter for SPAD Array Readout », *Sensors*, vol. 21, juin 2021, doi: 10.3390/s21123949.

Asynchronous method

Synchrone



Asynchrone



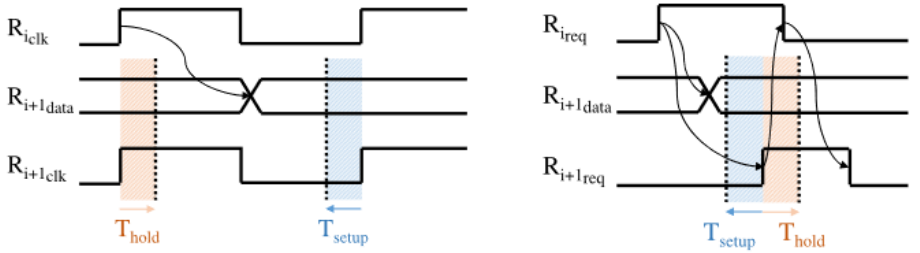
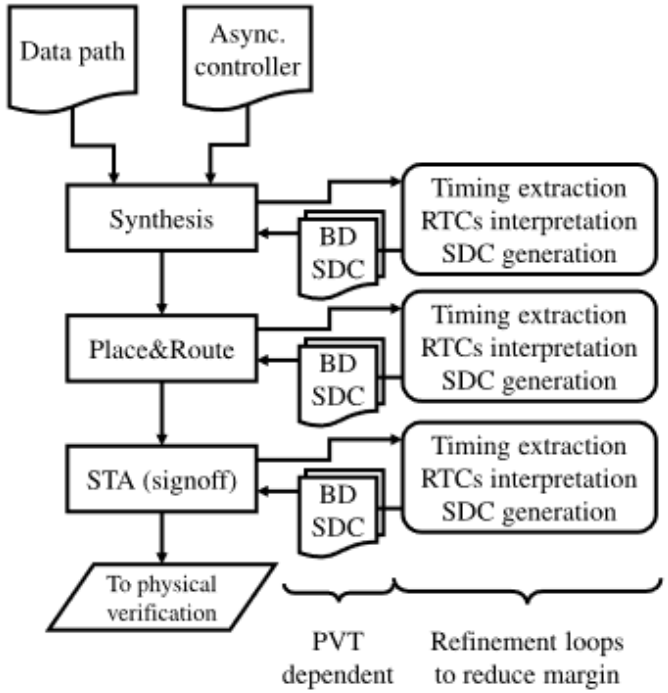


Figure 5: Timing waveform for a 2-stage (a) synchronous and (b) asynchronous pipeline.

[3] G. Gimenez, A. Cherkaoui, G. Cogniard, et L. Fesquet, « Static Timing Analysis of Asynchronous Bundled-Data Circuits », in *2018 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, mai 2018, p. 110-118. doi: 10.1109/ASYNC.2018.00036.

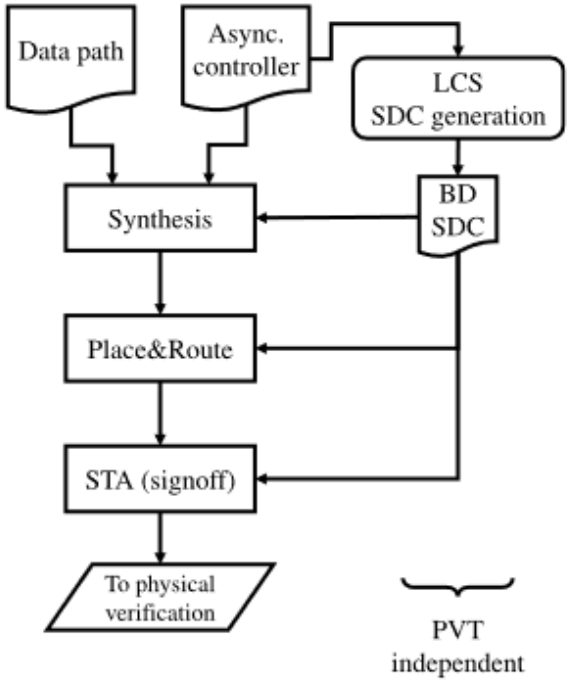
Asynchronous method

Method based on min/max delays



- ✓ Simpler to do
- ✗ Could be fastidious
- ✗ Highly design dependent
- ✗ PVT dependent

Method based on LCS (Local Clock Set)

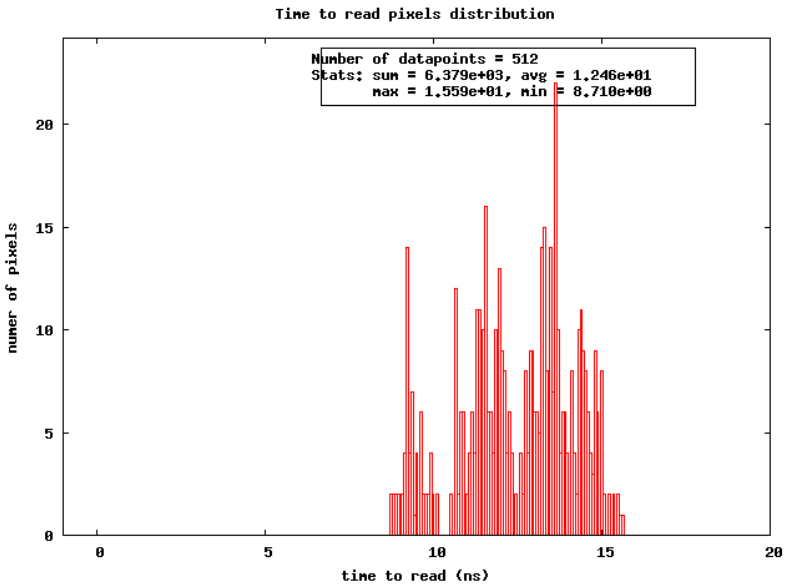


- ✗ Complex to do
- ✓ Easy to script
- ✓ Less design dependent
- ✓ Not PVT dependent

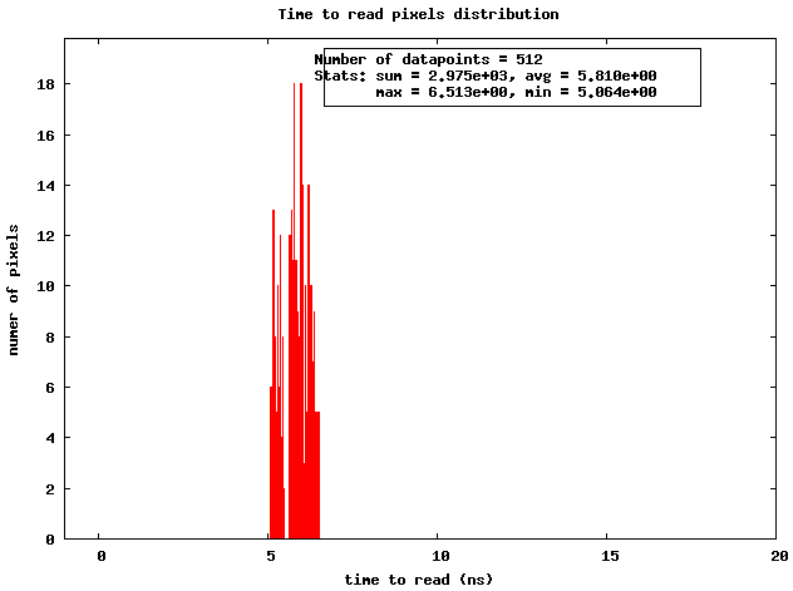
[3] G. Gimenez, A. Cherkaoui, G. Cogniard, et L. Fesquet, « Static Timing Analysis of Asynchronous Bundled-Data Circuits », in *2018 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, mai 2018, p. 110-118. doi: 10.1109/ASYNC.2018.00036.

Mean time to read one pixel around the column

Size 1 (9 levels of 2 to 1):



Size 3 (3 levels of 8 to 1):



Size 9 (1 level of 512 to 1):