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# New performance for MAPS readout using an asynchronous architecture based on priority arbiters

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Monolithic CMOS pixel sensors (or MAPS) offer a particularly advantageous balance between pixel granularity, hit rate and power dissipation, making them attractive devices for vertexing and tracking. Existing reticule-size sensors [1, 2, 3] display power ranging roughly from 35 to 100 mW/cm2 for corresponding hit rates in the range 10 to 100 MHz/cm2 and timestamping capabilities from 5 µs down to 25 ns. The readout performance of pixel matrices results obviously from a compromise between the bandwidth and power consumption. Future projects including MAPS require to reach new optimization approaching or exceeding maximal current bandwidth (100 MHz/cm2), nanosecond timestamping and power compatible with very light colling system (few tens of mw/cm2 at most).
To achieve this goal, new back-end architectures are proposed mainly based on clock-gating or asynchronous design [2]. This work presents an implementation for MAPS readout of the architecture proposed in [4]. This circuit is based on Fixed Priority Arbiters (FPA) and acts as an asynchronous multiplexer. The initial circuit designed for visible light detection is adapted to charged particle sensors, having in mind the requirements set above as well as compactness for minimal pixel pitch (around 20 µm).
The architecture performance depends strongly on the size of the basic elements that composed the reading tree of the matrix. While a two-to-one basic element is proposed in [4] for the arbiter size, we explore all sizes from two to one until ten-to-one. Merging basic elements leads to sharing memories at each level of the tree and first reduce the layout area. In addition, power consumption is also mitigated since fewer gates are used. However, the bandwidth is reduced since there are fewer temporary memory across the whole tree.
A representative double-column read-out circuit is developed for a matrix featuring 512 pixels per column, with variants corresponding to the different arbiter sizes. All results are extracted from a layout in a 65nm node, based on the method presented in [5] and compared to an existing synchronous priority encoder implemented in the MOSS circuit [3]. We conclude on the best suited approach depending on the MAPS requirements in terms of hit rate bandwidth, power dissipation and timestamping.

[1] G. Aglieri Rinella, 'The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System', Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 845, pp. 583–587, Feb. 2017, doi: 10.1016/j.nima.2016.05.016.

[2] R. Cardella et al., 'MALTA: an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade', J. Inst., vol. 14, no. 06, pp. C06019–C06019, Jun. 2019, doi: 10.1088/1748-0221/14/06/C06019.

[3] P. Vicente Leitao et al., « Development of a Stitched Monolithic Pixel Sensor prototype (MOSS chip) towards the ITS3 upgrade of the ALICE Inner Tracking system », J. Inst., vol. 18, no 01, p. C01044, janv. 2023, doi: 10.1088/1748-0221/18/01/C01044.
[4] E. Aguénounon et al., « Design and Characterization of an Asynchronous Fixed Priority Tree Arbiter for SPAD Array Readout », Sensors, vol. 21, juin 2021, doi: 10.3390/s21123949.

[5] G. Gimenez, A. Cherkaoui, G. Cogniard, et L. Fesquet, « Static Timing Analysis of Asynchronous Bundled-Data Circuits », in 2018 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), mai 2018, p. 110 118. doi: 10.1109/ASYNC.2018.00036.

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