02.03.2023

TREDI 2023

A low-power, 64-channel ASIC for space applications for Cherenkov radiation detection

ASI-INFN agreement for EUSO-SPB2

A. Di Salvo[1], S. Garbolino[1], S. Tedesco[1, 2],
A. Rivetti[1], M. E. Bertaina[1, 3], Antonio Palmieri[1, 3]

Agenzia Spaziale Italiana

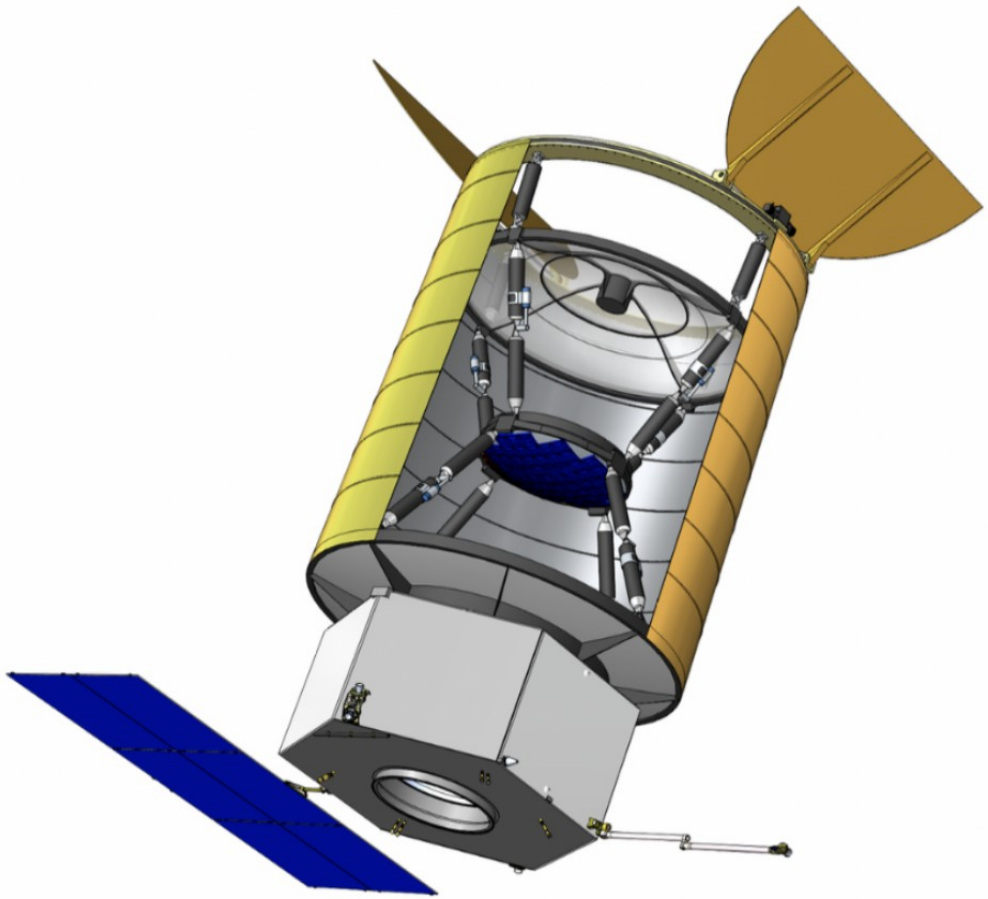
Istituto Nazionale di Fisica Nucleare

[1] National Institute for Nuclear Physics, Section of Torino, Torino, Italy

[2] Politecnico di Torino, Dipartimento di Elettronica e Telecomunicazioni, Torino, Italy

[3] University of Torino, Physics, Torino, Italy

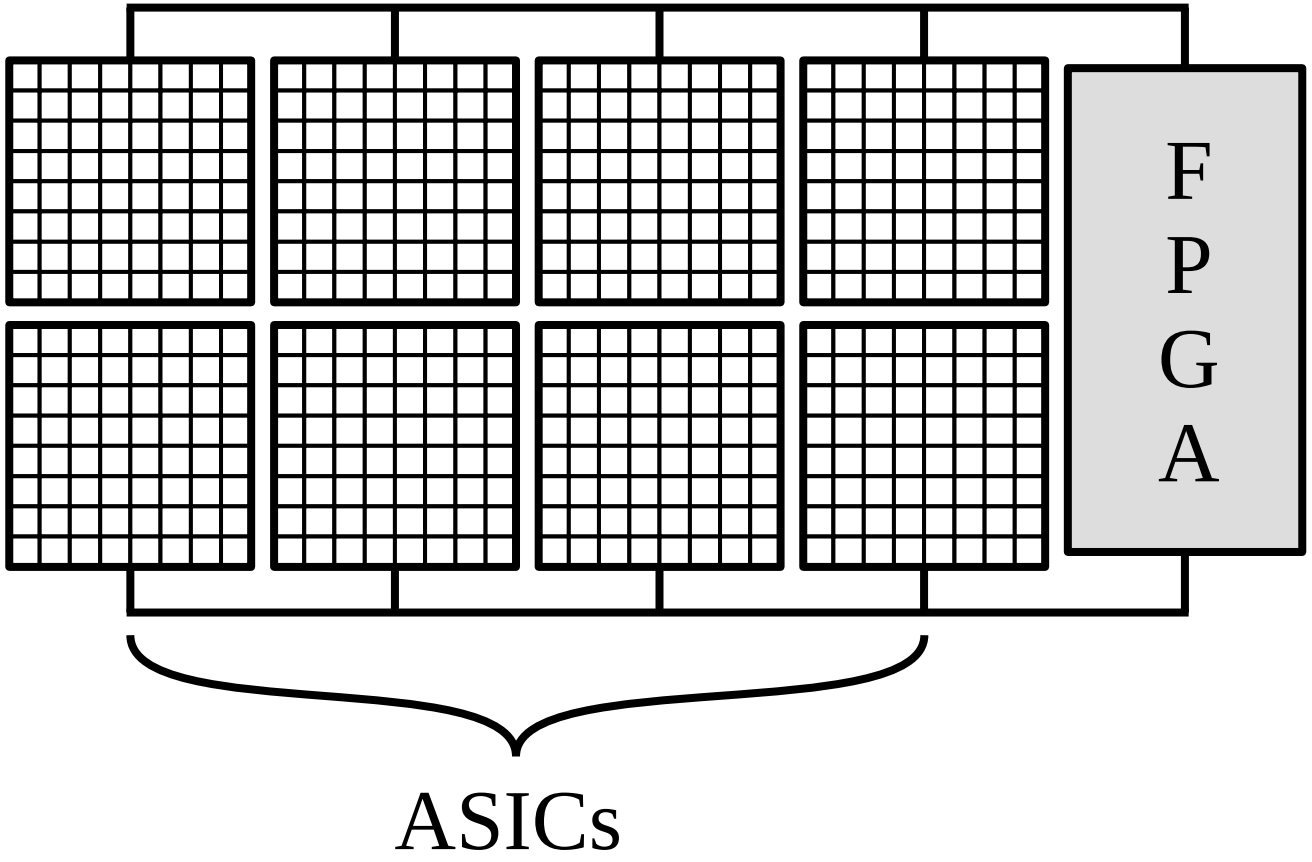
Research context



Angela V. Olinto, POEMMA and EUSO-SPB: Space Probes of the Highest Energy Particles, 2018

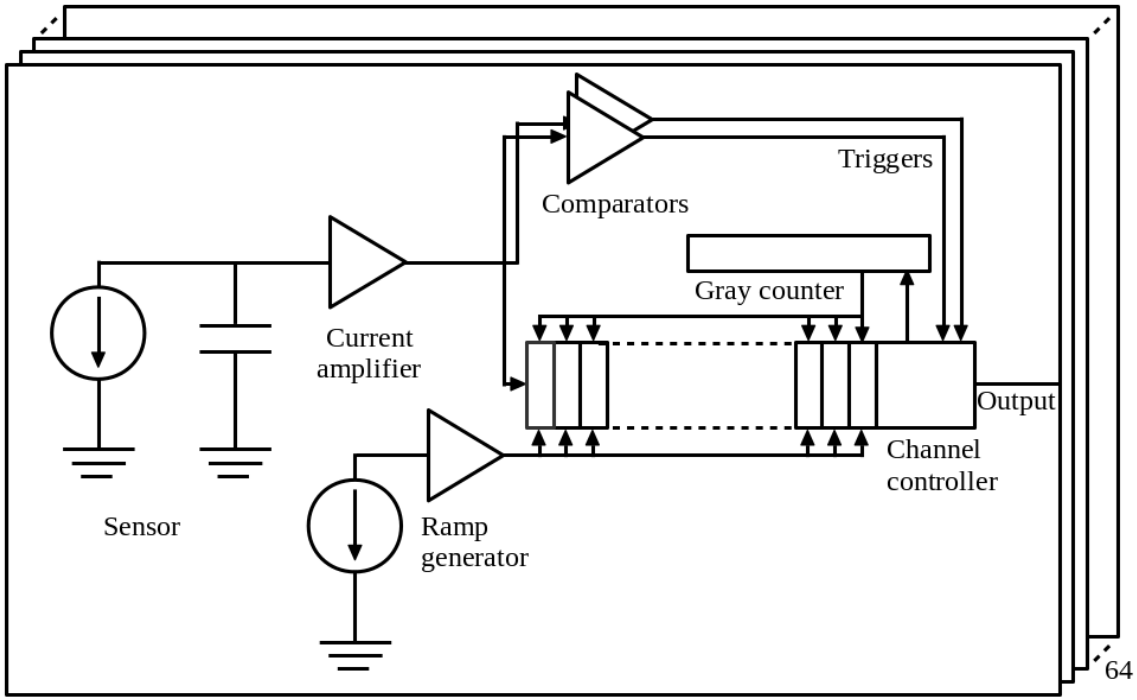
- Detection of **Extensive Airshowers** (EASs) generated by **Ultra-High Energy Cosmic Rays** (UHECRs) beyond 100 PeV and **Cosmic Neutrinos** (CNs) through Cherenkov radiation processes.
- The fast sampling of the signal is mandatory: 200 MHz.
- 64-channel ASIC implemented in a commercial 65 nm CMOS technology.
- A system to readout a camera plane composed by a matrix of Silicon Photo-Multipliers (SiPMs).

Camera architecture



- Upper array: background (light pollution and storms).
- Lower array: region of interest.

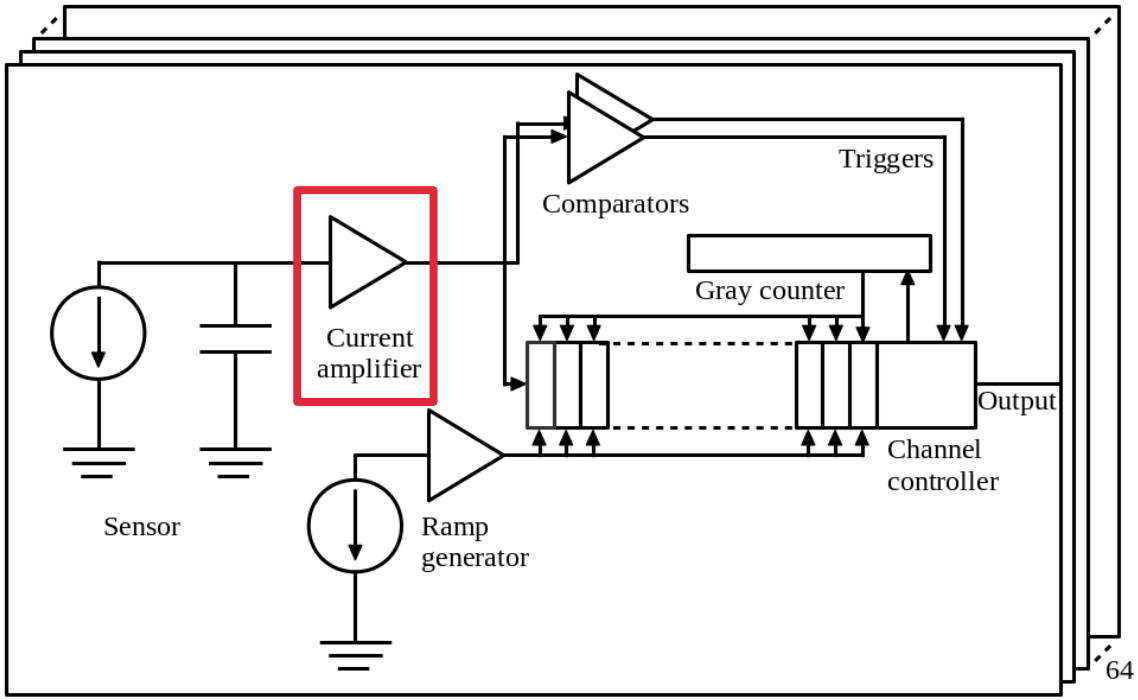
ASIC architecture



- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- A digital Gray counter.

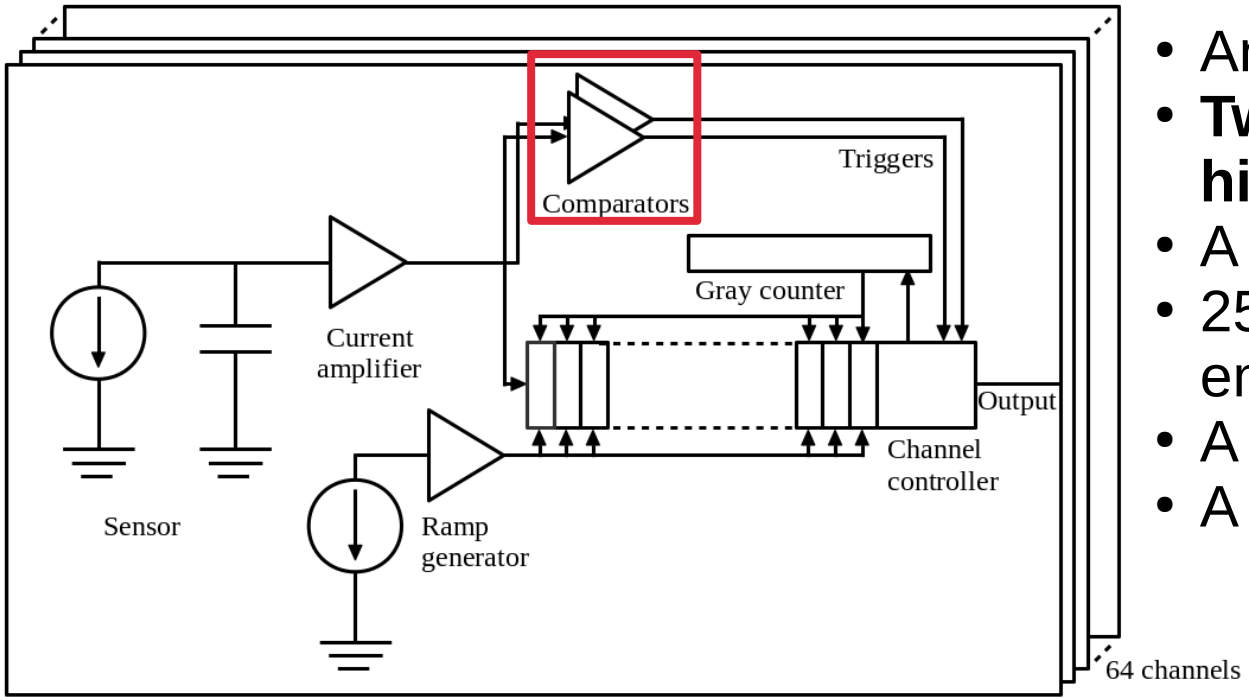
No full sampling system.

ASIC architecture

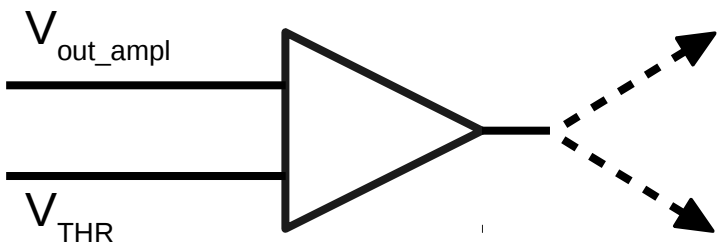


- **An input amplifier**.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- A digital Gray counter.

ASIC architecture



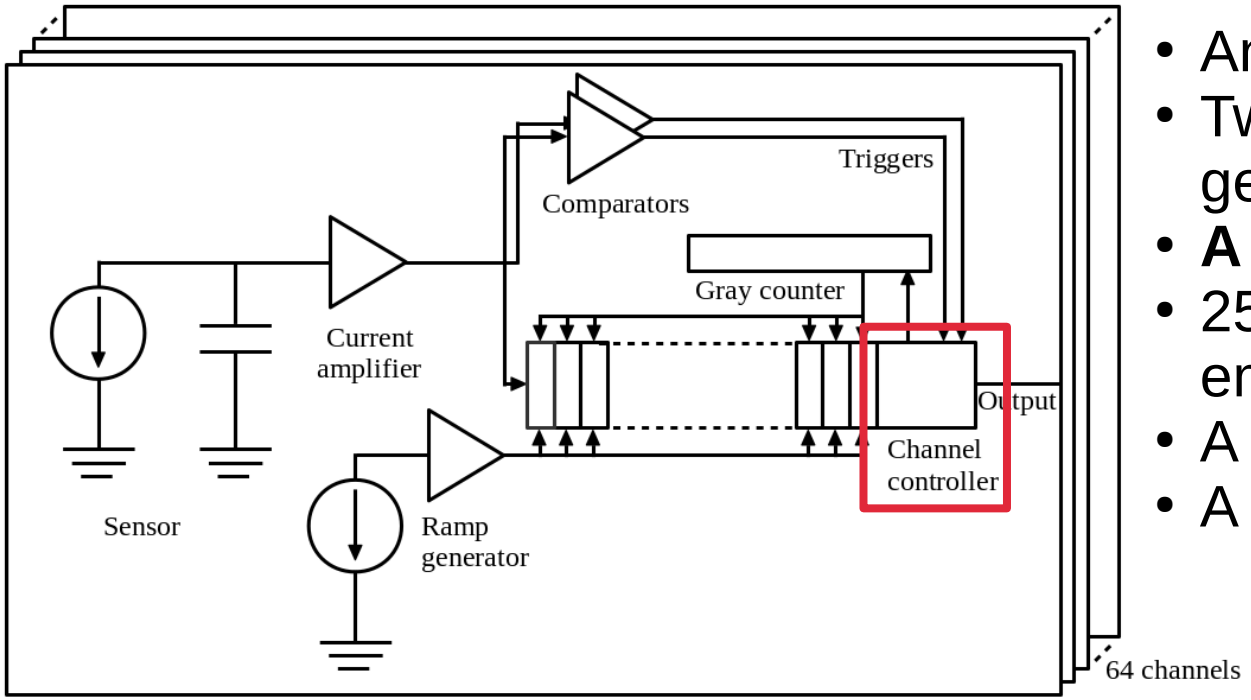
- An input amplifier.
- **Two comparators for hitmaps generation.**
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- A digital Gray counter.



0: sampling, signal is not acquired.

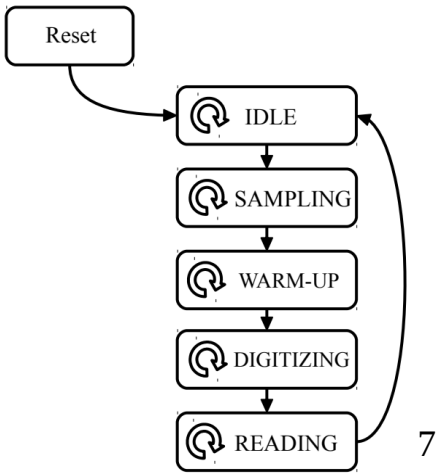
1: sampling, a **trigger** is generated and the signal is acquired.

ASIC architecture

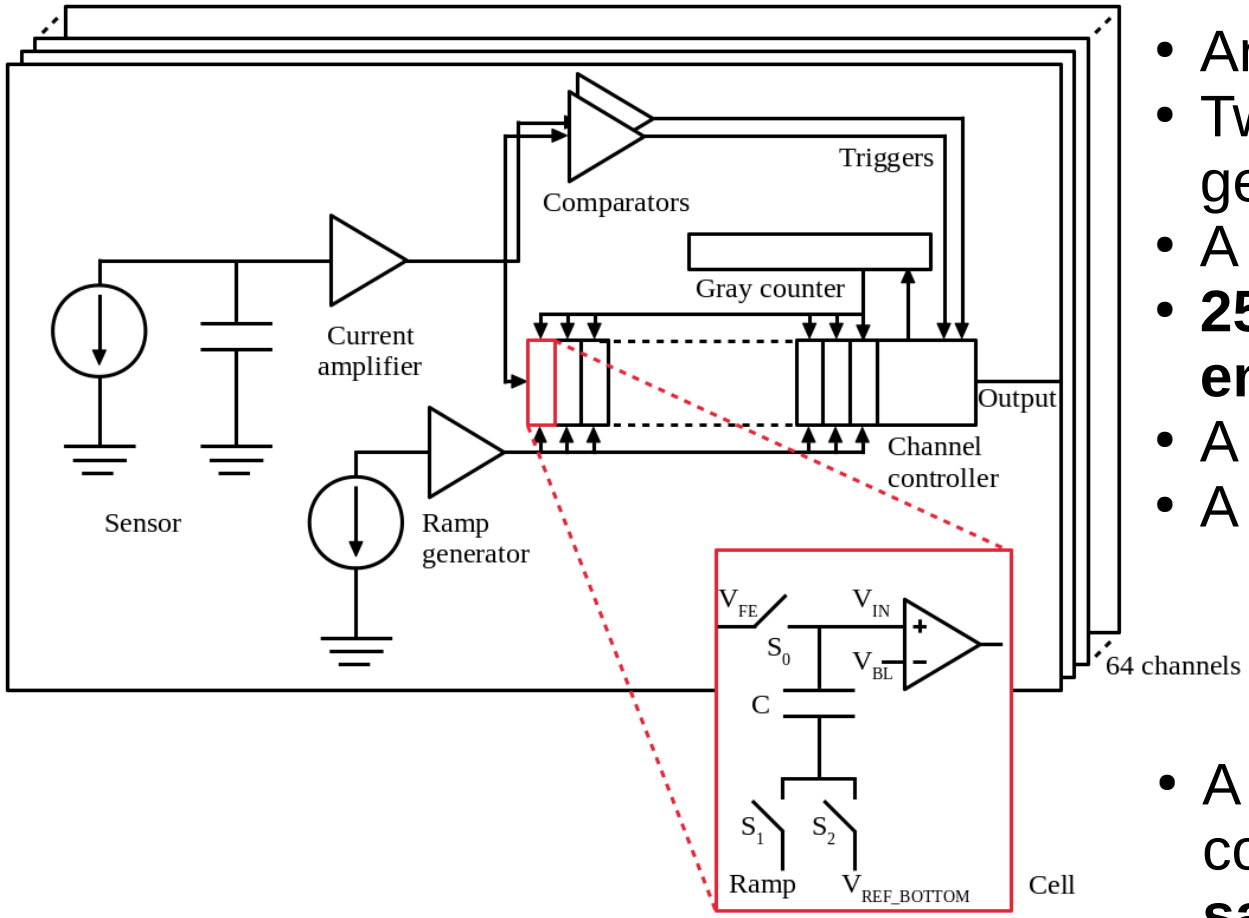


- An input amplifier.
- Two comparators for hitmaps generation.
- **A digital channel controller.**
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- A digital Gray counter.

- Manager of the sections (namely of the cells).
- The cells must address **5 states**: idle, sampling, warm-up, digitizing and reading. These processes are implemented with a **Finite State Machine** (FSM).
- **Channel configurability** (256, 64, 32 cells).



ASIC architecture

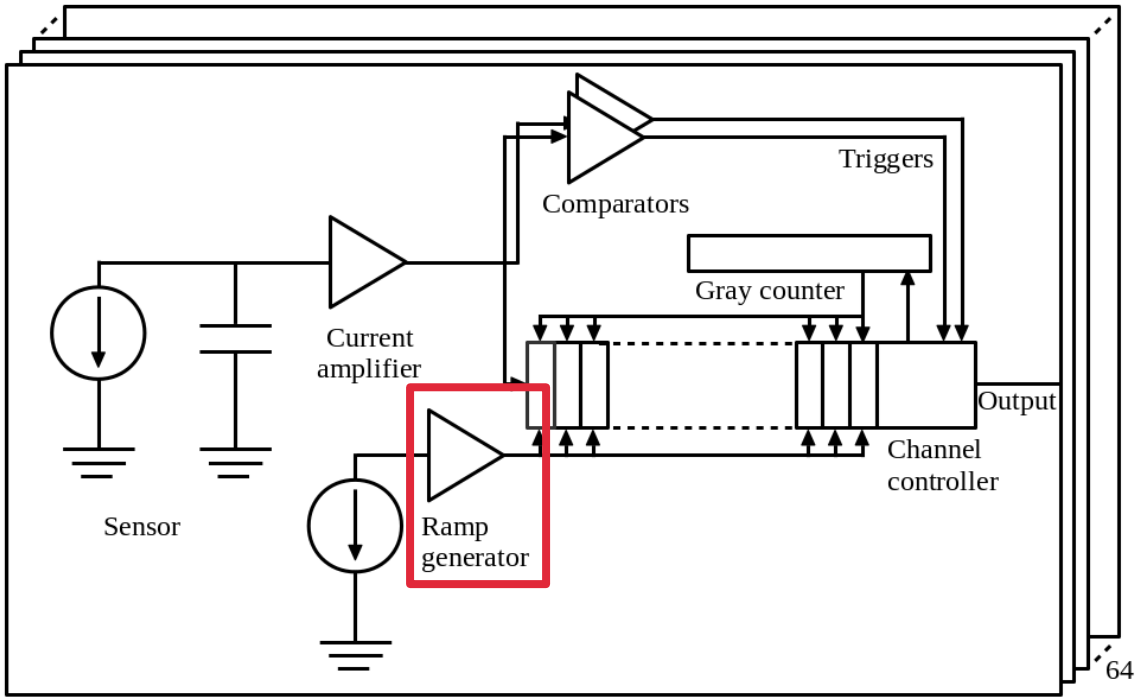


- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- **256 memory cells with embedded Wilkinson ADC**.
- A ramp generator.
- A digital Gray counter.

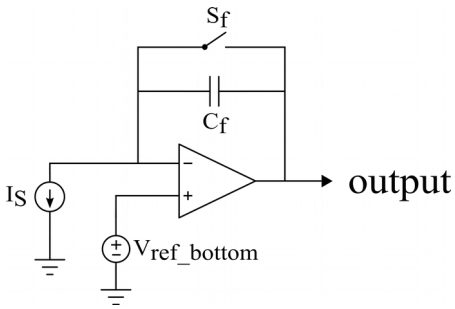
- A single ramp generator is connected to all the cells → **same gain**.

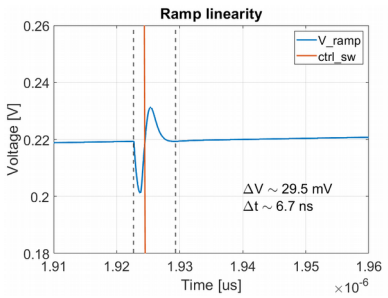
- The 256 cells are partitioned into smaller **segments** to **derandomize** the incoming signal: a group of 32 cells is organized into a **section**. The chip can be configured to operate with 32, 64 or the full 256-cells depth.

ASIC architecture



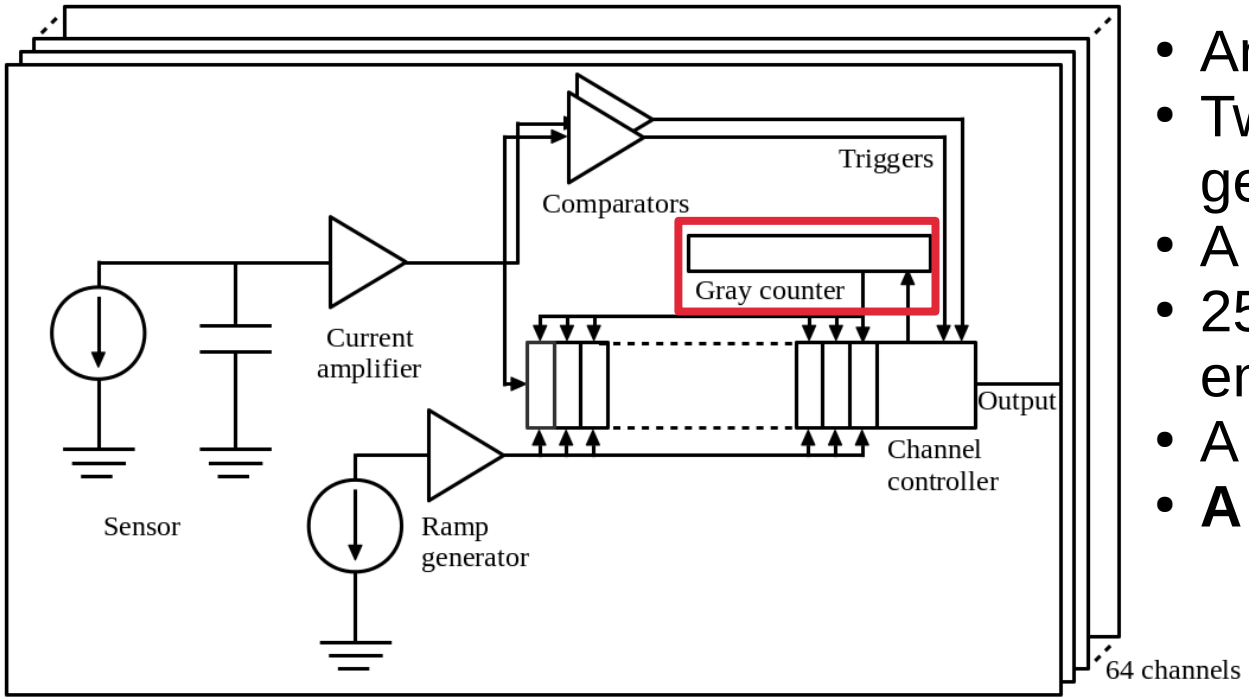
- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- **A ramp generator.**
- A digital Gray counter.





- **Sampling**: the switch is closed so the output is equal to the reference voltage.
- **Conversion**: the switch is open and C_f integrates the current thus providing a ramp.

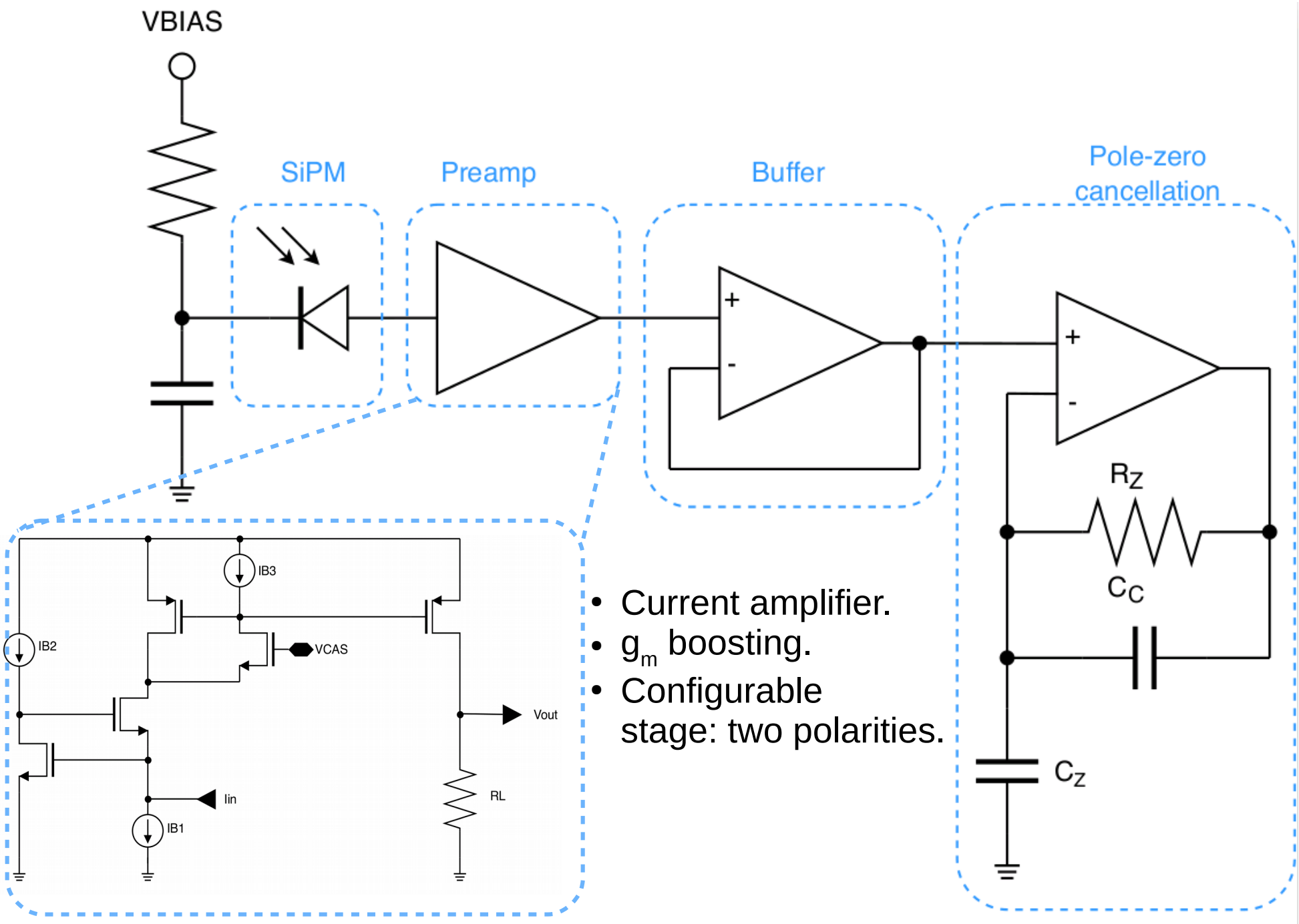
ASIC architecture



- An input amplifier.
- Two comparators for hitmaps generation.
- A digital channel controller.
- 256 memory cells with embedded Wilkinson ADC.
- A ramp generator.
- **A digital Gray counter.**

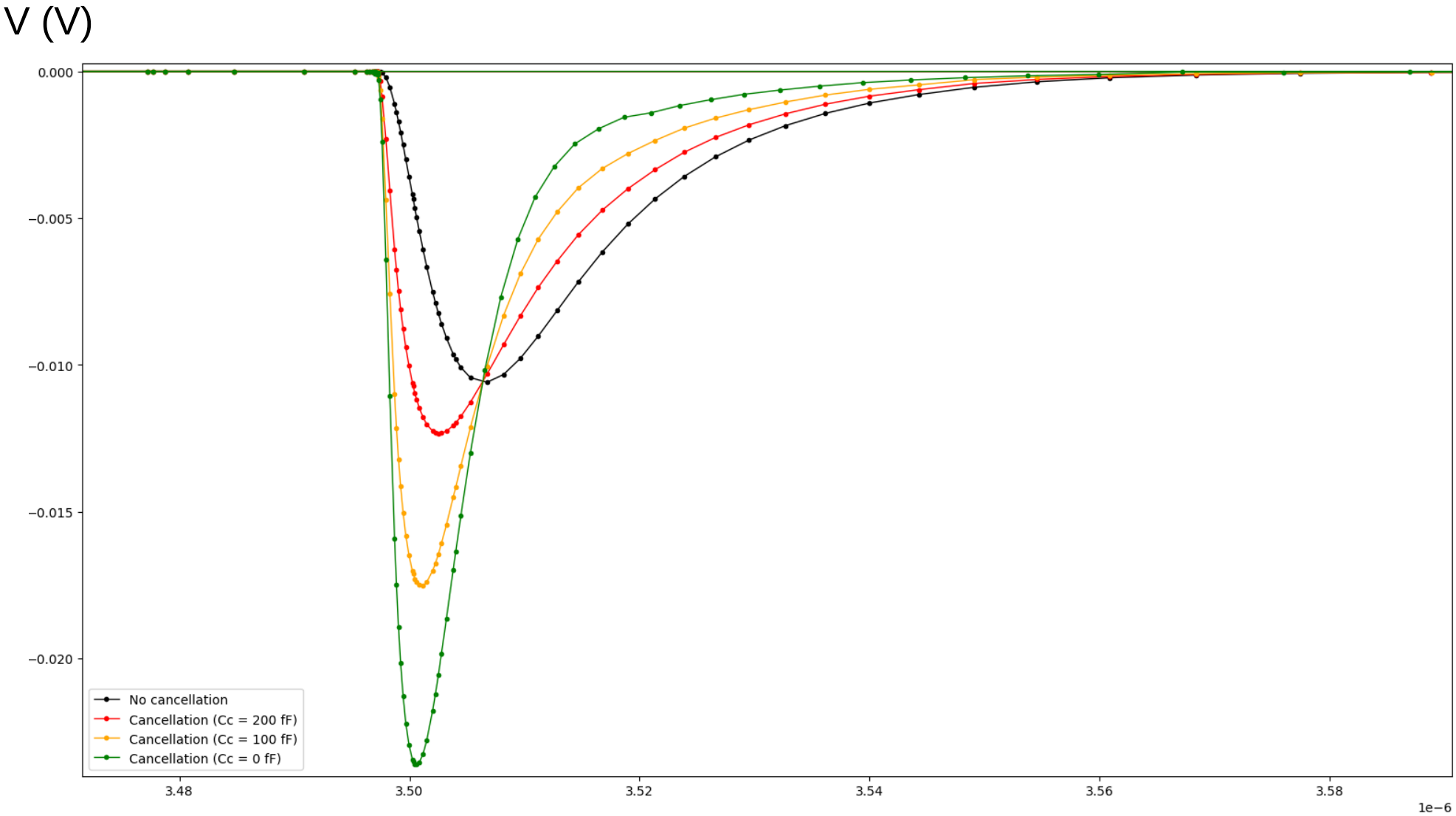
- It is exclusively driven by the channel controller and enabled during the **digitizing** process.
- The counter is progressively increased by one at each clock cycle until the saturation of the counter itself occurs. The ramp generator is accordingly activated during this time window.
- **Configurable** in the range 8-12 bits.

Front-end

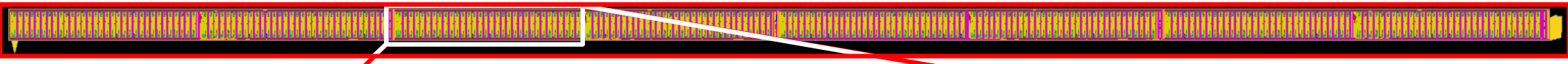


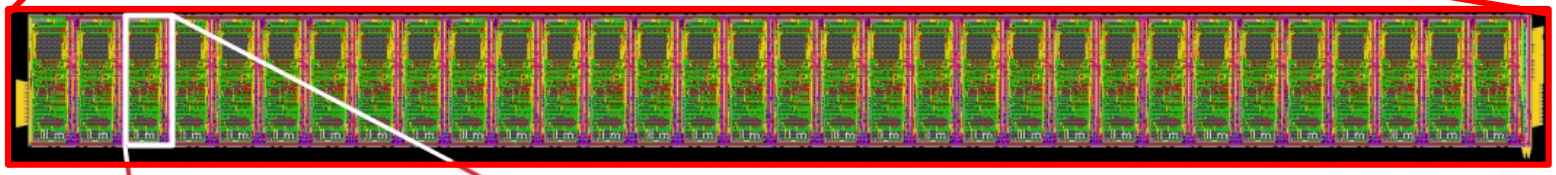
- Current amplifier.
- g_m boosting.
- Configurable stage: two polarities.

Front-end

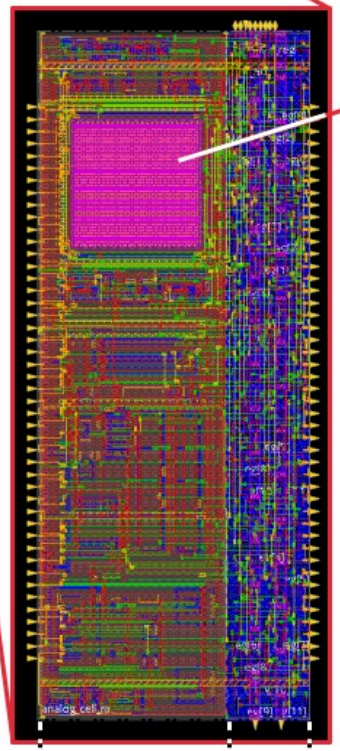

V (V)
0.000
−0.005
−0.010
−0.015
−0.020
3.48
3.50
3.52
3.54
3.56
3.58
1e−6
No cancellation
Cancellation (Cc = 200 fF)
Cancellation (Cc = 100 fF)
Cancellation (Cc = 0 fF)
Time (s)

Place & Route





Section: 32 cells

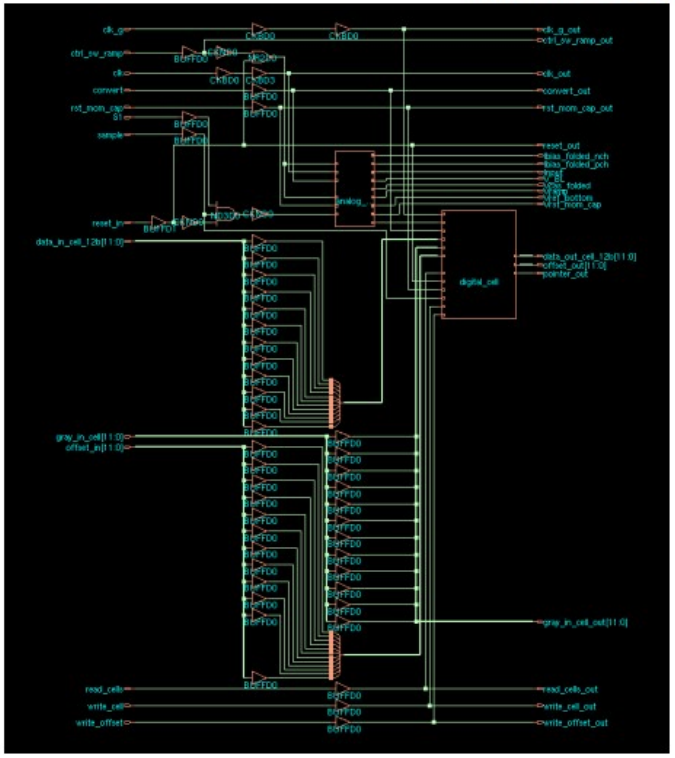


Capacitor

Cell layout

Analog slice

Digital slice



Cell schematic

Cell area: 20 x 44 μm²

Power

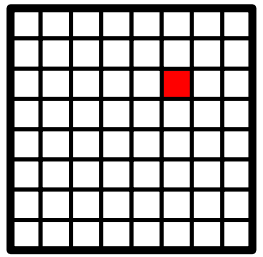
Block	Power (μW)	Area (μm^2)	N	Power$_T$ (μW)	Area$_T$ (μm^2)
Cell	2.5	352.44	256	640	90224.64
Section	2.5	96.48	8	20.0	771.84
Section controller	31.36	839.88	4	125.44	3359.52
Gray counter	42.4	376.20	1	42.4	376.20
Gray decoder	2.86	357.48	1	2.86	357.48
Channel controller	430	8083	1	430	8083
Total				1260.7	103172.68

- Worst case, low power library.
- Estimation before P&R, based on the area of standard cells (no routing).
- Imaging mode.
- Segmentation 32.
- clock gating enabled.
- Range: 2135 ns (from sampling to readout stage) at f_s = 200 MHz.

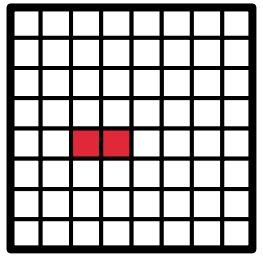
Readout

Hitmap generation.
Steps:

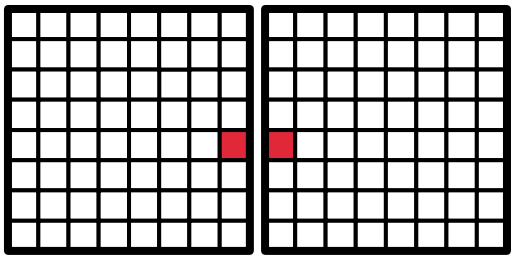
- Comparator values are stored in latches.
- Low level trigger evaluated: first hitmap (ASIC level).
- High level trigger evaluated: second hitmap (ASIC level).
- Read hitmap request generated.
- Acknowledge signal from FPGA.
- Sending hitmap to FPGA (130 ns at 400 MHz in DDR).
- Read data request generated.
- Acknowledge signal from FPGA.
- Sending data to FPGA.



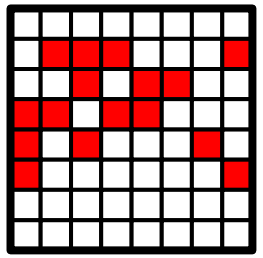
High threshold



Low threshold



On the edge



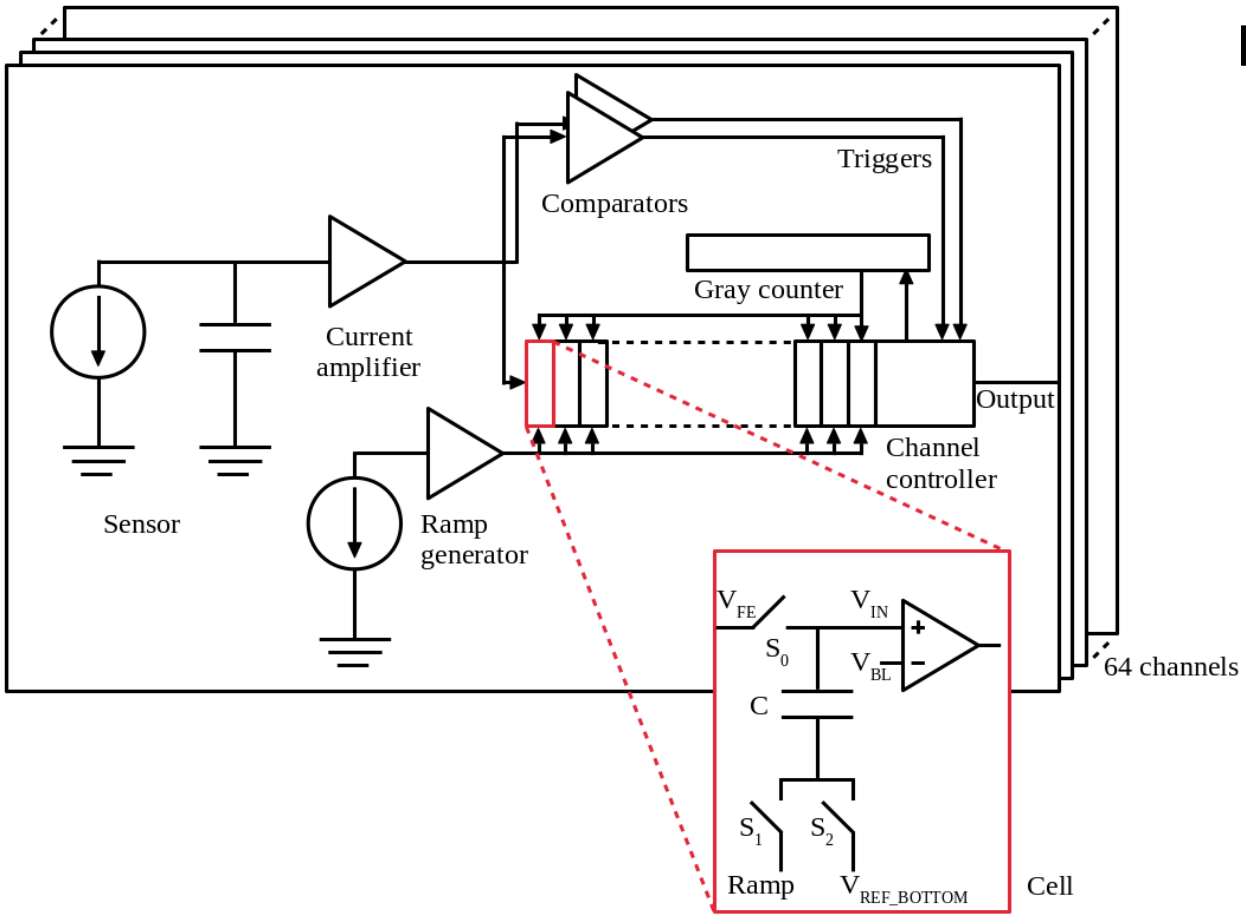
Light pollution

Summary

- Detection of Extensive Airshowers.
- 64-channel ASIC implemented in a commercial 65 nm CMOS technology.
- High level of configurability:
  - Segmentation:
    - 32 cells
    - 64 cells
    - 256 cells
  - Resolution:
    - 8 - 12 bits
  - Trigger:
    - Internally generated
    - Externally provided
  - Mode:
    - Sparse
    - Imaging
- **Production run** before the summer.

Backup

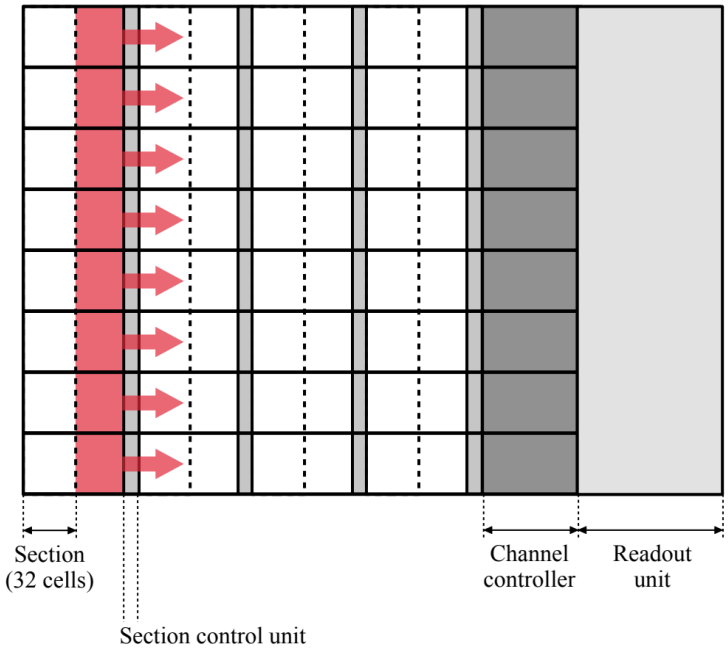
ASIC architecture



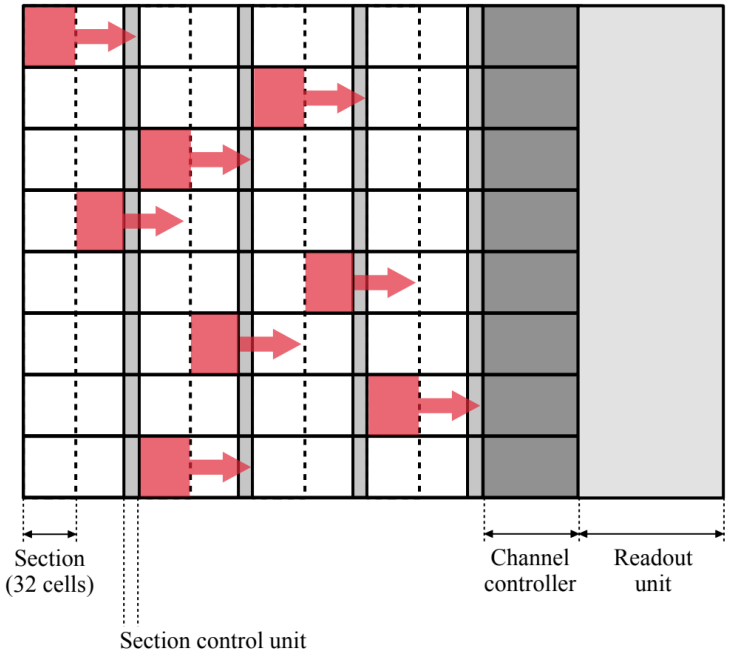
Design status:

- Mode:
  - Sparse
  - Imaging
- Segmentation:
  - 32 cells
  - 64 cells
  - 256 cells
- Resolution:
  - 8 - 12 bits
- Trigger:
  - Internally generated
  - Externally provided
- 8-channels readout

Mode



Imaging mode



Sparse mode

Derandomization

The input signal follows the Poisson distribution. The probability of receive n events is:

$$P_n = \mu^n \frac{e^{-\mu}}{n!}$$

Supposing to have an event rate of **100 kHz**, and a dead-time of **8 μs**, the probability of loosing an event is:

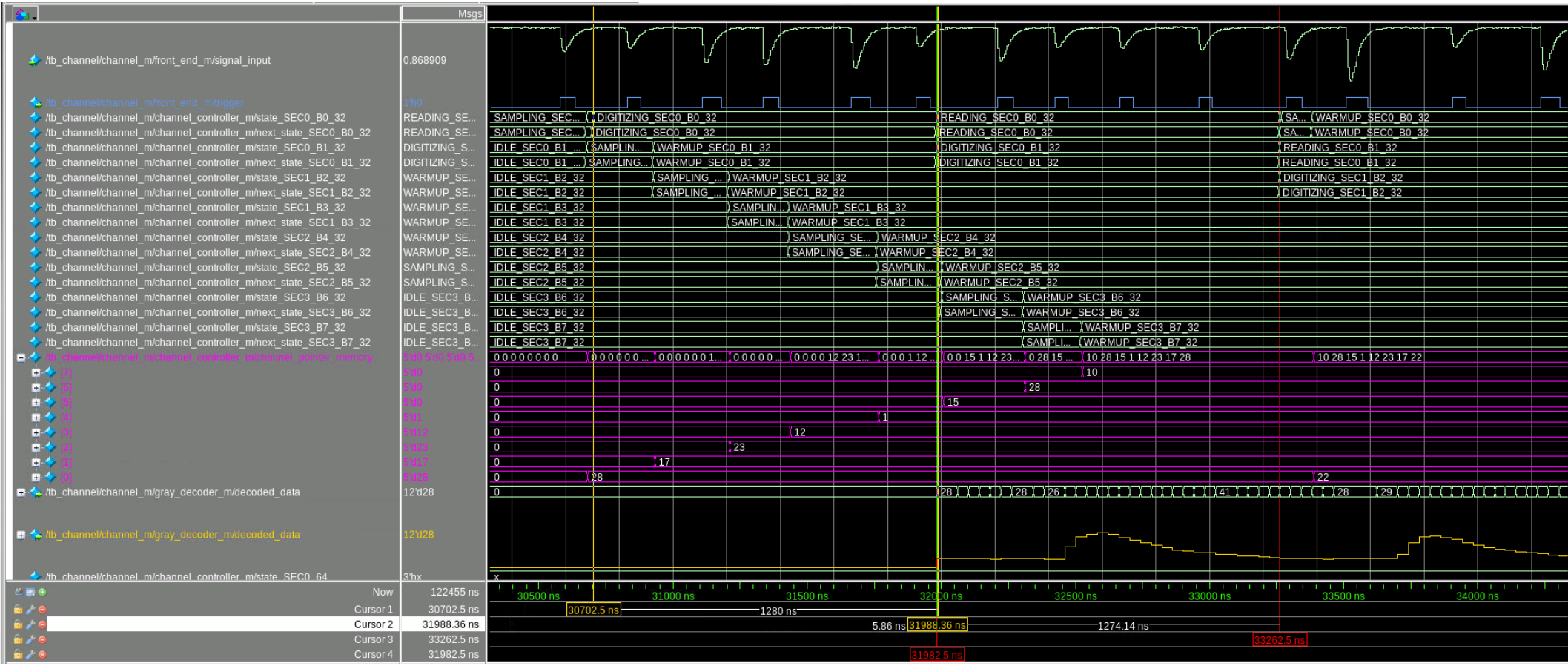
$$P_{loss} = 1 - e^{-0.8} \simeq 0.55$$

By using **n segments** this probability is evaluated as:

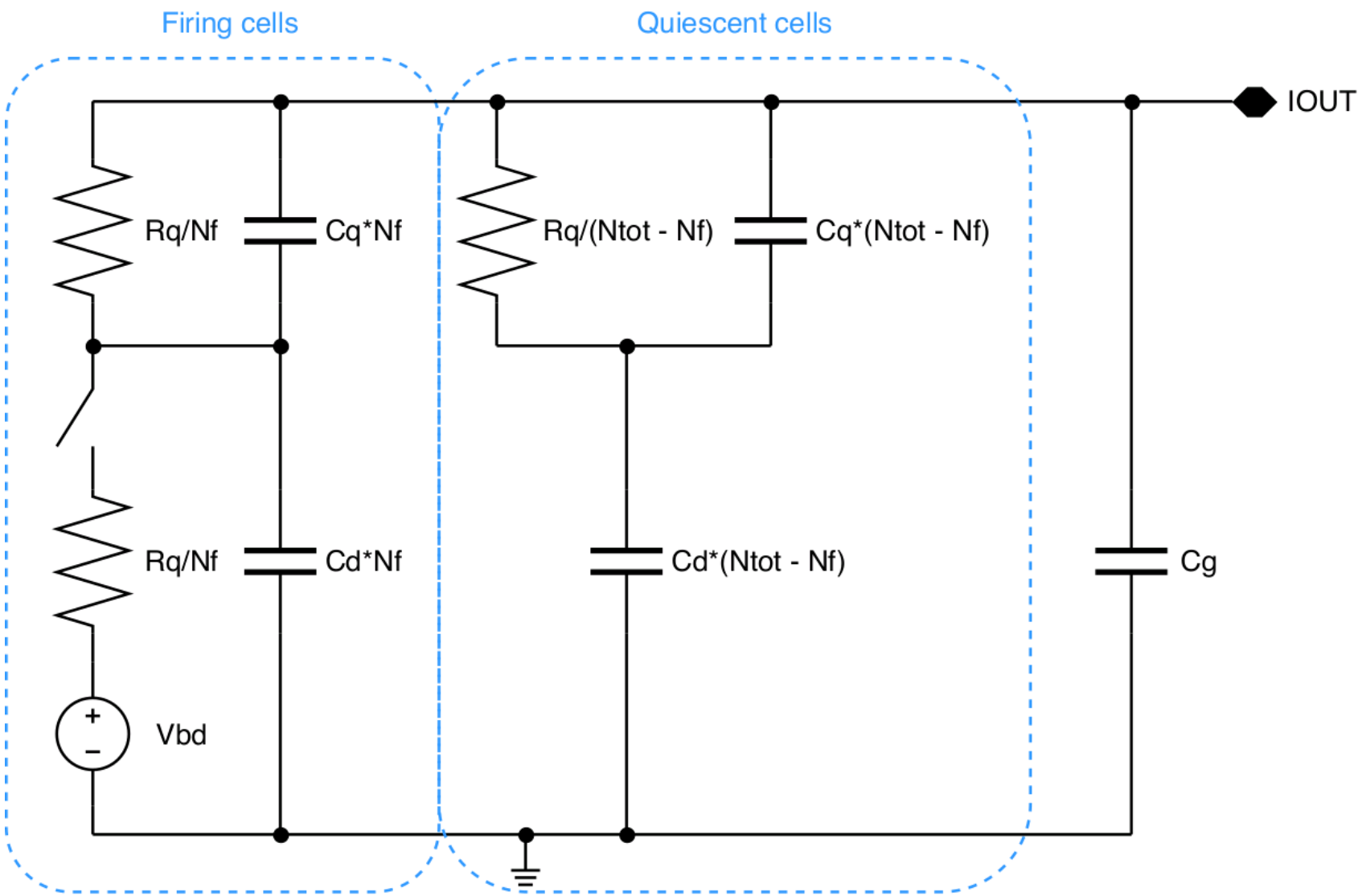
$$P_{loss} = 1 - \sum_0^n \mu^n \frac{e^{-\mu}}{n!}$$

With 4 segments P_{loss} would be equal to about 0.5%

Channel controller simulation



SiPMs



SiPMs: FBK, pitch of 25 μm, 3 x 3 mm, 2 arrays of 8 x 8 pixels.

SiPMs

- Background:
  - Radiation damage.
  - Background photons due to scintillation processes or fluorescent materials.
  - A signal can be directly induced in SiPM by high charge ions.
- By considering a **threshold** at 7 photon-electrons, the estimated **background rate** is ~1 kHz and it will rise up to 200 kHz.
- The estimated **event rate** is ~100 events per year.
- The estimated **total dose** is ~1 krad/year.
- The expected **Dark Count Rate** (DRC) is ~ 22 Mhz at the end of the mission (3 years).

Power

Block	Power (μW)	Area (μm^2)	N	Power$_T$ (μW)	Area$_T$ (μm^2)
Cell	2.5	352.44	256	640	90224.64
Section	2.5	96.48	8	20.0	771.84
Section controller	31.36	839.88	4	125.44	3359.52
Gray counter	42.4	376.20	1	42.4	376.20
Gray decoder	2.86	357.48	1	2.86	357.48
Channel controller	430	8083	1	430	8083
Total				1260.7	103172.68

- Digital block designed for the readout of a group composed by 8 channels (this circuit is not included in the table):
  - Digital readout controller: area 2896 μm², power 0.3495 mW
  - Serializer: area 896 μm², power 0.1464 mW.
  - Divided by 8: + ~0.06 mW per channel.