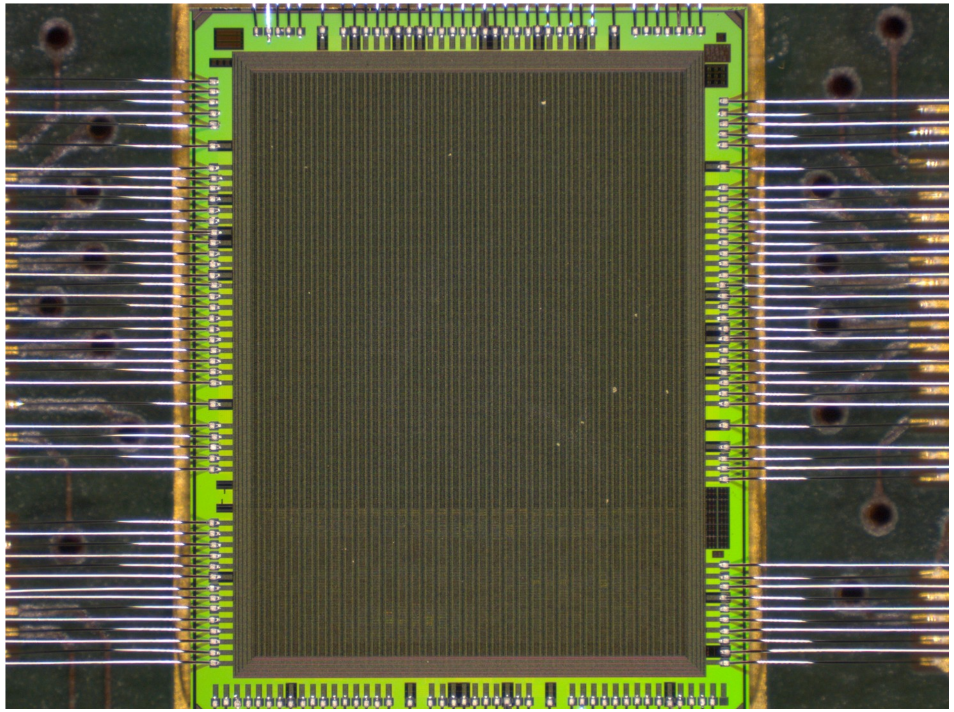
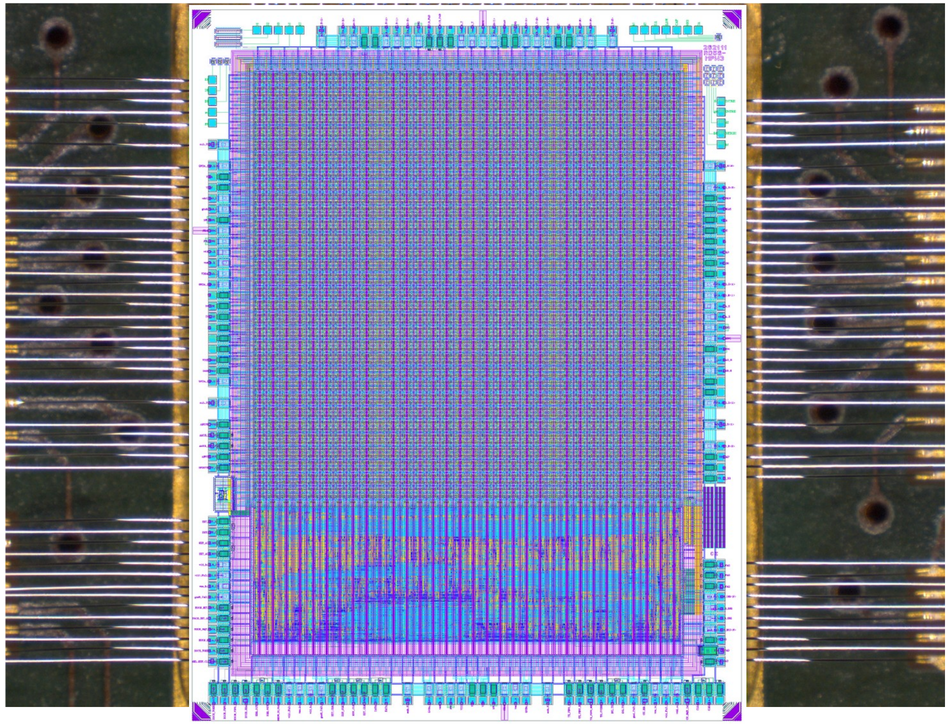
Performance of the RD50-MPW3 HV-CMOS Detector





TREDI 2023

Uwe Kraemer on behalf of RD50

01 Mar. 2023

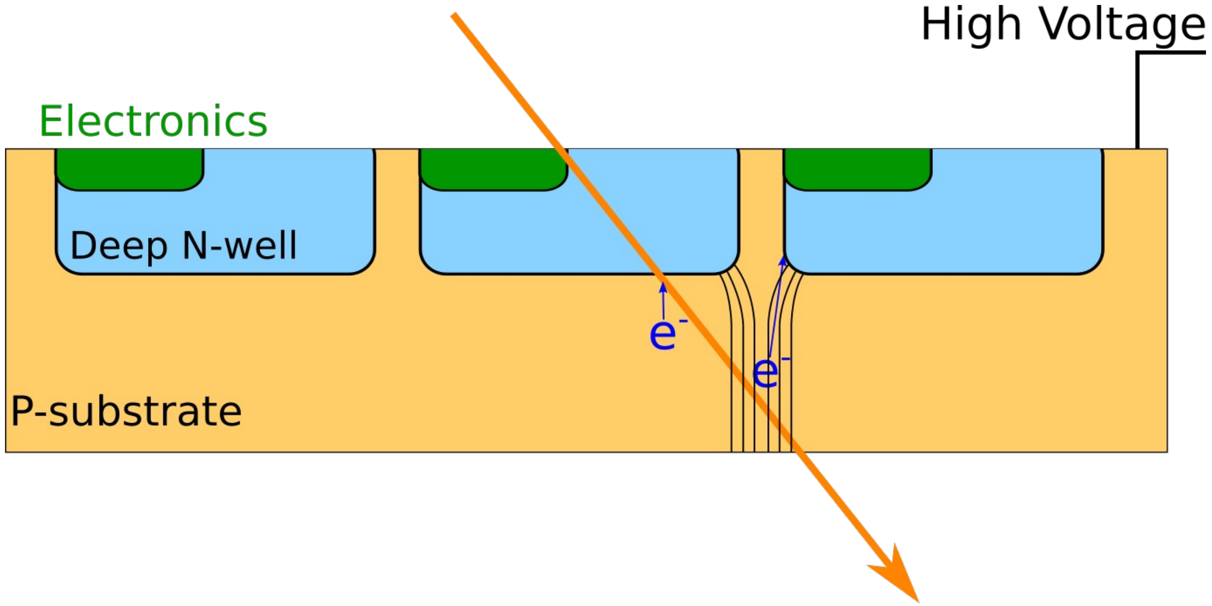
CERN-RD50 Collaboration

- CERN-RD50
  - 66 institutes, more than 400 members
  - Development of radiation hard semiconductor detectors

- CMOS working group
  - 17 institutes
  - Focus on radiation hard monolithic CMOS sensors
    - ASIC design
    - TCAD simulations
    - DAQ development
    - Chip characterization

HV-CMOS for radiation hard depleted MAPS

- Electronics embedded in a large deep N-doped well to shield from high voltage
  - Allows for application of ~O(100 V) reverse bias
    - Large depletion zone
    - Fast charge collection
      - → Less sensitive to trapping
      - → Improved time resolution



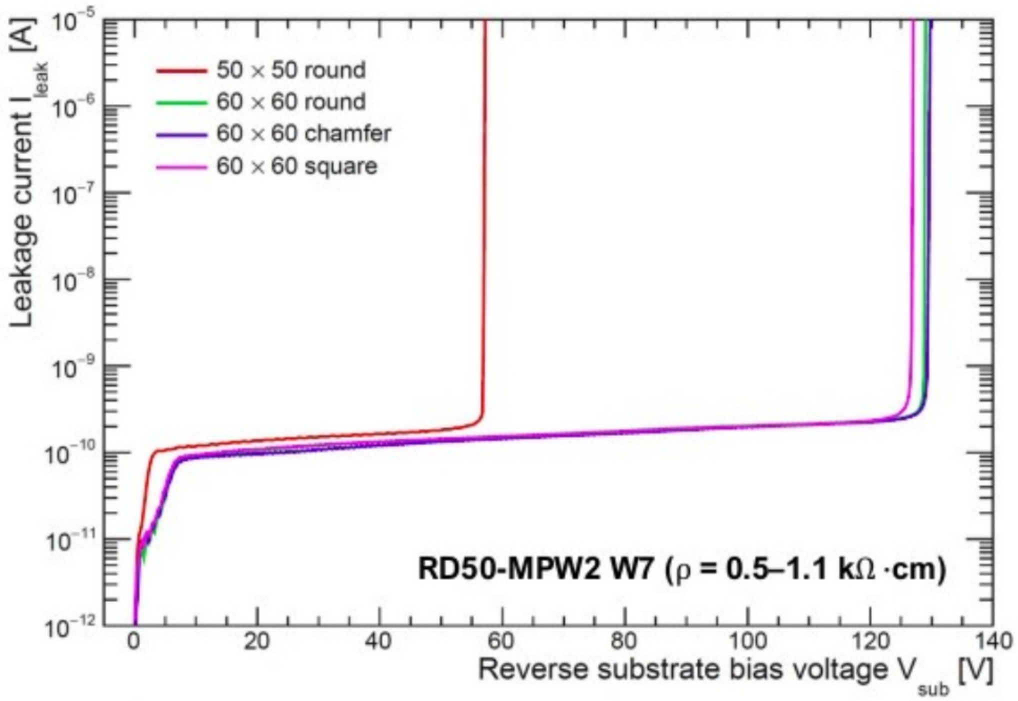


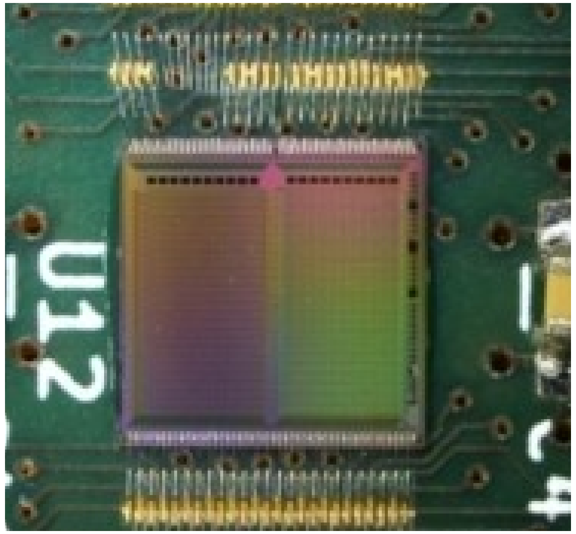
Fig.: IV of the MPW2 HV-CMOS (Vertex 2020)

The RD50 DMAPS sensors

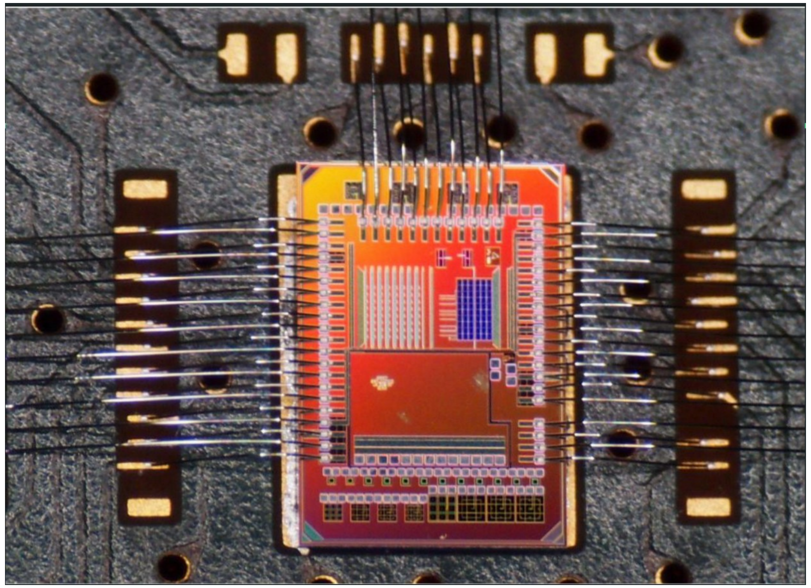
- Currently three iterations of Depleted Monolithic Active Pixel Sensors (DMAPS) as part of RD50 project
  - All manufactured by LFoundry in 150 nm HV-CMOS process
  - Recent prototype RD50-MPW3 was delivered in July 2022

2017 | 2019 | 2022

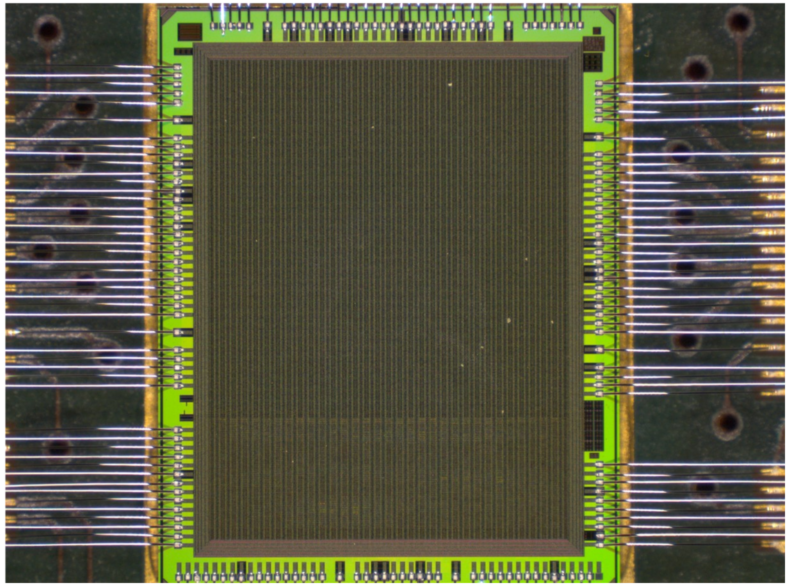
RD50-MPW1



RD50-MPW2

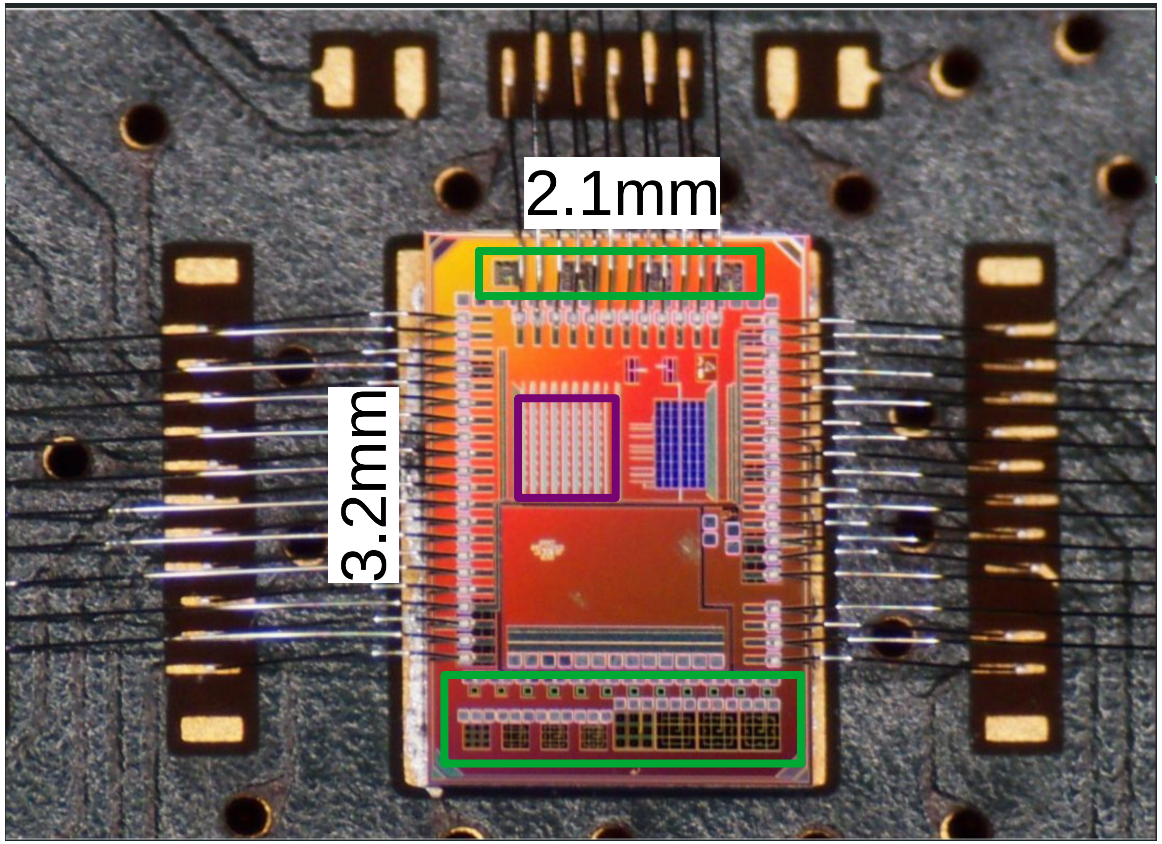


RD50-MPW3



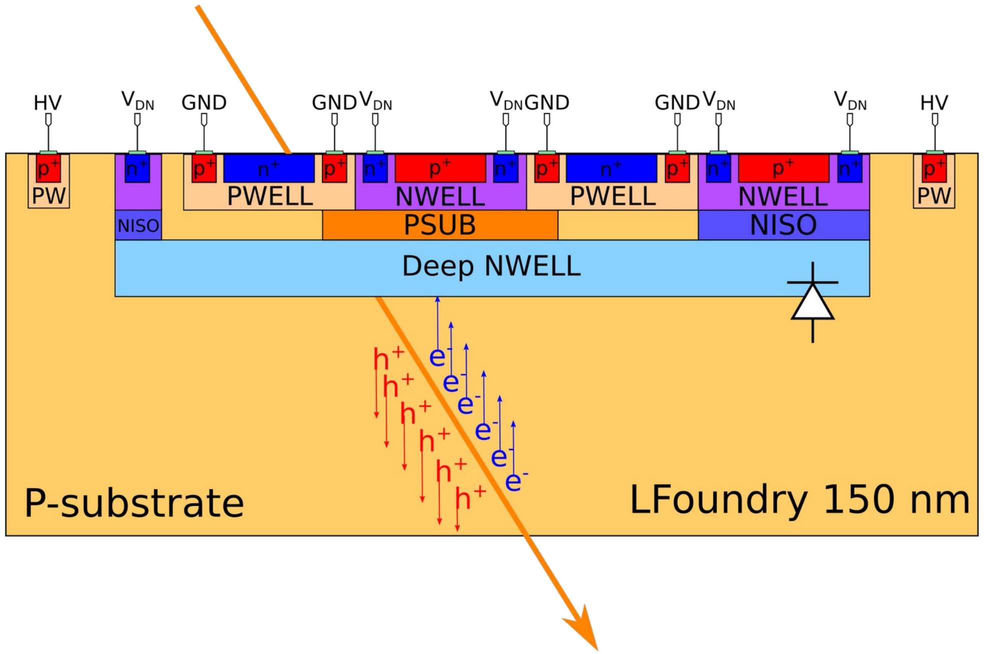
MPW2, the previous generation

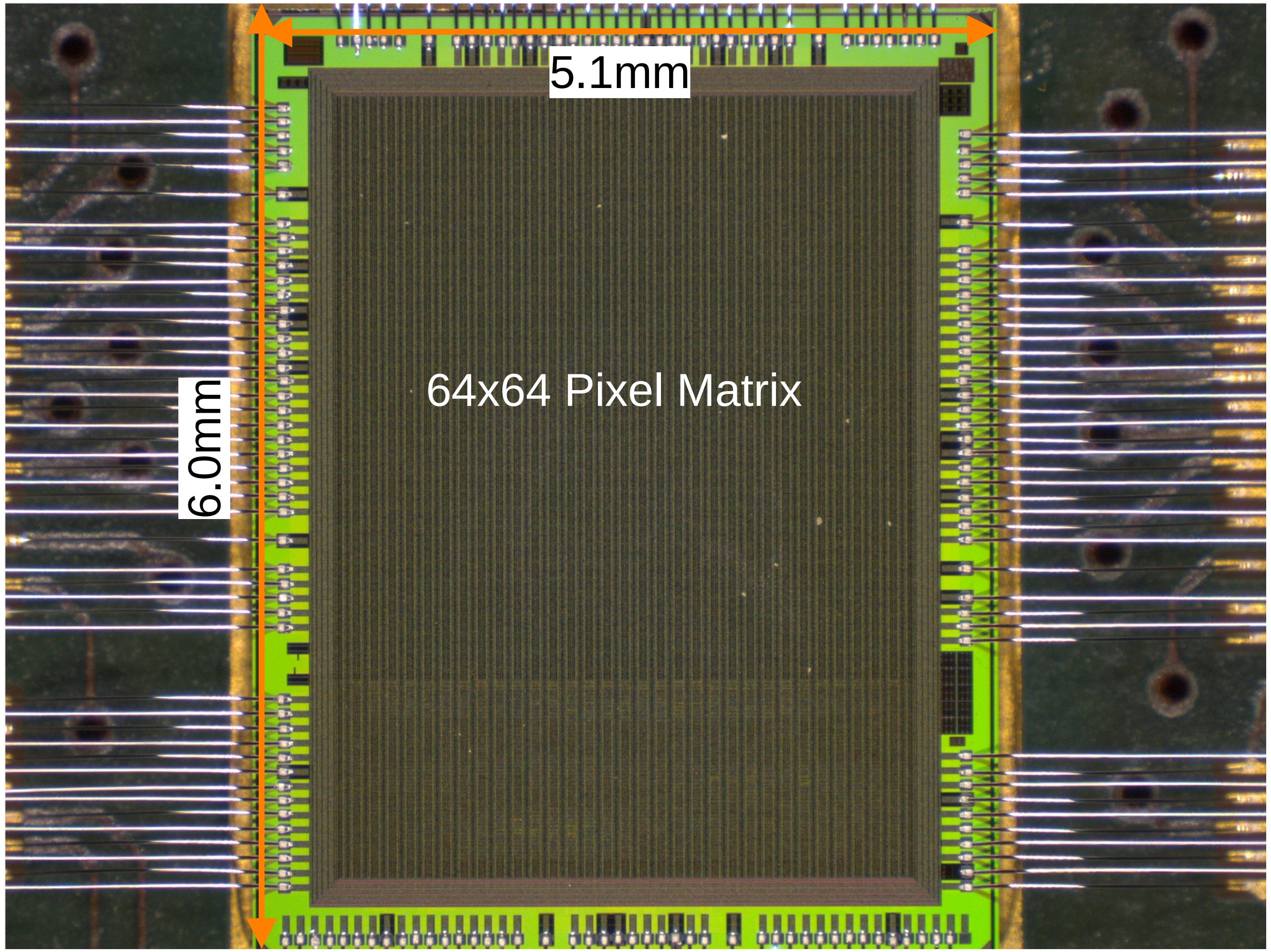
- 8x8 pixel matrix
- Two pixel flavors
- Large variety of test structures
- Purely analog readout
- Depletion depths of ~190 µm
- Produced in 1.9 kΩ·cm and 3.0 kΩ·cm resistivities



The RD50-MPW3

- CMOS chip with full analog and digital electronics
- 1.9 kΩ·cm and 3.0 kΩ·cm resistivities
- 320 MHz input clock





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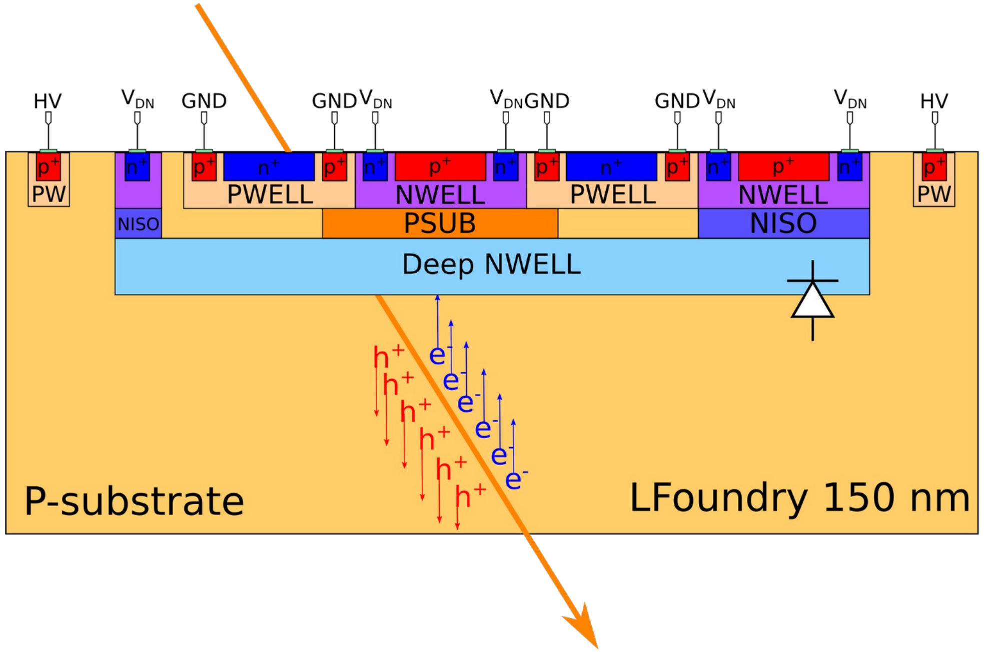
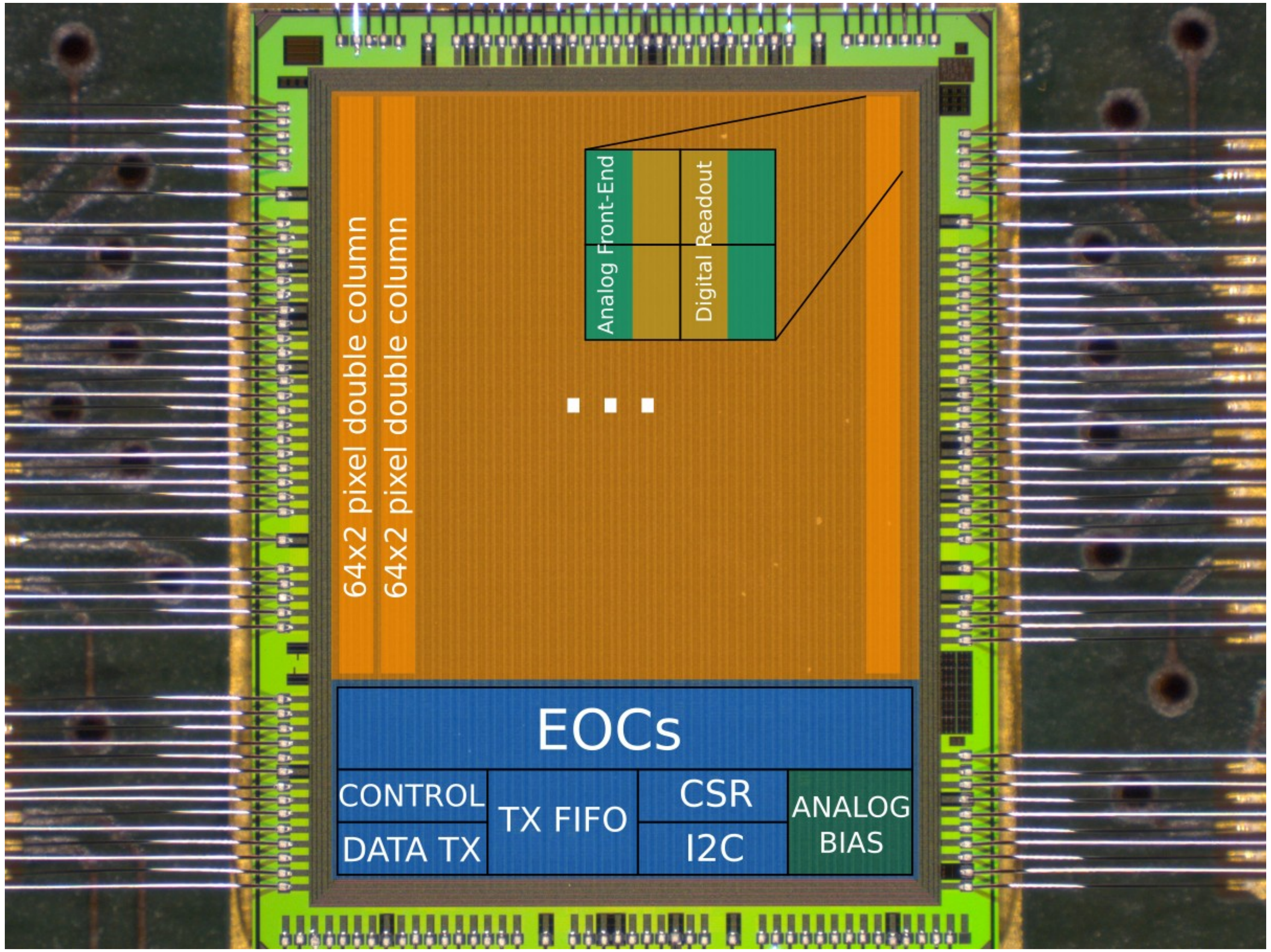
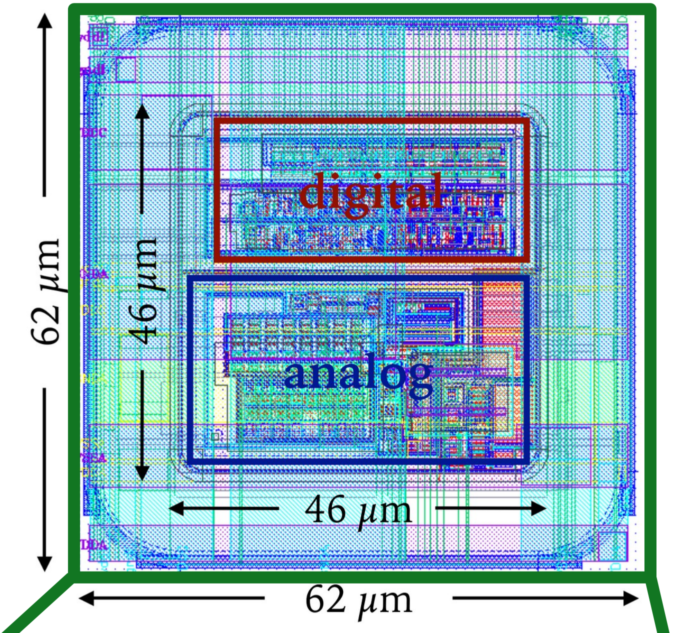
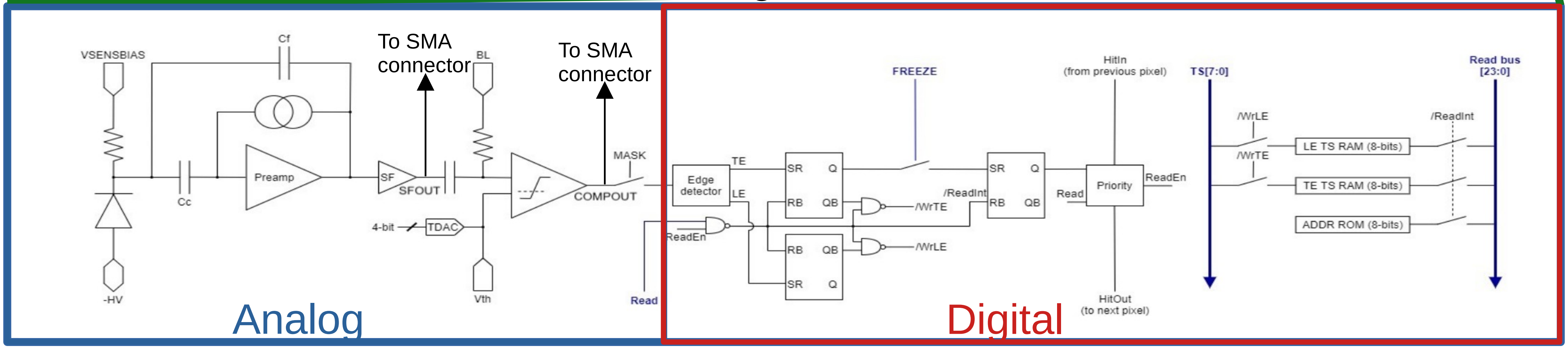




The pixel logic

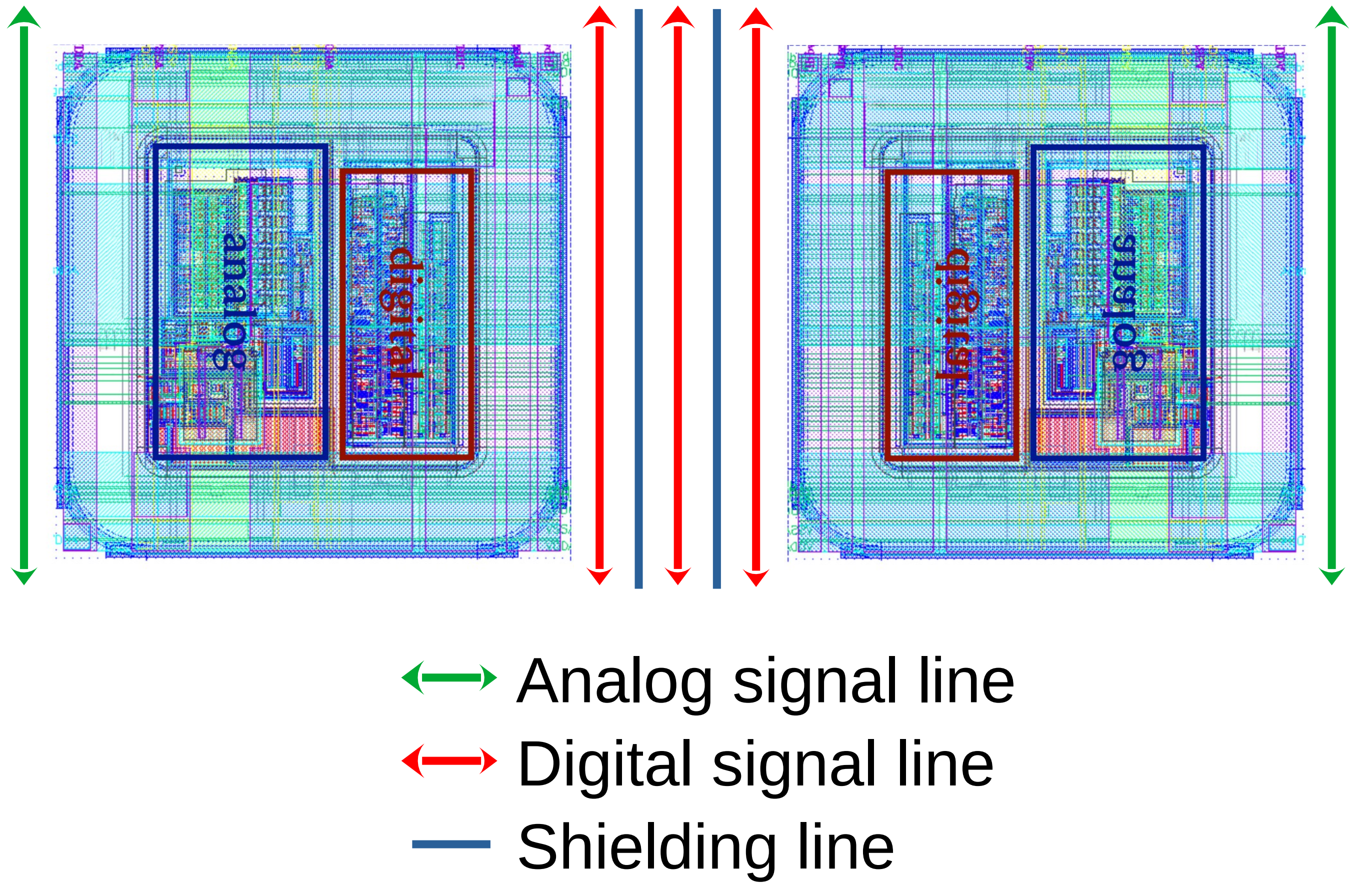
- Inherited analog pixel design from MPW2
  - 4-bit trim DAC for threshold adjustment
  - Continuous reset current readout
  - Injection circuit for calibration
  - Routing of analog pixels to SMA
- Digital logic newly integrated
  - 8-bit timestamp of leading and trailing edge
  - Double column drain readout and rolling shutter





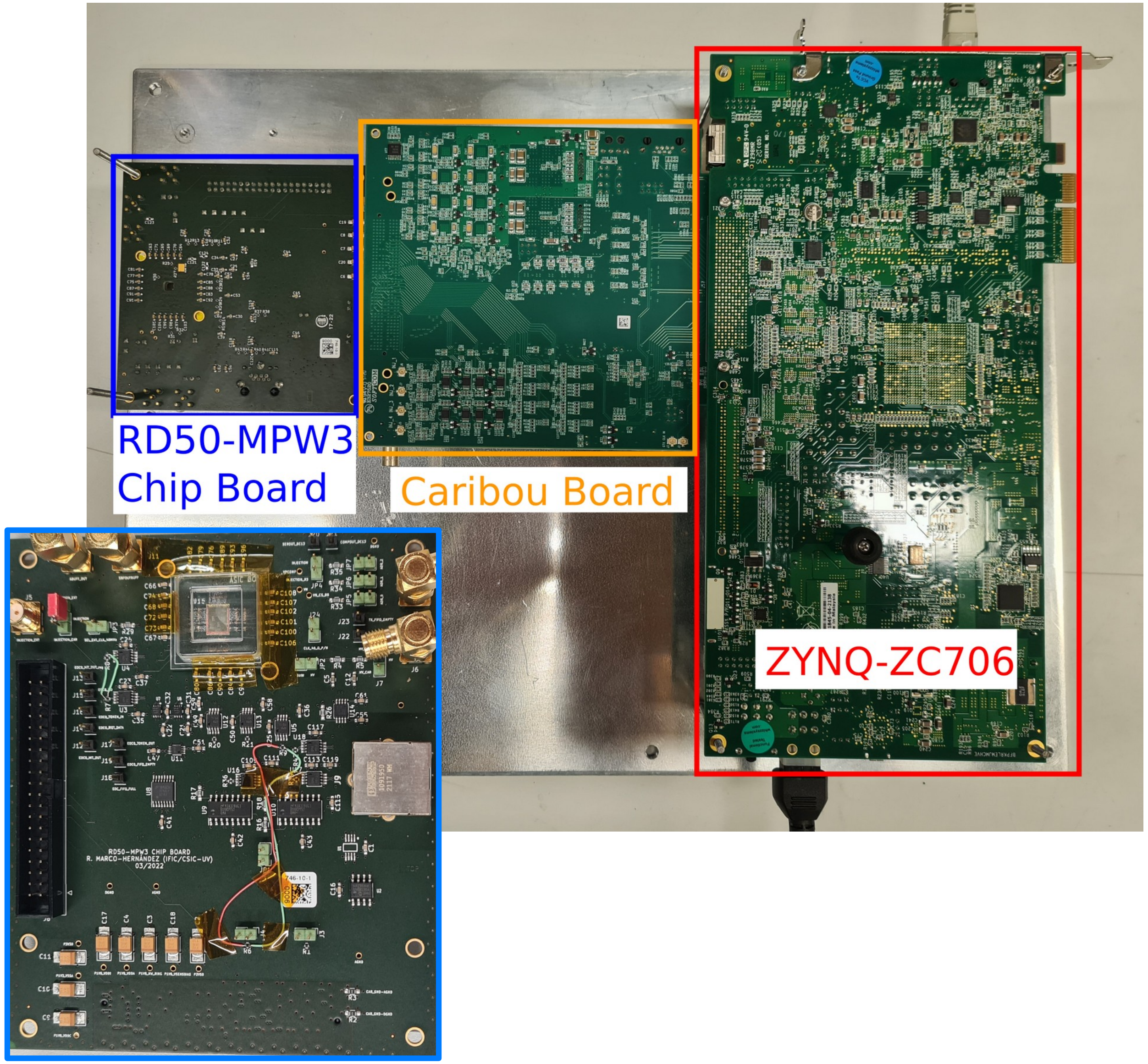
Double column readout

- Pixels within double column are mirrored
- Double columns with digital signal line in between pixels
- Columns are separated by analog signal lines
- Voltage via mesh from all sides



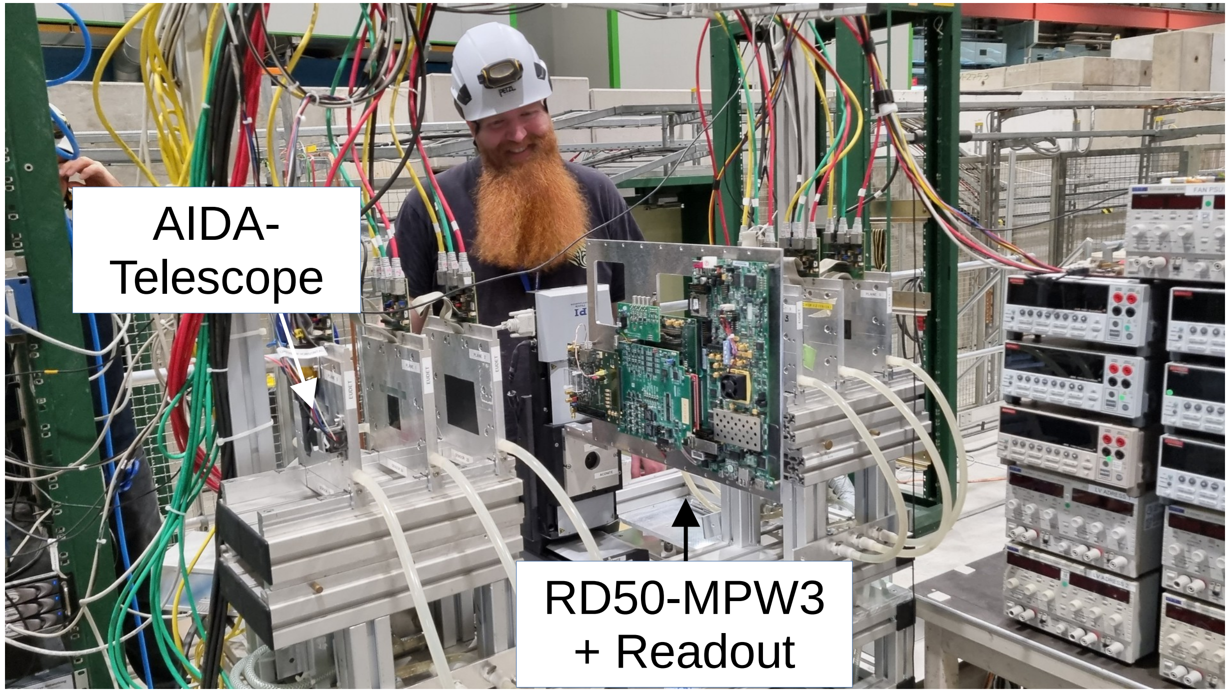
DAQ system

- Chip readout based on Caribou readout system
  - ZYNQ-ZC706 with Yocto based linux
  - Caribou for power distribution
  - Custom chip carrier board
    - Allows chaining of second chip board
    - SMA connectors to probe analog outputs from circuitry



SPS test beam campaign

- SPS test beam week in October 2022
- Placed within SPS proton beam line
- EUDET-type telescope used as reference
  - Based on Mimosa26
    - 115 μs rolling shutter frame readout
    - No timestamps
    - O(1 μm) track resolution
- Synchronized data taking via AIDA TLU using EUDAQ2
- Analysis using Corryvreckan



Spatial matching

- AIDA Telescope provides reference tracks
- Only accepted hits matched to tracks are shown in further results
- For in-pixel measurements the interpolated track position is used

90 µm corresponds to 5 sigma binary resolution

Cluster size distribution

- 94% 1 hit clusters
- Homogeneous distribution of 1 hit clusters within pixel
- Reduction towards the edges due to charge sharing

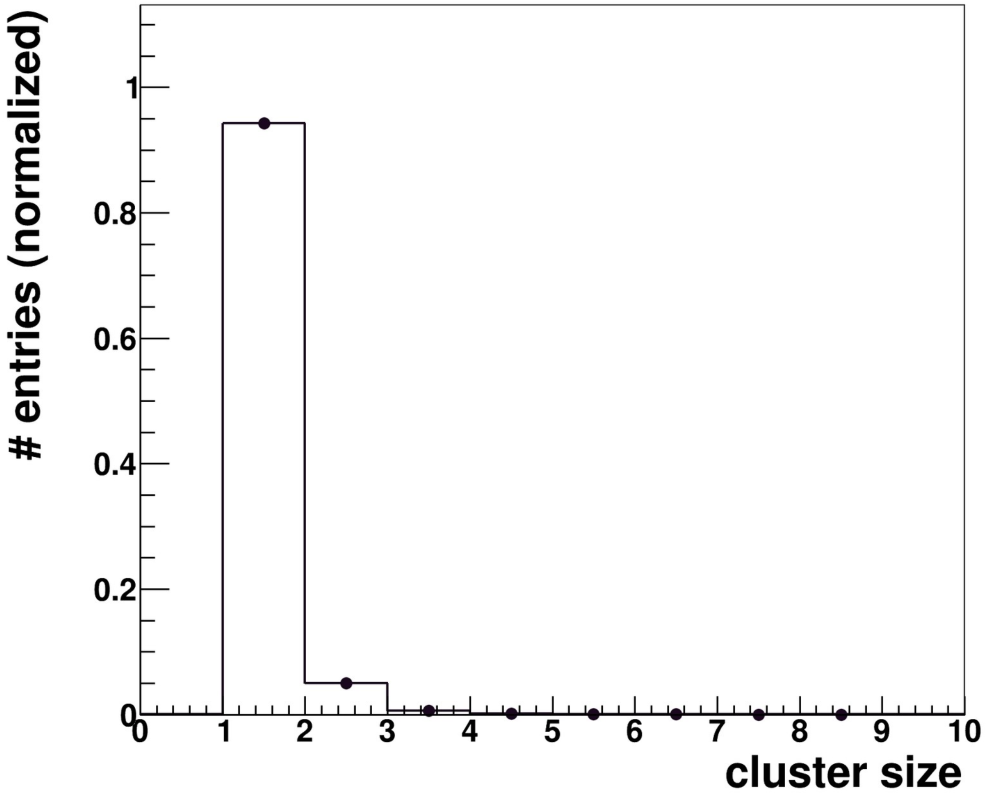


Fig.: Cluster size distribution

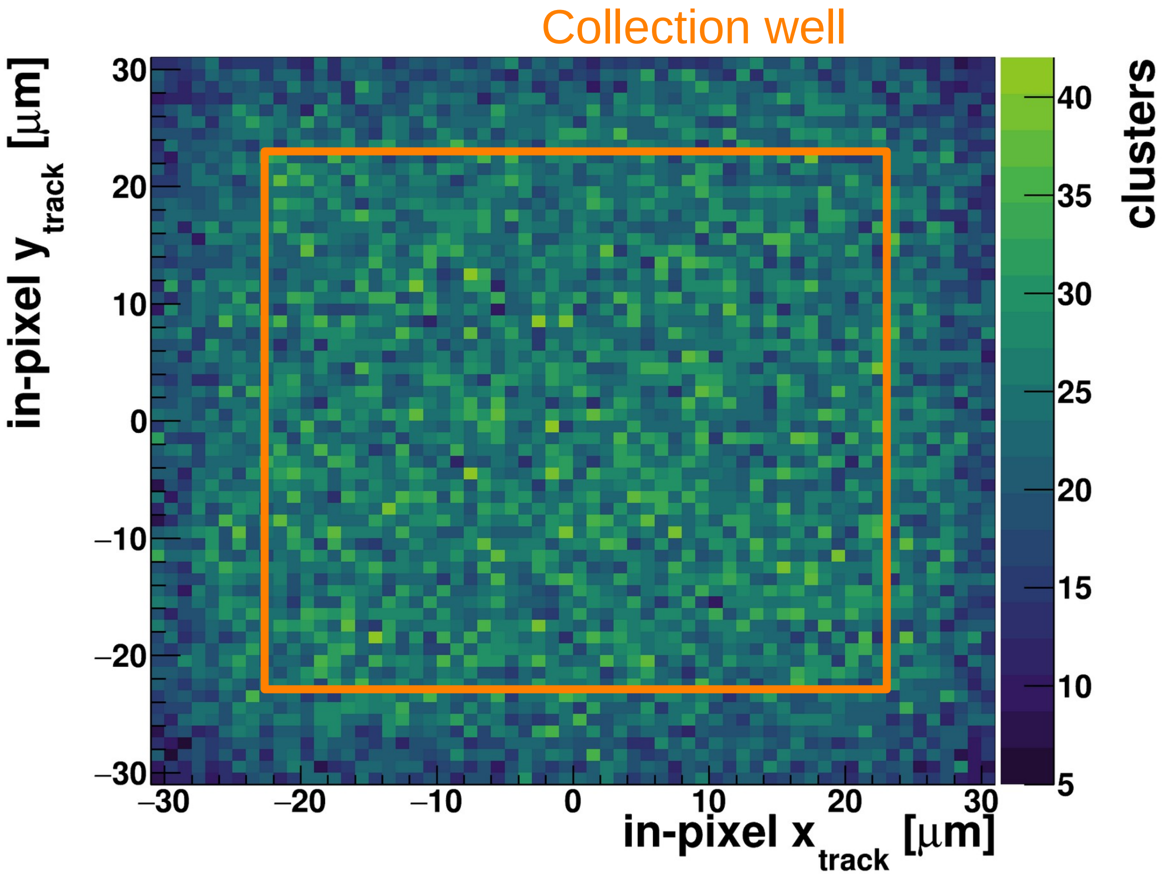
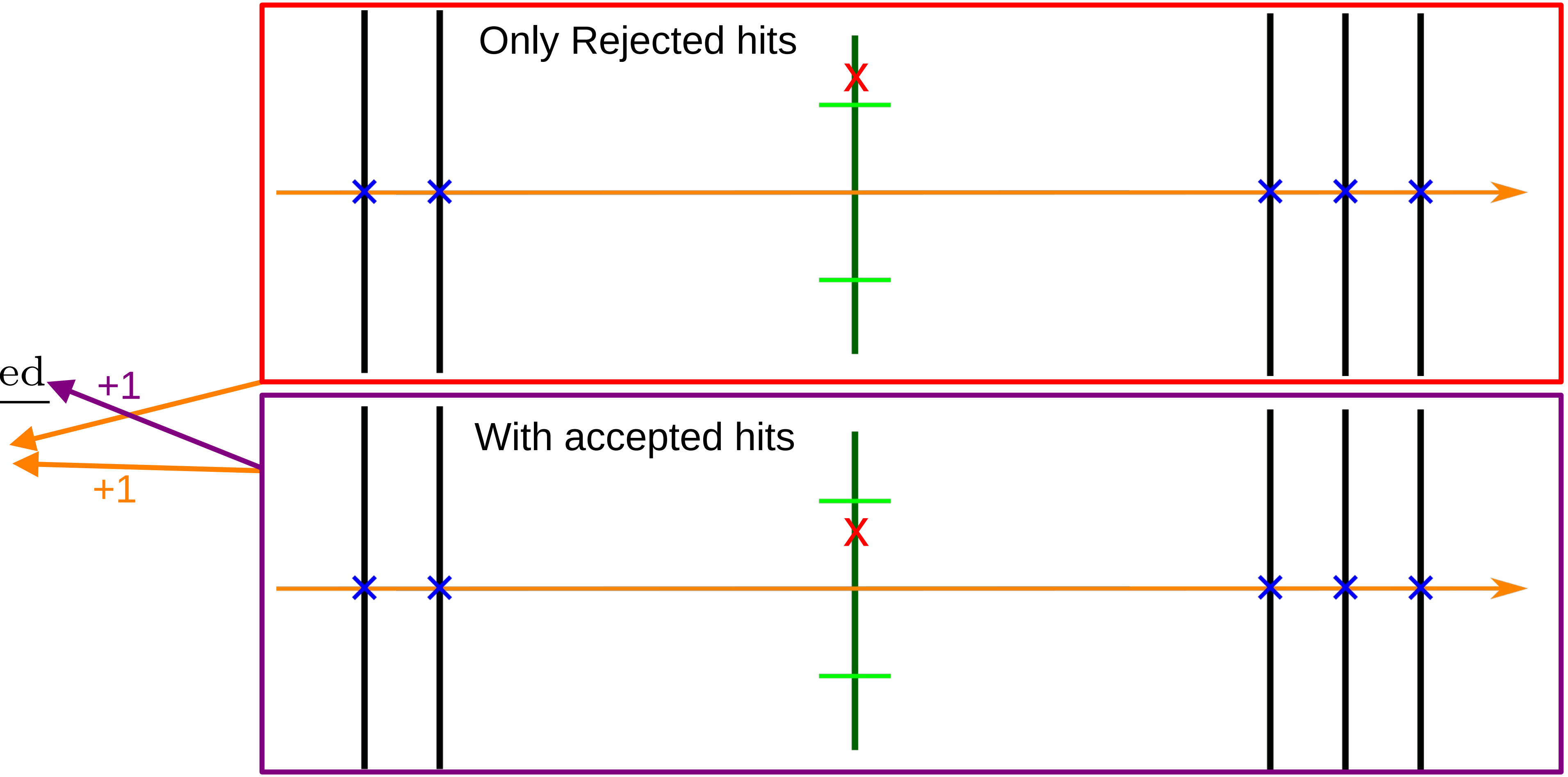


Fig.: In-pixel distribution of 1 pixel clusters

Chip and In-Pixel Efficiency

- Efficiency based on ratio of matched to total tracks

$$\epsilon = \frac{N_{\mathrm{tracks\_matched}}}{N_{\mathrm{track\_total}}}$$



Chip and In-Pixel Efficiency

- Average efficiency of active sensor of 60%
- Efficiency hindered by threshold
  - Set at 1/3 MIP MPV for 190 µm depletion depth

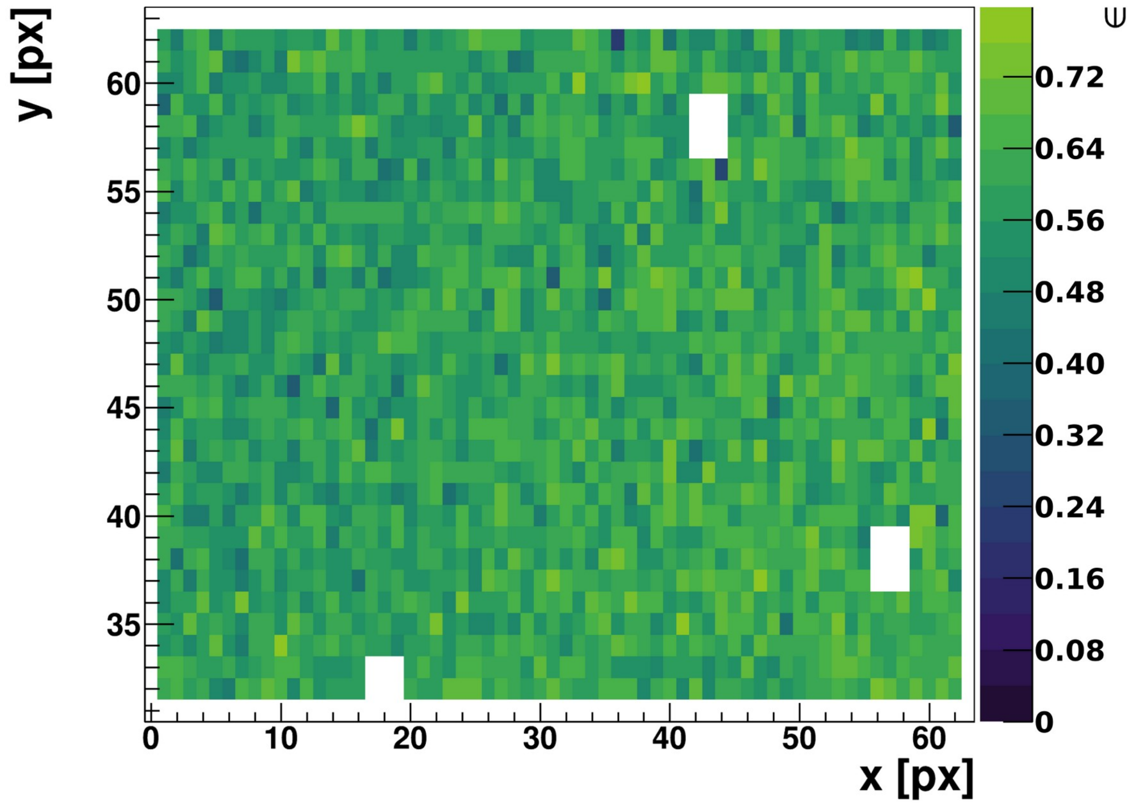


Fig.: Efficiency of the pixel matrix

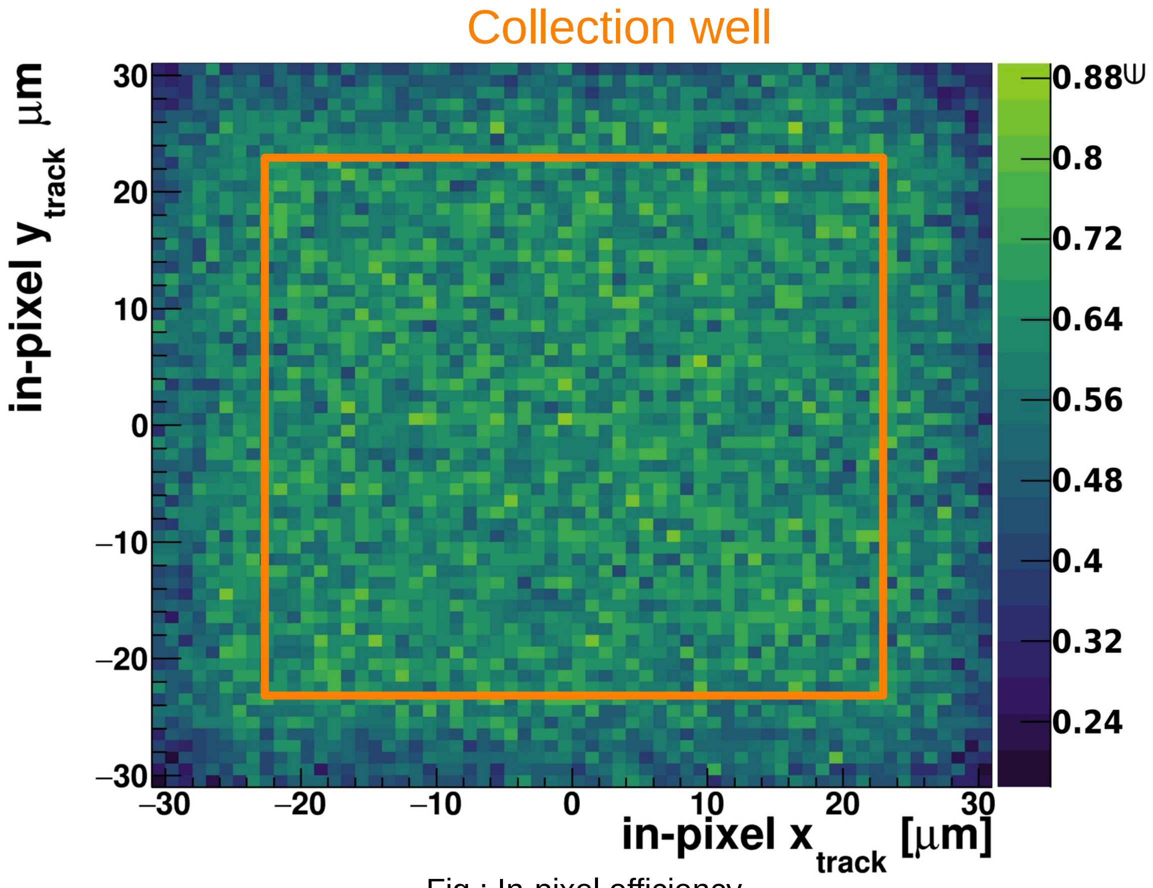
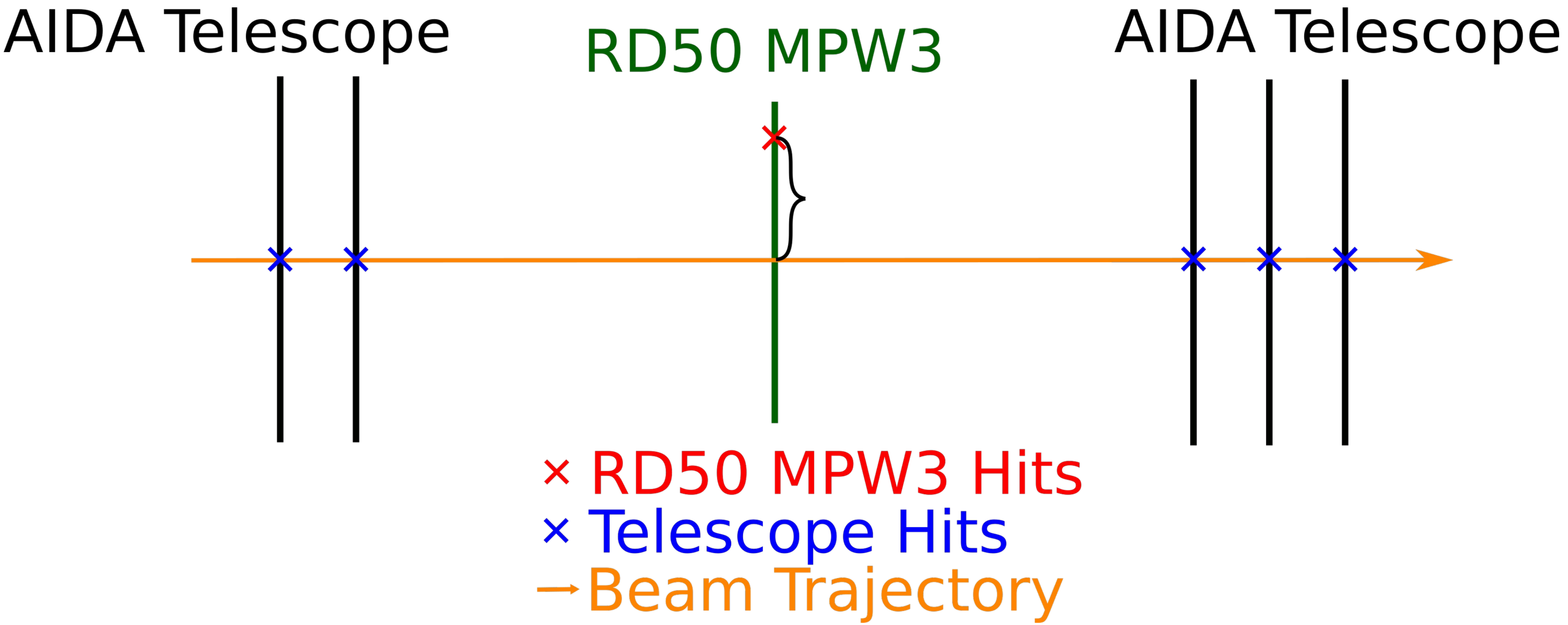


Fig.: In-pixel efficiency

Spatial Resolution

- Residual between:
  - interpolated track position
  - measured pixel hit location



Spatial Resolution

- Low double hit clusters results in almost binary distribution

$$\sigma_{\text{meas}} = 18\mu\text{m} \approx \frac{62\mu\text{m}}{\sqrt{12}} = \sigma_{\text{binary}}$$

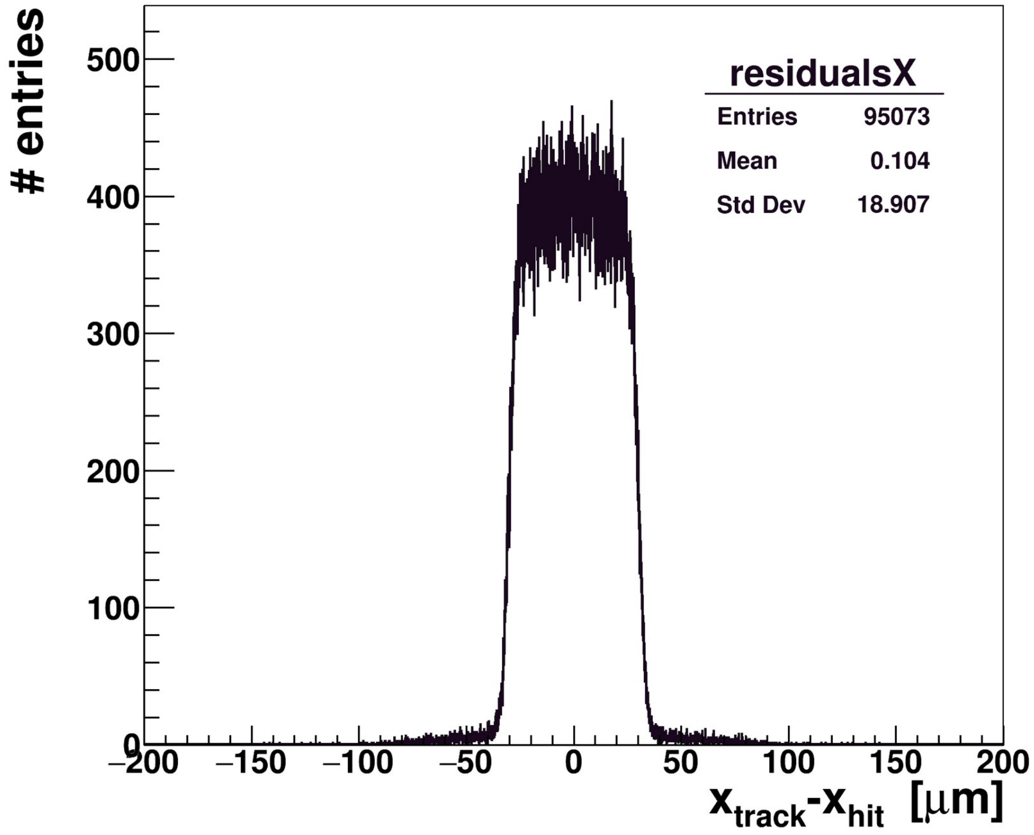


Fig.: Residual in x

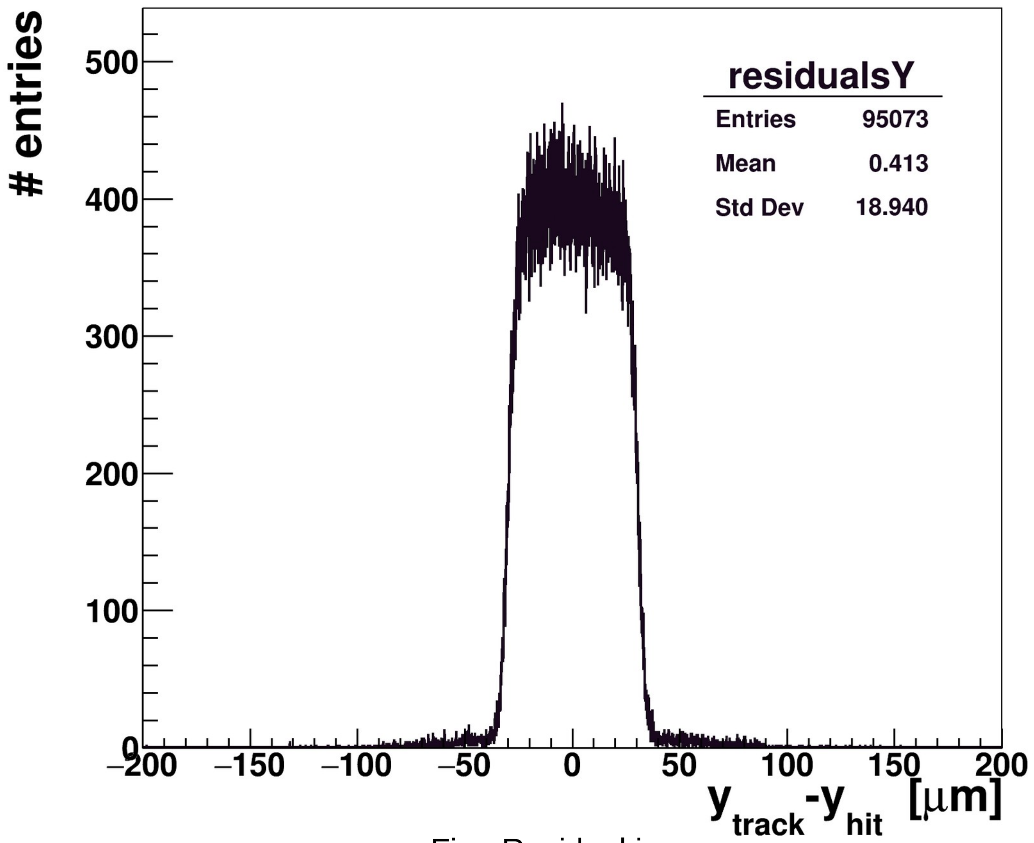


Fig.: Residual in y

Summary

- New RD50-MPW3 chip produced by LFoundry
  - Larger matrix
  - Full digital and analog readout
  - Different resistivities
- System was tested at the CERN SPS beamline and operated with EUDET-type telescope
  - Completed full test beam campaign and performed analysis of combined data
  - Chip performance acceptable considering sub-optimal settings
- Gained valuable insight for system operation for both laboratory and future test-beam measurements.

Outlook

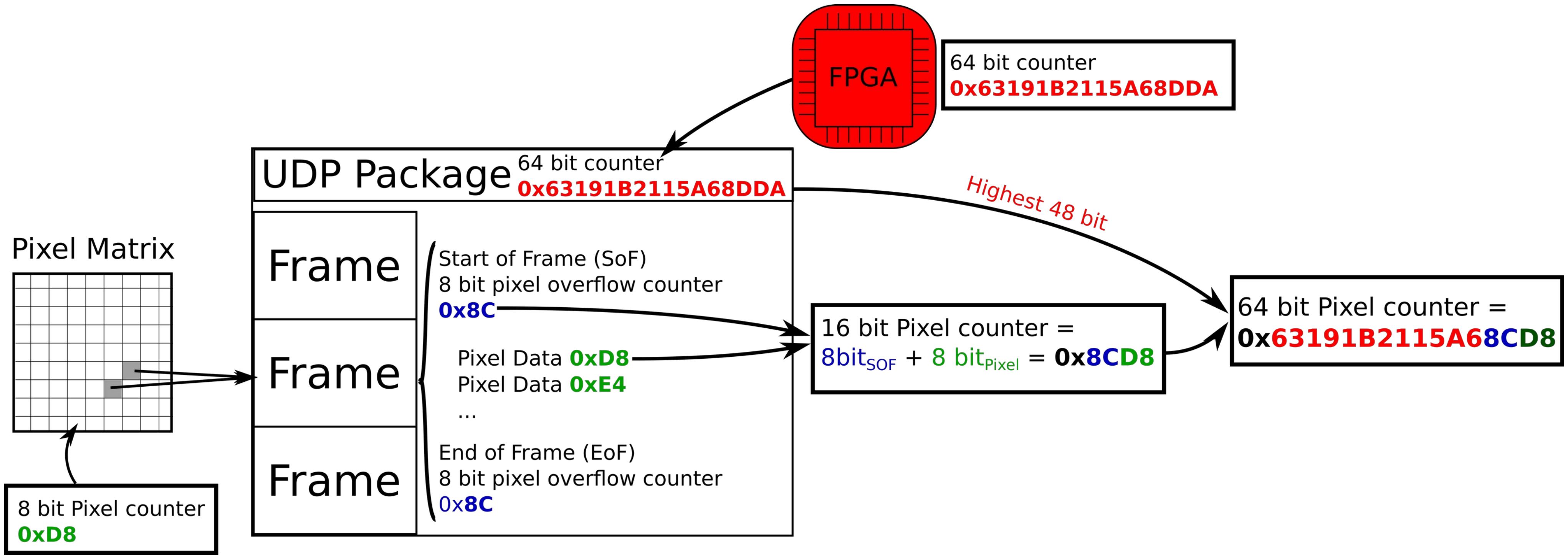
- Further tests of operation and improvements being worked on:
  → New firmware to increases overflow counter used for time synchronization
  → Threshold and noise optimizations
  → Ramping up lab measurements concerning analog and digital performance
  → First irradiated sensors expected in spring
  → Further test beam campaigns at the DESY II Test Beam Facility in July 2023 and CERN SPS in October 2023

Backup slides

Test beam data synchronization

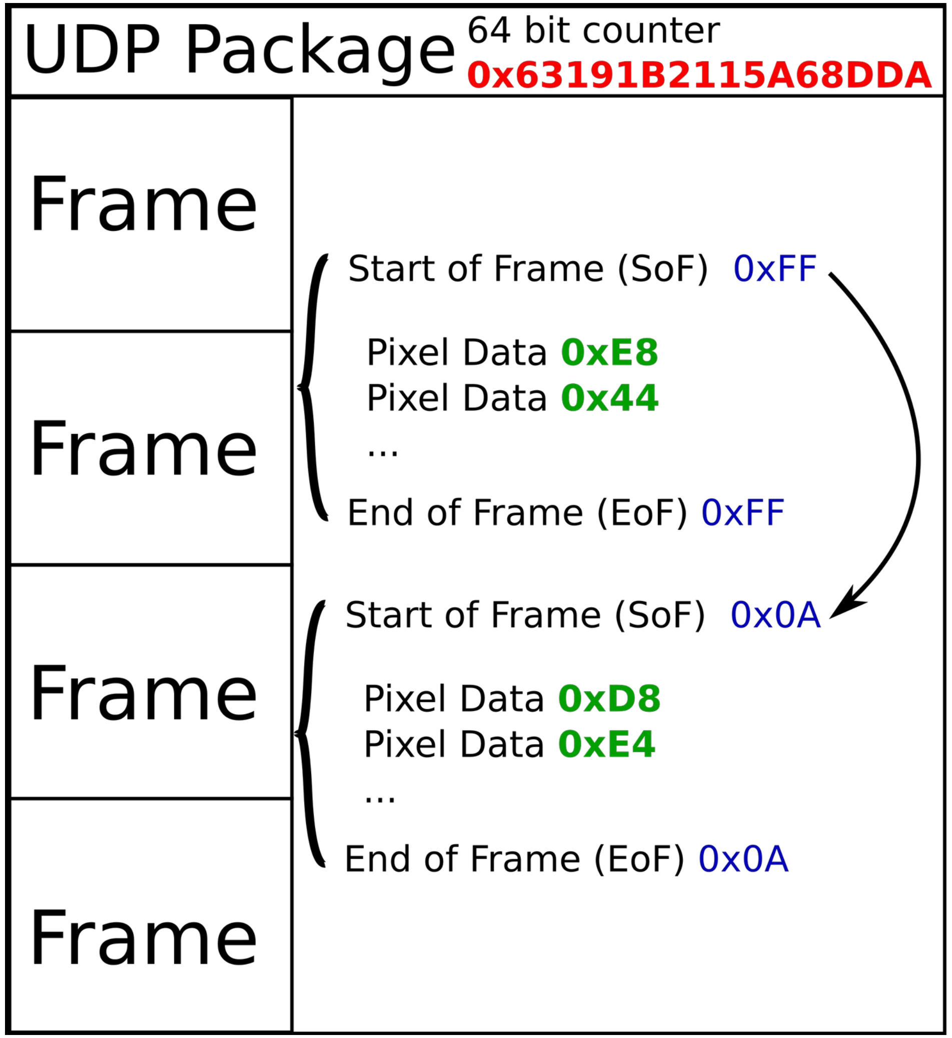
- Timestamp of the system given by:
  - in-Pixel logic (8 bit)
  - Data package overflow counter (8 bit)
- Overflows every 3.27 ms (accounted for in analysis)

  → Combined with 64 bit counter from FPGA for global timestamp



Testbeam Data Synchronization

- Time shift can vary depending on number of overflows within UDP package
- Data can be shifted in multiples of the overflow to match with telescope
- Actual shift per pixel is unknown requires external data handling

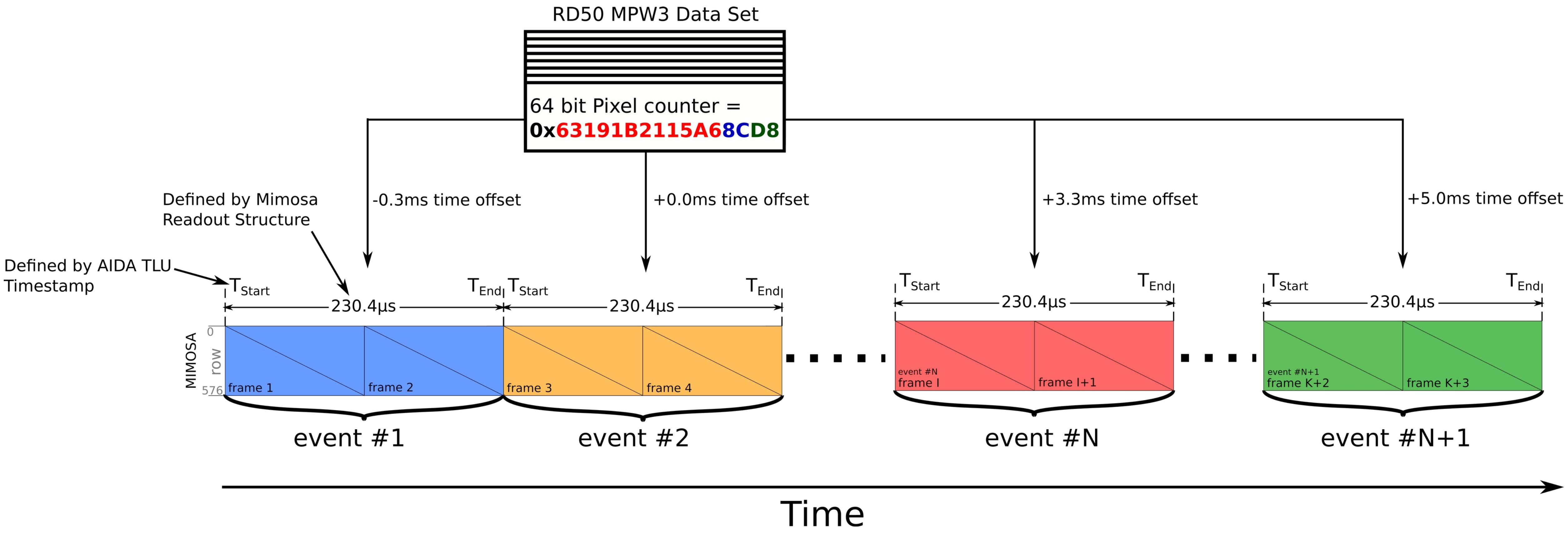


Overflow Within UDP package
Need to adjust 17th bit
(and possible higher for multiple OF)

50ns * 2^16 = 3.2768 ms

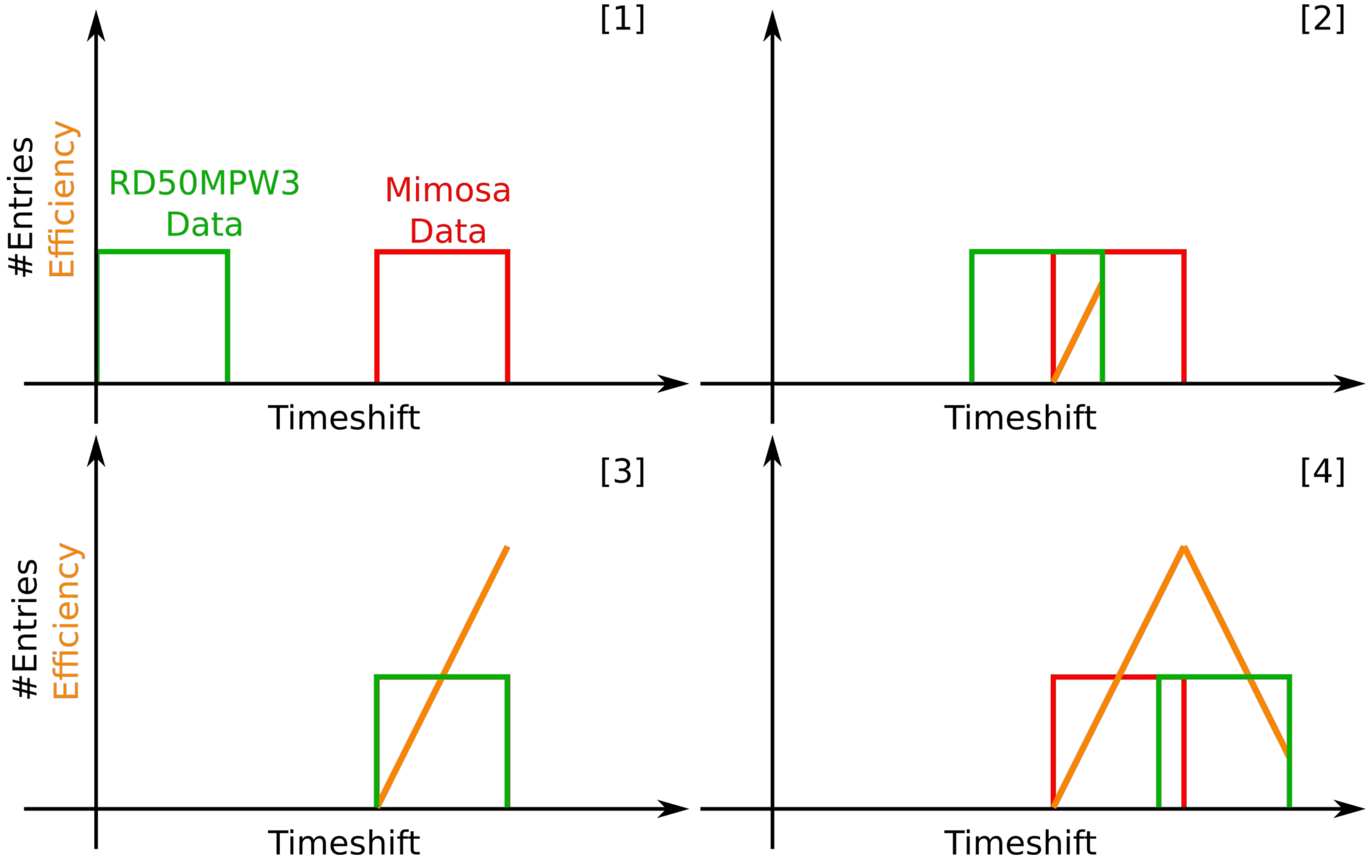
Test beam data Synchronization

- Global pixel timestamp is used to assign to the correct “event” which is defined by the AIDA TLU + Mimosa Telescope



Timeshift scan

- Scanned over a larger range with newly implemented buffer to:
  - see what the sum of the results are
  - how many events can be matched beyond 3.3 ms
  - determine if there is another offset except for the 16 bit overflow
- In effect a convolution of the two data distributions



Data combination

- Found clear correlation with the 16 bit TS overflow (3.27 ms)
- Slight offset O(100us) for first peak indicates some inherent offset that needs to be taking into account for the data
- Otherwise just random correlations with very minor contributions
- Total efficiency of the sensor = Sum of the peaks - N*baseline

  ≈ 60%
- Issue is resolved in new firmware with 48 bit overflow counter