



Contribution ID: 39

Type: **Oral**

## Performance of the RD50-MPW3 HV-CMOS Detector

*Wednesday, 1 March 2023 14:50 (20 minutes)*

The goal for tracking detectors is the combination of excellent spatial resolution, low material budget, high radiation tolerance and excellent timing resolution for the best achievable tracking performance.

Many different approaches are taken to reach this goal, with CMOS based silicon detectors providing one of the most promising angles of approach.

The CERN RD50 collaboration works on the development of radiation hard silicon detectors, with the CMOS working group focusing on monolithic detectors based on a 150 nm High Voltage CMOS process by LFoundry and investigates their viability for future particle physics experiments.

As part of the ongoing developments, the newest prototype, the RD50-MPW3, was delivered in July 2022 and has since been tested both in laboratories and at the CERN SPS test beam. The RD50-MPW3 consists of a  $64 \times 64$  pixel matrix arranged in a 32 double-columns. The  $62 \mu\text{m}$  pixels include both an analog front-end as well as a digital readout. Its predecessor, the RD50-MPW2, consisted of  $8 \times 8$  pixels of  $60 \mu\text{m}$  pixel pitch that only included the analog front-end.

In this talk I will present recent results on the performance of the newest RD50 HV-CMOS prototype such as the achieved time resolution, as measured in the laboratory, as well as first results about the achieved performance of the MPW3 gathered during the CERN test beam campaign conducted in October 2022.

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**Session Classification:** CMOS

**Track Classification:** CMOS