# Test results of the Timespot1 ASIC on 3D-trench sensors

A. Loi, A. Lai, A. Stabile, A. Cardini, D. Brundu, A. Lampis, G.-F. Dalla Betta, L. Piccolo, L. Frontini, M. Aresti, M. Boscardin, M. Garau,S. Ronchin, S. Cadeddu, V. Liberali, G.-M. Cossu

# Outline

- **Motivations and background**
- **Timespot-1**
  - **Architecture**
- **Tests**
  - **Setup**
  - **Test, only ASIC**
  - **Test on hybrid**
  - **Bump bonding yield**
  - **Test with LASER setup**

# Motivations and background

# Motivations and background

- **Scenario for future Phase-II LHCb upgrade:**
  - **Luminosity increment to $2*10^{34}$ $cm^{-2}s^{-1}$**
    - **x10 compared to LHCb phase 1**
  - **Requirement on hardware**
    - **Radiation hardness for sensors and electronics**
      - **$\Phi = 10^{16} \div 10^{17}$ 1 MeV neq/$cm^2$**
      - **Dose = 1 ÷ 2 Grad or higher**
    - **Material budget**
      - **1 ÷ 0.5 % of radiation length**
    - **Detector efficiency**
      - **Higher than 99 % per detection layer**
    - **High tracking efficiency with**
      - **Space resolution (< 42 µm)**
      - **Time resolution ( < 35 ps)**
    - **Power consumption**
      - **10 µW per pixel**

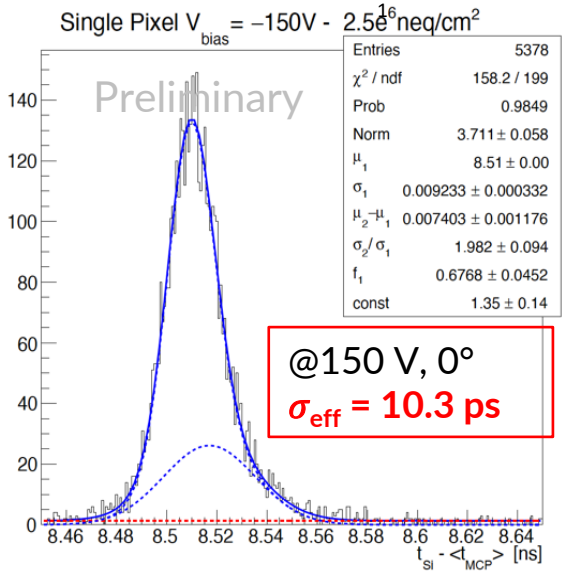
source:
*Considerations for the VELO detector at the LHCb upgrade II* – CERN-LHCb-2022-001

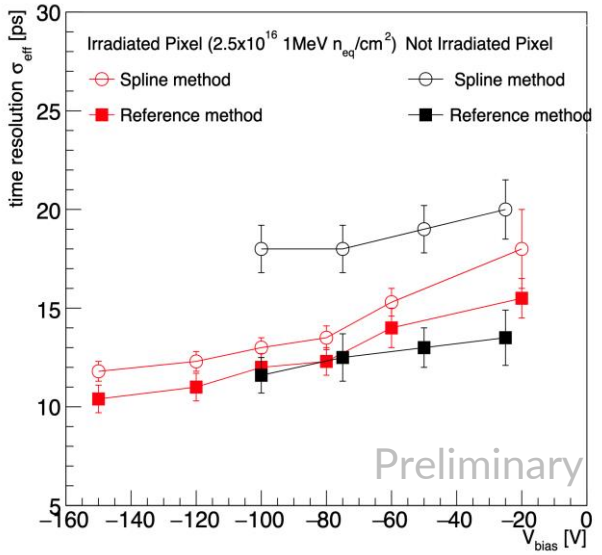
| Requirement | scenario $S_A$ | scenario $S_B$ |
|---|---|---|
| Pixel pitch [µm] | $\leq 55$ | $\leq 42$ |
| Lifetime fluence [$1 \times 10^{16}$ 1 MeV $n_{eq}/cm^2$] | $> 6$ | $> 1$ |
| TID lifetime [MGy] | $> 28$ | $> 5$ |
| Sensor Timestamp per hit [ps] | $\leq 35$ * | $\leq 35$ |
| ASIC Timestamp per hit [ps] | $\leq 35$ * | $\leq 35$ |
| Hit Efficiency [%] | $\geq 99$ | $\geq 99$ |
| Power per pixel [µW] | $\leq 23$ | $\leq 14$ |
| Pixel rate hottest pixel [kHz] | $> 350$ | $> 40$ |
| Max discharge time [ns] | $< 29$ | $< 250$ |
| Bandwidth per ASIC of 2 $cm^2$ [Gb/s] | $> 250$ | $> 94$ |
| Material budget | $\leq 0.8\%$ $X_0$ per station (all included) | |

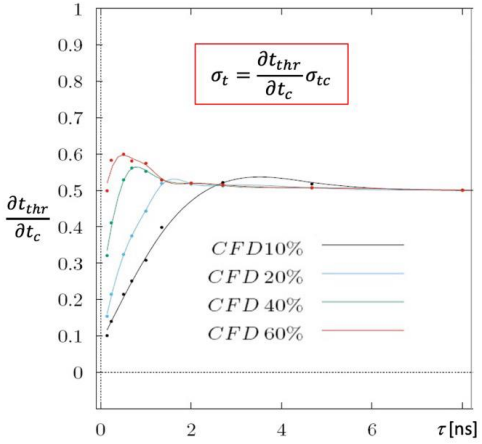
*Corresponds to < 50 ps on sensor+electronics

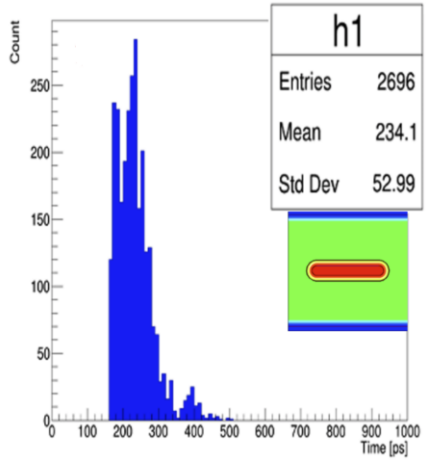
# Time resolution on silicon sensors and electronics

- **TimeSPOT 3D silicon sensor**
  - **Excellent time resolution after radiation**
    - **More about on Wednesday**
      - **M. Garau : https://indico.cern.ch/event/1223972/contributions/5262144/**
- **Sensor integration on dedicated ASIC**
  - **20-25 ps of resolution are theoretically feasible with the CSA approach**
    - **G. M. Cossu and A. Lai, *" Front-end Electronics for Timing with pico-seconds precision using Solid State Sensors", https://iopscience.iop.org/article/10.1088/1748-0221/18/01/P01039***
    - **A.Lai and G. M. Cossu, *"Timing performances of front-end electronics with 3D-trench silicon sensors", https://arxiv.org/abs/2301.11165***



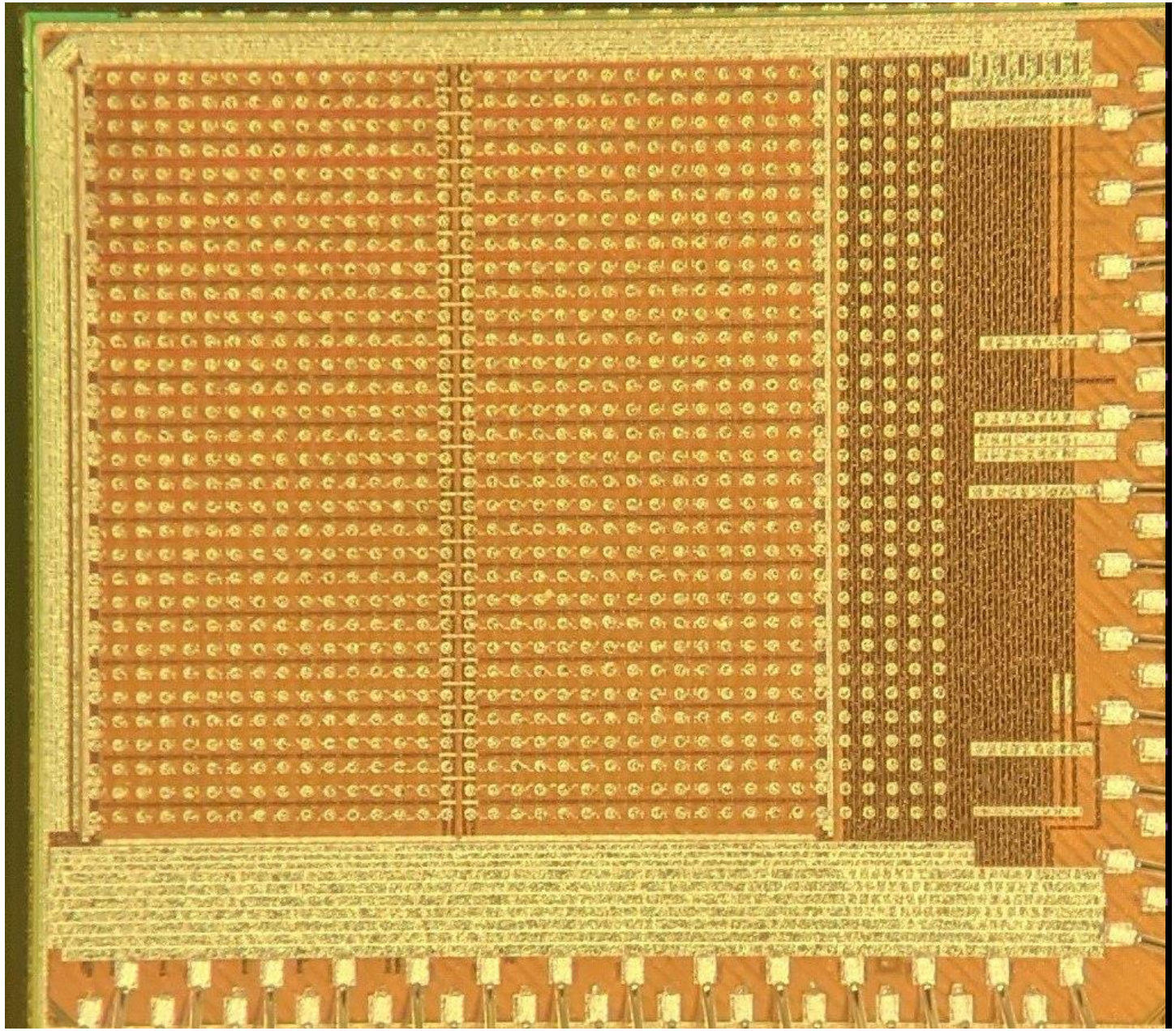

Time resolution vs std. dev. of CCT distribution
Fraction of rms is ½ for "slow" electronics (CSA)

# The TimeSPOT-1

## General architecture

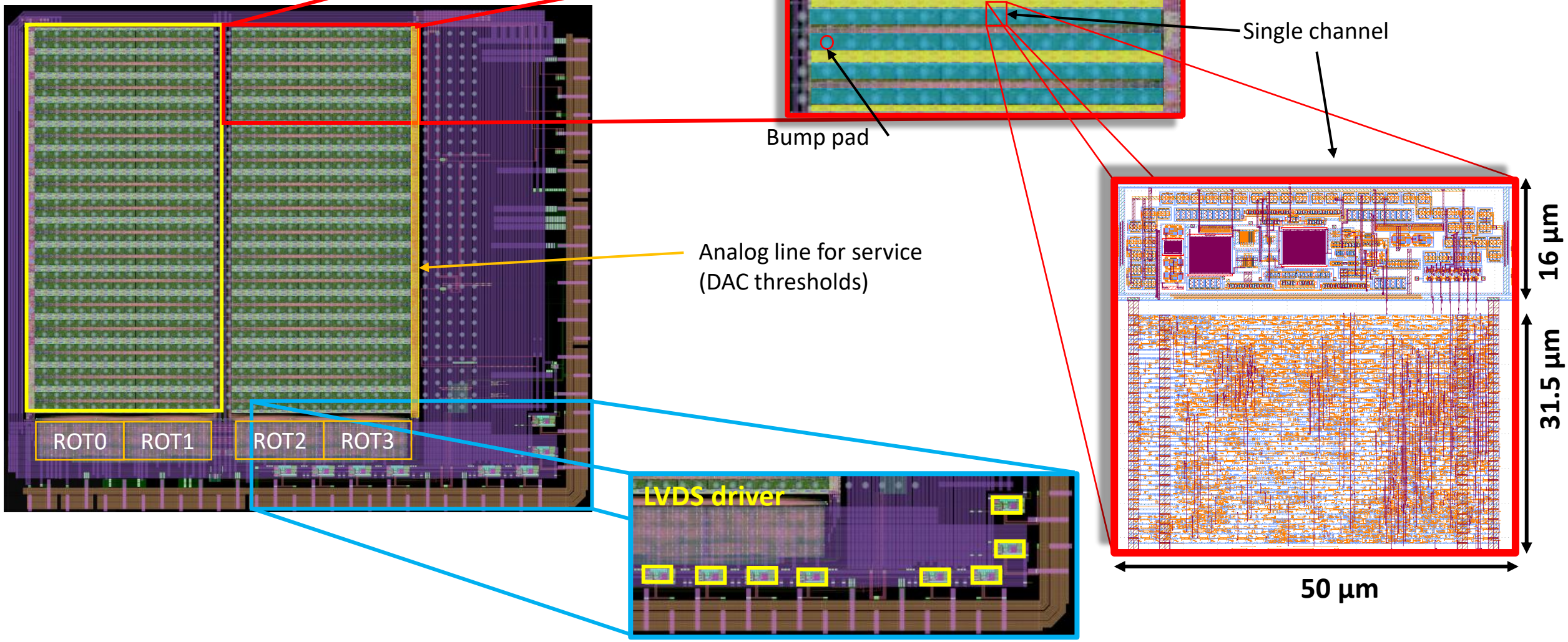
# Architecture

- **Technology:**
  - 28 nm CMOS
- **Structure:**
  - 32x32 pixel matrix
    - FE + TDC per single channel
  - Subdivision
    - 2 main blocks of 512 channels
    - 4 Readout trees
      - Each serves 256 channels
      - Output serialised and sent on 8 LVDS drivers (2 for each readout tree)
    - Analog (service) column
      - Provides DACs for analog level
      - Bias cell for power consumption
      - Bias replicas with source follower
  - Frequency
    - Device operated by 640 MHz master clock
    - Data output @ 640 MHz in DDR format



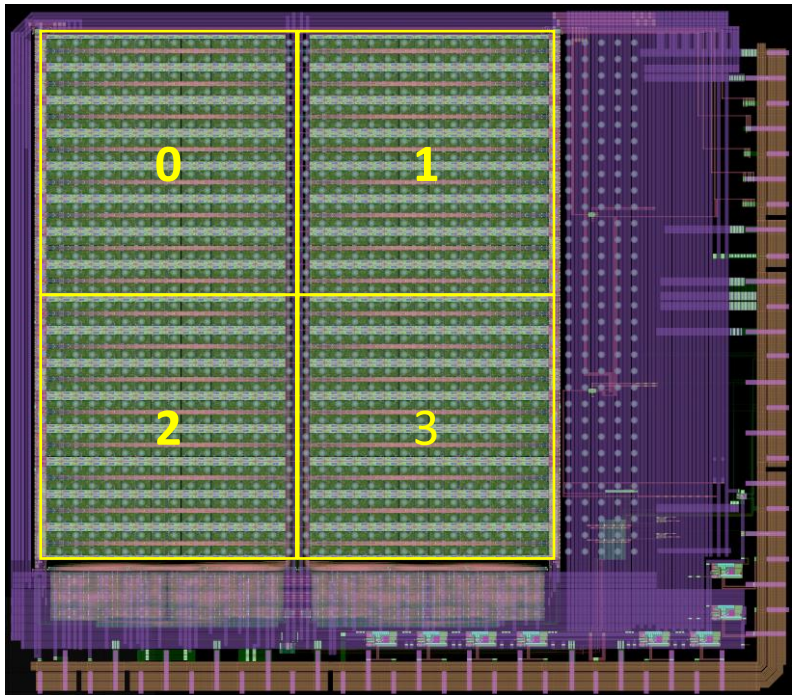
# Architecture

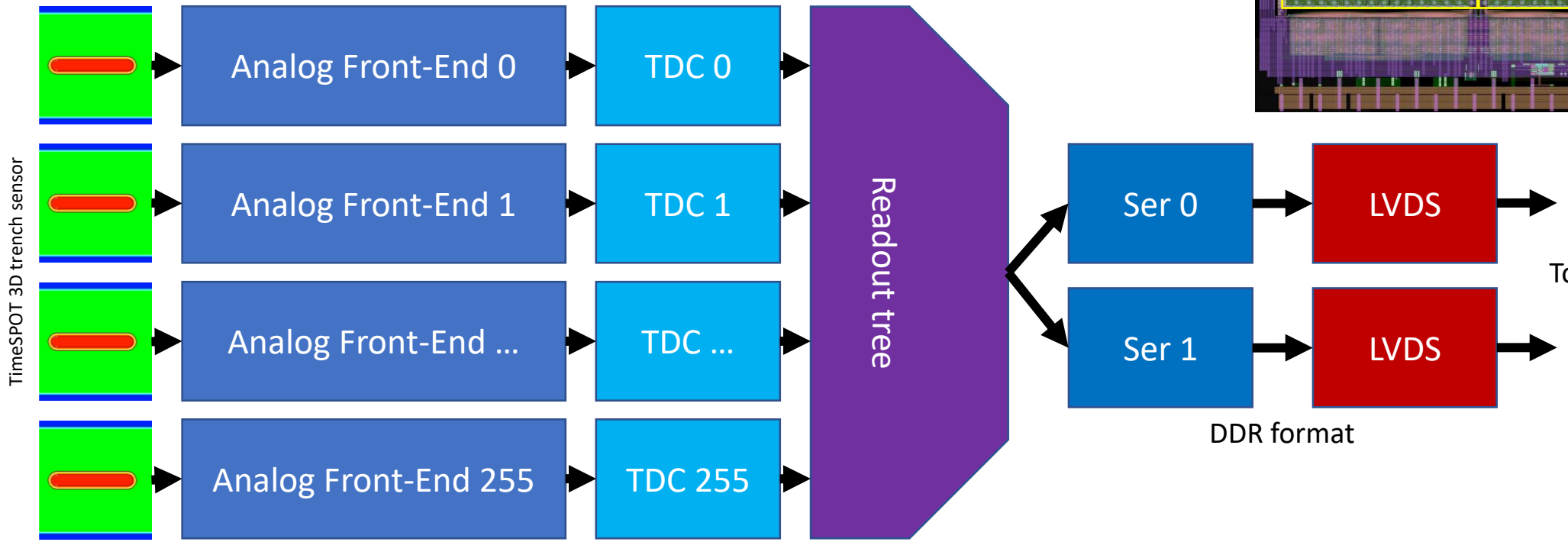
- **ASIC level**



# Architecture – Data flow

- **Active area of ASIC divided into 4 large areas**
  - 256 pixel each
    - Each channel has own TDC
  - All hits processed by a readout tree and send at 640 MHz in DDR format



# Test and measurements

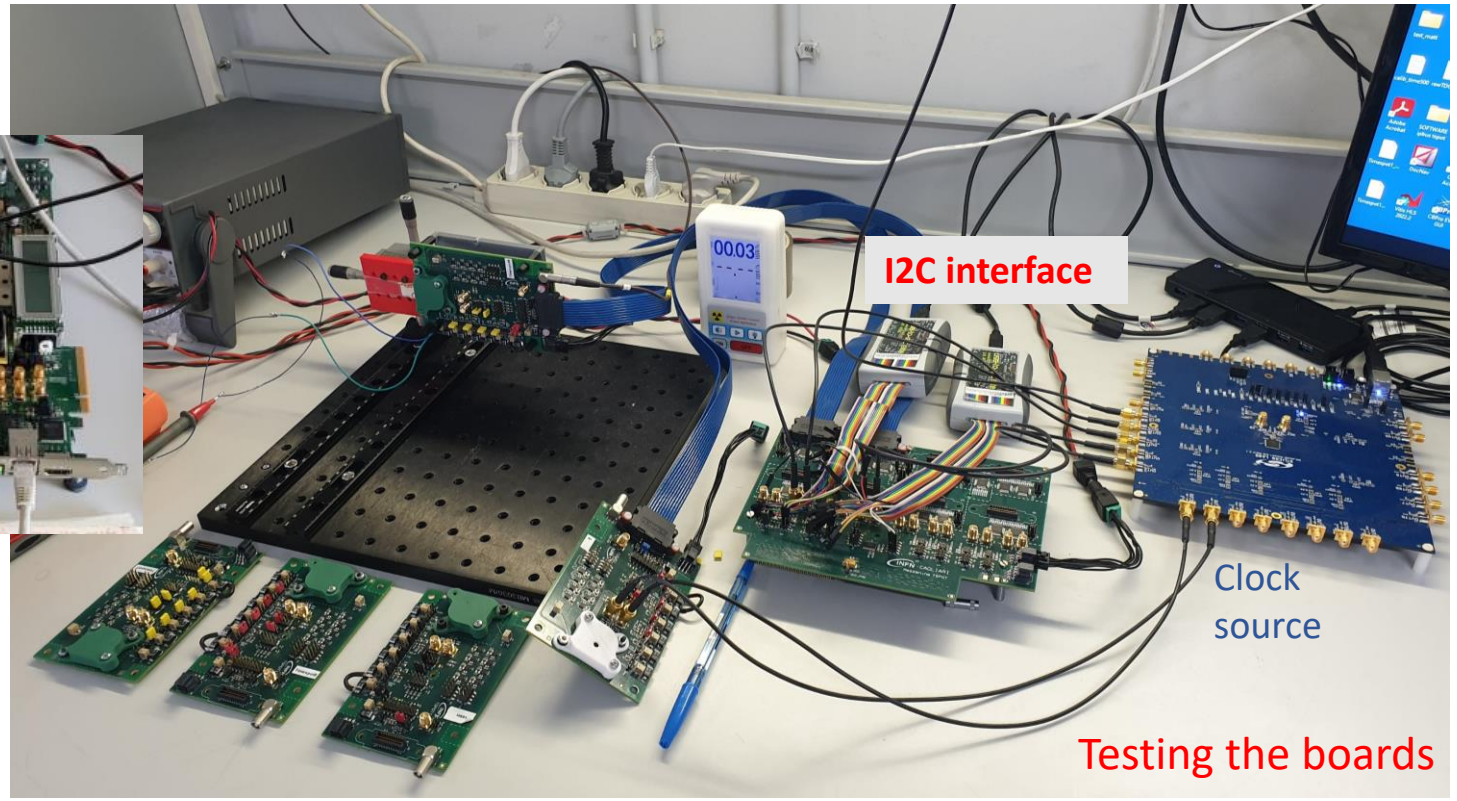
Only electronics

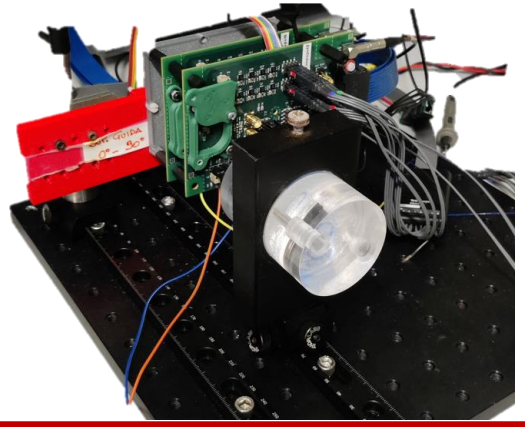
Sr-90 source

# Setup

- **Tspot-1 board**
  - Version with/without sensor
- **I2C interface**
- **Clock source**
- **FPGA + Mezzanine**
  - DAQ/CTRL system
- **Purpose:**
  - Performance of electronics
    - Front-end jitter
    - TDC resolution
  - Fabrication quality
    - Bump bond quality
  - Secondary
    - Test on FPGA-DAQ/CTR system

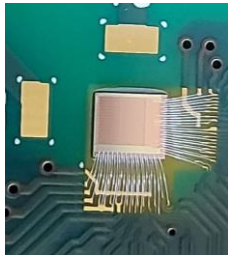
FPGA + Mezzanine



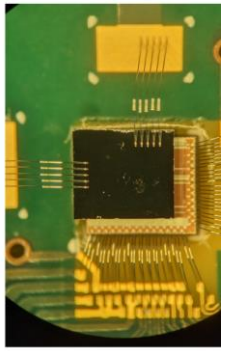



Configuration with Sr-90 source

Tspot-1 board with Timespot-1 ASIC

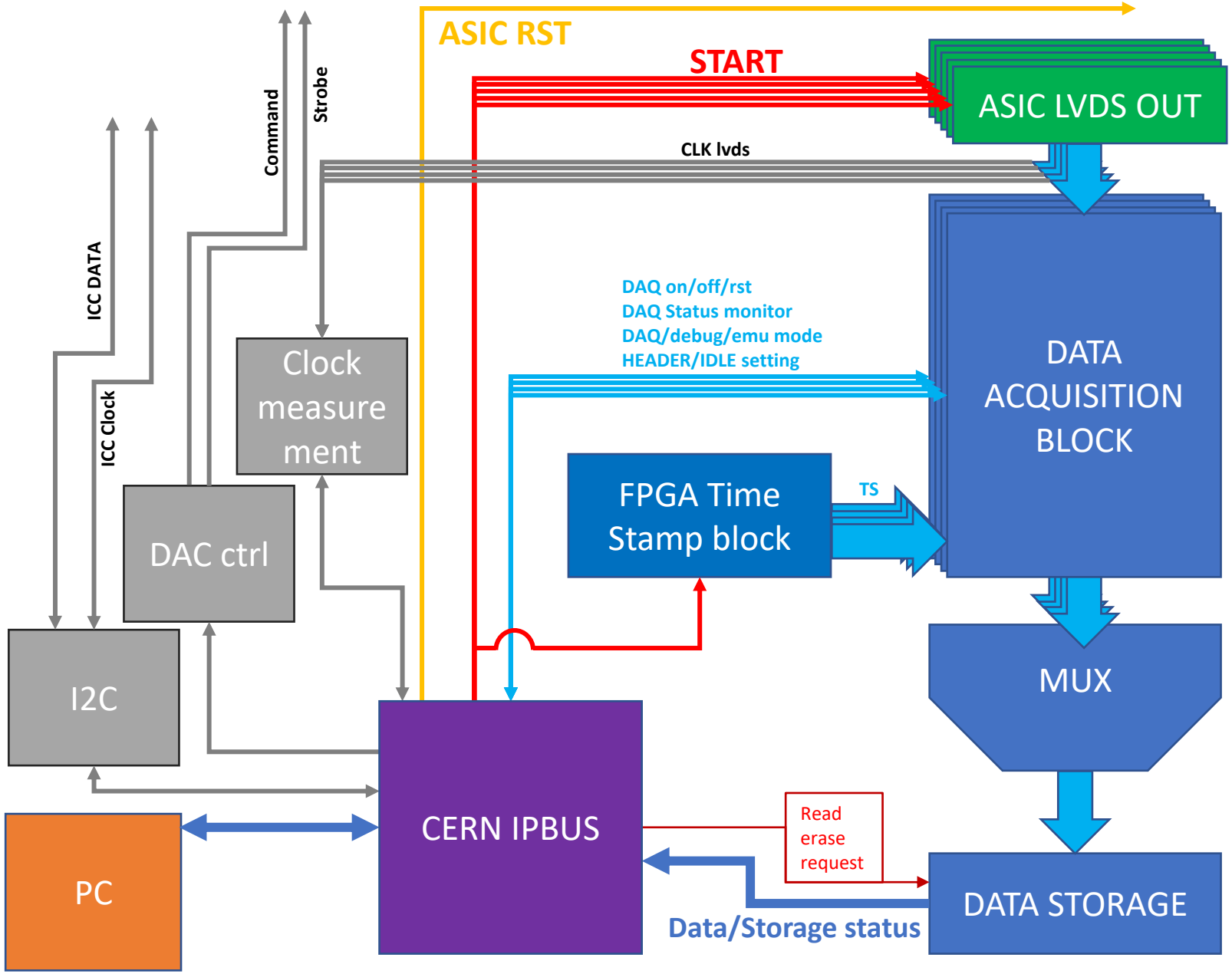


Tspot-1 board with Timespot-1 Hybrid



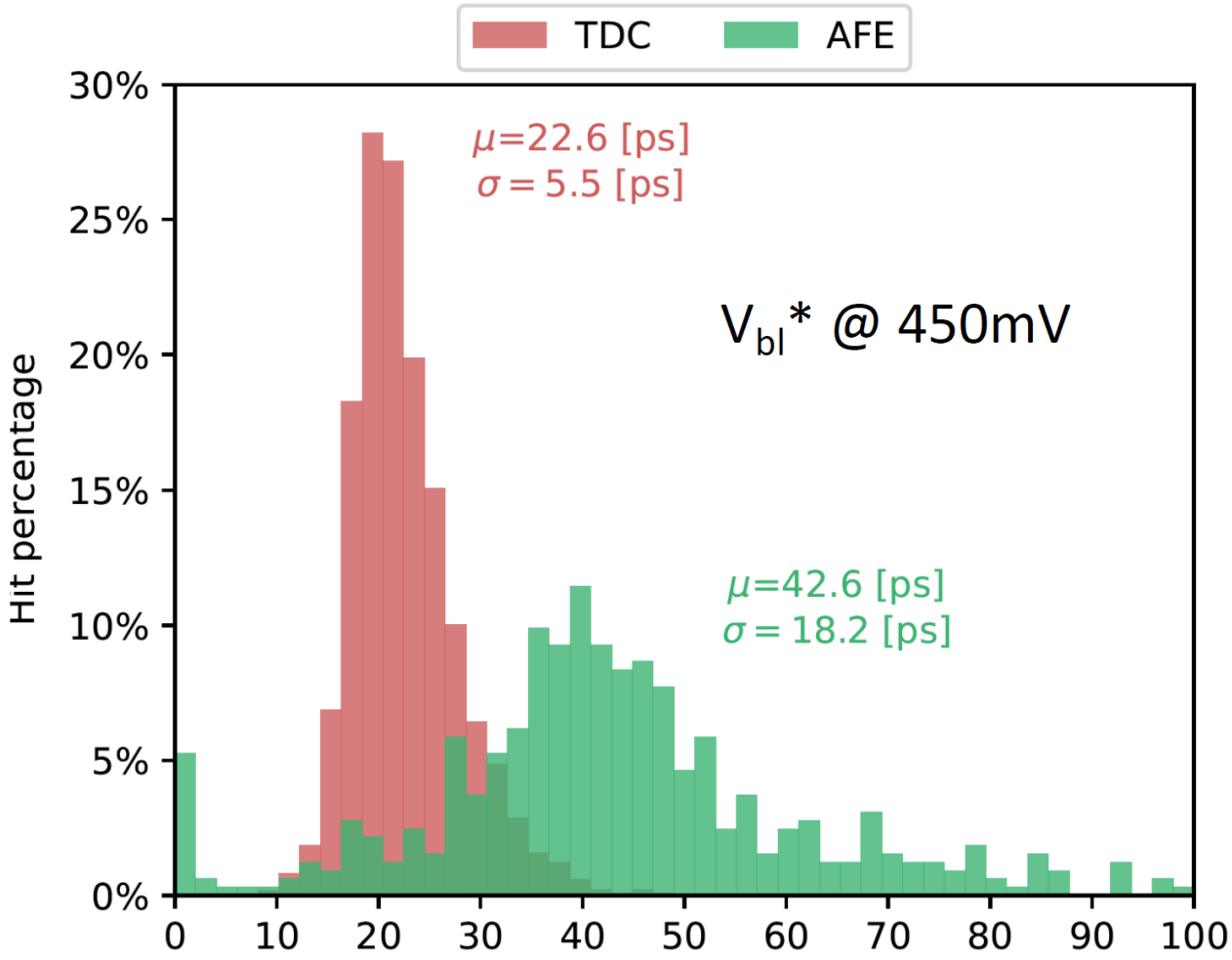
# DAQ/CTRL

- **DAQ**
  - Designed for max 8 Timespot1
    - 8 Data acquisition blocks for each ASIC (one for each LVDS data connection)
    - 64 Data acquisition blocks in total
  - Data is moved to final storage using a simple multiplexer
    - Scans simply over all 64 outputs and checks for stored events
      - Not very efficient but for now enough
- **System is also configured to used:**
  - External Tspot1 DACs
  - I2C interface (developed by INFN Milan)
  - ASIC clock measurement interface (for test purposes)



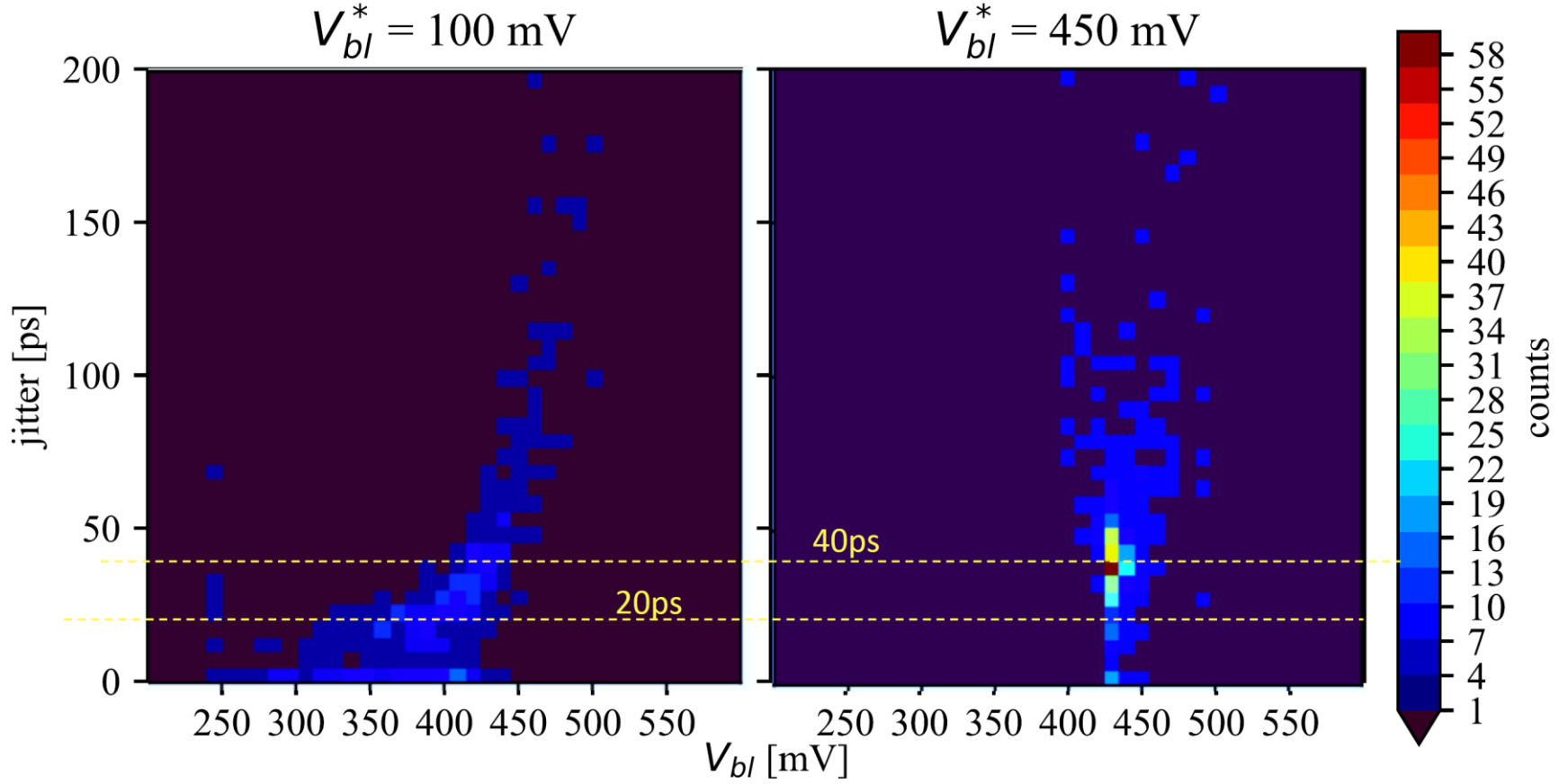
# Timing without Sensor (1)

- **Distribution of TA across 512 pixel:**
  - TDC average timing resolution:
    - $\sigma_{TDC} = 23\ ps$
  - Analog FE average timing resolution:
    - $\sigma_{FE} = 43\ ps$
    - ~ 10uW power consumption
  - Result is very promising, considering that the ASIC Offset compensation mechanism is suffering some issues.
    - Expected jitter: $10 \div 20\ ps$



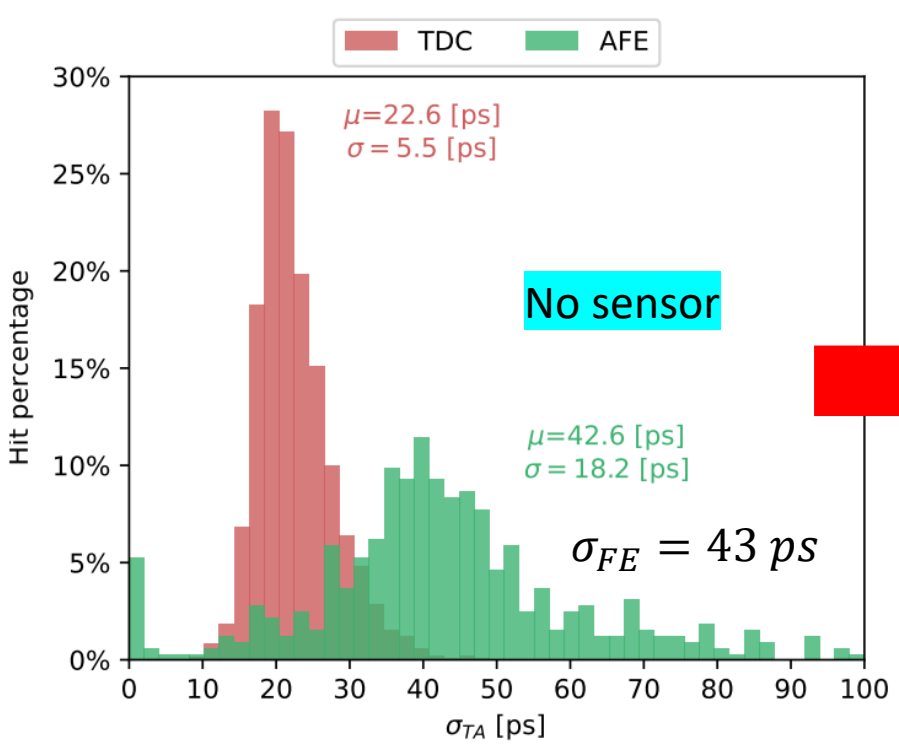
# Timing without Sensor (2)

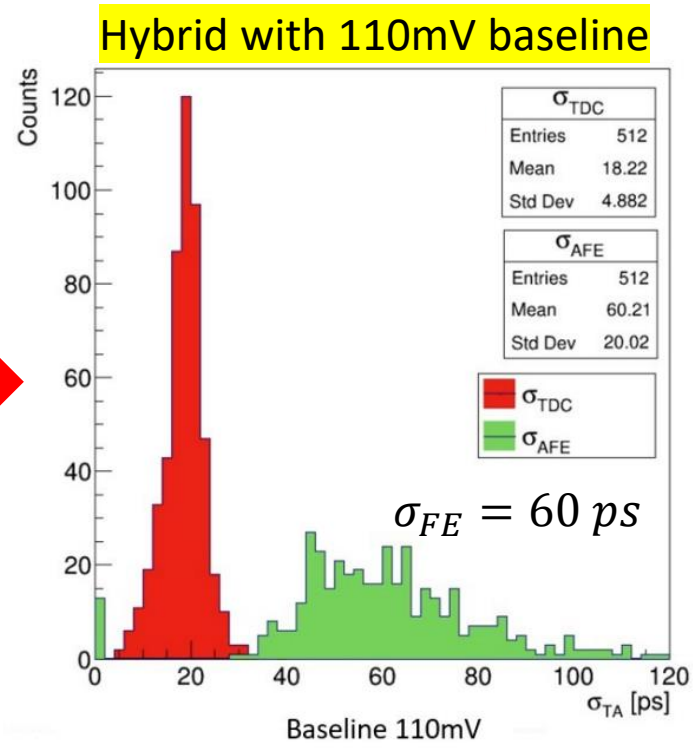
- **At low baseline setting, all channel do not behave properly and stay at different levels**
- **This setting works almost fine at higher level but with a worse jitter**
  - **Problem understood and debug ready for future ASIC**

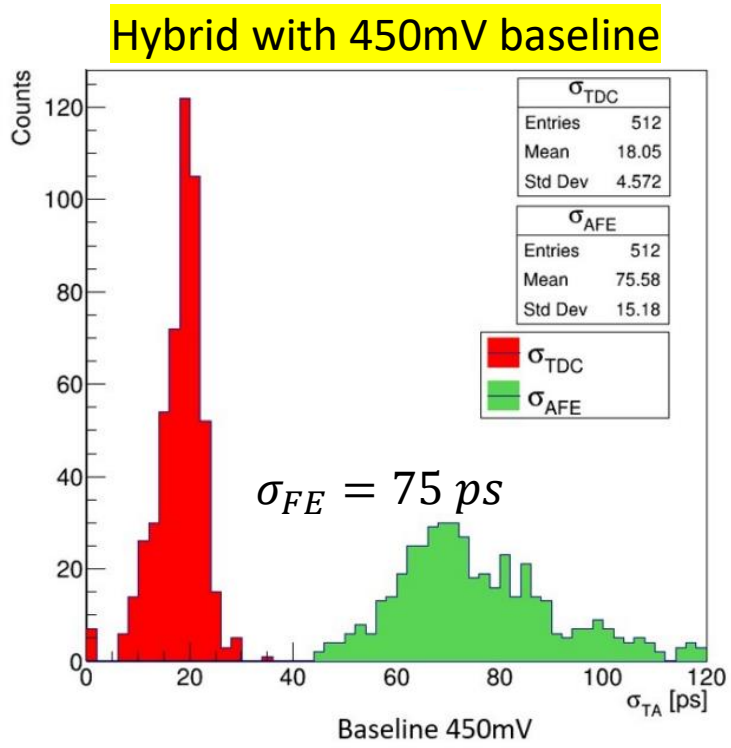


# ASIC performance after hybridization

- **TDC and FE tests repeated after hybridization**
  - Sensor capacitance increases jitter
  - TDC resolution is not affected

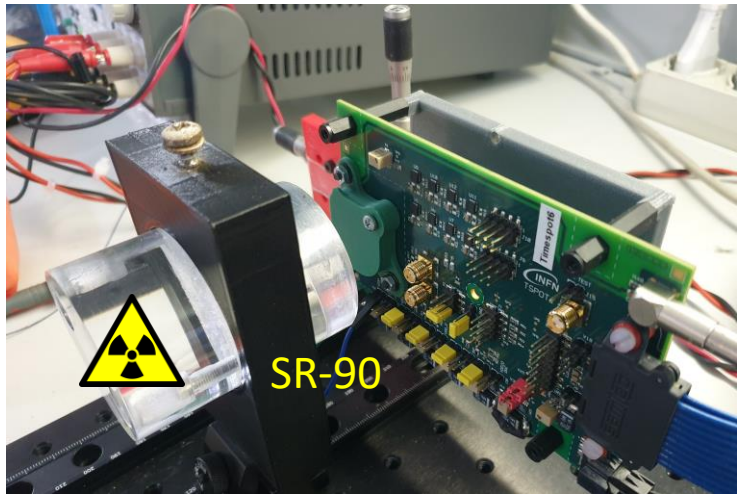


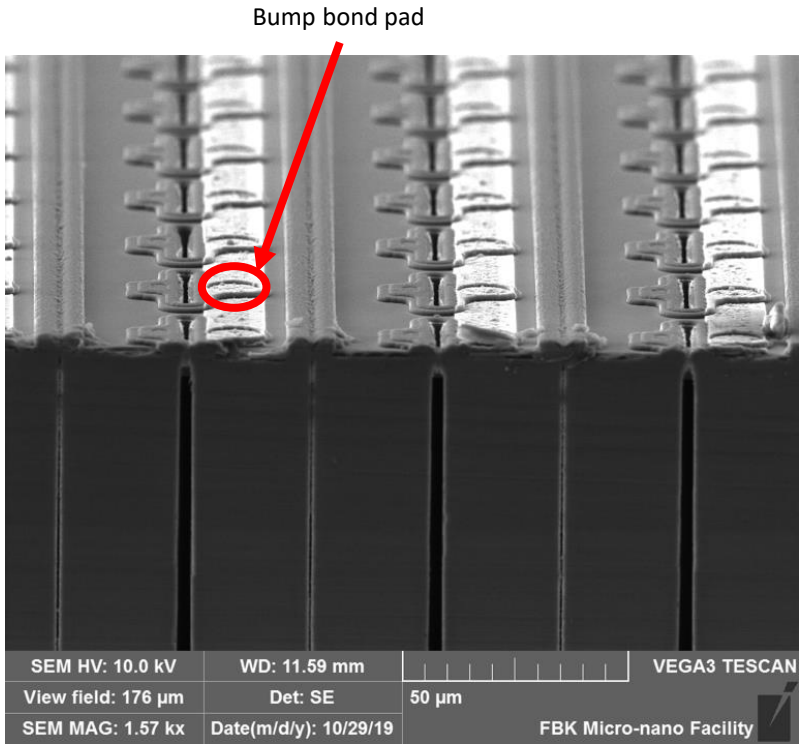



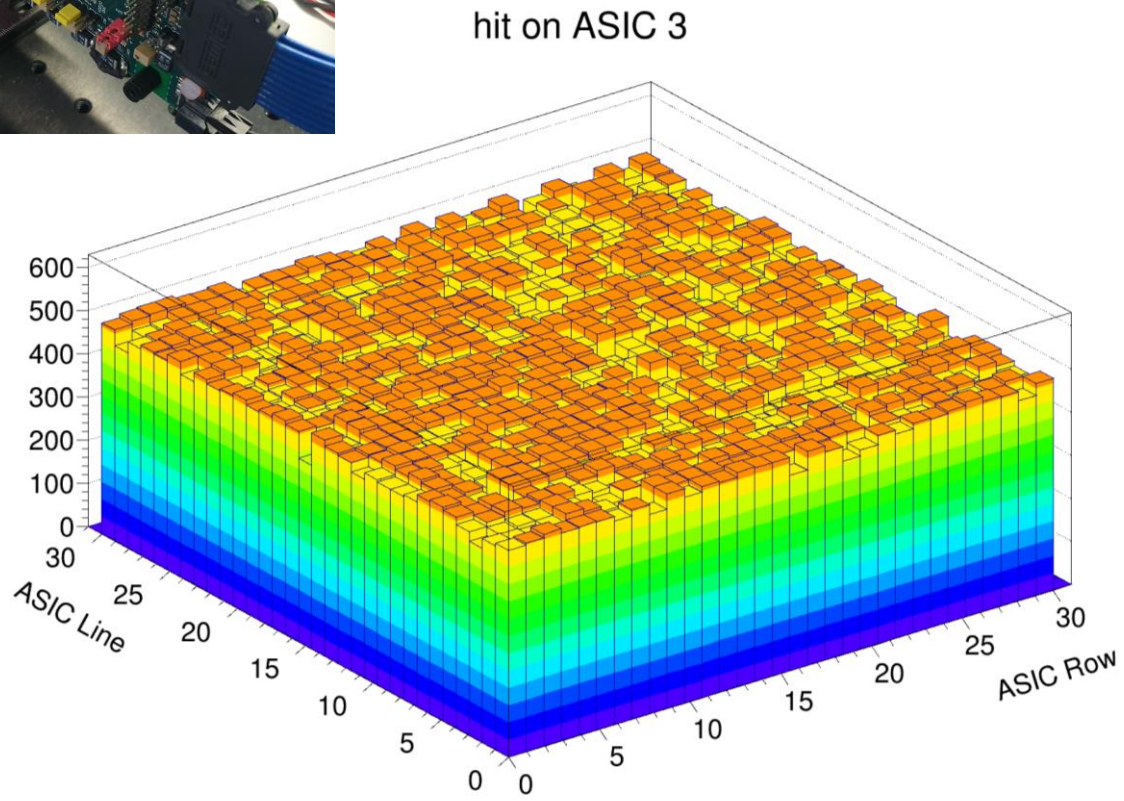
# BB bonding yield on ASIC

- **BB-yield checked using Sr-90 source**
  - **All channels capable of detecting incoming particles**
    - **Behaviour same for all tested matrices!**



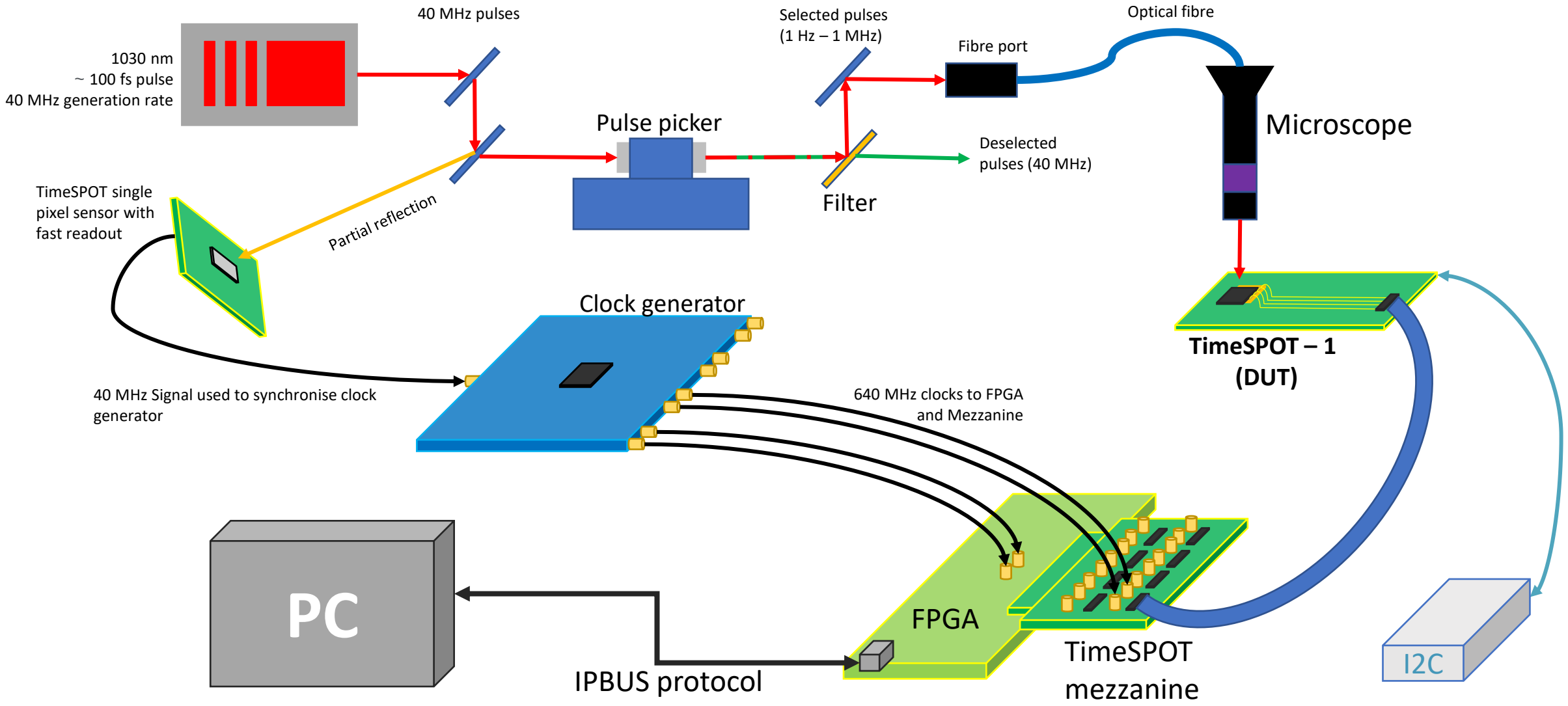

SEM photo of a TimeSPOT pixel matrix (photo source: FBK)



# Test and measurements

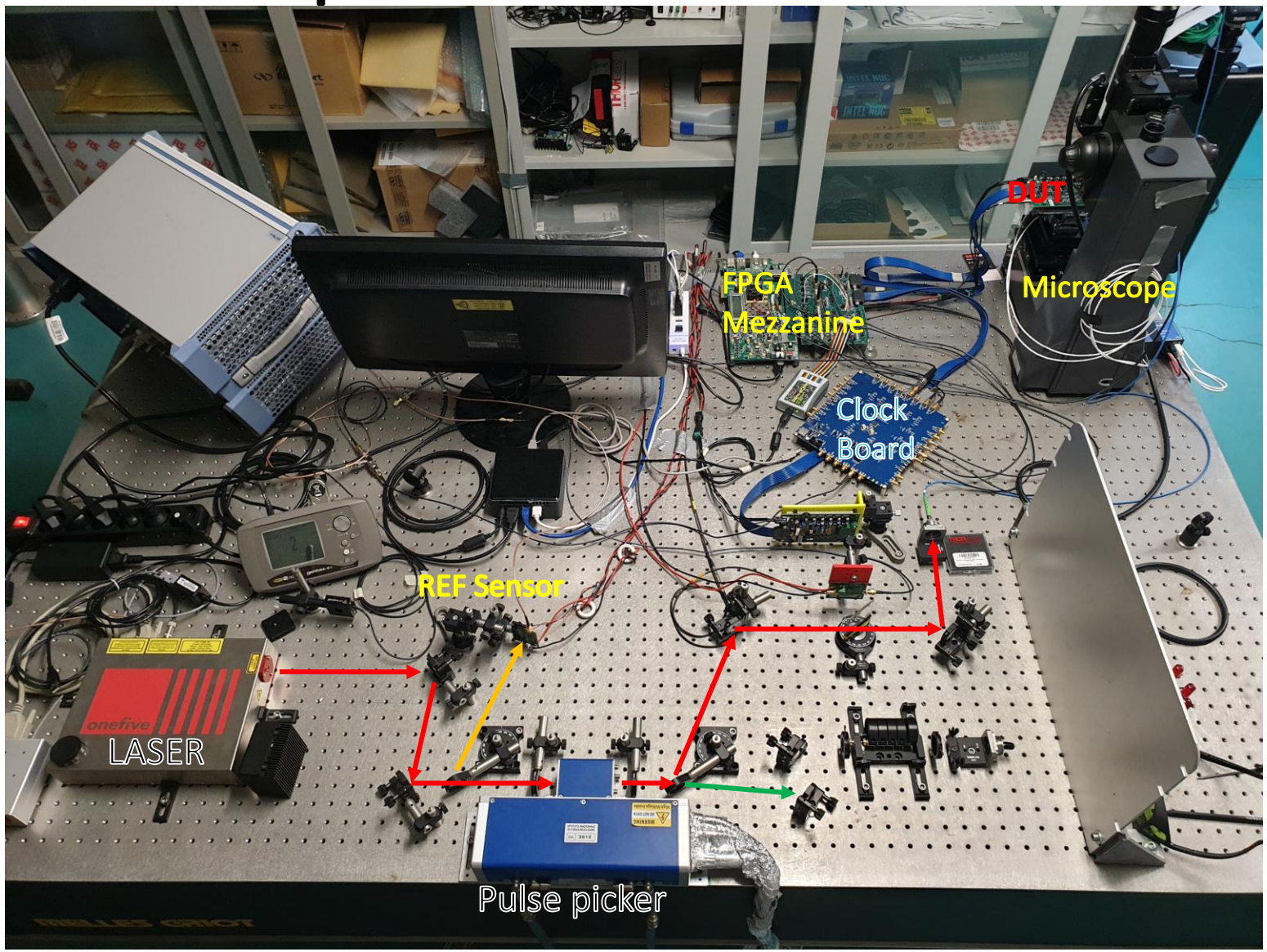
## First LASER tests

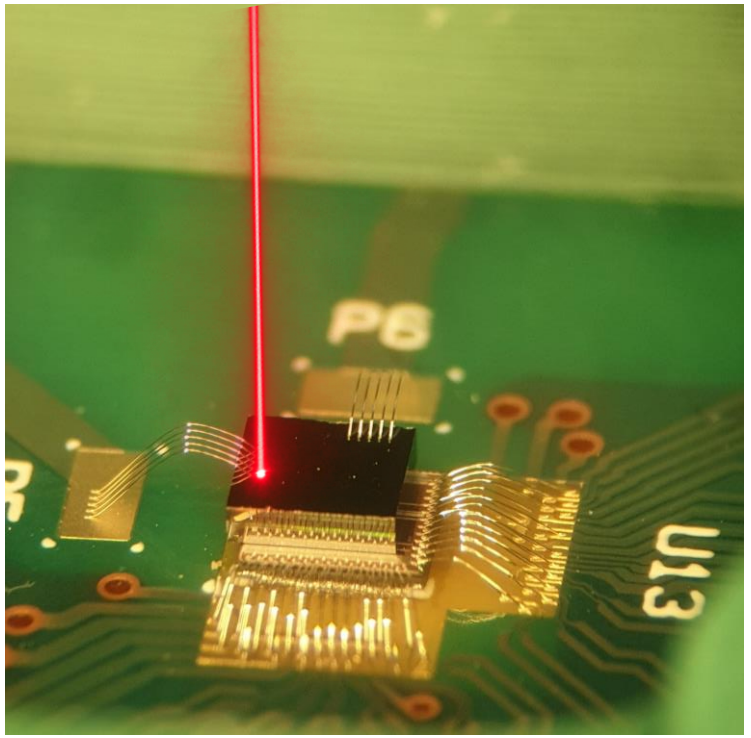
# The setup – schematic representation




Schematic representation

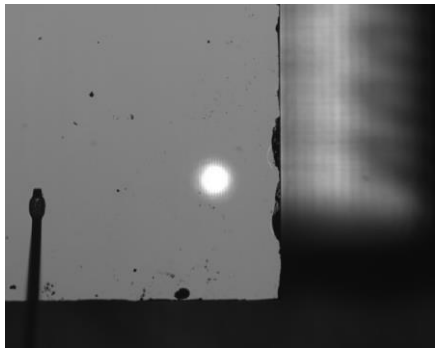
# The setup – view from above



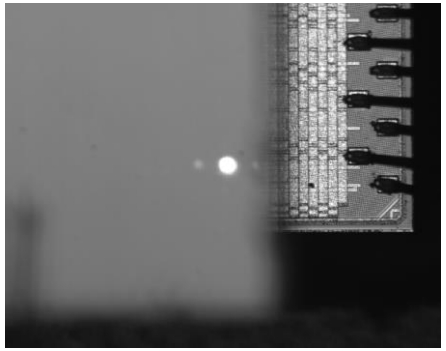




Artistic representation

TimeSPOT-1 hybrid



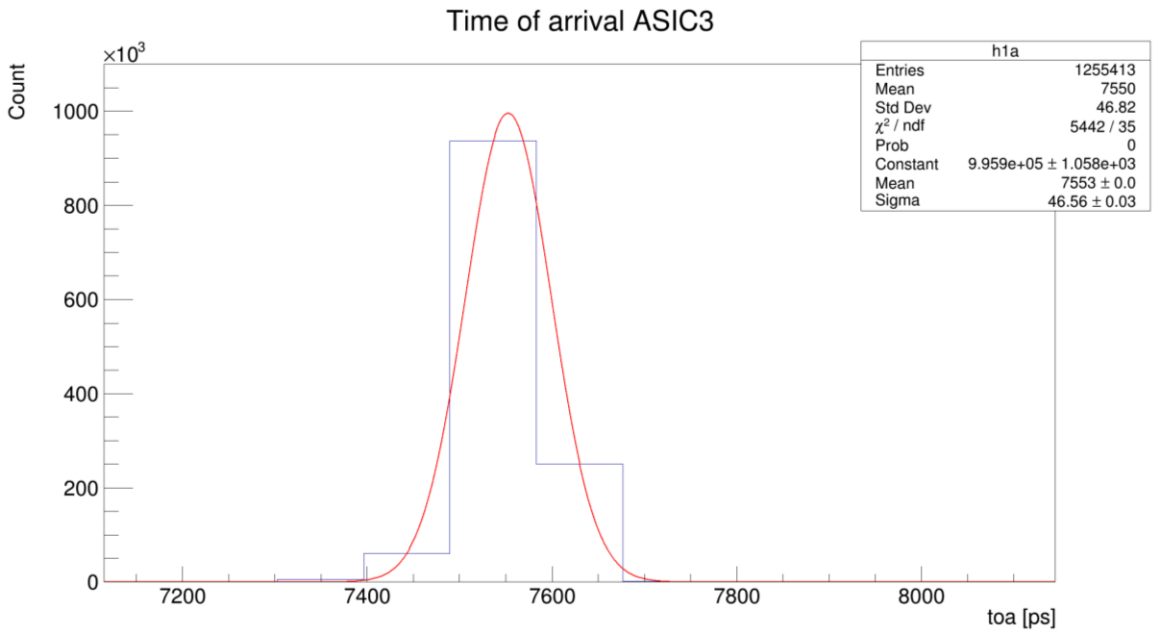
Focus on sensor

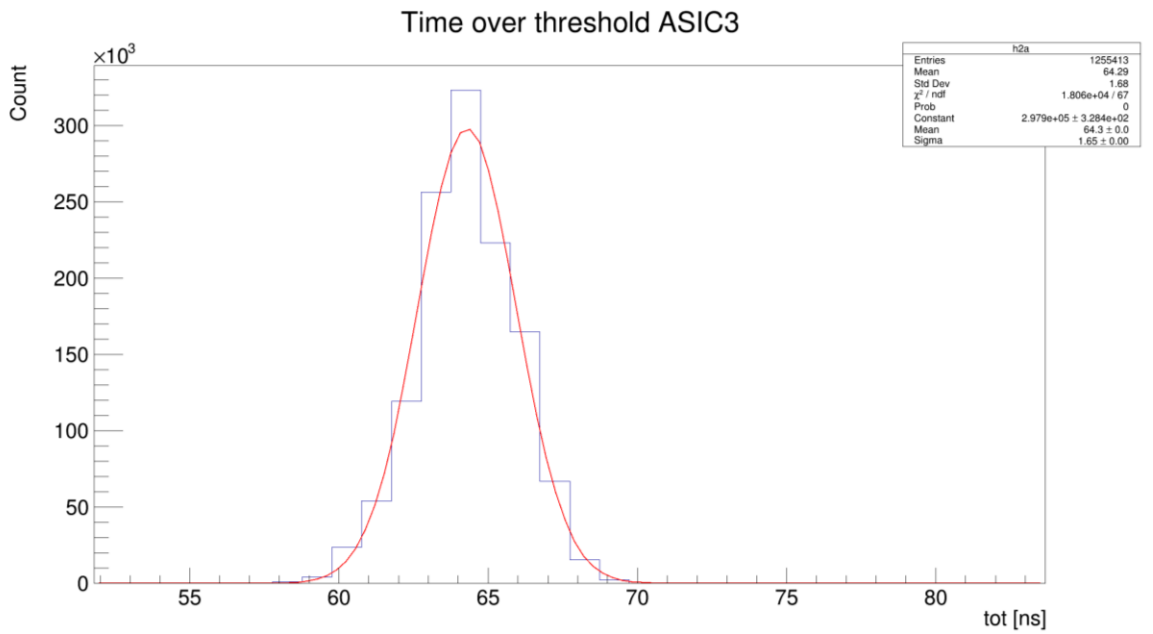


Focus on ASIC

# Results:

- **First LASER pulse tests performed recently**
  - **Single channel responds to LASER stimulation**
  - **Good timing observed**
    - **Example on plots:**
      - **σ of 47 ps on ToA and 1.7 ns on ToT**
  - **LASER energy and frequency need more fine tuning for future measurement campaigns**
- **Measurements and performances will be further investigated in the next days!**



# Perspectives and conclusions

# Perspectives:

- **Characterisation of the Timespot-1 performances are currently on full swing!**
  - Test campaign is helping very strongly to upgrade design and strategies on future ASICs for fast timing tracking
    - **Most of this experience is already merging within the activity of the INFN IGNITE initiative**
  - Confidence with the system and its behaviour is steadily growing

- **Next steps:**
  - Full characterisation the hybrid performance, channel per channel, using LASER setup
  - Possible use of Tspot-1 boards for test beam is under evaluation

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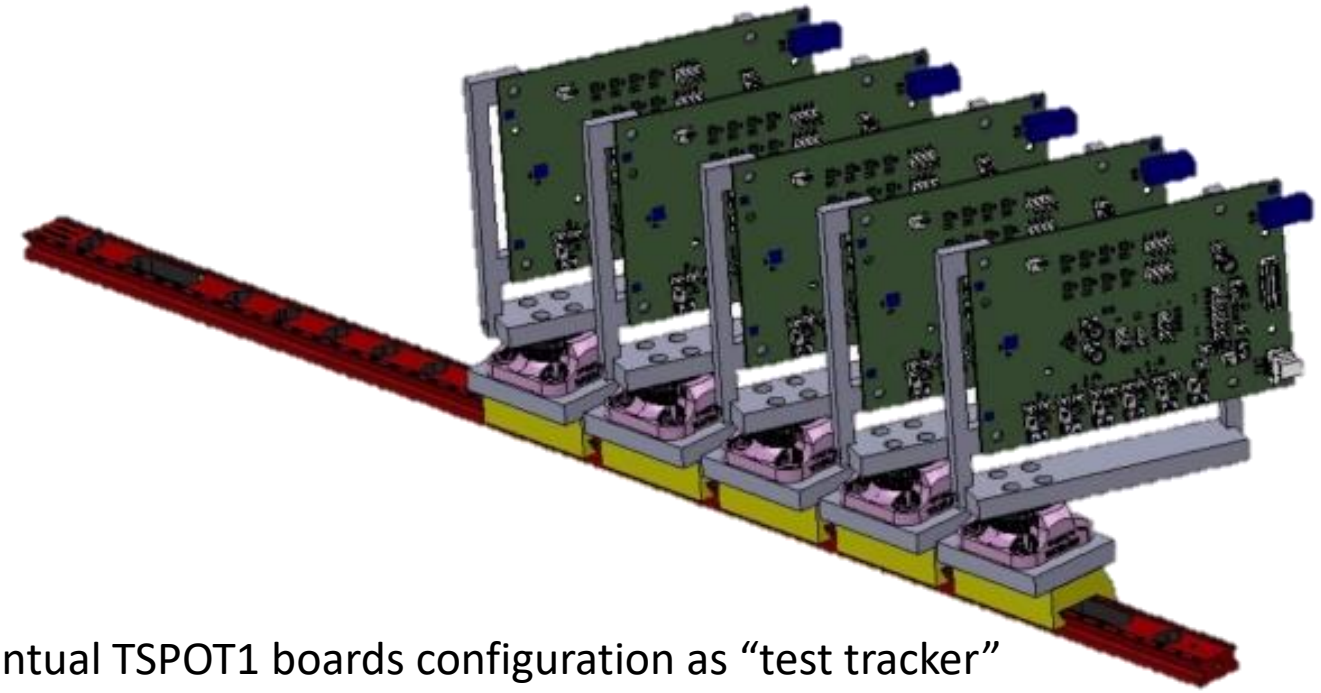
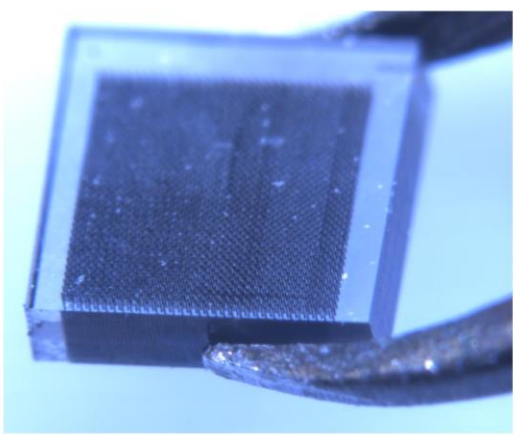


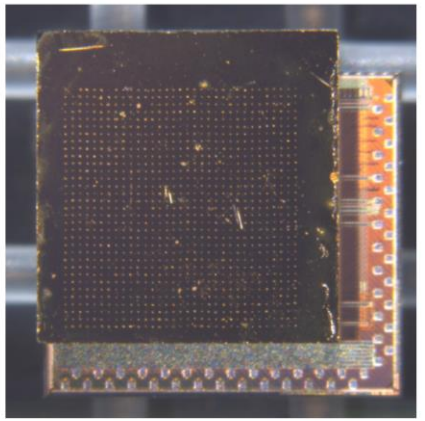
Eventual TSPOT1 boards configuration as “test tracker”

# Conclusions

- **Test activity on the Timespot-1 ASIC is ongoing**
  - **Measurements are ongoing on 3 different levels (only IC, Sr-90 and LASER)**
  - **First results are giving us important feedback on performance and functioning**
    - **Time resolution below 60 ps is achievable with current version**
      - **Lessons learned from test activity will be used in future designs within IGNITE**

- **Testing the hybrid:**
  - **Using TCT, recently started and showed device response**
    - **Resolution as expected**
    - **Setup is in running in conditions**
      - **Future Hydrid characterisation matter of few weeks**
  - **Eventual other tests in evaluation**
    - **Tests with Timespot-1 ASIC hybridised with diamond also started by our colleagues in Florence**



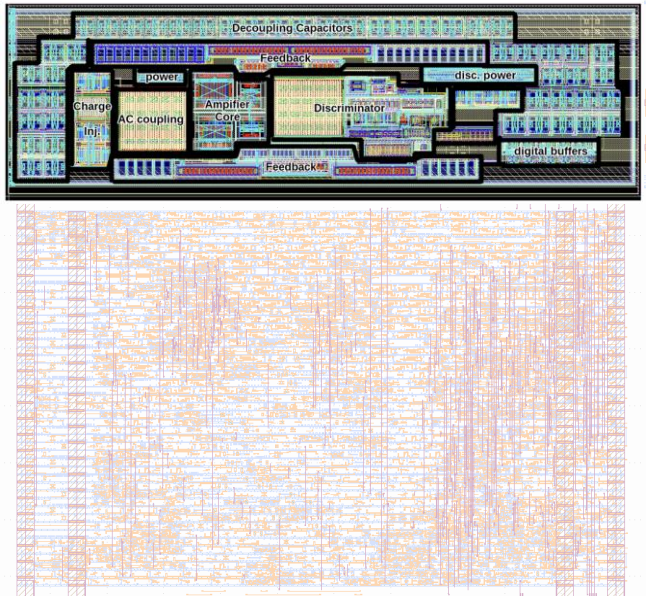


*Sensors* **2022**, *22*, 8722. https://doi.org/10.3390/s22228722

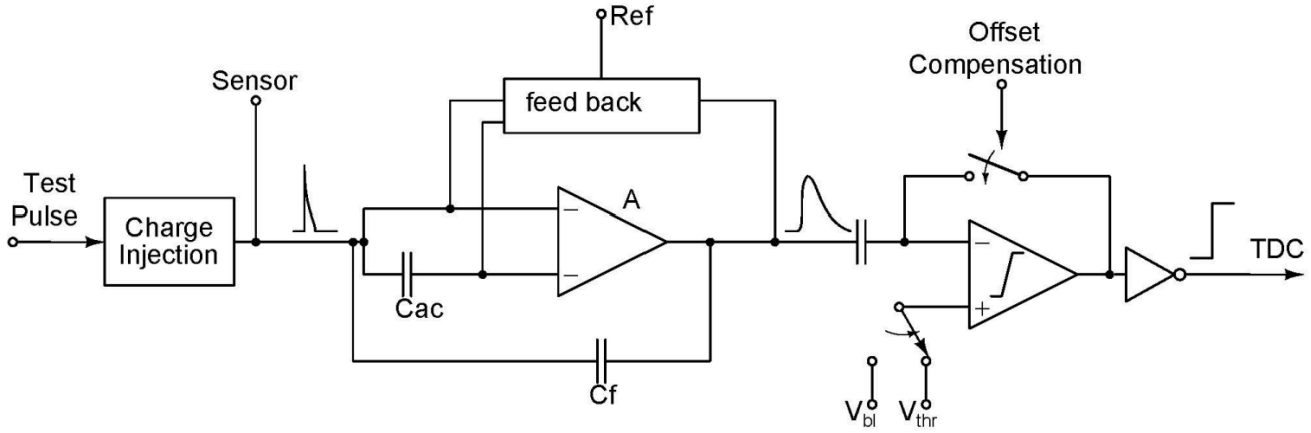
# Backup

# Architecture – Analog FE

- **Front-end**
  - Inverter based CSA
  - DC current compensation with Krummenacher Feedback circuit
  - Discrete offset compensation
  - Leading edge discriminator with discrete time offset compensation for threshold uniformity
- **Features**
  - Internal charge injector
    - Up to 7 fC charge
  - Programmable power consumption
    - 2.3 µW → 32 µW

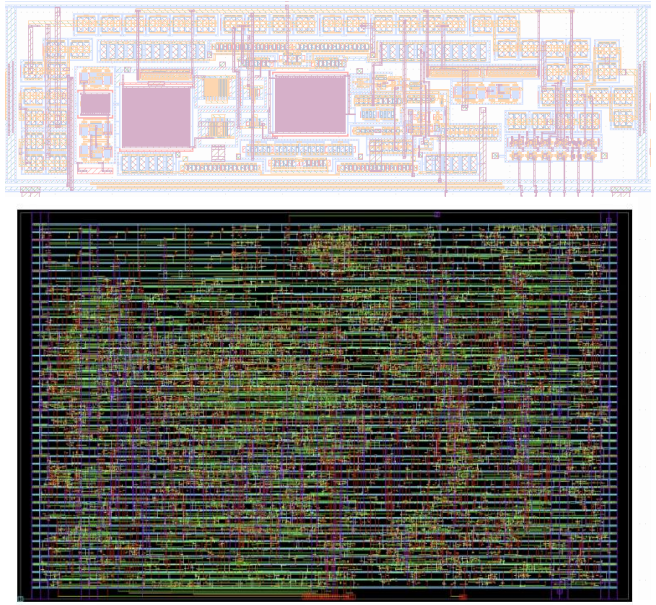


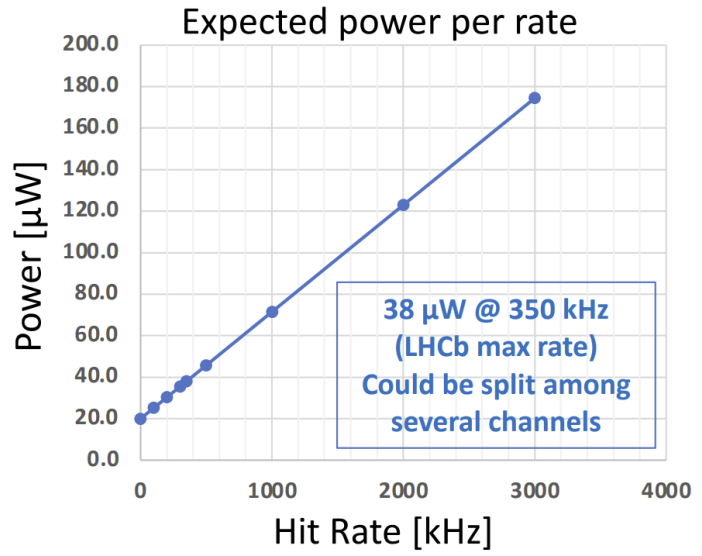

| Pwr regime | nominal | high |
|---|---|---|
| Pwr/channel [µW] | 18.6 | 32.9 |
| Slew rate [mV/ns] | 250 | 360 |
| $Z_{in}$ [Ω] in BW | 23k | 23k |
| Gain [dB] | 93 | 93 |
| RMS noise [mV] | 3.9 | 3.8 |
| BW [MHz] | 311 | 455 |
| Jitter [ps] | 15.6 | 10.5 |

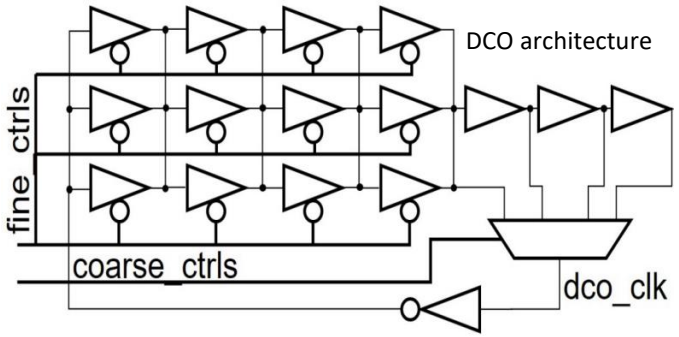


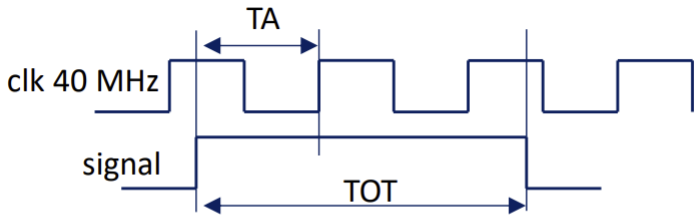
# Architecture – Digital

- **TDC with Vernier Architecture**
  - 2 DCO with frequency around 1GHz
  - DCOs can be turned off after measurement for power saving
- **Performance:**
  - TA measure with 10ps LSB
  - TOT measure with 1ns LSB
- **Max event rate of 3MHz**






$$TA = (cnt_0 - 1)T_0 - (cnt_1 - 1)T_1$$