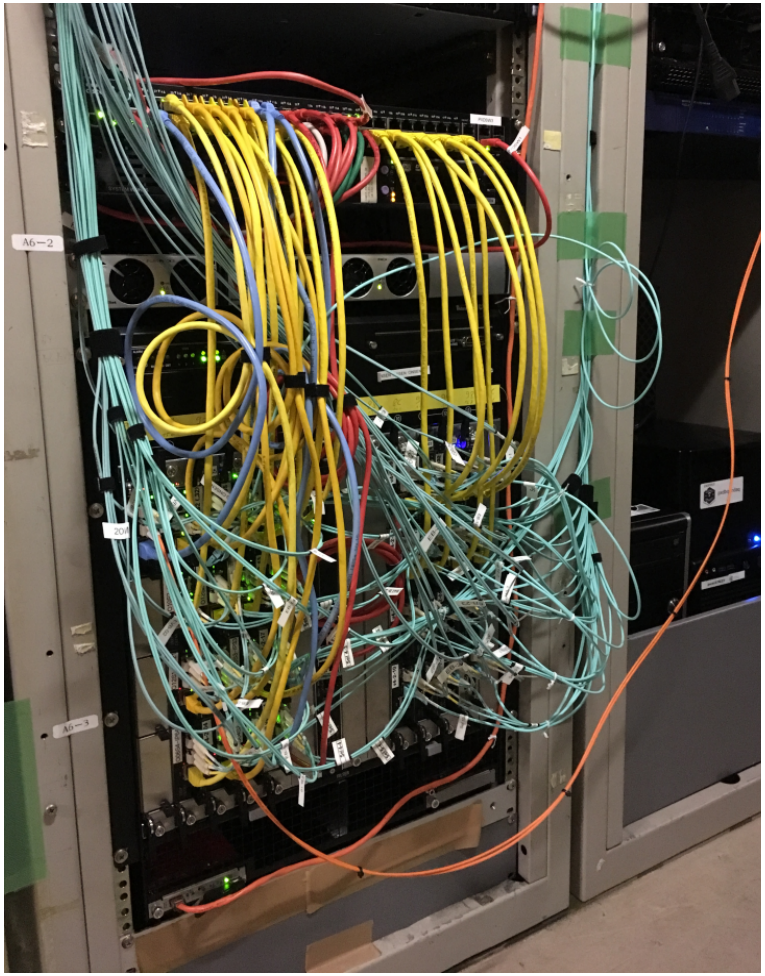

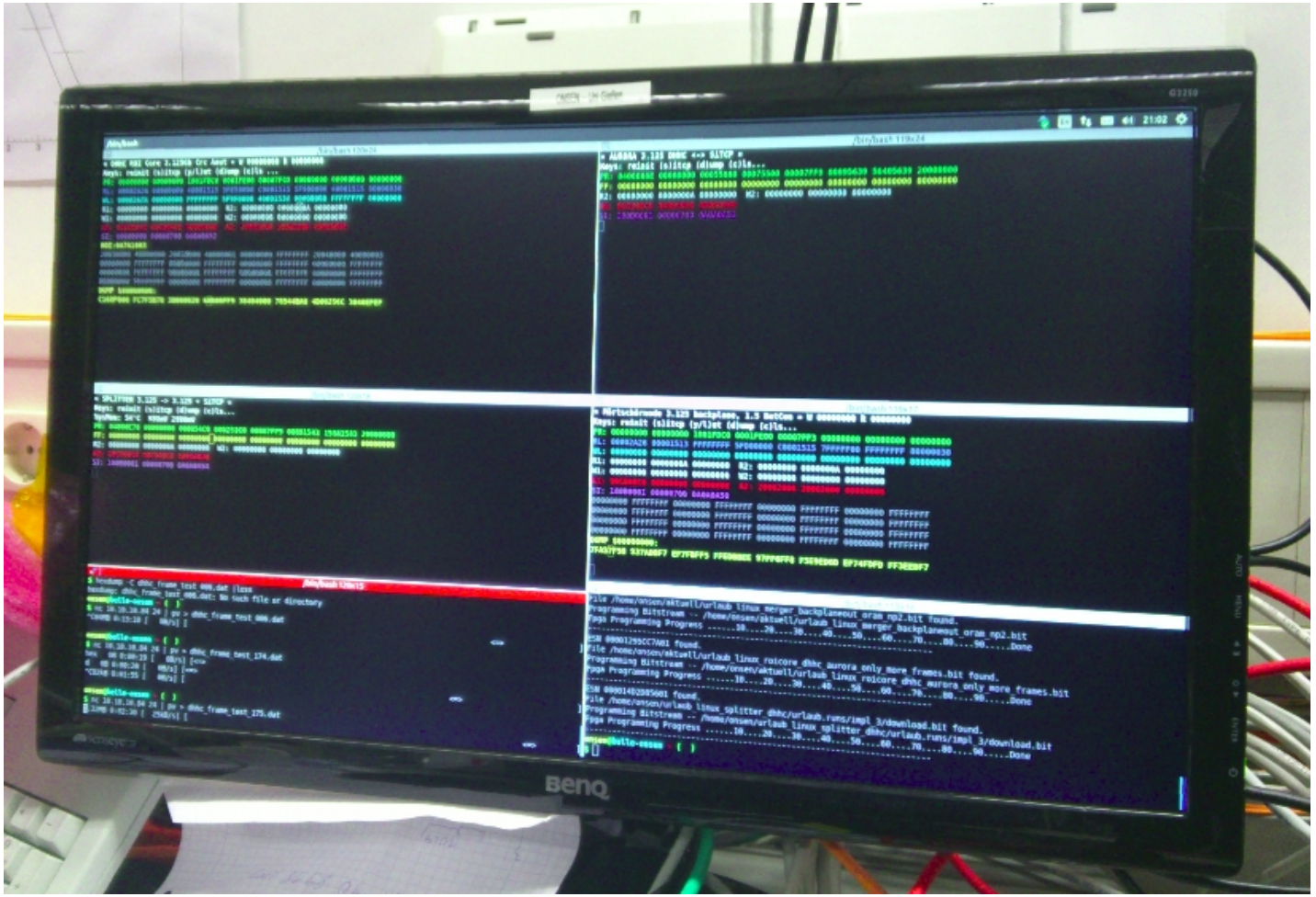

Jens Sören Lange
(Justus-Liebig-Universität Giessen)
EURIZON School, Wuppertal, 19.07.2023

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GIESSEN

DAQ & TRIGGER

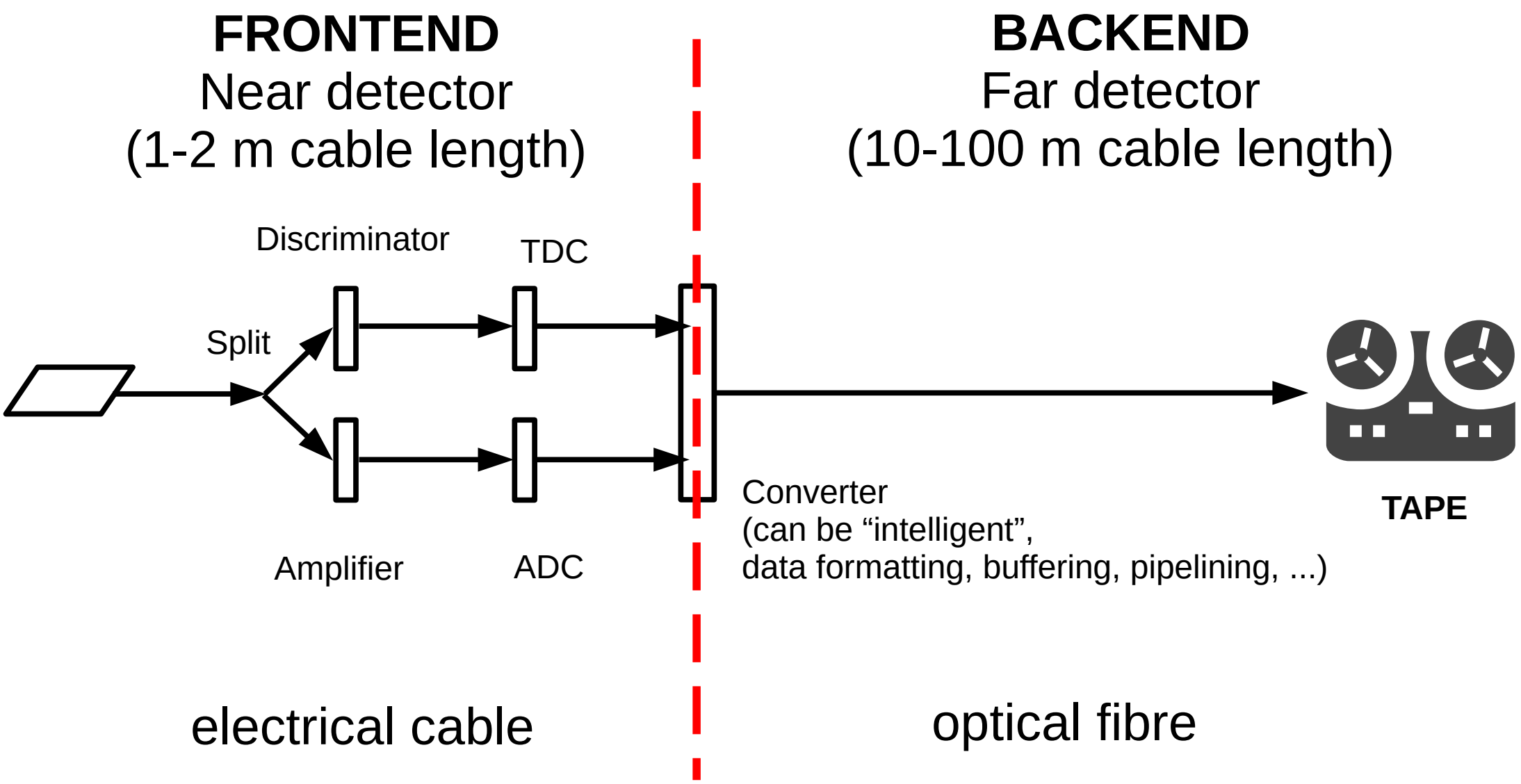
Part I

Delay

- Part I
  - The basics:
    frontend, backend, realtime, discriminator, ADC, TDC, eventbuilder, trigger, latency
  - Example of producing a frontend board
- Part II
  - Example for an experiment with many TDCs
    calculate the data bandwidth
  - Example for an experiment with many ADCs
    calculate the bandwidth
  - Introduction to FPGAs
  - Data links (1G, 5G, ...?)

non-CERN experiments

DAQ for one detector



We often say “Realtime DAQ”, but what is ,,REALTIME” ?

- Definition:

  reply to an INTERRUPT within *n* µs

  (typically n=10, for some systems more strict e.g. airbag in a car)

- Example code:

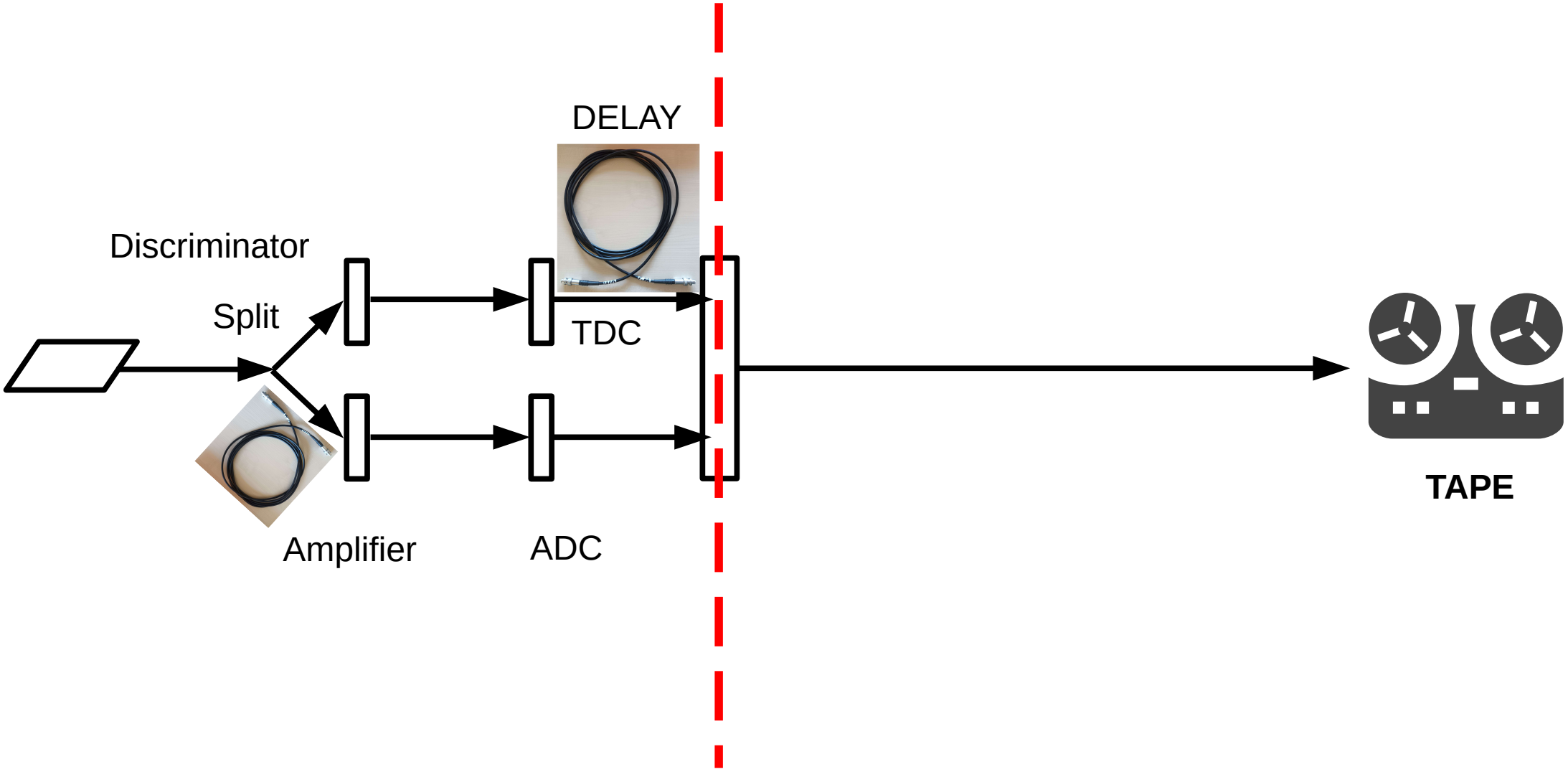
  measure the reply time to an interrupt (CTRL-C) on this computer

```
soeren@soeren-galaxy:~/SOEREN/soeren_BASE/CODE/TUTORIAL/TI/interrupt$ more signal_time.c
#include "stdio.h"
#include "signal.h"
#include "stdio.h"
#include "math.h"
#include "time.h"

struct sigaction naction;

clock_t t_1;
clock_t t_2;

void signal_received(int test)
{

  t_2 = clock();
  double time_taken = ((double)(t_2-t_1))/CLOCKS_PER_SEC;
  printf("Time for catching CTRL-C %f %f %f\n", (double)t_1, (double)t_2, time_taken);
  return;

}

int main()
{

  while(1) {
    t_1 = clock();
    sigaction(SIGINT, (struct sigaction *)0, &naction);
    naction.sa_handler = signal_received;
    sigaction(SIGINT, &naction, (struct sigaction *)0);
  }

  return 0;

}
```

Measure the time of ,,catching'' an interrupt on a PC

```
soeren@soeren-galaxy:~/SOEREN/soeren_BASE/CODE/TUTORIAL/TI/interrupt$ gcc signal_time.c
soeren@soeren-galaxy:~/SOEREN/soeren_BASE/CODE/TUTORIAL/TI/interrupt$ ./a.out
^CTime for catching CTRL-C 1546174.000000 1546179.000000 0.000005
^CTime for catching CTRL-C 1901502.000000 1901507.000000 0.000005
^CTime for catching CTRL-C 2139984.000000 2139991.000000 0.000007
^CTime for catching CTRL-C 2334249.000000 2334255.000000 0.000006
^CTime for catching CTRL-C 2556517.000000 2556523.000000 0.000006
^CTime for catching CTRL-C 2813186.000000 2813192.000000 0.000006
^CTime for catching CTRL-C 3011919.000000 3011925.000000 0.000006
^CTime for catching CTRL-C 3174031.000000 3174038.000000 0.000007
^CTime for catching CTRL-C 3345678.000000 3345683.000000 0.000005
^CTime for catching CTRL-C 3561479.000000 3561486.000000 0.000007
^CTime for catching CTRL-C 3755866.000000 3755871.000000 0.000005
^CTime for catching CTRL-C 3944870.000000 3944877.000000 0.000007
^CTime for catching CTRL-C 4100340.000000 4100346.000000 0.000006
^CTime for catching CTRL-C 4300448.000000 4300455.000000 0.000007
^CTime for catching CTRL-C 4483679.000000 4483685.000000 0.000006
^CTime for catching CTRL-C 4677947.000000 4677952.000000 0.000005
^CTime for catching CTRL-C 4855793.000000 4855799.000000 0.000006
^CTime for catching CTRL-C 5033488.000000 5033494.000000 0.000006
^CTime for catching CTRL-C 5238807.000000 5238813.000000 0.000006
^CTime for catching CTRL-C 5449759.000000 5449765.000000 0.000006
^CTime for catching CTRL-C 5643917.000000 5643924.000000 0.000007
^CTime for catching CTRL-C 5821592.000000 5821598.000000 0.000006
```

DAQ for one detector



Signals (arrival and propagation) and processing times may have different timings and may need **DELAY**

Delay

- There are fast detectors (e.g. 1 ns), there are slow detectors (e.g. 100 ns)
- There are fast modules, there are slow modules
- Needs compensation (signals should arrive synchronously)
- Easiest and cheapest solution: cable!
- Speed of light is ~30 cm/ns,
  speed of light in the cable is about ~20 cm/ns
- Cables can be purchased not as “length 40 cm” but as “length 2 ns”,
  which includes any delay in the connectors (guaranteed by the company)

DAQ for many detectors

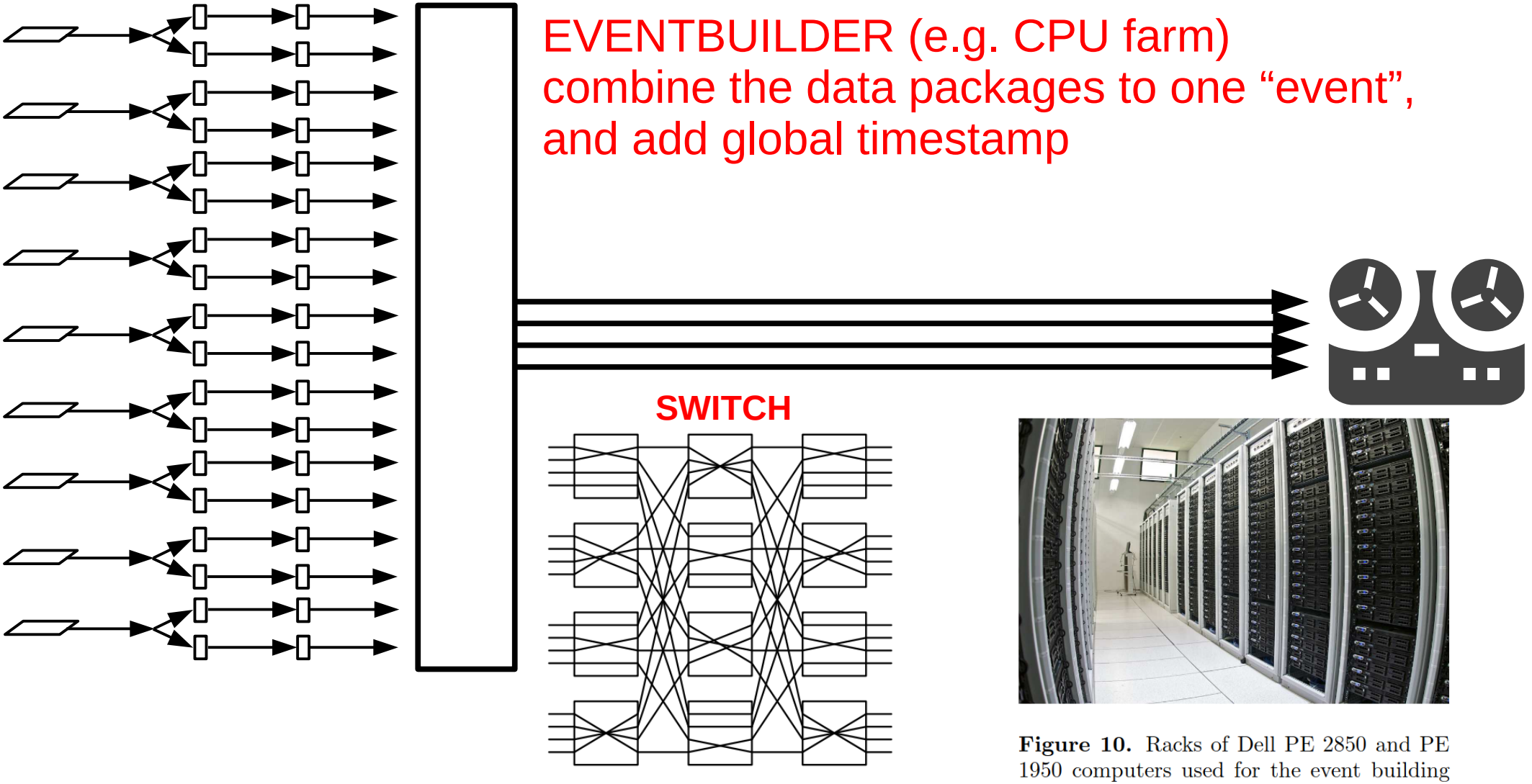


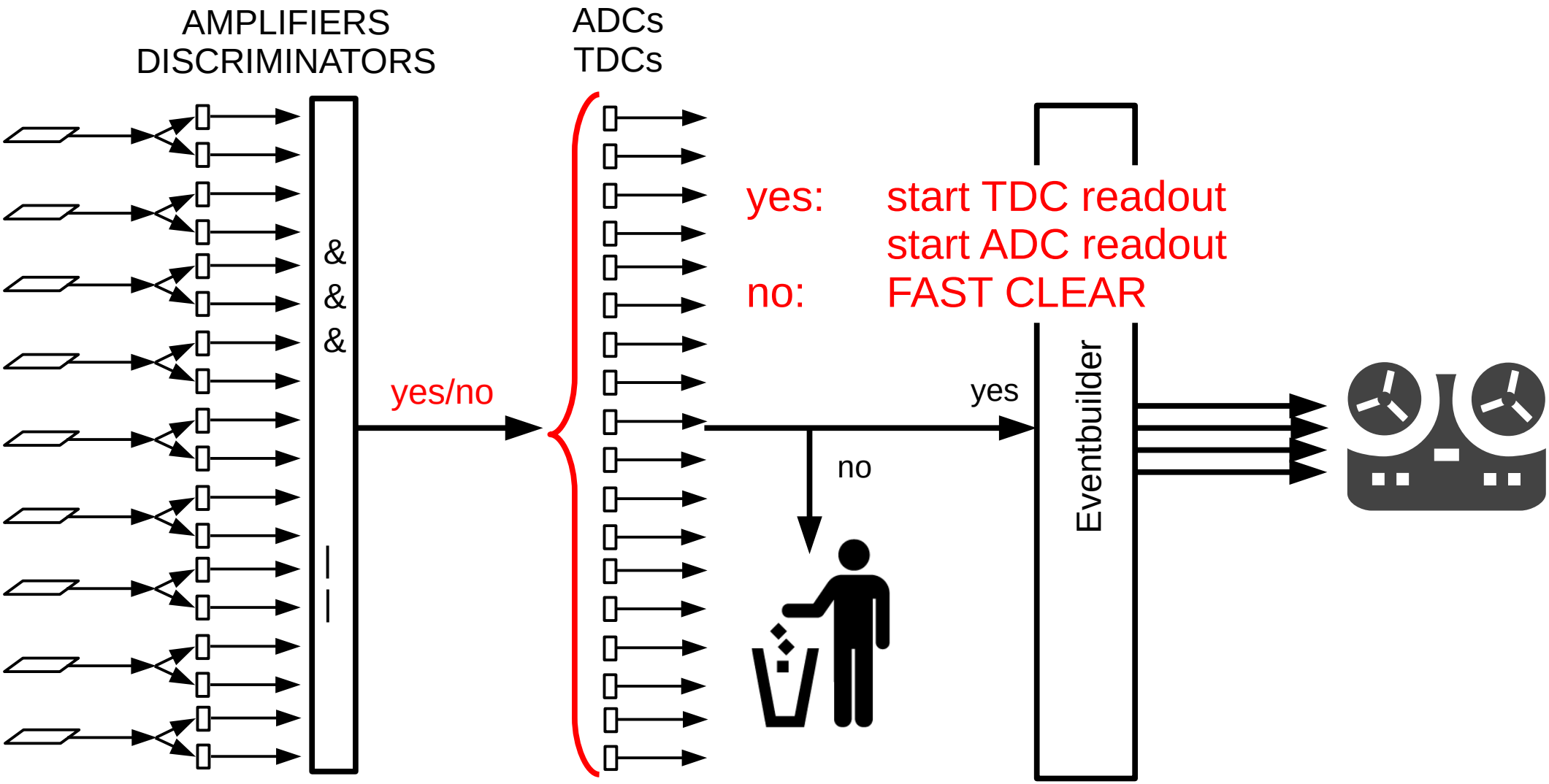
Figure 10. Racks of Dell PE 2850 and PE 1950 computers used for the event building and for the high-level triggers.

https://www.wikiwand.com/en/Nonblocking_minimal_spanning_switch#Media/File:Minimal_spanning_switch_4_4_4.svg

G. Bauer et al. (CMS), Journal of Physics: Conf. Ser. 219 (2010) 022038

Level-1 Trigger

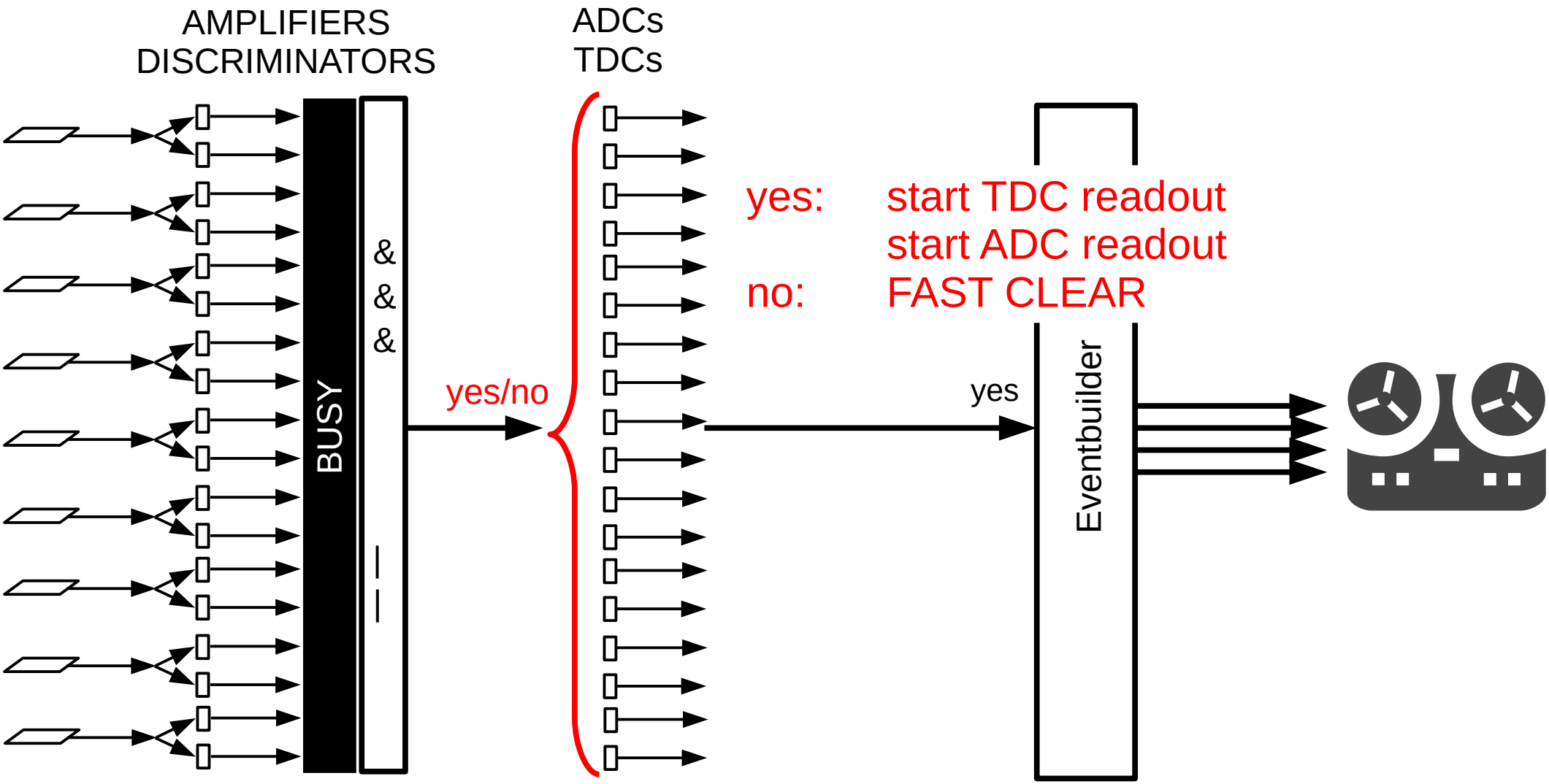
Hardware trigger
sometimes called Level-0 trigger



Logical operations (AND, OR) can be quite complex
(e.g. detector hits combined to clusters and tracks, and counted)
trigger rate can be ~1 kHz to ~1 MHz

Level-1 Trigger

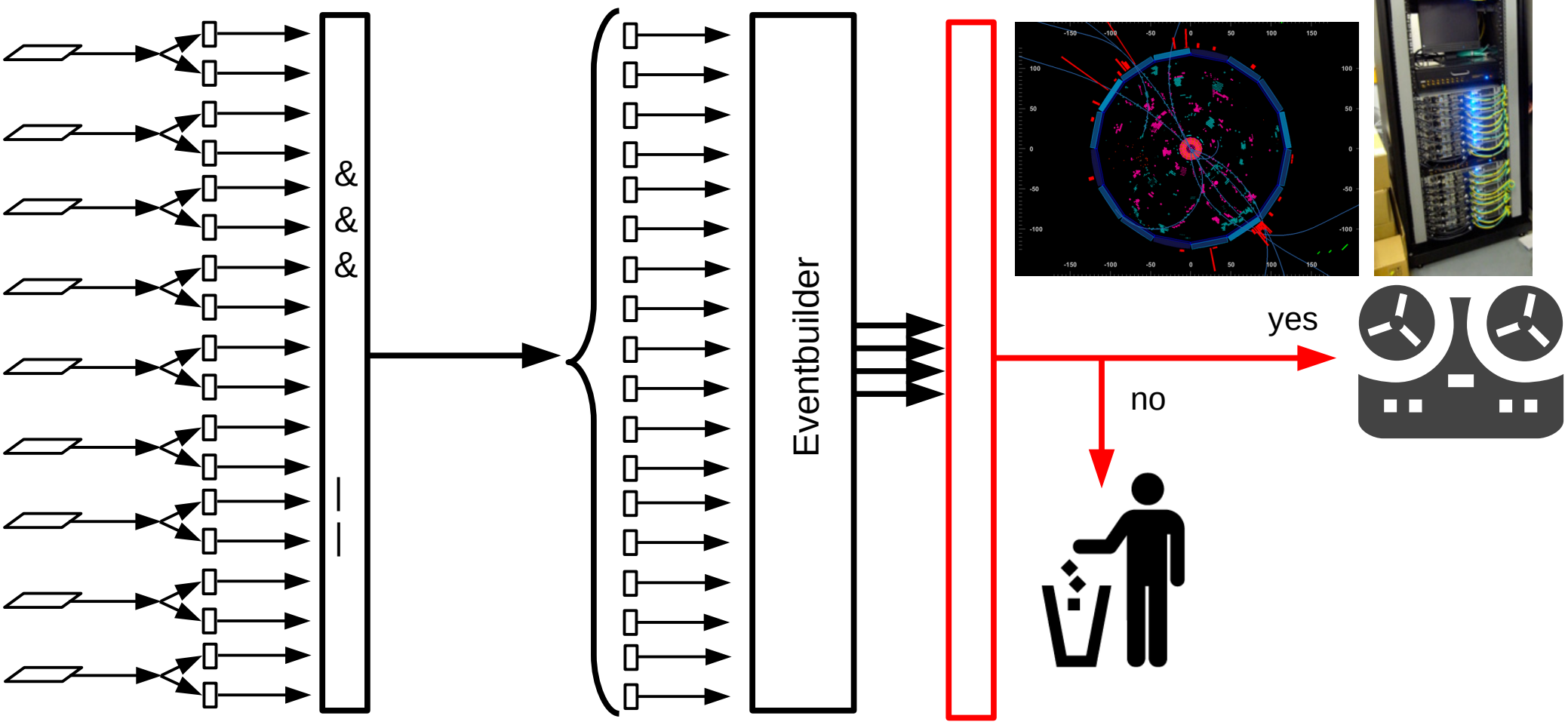
Hardware trigger
sometimes called Level-0 trigger



Logical operations (AND, OR) can be quite complex
(e.g. detector hits combined to clusters and tracks, and counted)
trigger rate can be ~1 kHz to ~1 MHz

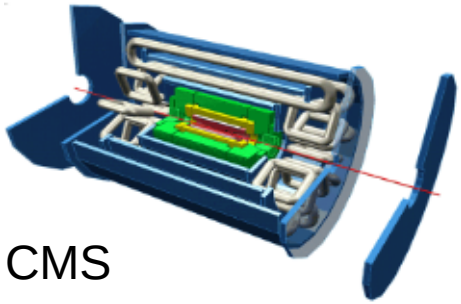
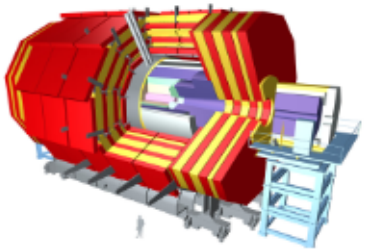
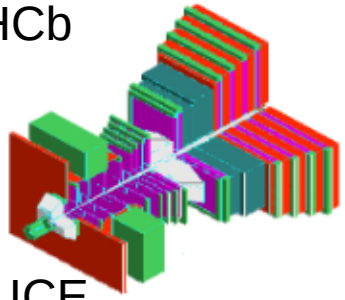
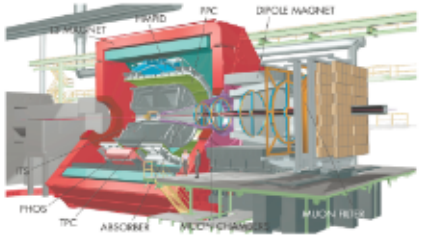
High Level Trigger

Software trigger
sometimes called Level-3 trigger



Full event reconstruction
(invariant mass, topology, missing energy, ...)

Trigger and DAQ numbers at CERN

	No.Levels Trigger	Level-0,1,2 Rate (Hz)	Event Size (Byte)	Readout Bandw.(GB/s)	HLT Out MB/s (Event/s)
ATLAS 	3	LV-1 10^5 LV-2 $3x10^3$	$1.5x10^6$	4.5	300 ($2x10^2$)
CMS 	2	LV-1 10^5	10^6	100	100 (10^2)
LHCb 	2	LV-0 10^6	$3x10^4$	30	40 ($2x10^2$)
ALICE 	4	Pp-Pp 500 p-p 10^3	$5x10^7$ $2x10^6$	25	1250 (10^2) 200 (10^2)

C. Schwick (CERN/CMS), DESY Seminar, 17.10.2007

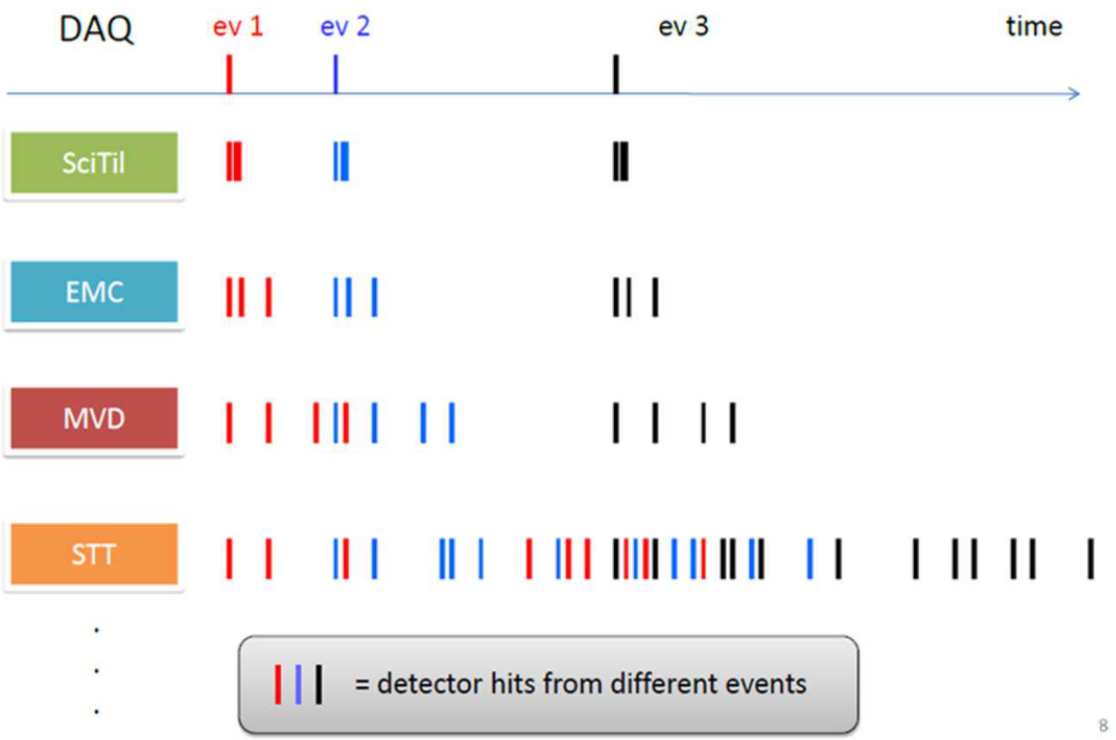
Belle II (10^4 Events/s)

What is ,,triggerless" DAQ?

There is a new generation of experiments, in which no Level-1 trigger is issued.

The frontend is pushing all data ,,self-triggered''.

Examples: LHCb, DUNE, Panda (see below).



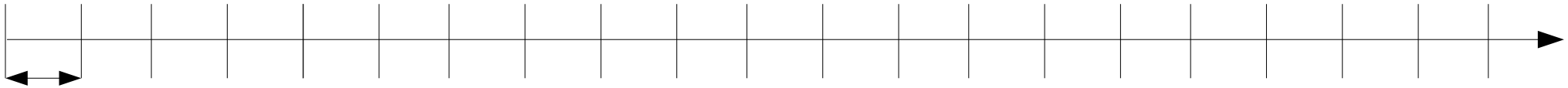
Data are ordered and combined based upon time stamps.

S. Spataro, Journal of Physics: Conference Series 396 (2012) 022048

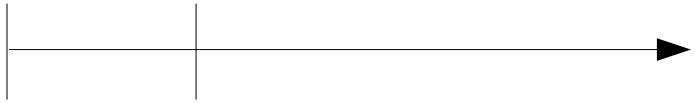
What is “latency” ?

The time to form the trigger decision and send it to the TDCs and ADCs.

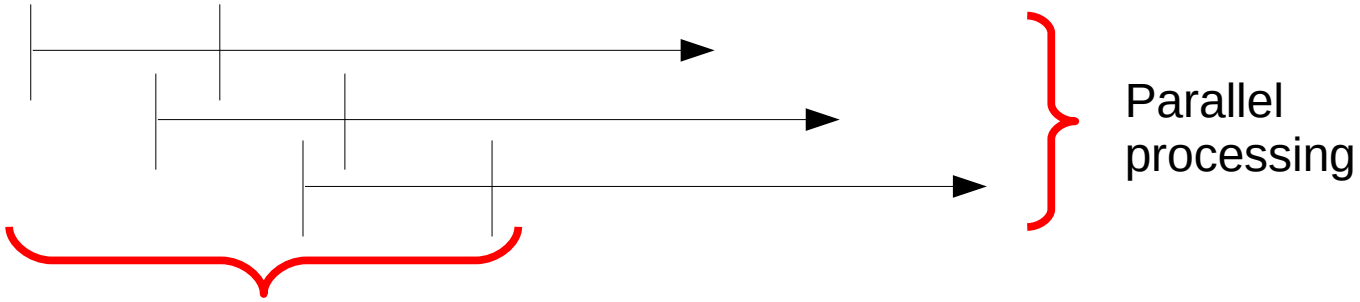
Example: trigger rate 10 kHz



0.1 ms
i.e. average time distance between 2 triggers arriving.



Latency can be larger, e.g. 1 ms !
i.e. average time in which the trigger is working on the frontend data.



Example
STAR Experiment

	τ
Level-0	1.5 μs
Level-1	100 μs
Level-2	5 ms
Level-3	200 ms

Data links

- Central components of every DAQ system, for data transfer

- Electrical links
  - backplane (inside a crate)
  - cables (twisted pair or shielded)
- Optical links
  - fibres

Cables and connectors

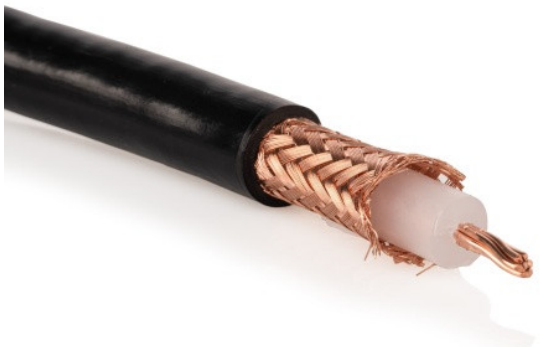
- Type I: Coaxial cables (with shielding)
- Type II: Differential cable, often “twisted pair”
- We say “50 Ohm cable”
- This is stable impedance up to high frequencies (e.g. 3 GHz).

Amphenol Cables on Demand

RG58 cable with BNC adapters

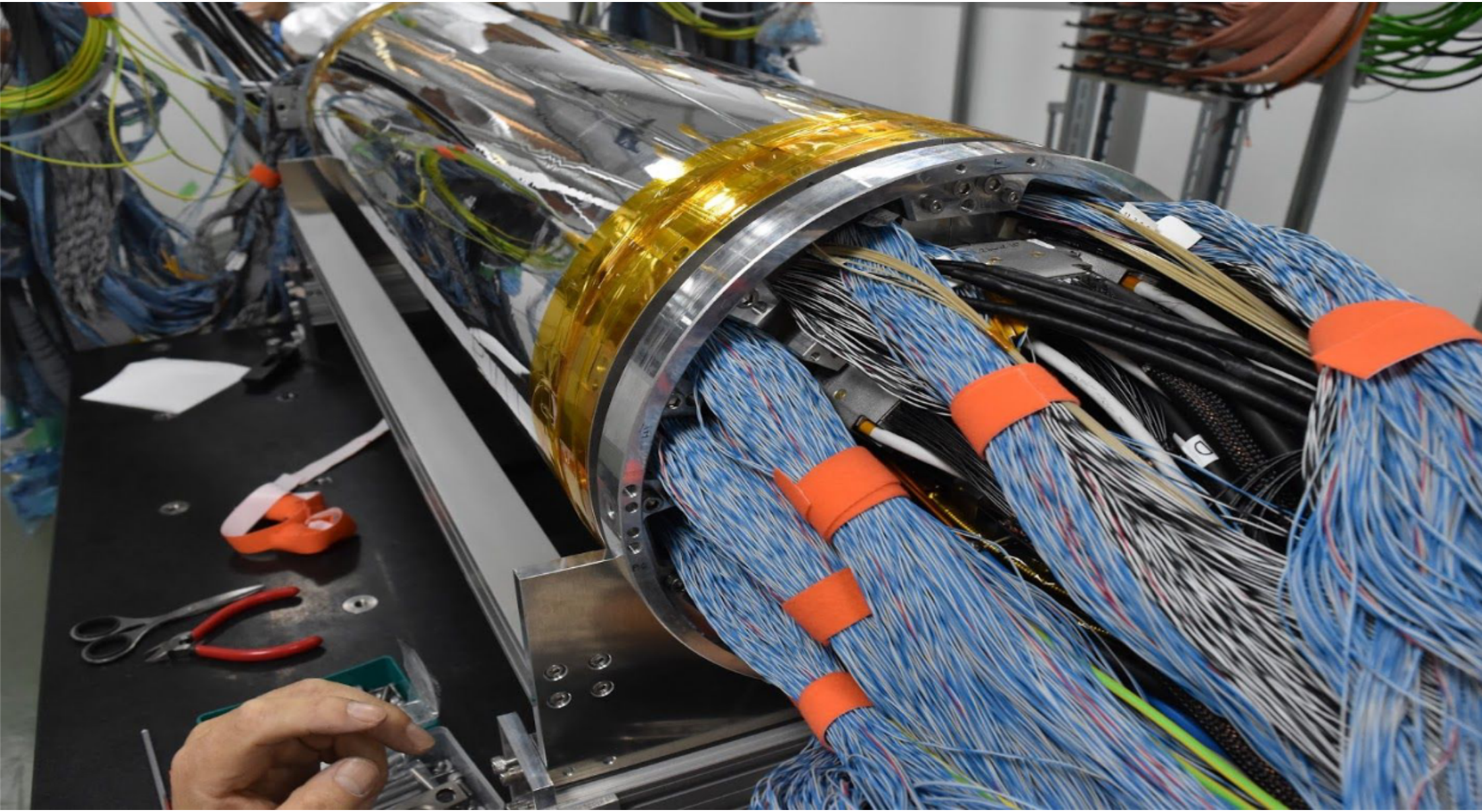
S Fifteen Instruments

Lemo cable with lemo connector

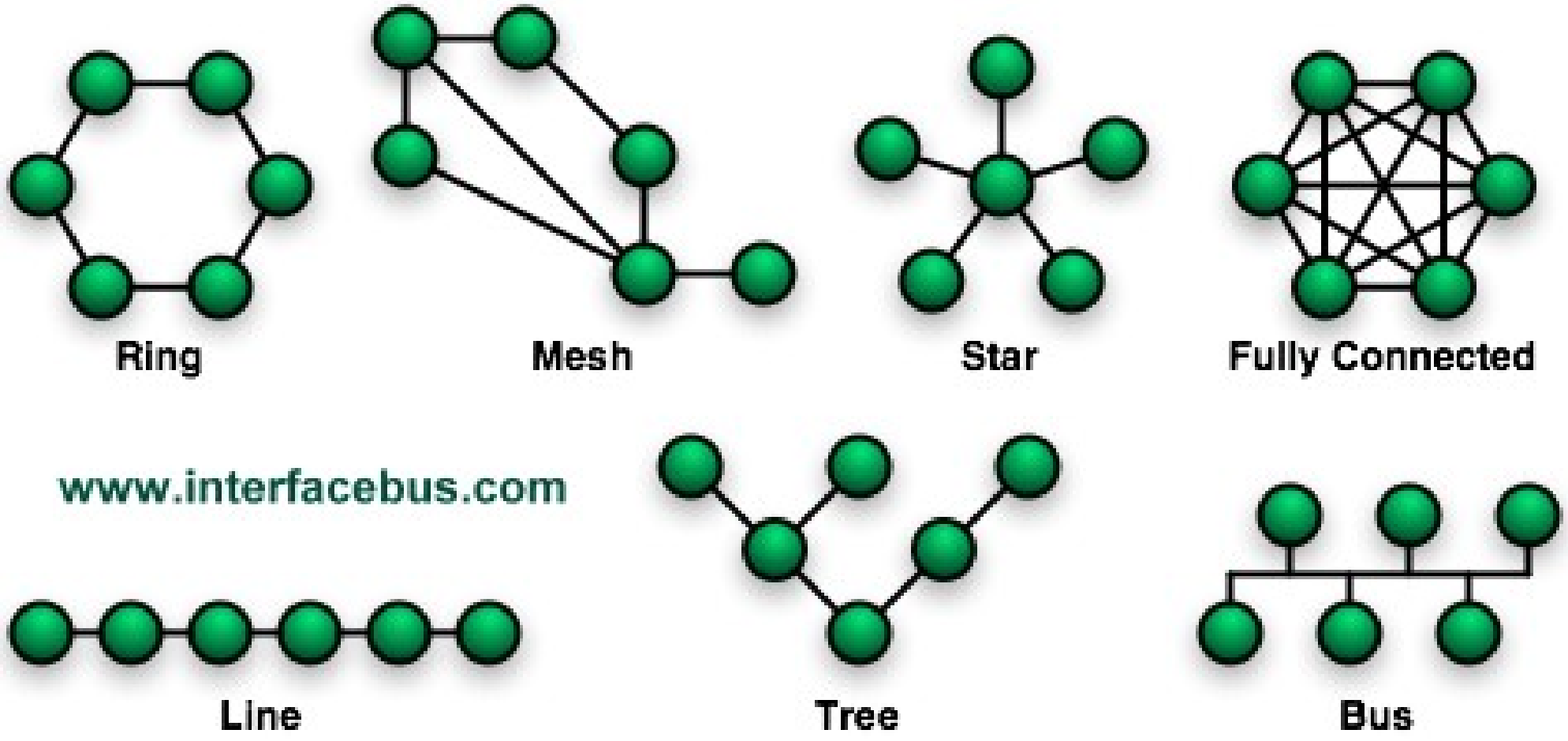


https://www.mcgillmicrowave.com/product/rg58/

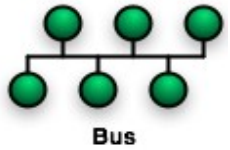
Twisted pair cable (Belle II Vertexdetector)



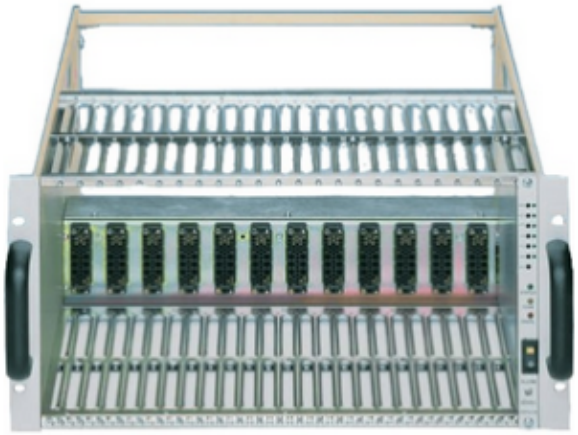
Topologies of DAQ systems



Crates



wiener-d.com



NIM Crates

12 slots, unintelligent,
e.g. for discriminators, amplifiers
power on pins (e.g. $\pm$12 V)

CAMAC Crates

25 slots
intelligent (data bus, CNAF)
e.g. for TDC, ADC
bandwidth 4 Mbytes/s

VME Crates

21 slots
bandwidth 40 Mbytes/s
2 x 160 pins (many!)
Parallel, asynchronous bus
industrial standard (cheaper!)

PCIexpress

- Crates are nowadays
  often slots in a PC
- Not a bus anymore,

  but a point-to-point link
- Data not transferred on parallel lines
  but on one or several serial lanes

  (serial here means:
  1 byte is transmitted as 8 bits serial)
- Lane: one pair of differential lines per direction

  (low voltage differential signal)
- 250 MB/s (PCIe 1.0)
  data transfer rate per lane
- Devices (DAQ boards)
  support up to 32 lanes

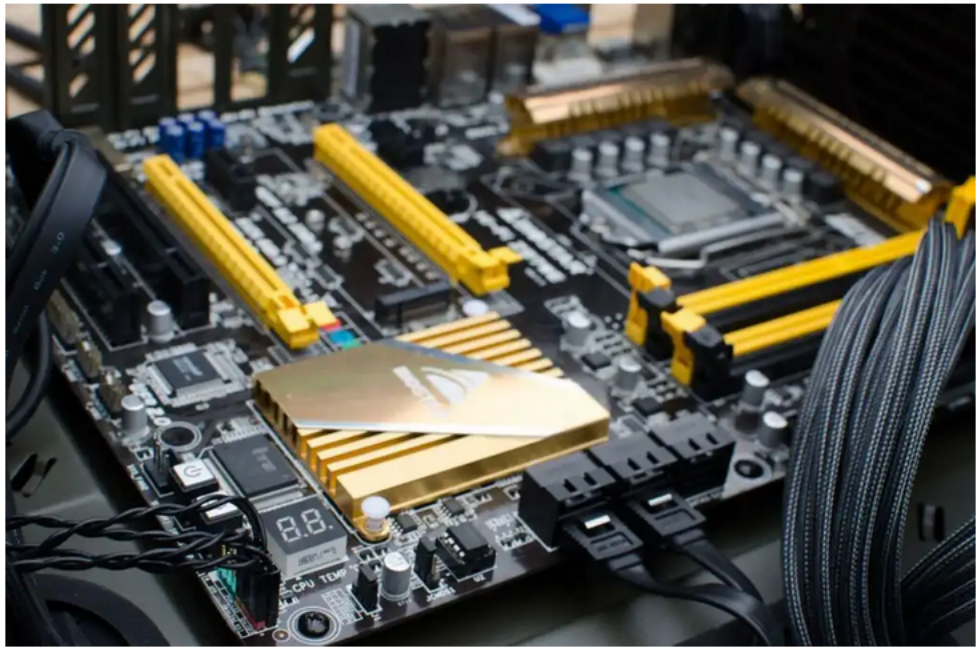
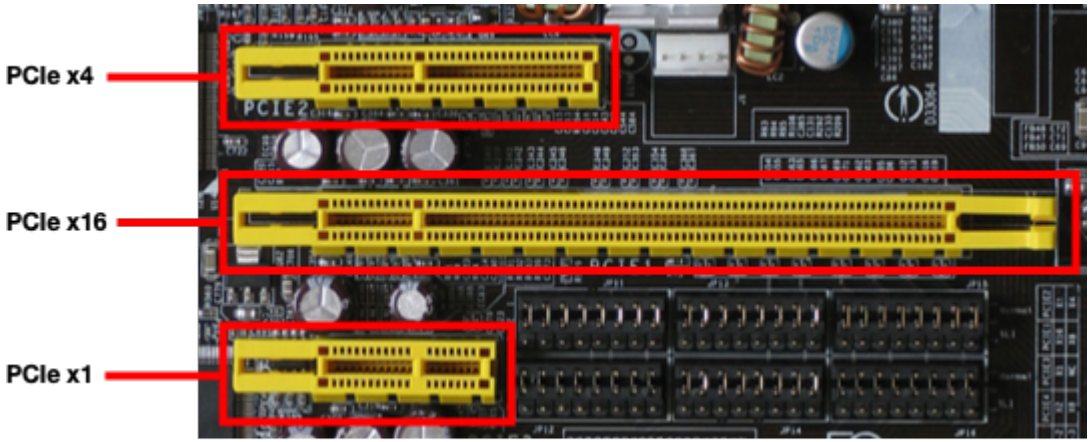


Image: Thomas Ryan/IDG

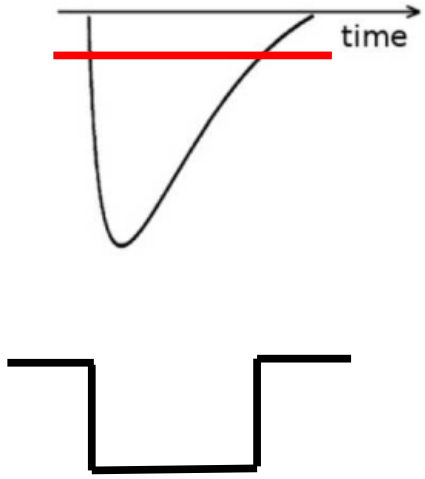
pcwelt.de

Elektronik-Kompendium.de



Discriminator

CAEN N605



- Transforming an analog signal into a digital signal
- Type I: Leading edge discriminator
  "walk" (different t_{START} for different amplitudes)
- Type II: Constant fraction discriminator

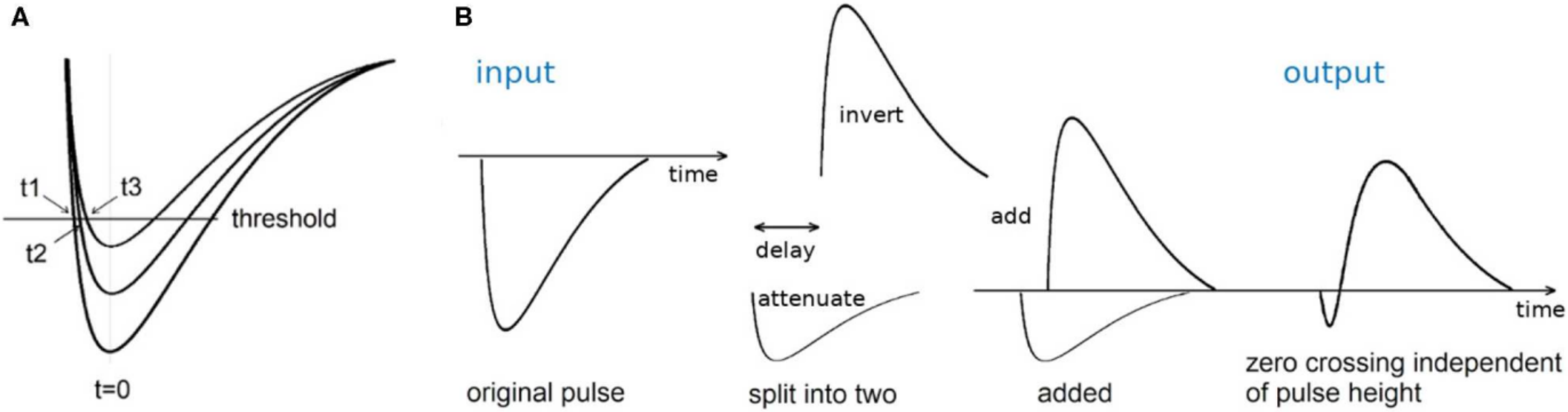
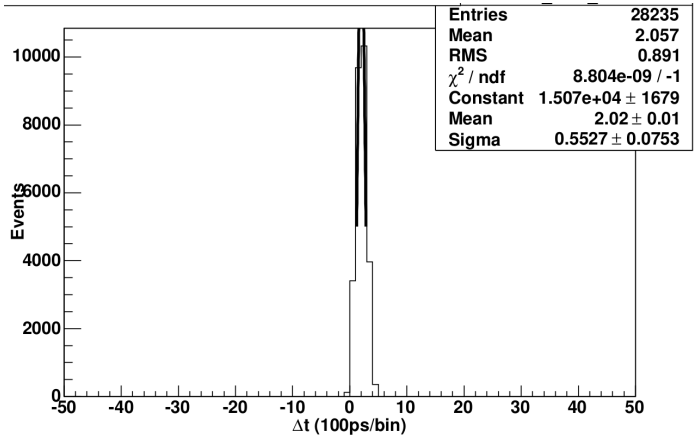


FIGURE 8 | (A) Schematic of leading edge discrimination. The fixed threshold times the pulses (all arriving at the same time t = 0) at different times t1, t2, and t3, depending on the pulse height. **(B)** Schematic of constant fraction discrimination. The original input pulse is split into two, one is attenuated, and one is delayed and inverted. The zero-crossing when the two pulses are added is independent of the pulse height.

Hirvonen, Suhling, Frontiers in Physics 8 (2020) 161

TDC (Time-to-Digital Converter)

- As a board (CAMAC or VME) or as a chip
- Typical time-of-flight s=3 m → t=10 ns
- Typical time resolution 25 ps
- Needs 2 signals: START, STOP



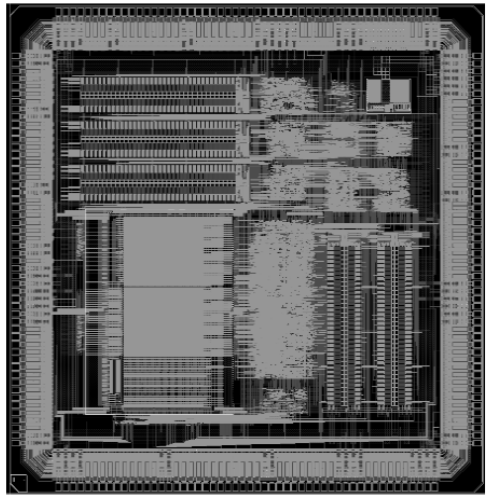
Version: 2.2

HPTDC

High Performance Time to Digital Converter

Version 2.2, March 2004

for HPTDC version 1.3



J. Christiansen
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V1290A-2eSST

32 Channel Multihit TDC (25 ps)

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Manuals | Downloads

Features

- 25 ps LSB
- 21 bit resolution
- 52 µs full scale range
- ECL/LVDS Input Signals
- 5 ns Double Hit Resolution
- Trigger Matching and Continuous Storage acquisition modes
- Leading and/or Trailing Edge detection
- 32 k x 32 bit output buffer
- MBLT, CBLT and 2eSST data transfer
- Multicast commands

https://cds.cern.ch/record/1067476/files/cer-002723234.pdf

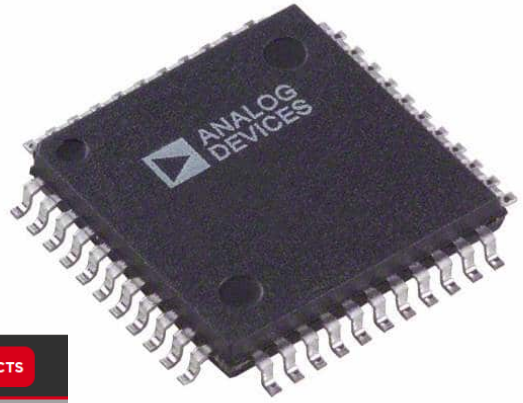
ADC (Analog-to-Digital Converter)

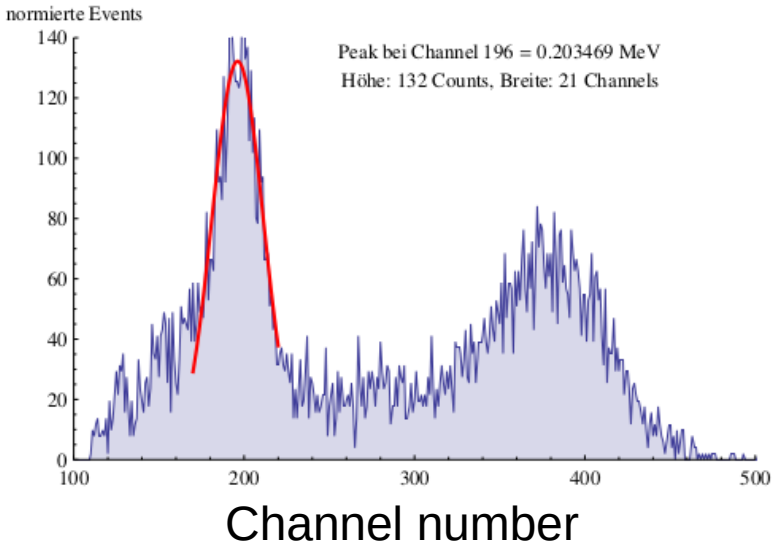
AD9042
12-bit
41 MSPS
only 595 mW
(e.g. used by CMS)

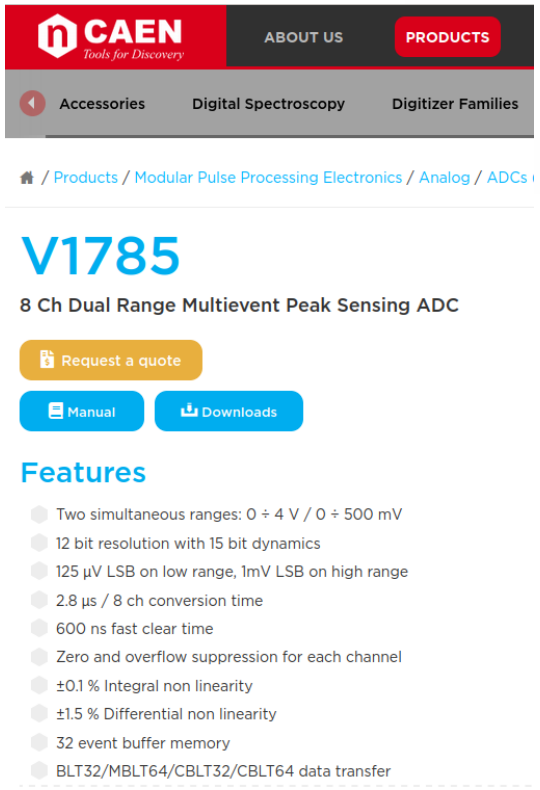
- As a board (CAMAC or VME) or as a chip
- “8 bit ADC” means amplitude is divided and digitized into 2^8=256 steps
- Type I: peak sensing (“ADC”)
- Type II: charge integrating (“QDC”)
- conversion time often order of µs

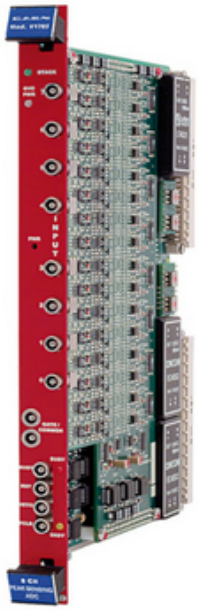
  ,,slow’’

  (needs delay in parallel DAQ path)



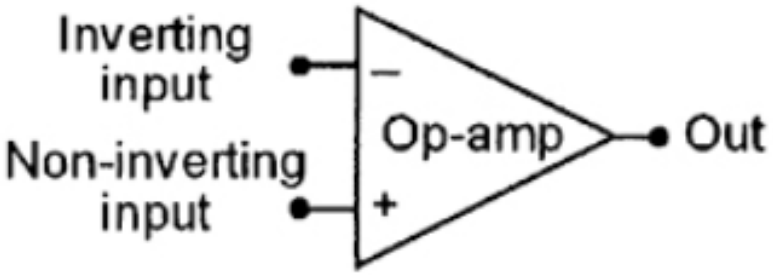






Central element in an ADC: comparator

Operational amplifier, but without capacitors (used for frequency stabilisation)



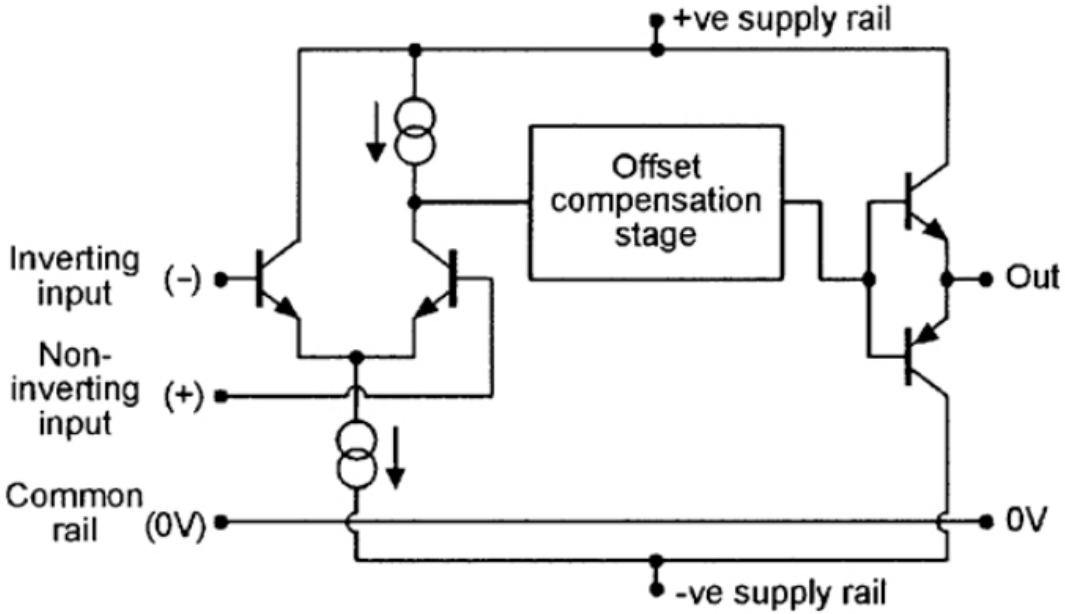
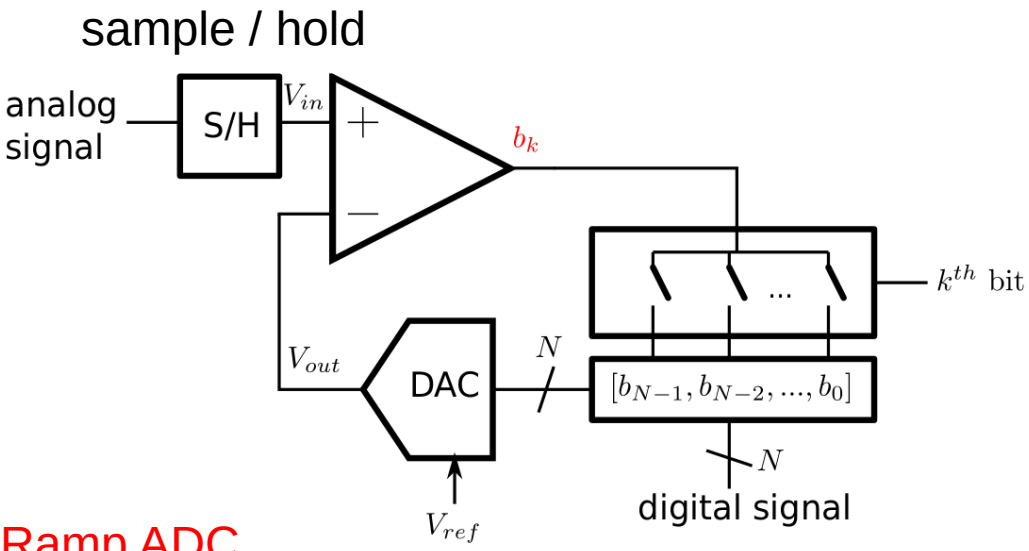


FIGURE 1. Simplified op-amp equivalent circuit.

https://www.nutsvolts.com/magazine/article/op-amp-cookbook

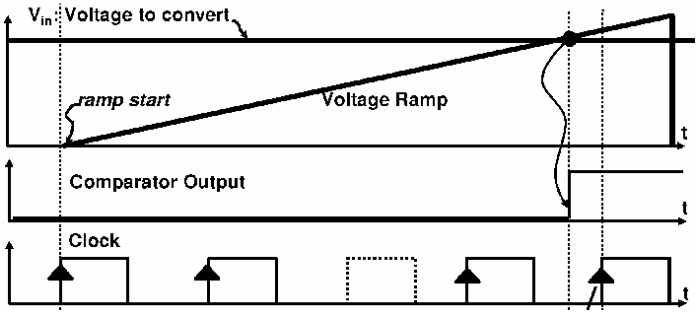
What is inside an ADC?

SAR (successive approximation register) ADC

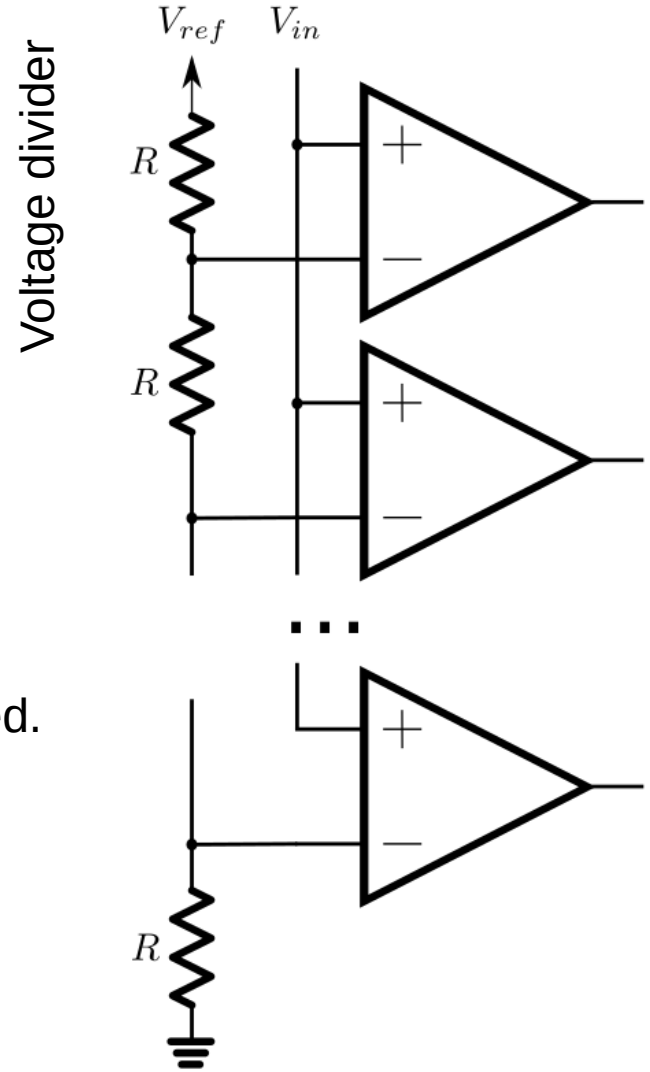


Ramp ADC

During sampling phase, a capacitor is charged.
While discharging, number of clocks of given frequency are counted.



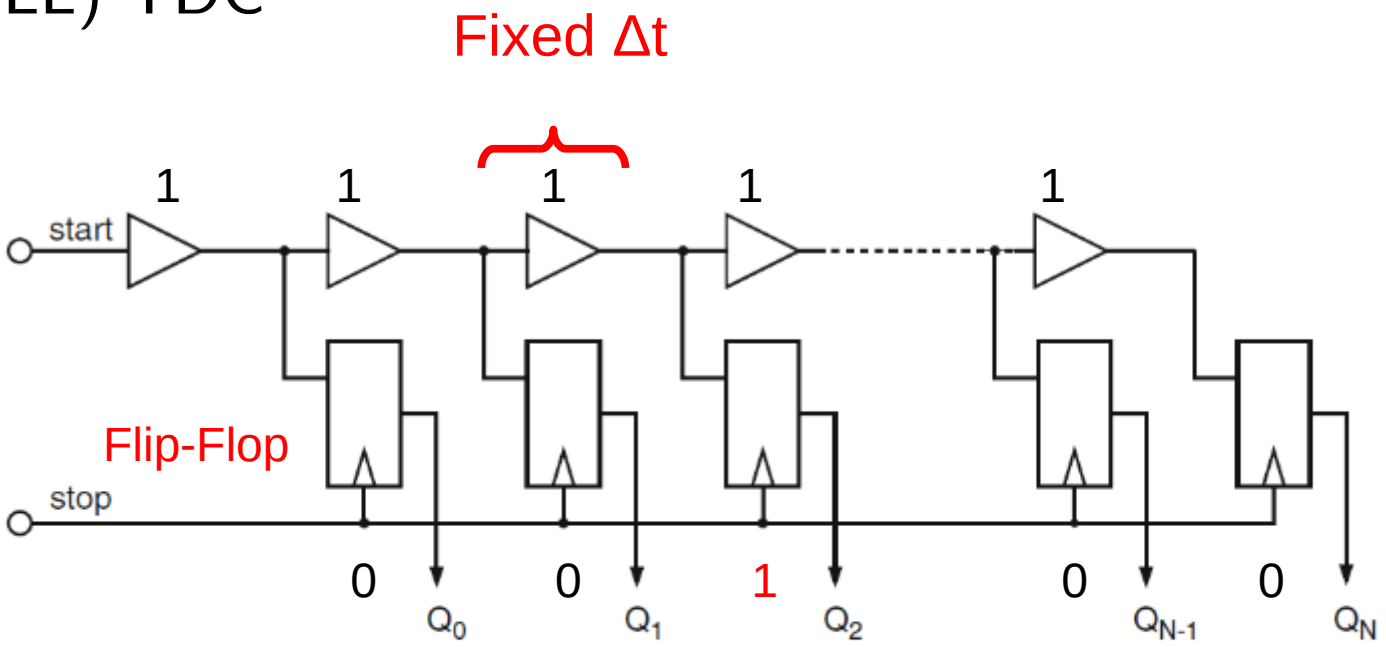
Flash-ADC



http://book.itep.ru/depository/ADC/Analog-Digital_Converters_(ADC)_Tutorial.htm
https://www.nutsvolts.com/magazine/article/op-amp-cookbook
E. Delagnes, IEEE Transactions on Nuclear Science 54 (2007) 1735

What is inside a TDC?

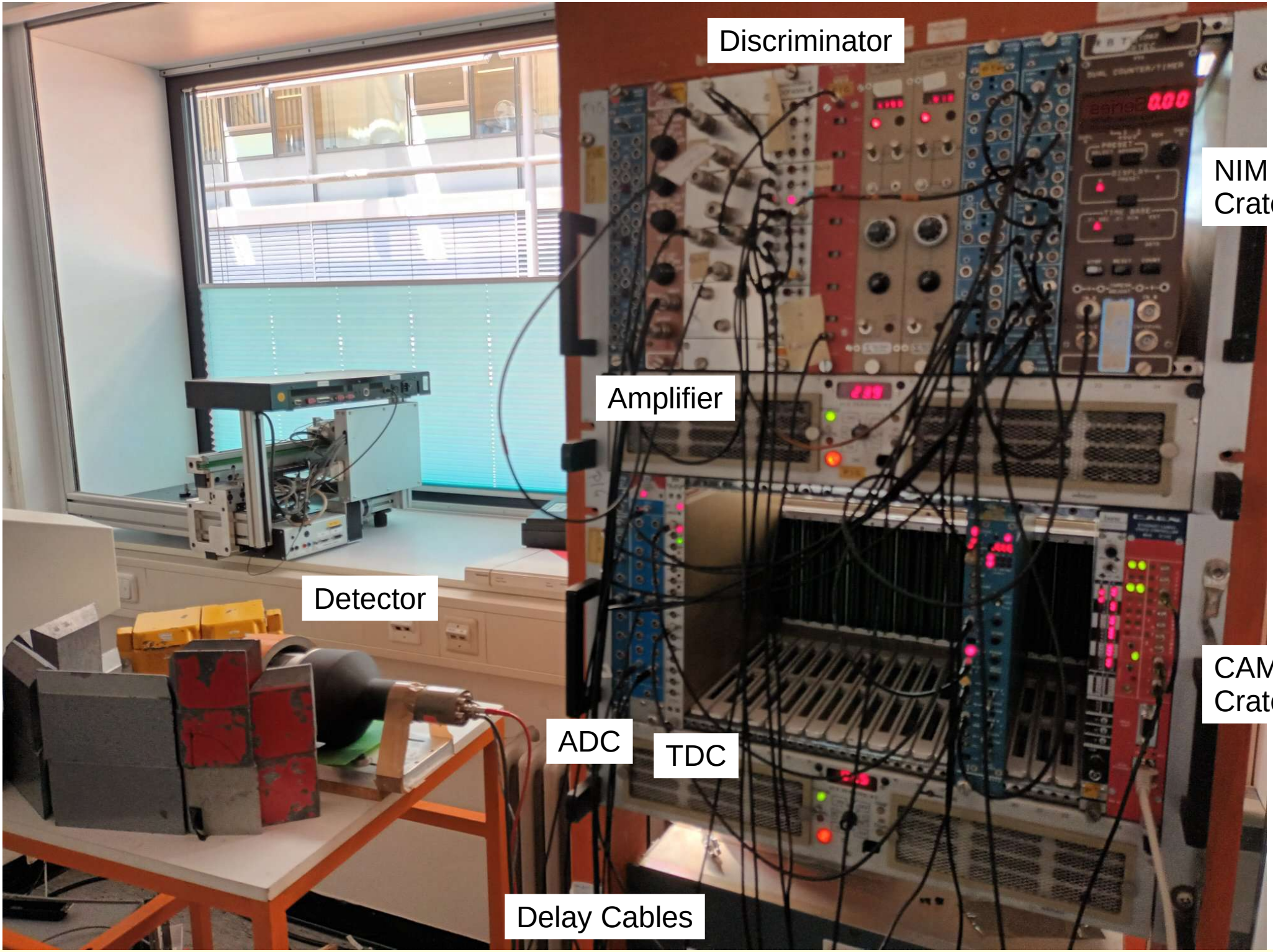
Delay line (DLL) TDC



Vernier TDC, 2 delay lines, start & stop with 2 different delays

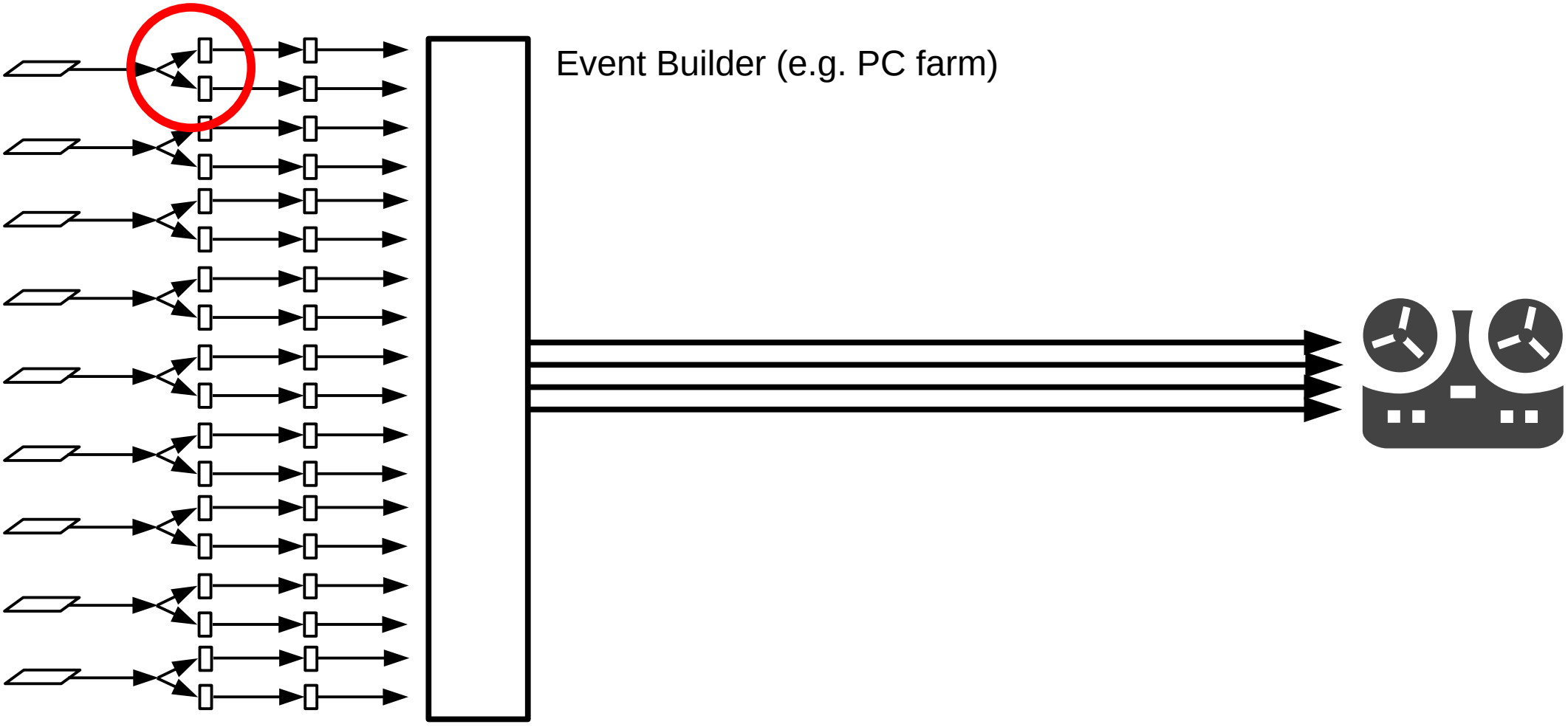
(Trick! Increases the time resolution)

C. Yao, Master Thesis TRITA-ICT-EX-2011:212, Stockholm, 2011


Discriminator
NIM Crate
Amplifier
Detector
CAMAC Crate
ADC
TDC
Delay Cables

DAQ for many detectors

Build a frontend board



Build your own frontend circuit

- Let's say, we need a circuit
  with an amplifier and/or ADC, or discriminator and/or TDC
- Let's say, it is a big experiment (many detectors)
- Possible approaches

1. PCB
   (Printed Circuit Board)
2. FPGA
   (Field Programmable Gate Array)
3. ASIC
   (Application Specific Integrated Circuit)

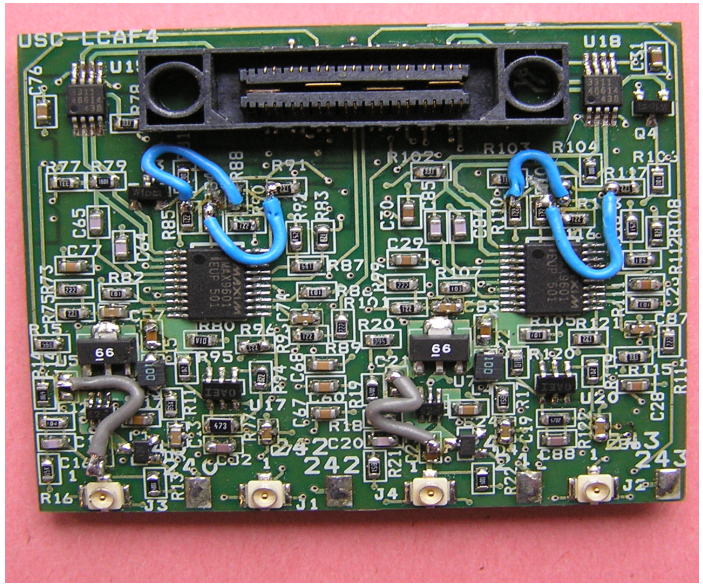
1. PCB

- Components soldered on a board
  (e.g. resistors, capacitors, transistors, small chips, ...)
- Design and production has 7 steps
- See example (HADES RPC)

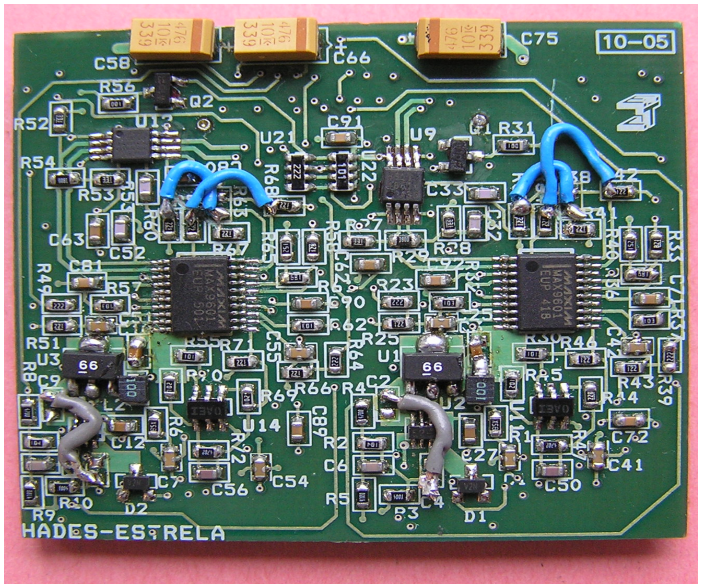
HADES RPC Frontend Board

amplifiers & discriminators

4 channels



LEMO connectors
for cable from detector



2. FPGA

- Circuit on a chip, programmed
- (empty, non-programmed) FPGA purchased from a company
  e.g. XILINX*, ALTERA**, LATTICE
  (taken over by *AMD, **intel)
- programming is in a special, logic-based language
  e.g. VHDL, VERILOG
- once programmed, can be changed again!

xilinx.com

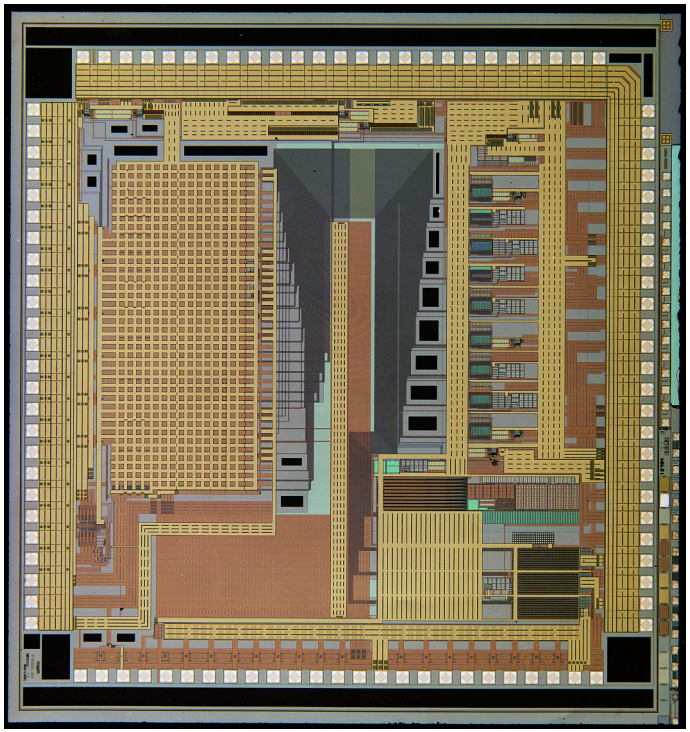
intel.com

latticesemi.com

3. ASIC

- Circuit on a chip,

  designed by electronics expert
  (member of the collaboration),
  then submitted to a company
  (TSMC, IBM)
- Nowadays down to 65 nm silicon process,
  more radiation tolerant
  (digital part needs less area)
- Fabrication in 2 steps:
  - prototype run, a few ASICs for testing
  - then mass production
- Price 50.000+ Euros
- Once produced, cannot be changed anymore



FRICO ASIC (Fermilab)

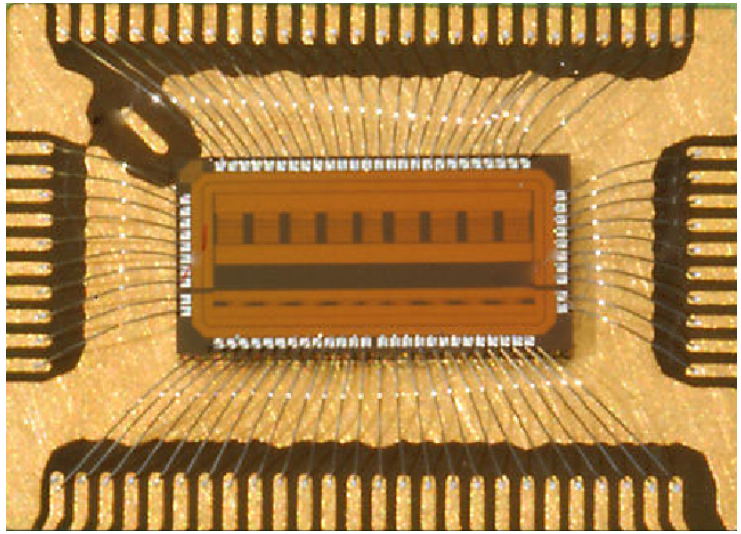
Supernova/Acceleration Probe
(SNAP) space telescope

https://ppd.fnal.gov/eed/asic/ASIC_images.html

ASIC examples

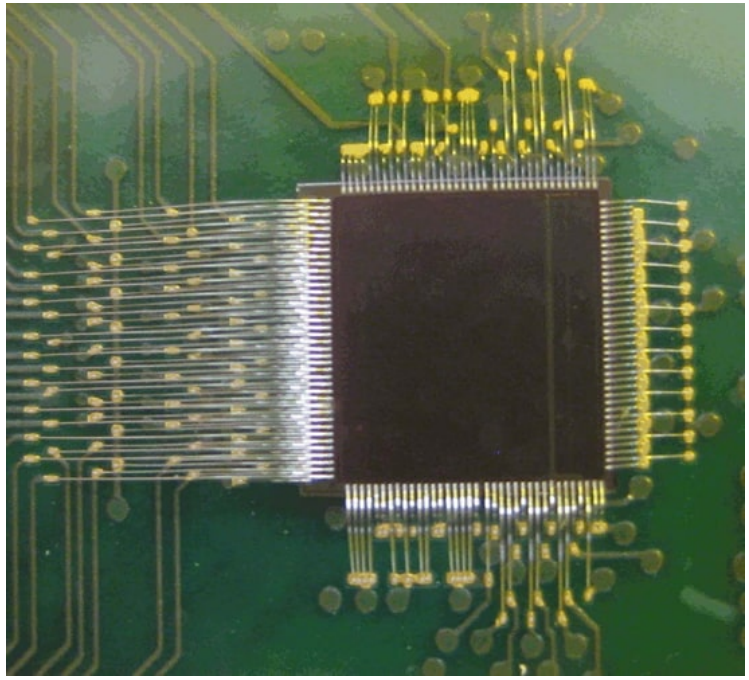
- NINO ASIC (e.g. ALICE)
  250 nm CMOS process
  4-stage amplifier, factor 30
  discriminator 20 ps resolution
  8 channels
- TOFPET ASIC (e.g. Eurizon Cherenkov)
  130 nm CMOS process
  TDC, 50 ps resolution
  64 channels
- DCD (e.g. Belle II PXD)
  UMC 180 nm technology
  ADC 8-bit
  256 channels
  (continuous data stream 2.56 GBytes/s,
  needs special DAQ, see next lecture)

2 x 4 mm



Nucl. Instr. Meth. A 533 (2004) 183

2.5 x 2.5 mm



www.petsyselectronics.com