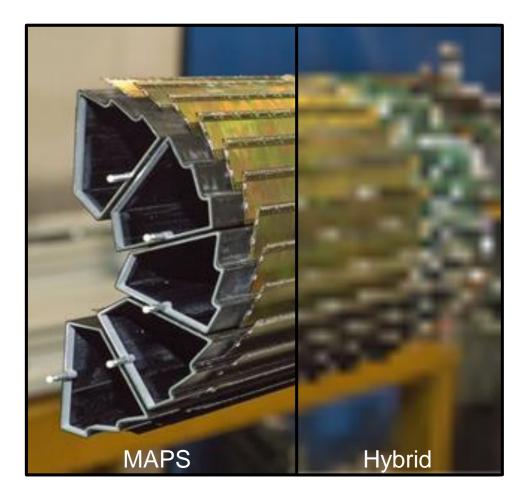


# Silicon detectors IV

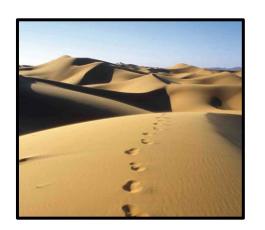
The rising of MAPS

M. Deveaux, GSI

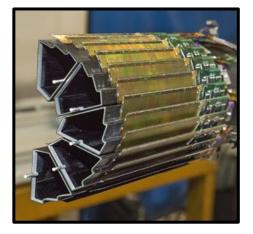


## **Outline**





+ ? =



1) Things you should know on silicon device production

2) CMOS Monolithic Active Pixel Sensors (MAPS)

Why MAPS are cool.

How not to collide the moon.

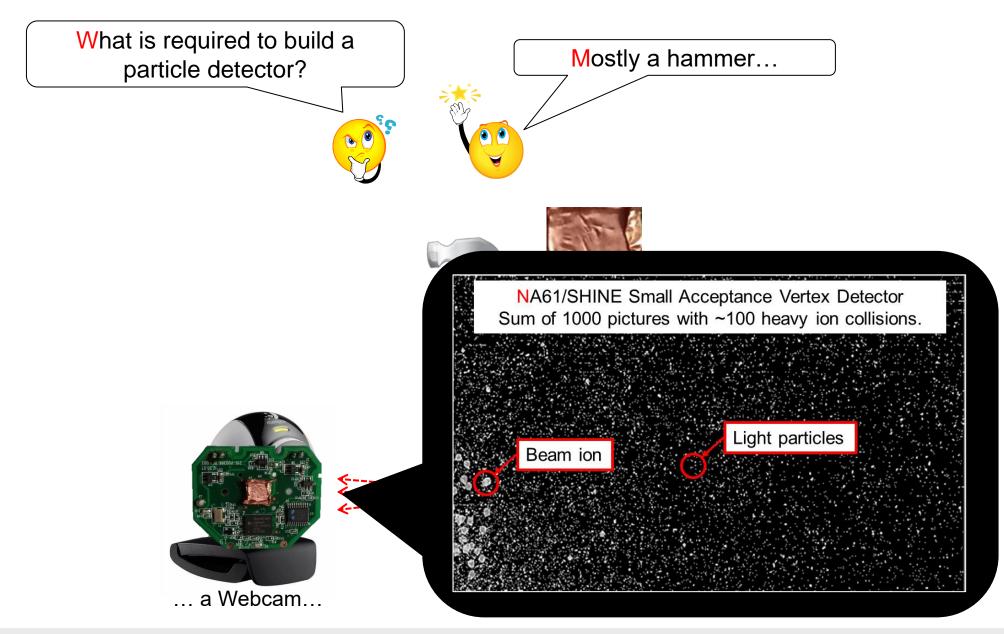
The struggle for radiation tolerance.

One chip is not enough.

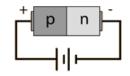


## Reminder





# **Some equations**

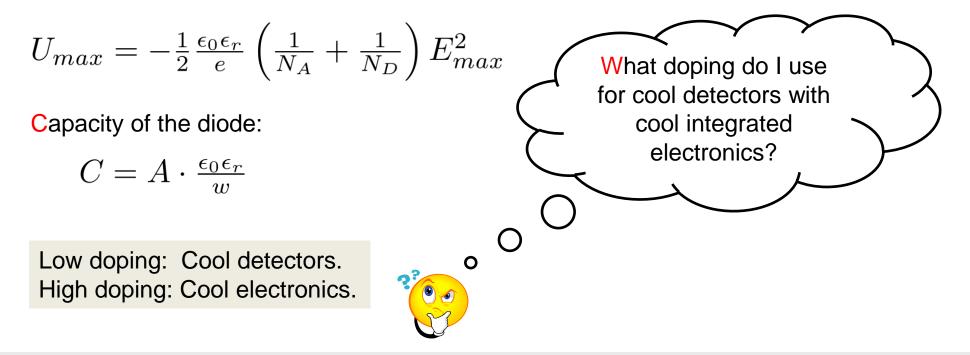




Width of the depleted zone:

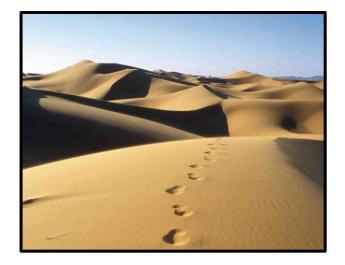
$$w = \sqrt{\frac{2\epsilon_0\epsilon_r}{e} \left(\frac{1}{N_A} + \frac{1}{N_D}\right) U_{ext}}$$

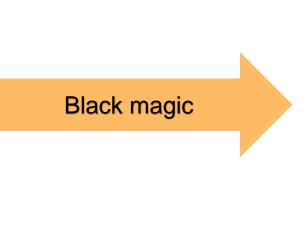
Break down voltage:



## How to build silicon devices: Wafers



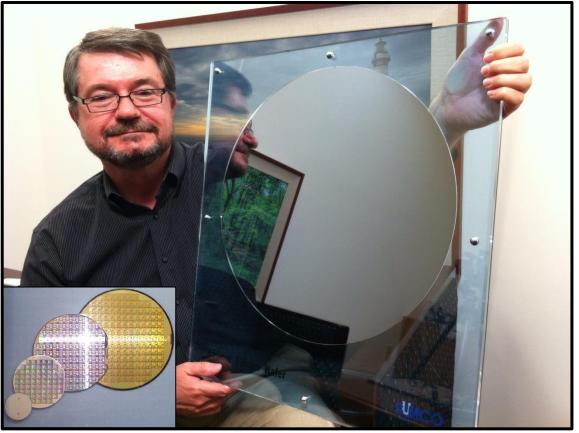




Silicon is melted into high purity mono-crystals.

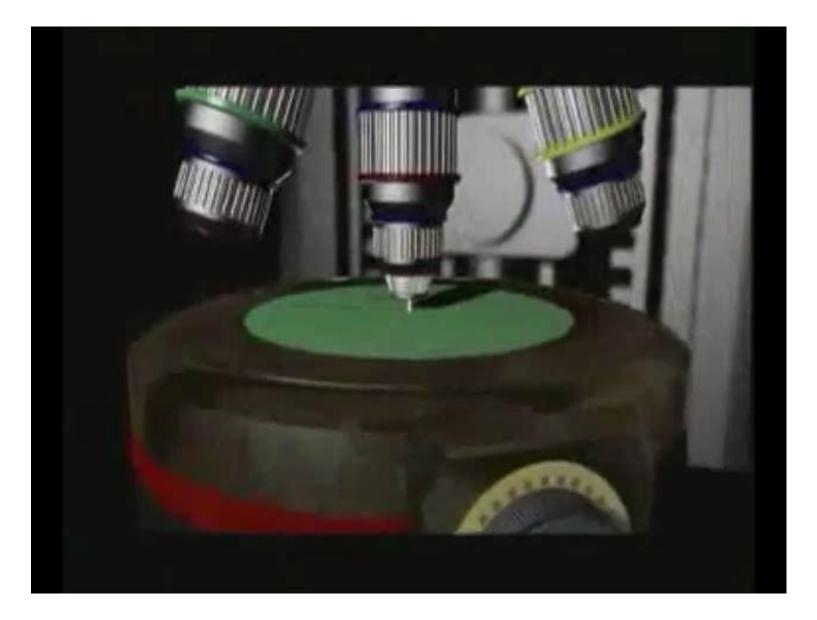
- Purity = cost
- Remaining inpurities are controlled by doping.
- $\Rightarrow$  All wafers are doped.
- $\Rightarrow$  Low doing wafers are expensive.
- $\Rightarrow$  Expensive stuff is rare industry (thus you don't get what you want).

Wafers exist in very different sizes, size matters.



# **Epitaxial layer**





## Words you should know

Minimum feature size (e.g. TJ 180 nm):

- Size of smallest structure on my realize with a process (typically transistor gate)
- Relevant sizes:
  - 5 nm (~50 atom layers) for modern digital electronics (e.g. smart phones).
  - 180 250 nm (detector electronics in production)
  - 28 65 nm (detector electronics under preparation)  $\int$

Reticle size: Biggest structure one can build with one lithography mask, typically ~3 x 2 cm<sup>2</sup>.

Stitching: Build > reticle size devices by using repetitive structures

CU

2

В В В В В В В Α С D D D D D D D Masks С D D D D D D D В CU **Stepping magic** С D D D D D D D S D D D D D D D 2 cm 8 cm

Analog/radiation hard electronics: A bit bigger is often better.

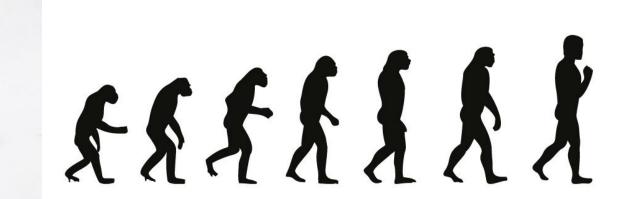
Final device







Geiger-counter (1932)





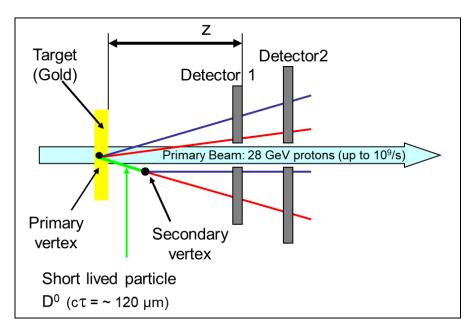
MAPS (nowadays)



Works for "stable" particles reaching the detectors.

What about less stable particles?

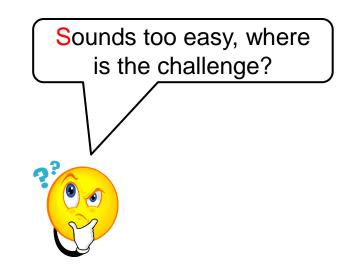
Open strange:  $c\tau \approx 10$  mm, Open bottom:  $c\tau \approx 1$  mm, Open Charm:  $c\tau \approx 0.1$  mm



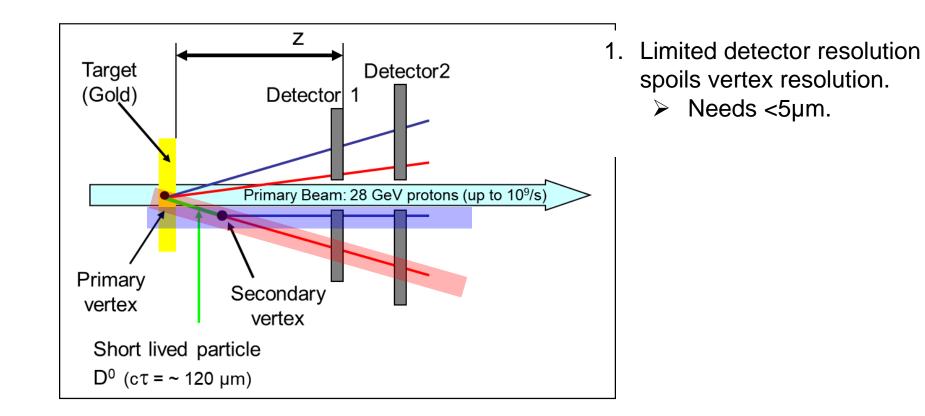
Prove existence of short lived particle by separating primary and secondary vertex.

Compute its properties by:

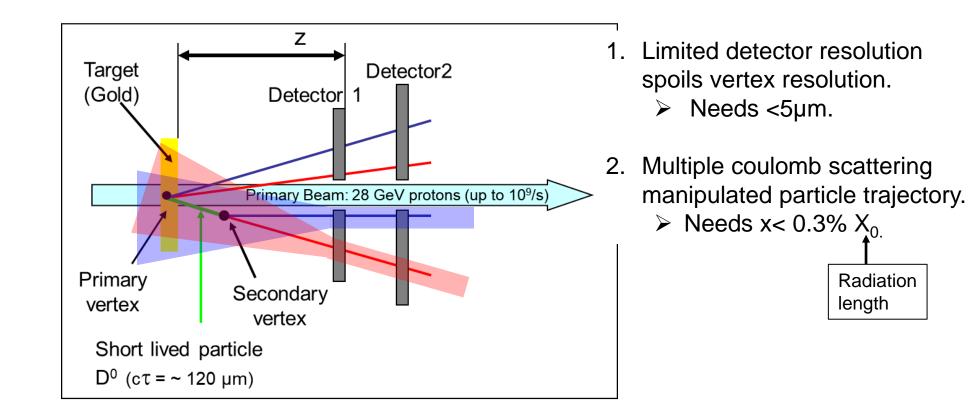
- Adding 4-vectors of daugters (invariant mass).
- "Add" quark content of daughters.



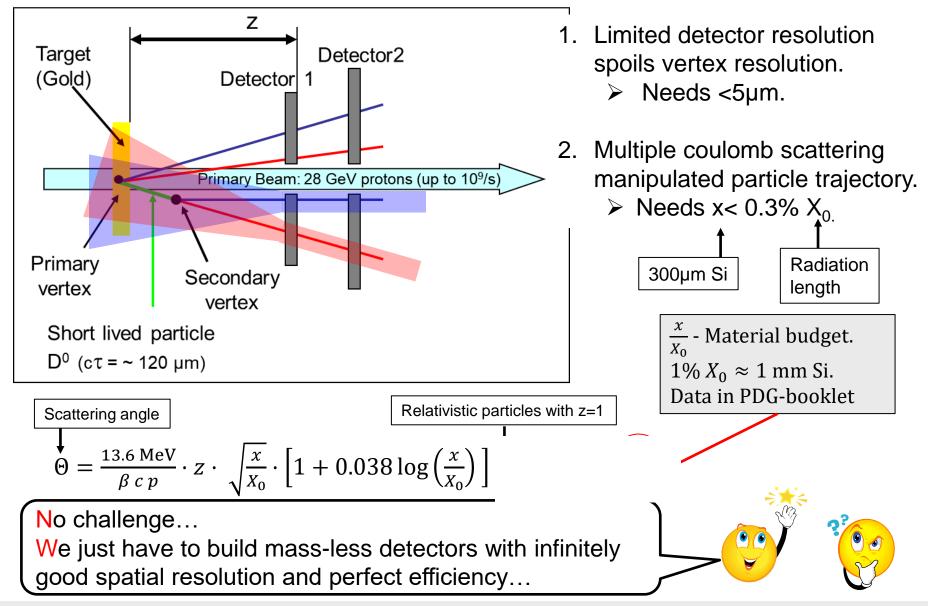






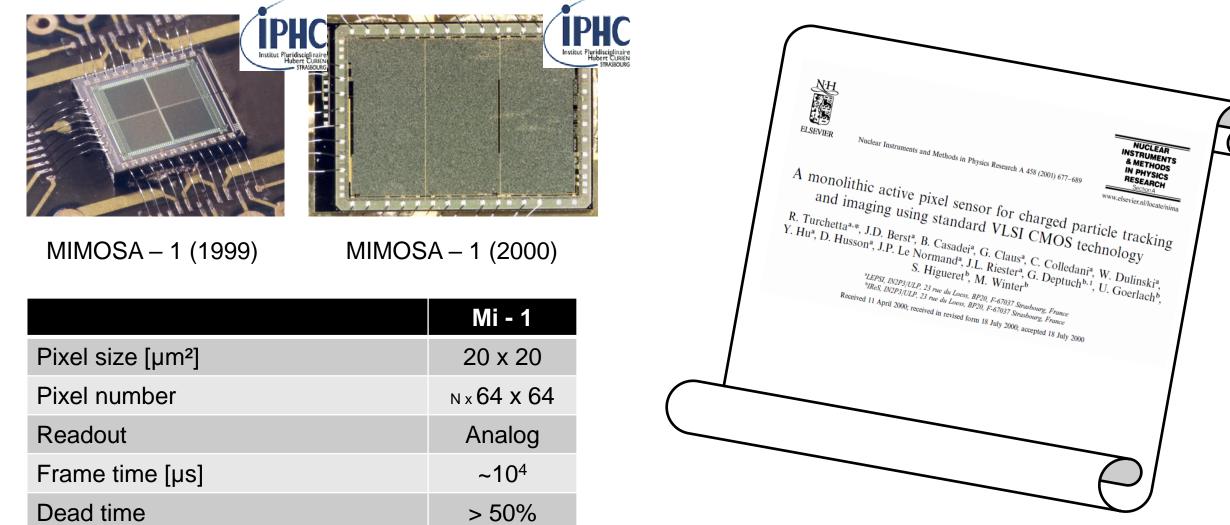






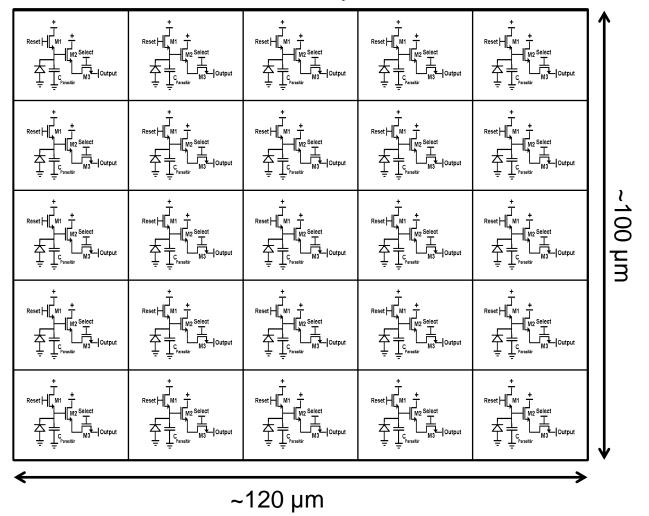
## MAPS – the beginning

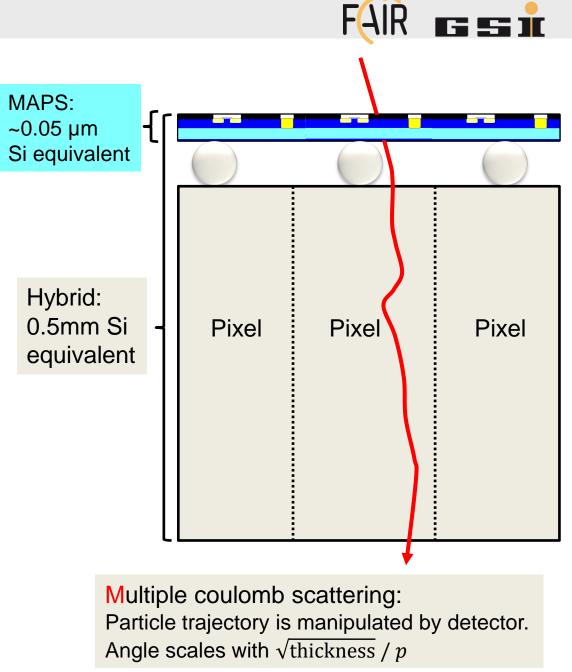




MAPS vs. Hybrid pixels

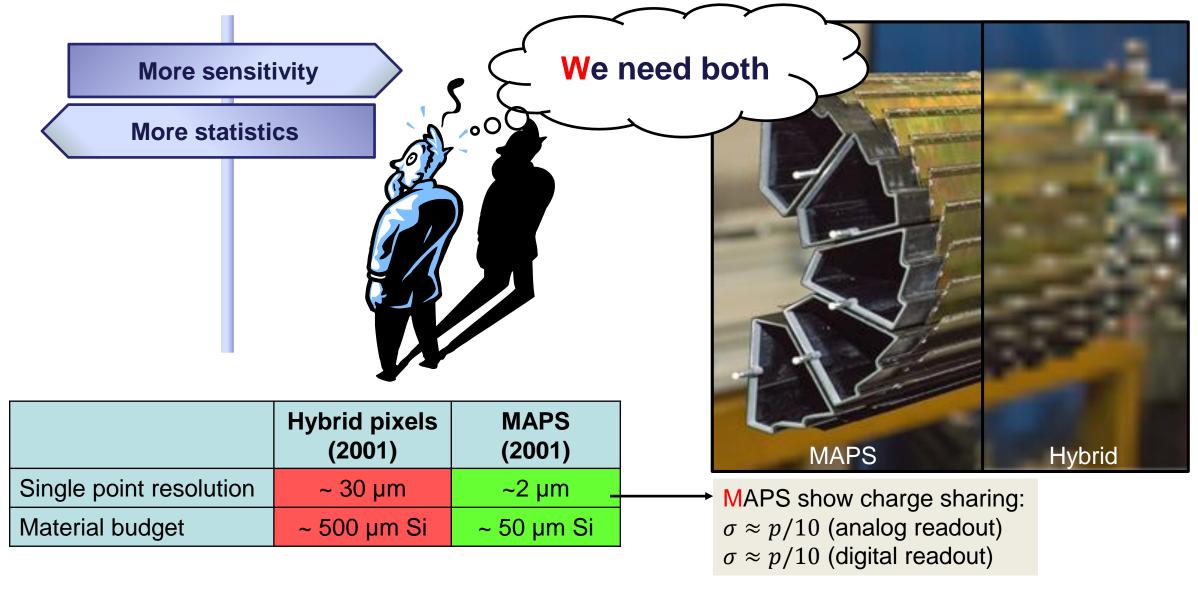
CMS @ LHC – Hybrid Pixel





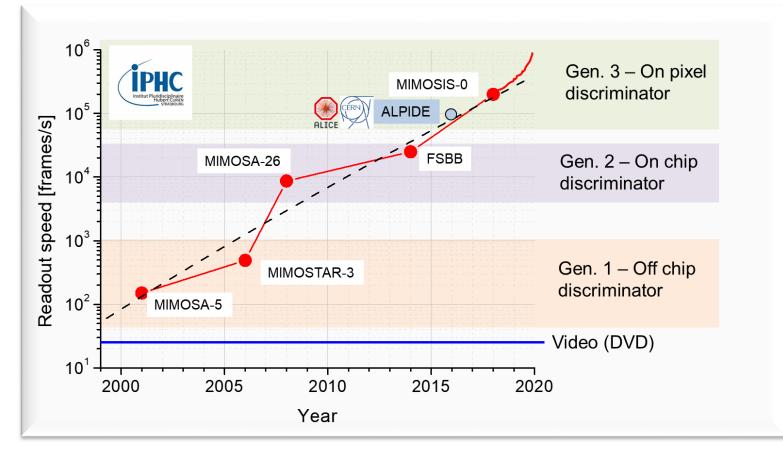
## **MAPS** – the hope and limitations

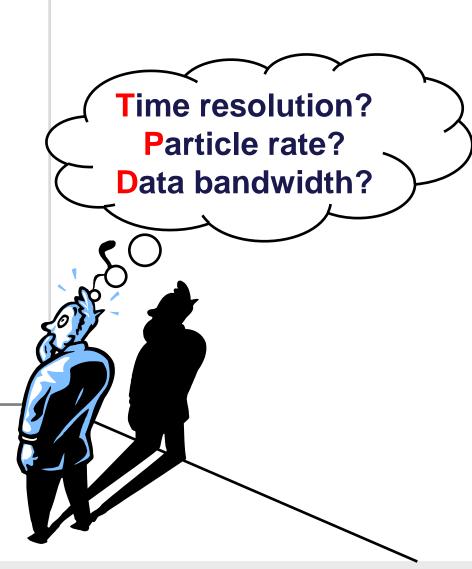




## The need for speed

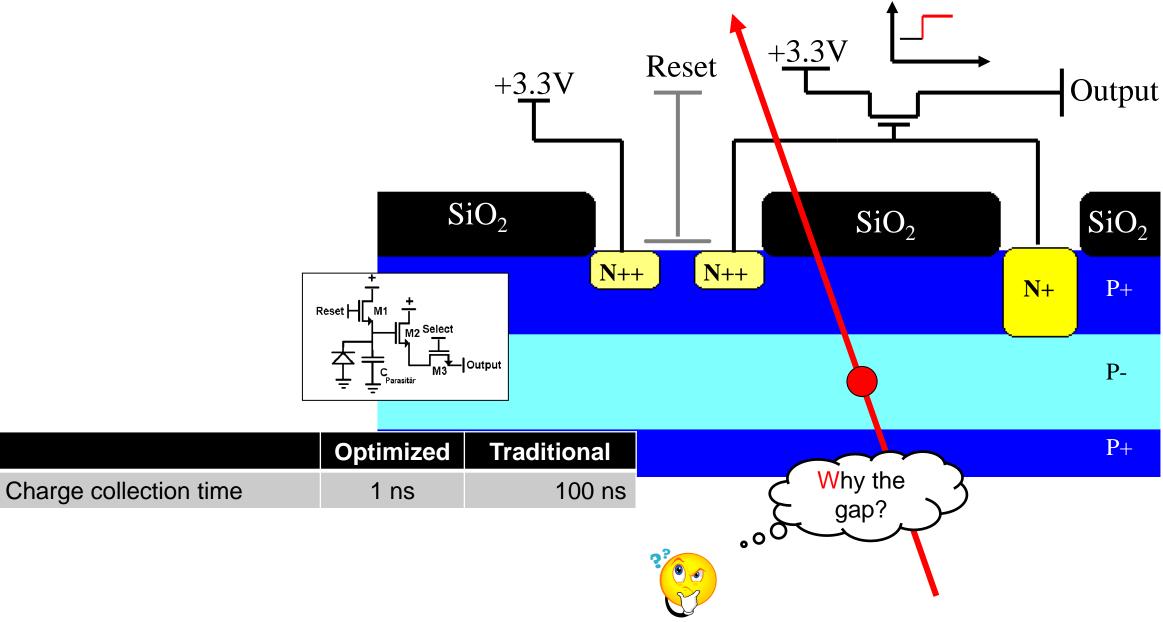






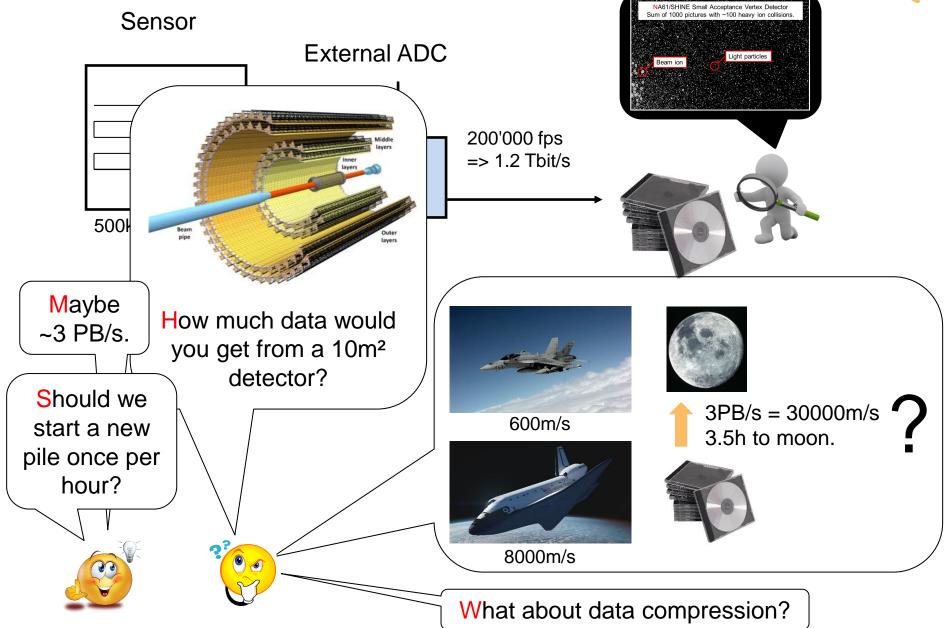
## **Speed of MAPS: Limiting factors**





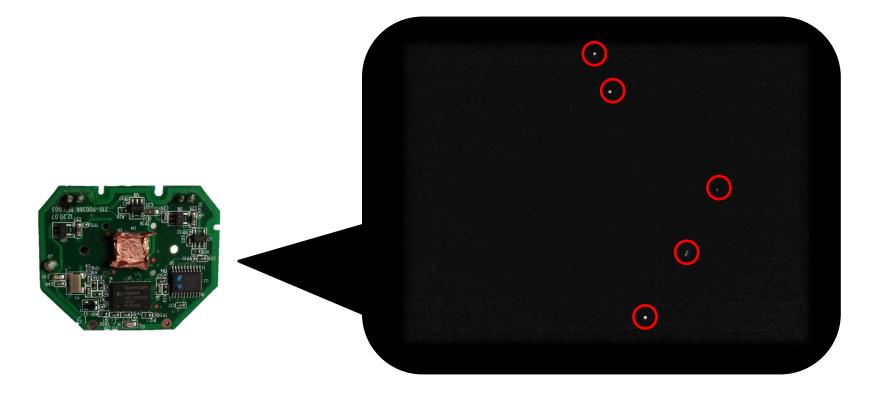
#### Block diagram of Gen. 1 MAPS





#### How do to data compression



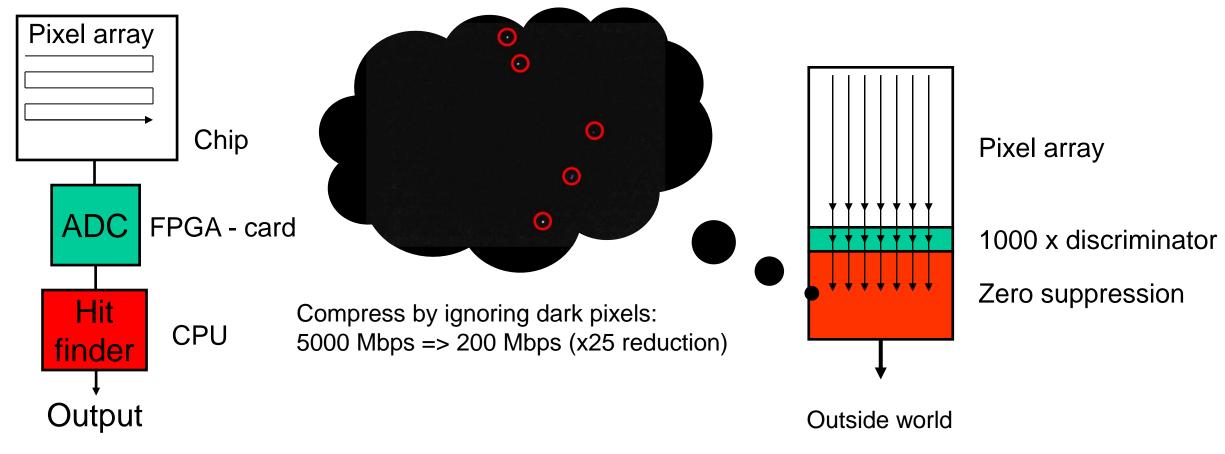


Most pixels in the frame (>99.5%) show black. Only few pixels show white.

Idea: Ignore all black pixels.

## How to readout the pixels?



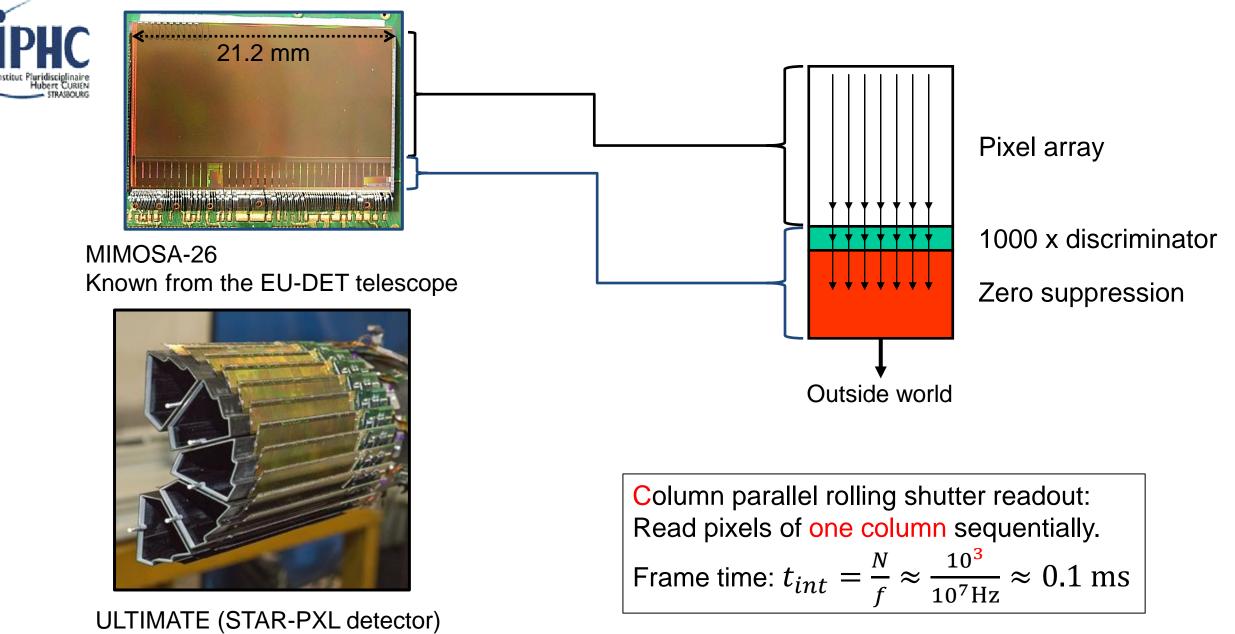


Rolling shutter readout:  
Read pixels sequentially.  
Frame time: 
$$t_{int} = \frac{N}{f} \approx \frac{10^5}{10^7 \text{Hz}} \approx 10 \text{ ms}$$

Column parallel rolling shutter readout: Read pixels of one column sequentially. Frame time:  $t_{int} = \frac{N}{f} \approx \frac{10^3}{10^7 \text{Hz}} \approx 0.1 \text{ ms}$ 

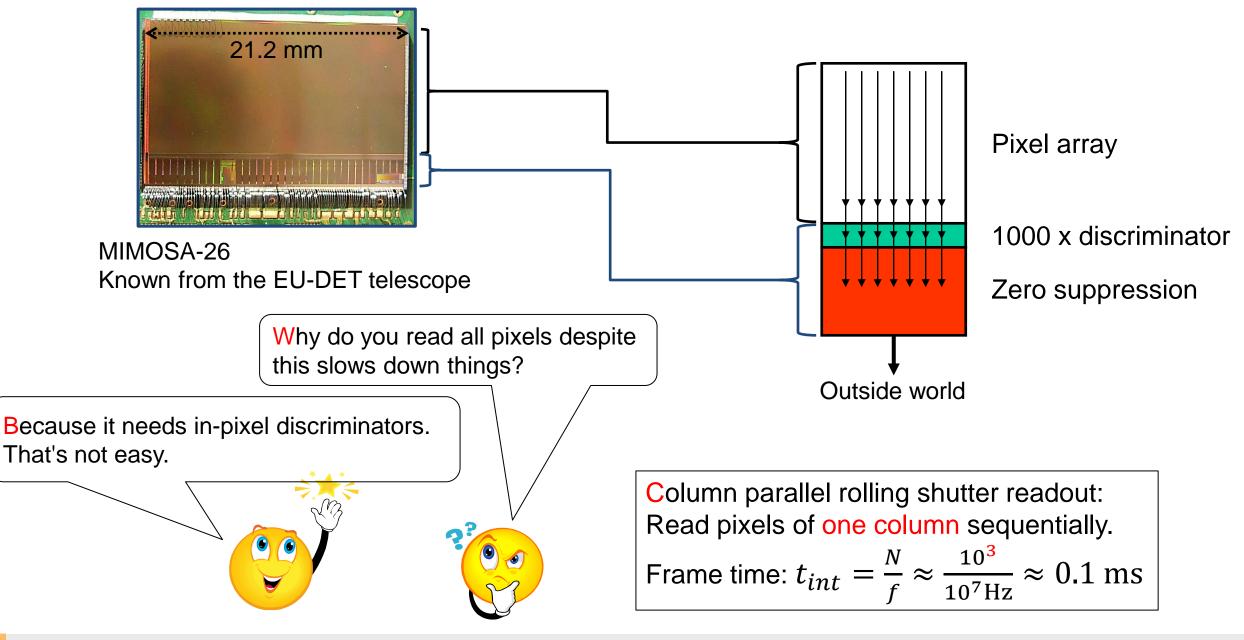
## **Generation 2 Sensors**

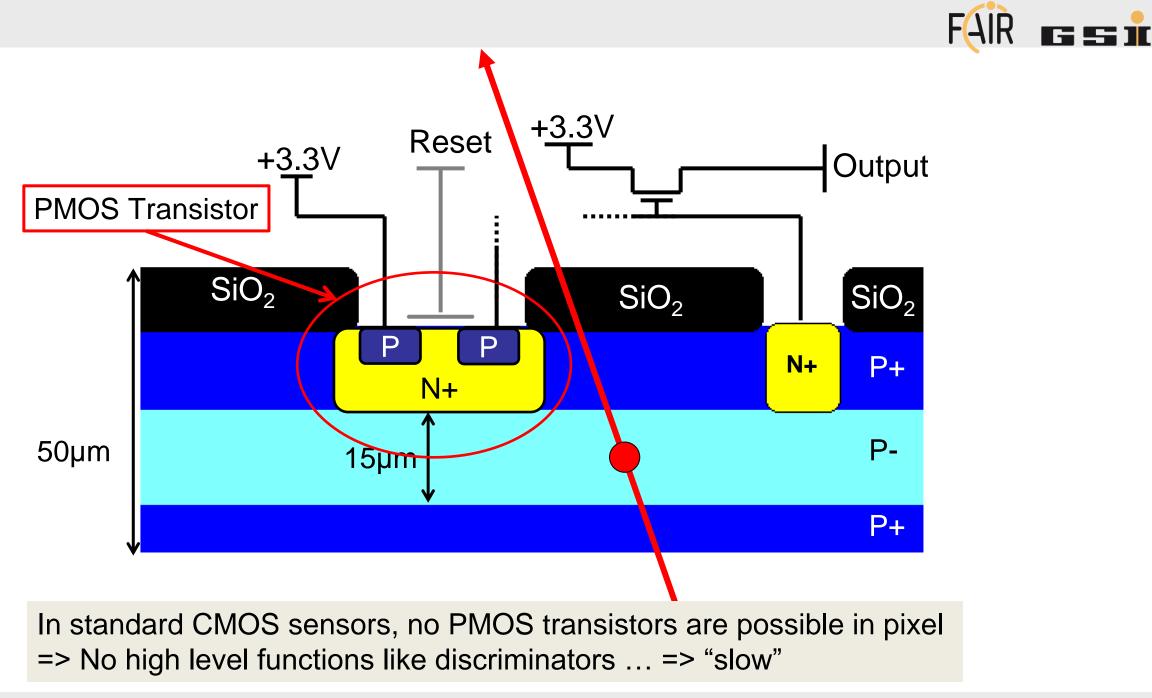




### **Generation 2 sensors**

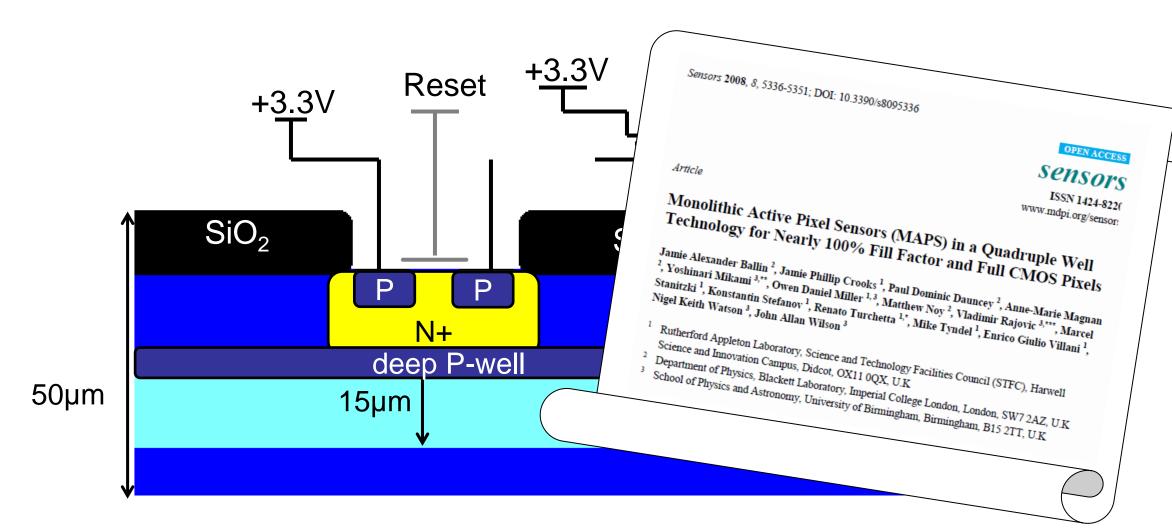






## **Quad – Well process**

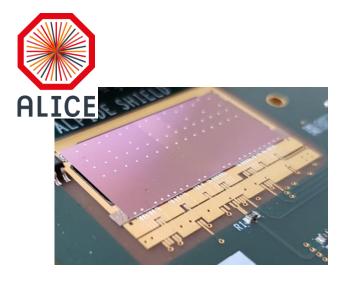




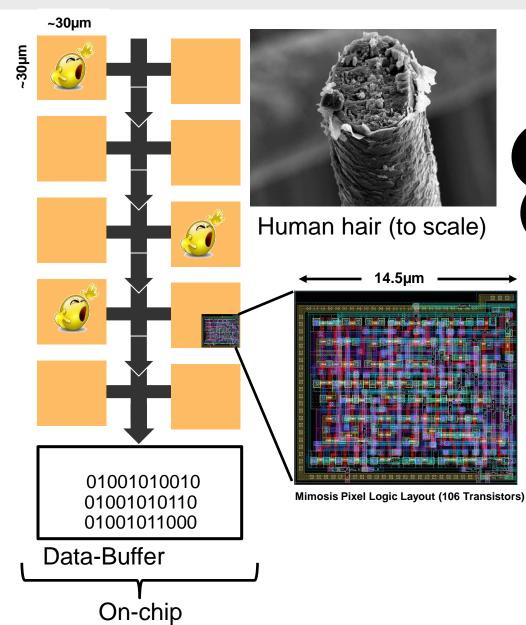
Progress was reached with Quad-well CMOS as provided by the manufacturer TowerJazz (180 nm).

## How to get the data out?





ALPIDE Sensor. ~ 50 mW/cm<sup>2</sup>





Off-chip



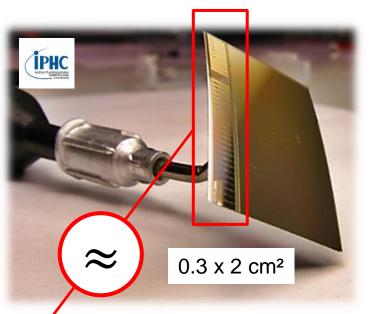
#### Side band contains:

• Data buffers.

. . .

- Voltage regulators, trim DACs.
- Slow control interface.
- Temperature sensors.

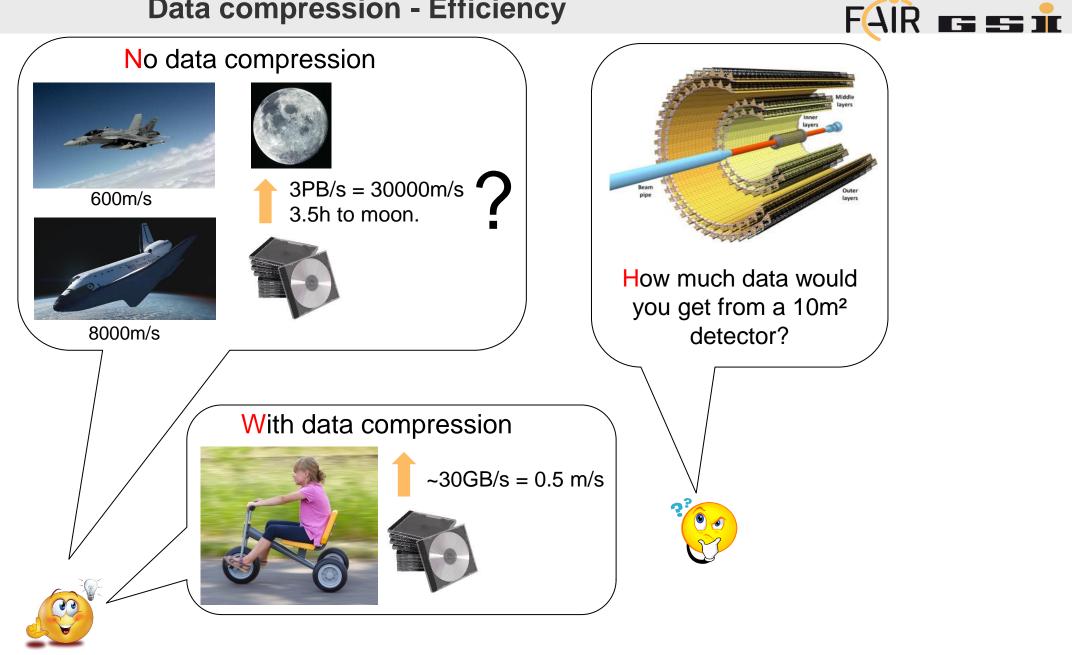




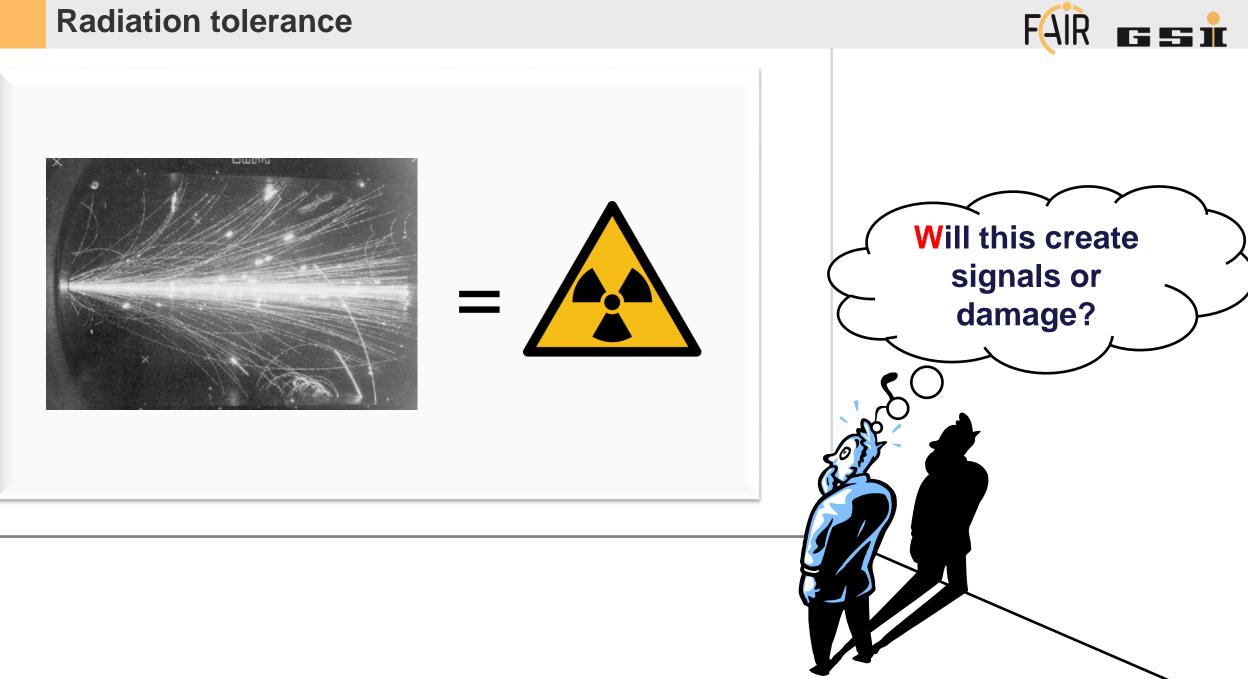
#### CMOS technology integrates:

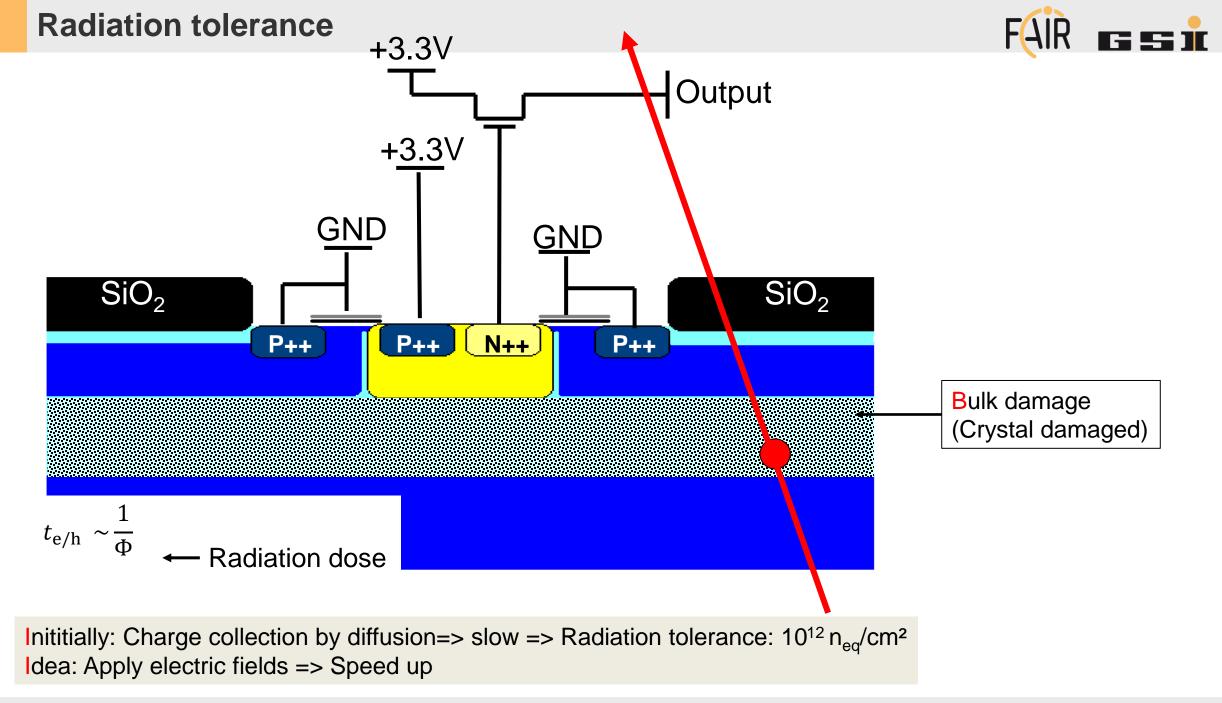
- Sensors.
- Analog electronics.
- Digital data processing.

#### **Data compression - Efficiency**









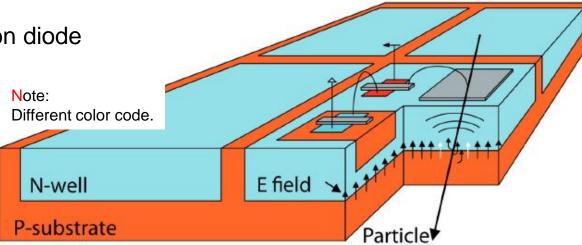


 $\left|\frac{2 \varepsilon_{s} \left(U_{bi} - \boldsymbol{U}\right)}{e N}\right|$ 

Idea:

Use "High Voltage" CMOS Process. Embed all electronics into the collection diode  $\Rightarrow$  Allows for fast readout.

 $\Rightarrow$  Allows to apply >50 V.



W =

I.Peric, P. Fischer et al., NIM A 582 (2007) 87

#### Pro:

- Worked with HV triple well process (best option at the time).
- Very fast time resolution (<10 ns) for individual hits.
- Very radiation hard due to big diodes and high voltage.

#### Limits:

- Rather sizeable pixels (e.g. 80x80µm<sup>2</sup>).
- High capacitive noise.
- Relatively high power consumption.

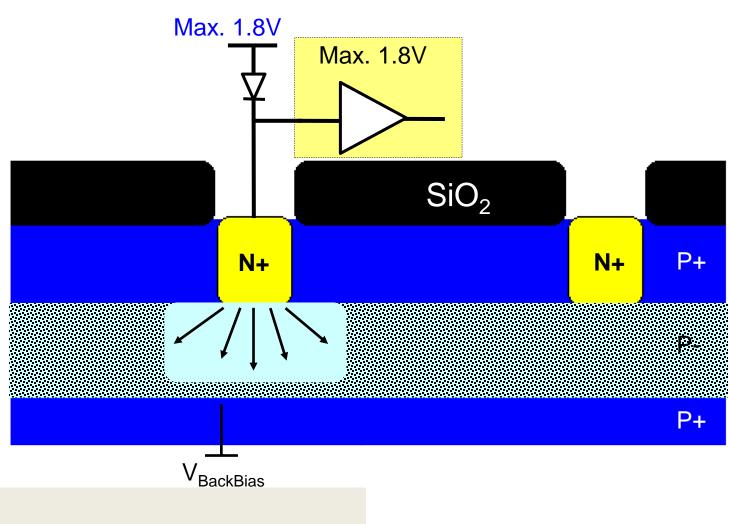


Flat diodes:

$$W = \sqrt{\frac{2 \varepsilon_s \left( U_{bi} - \boldsymbol{U} \right)}{e N_A}}$$

Point diodes:

$$W = \oint_{(?)} \sqrt{\frac{2 \varepsilon_s (U_{bi} - U)}{e N_A}}$$



Improvements

• Reduce doping, add back bias, e.g. ALPIDE (hard for >6V).

## **Radiation tolerance: D-MAPS**

FAIR E = i

Flat diodes:

$$W = \sqrt{\frac{2 \varepsilon_s \left( U_{bi} - \mathbf{U} \right)}{e N_A}}$$

Point diodes:

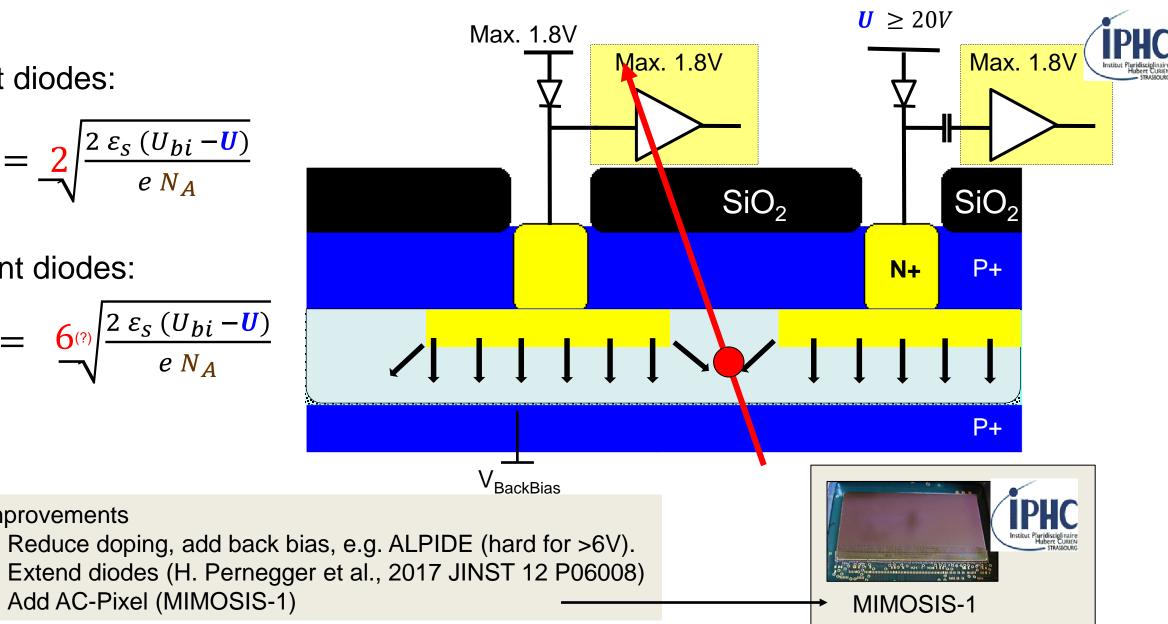
Improvements

•

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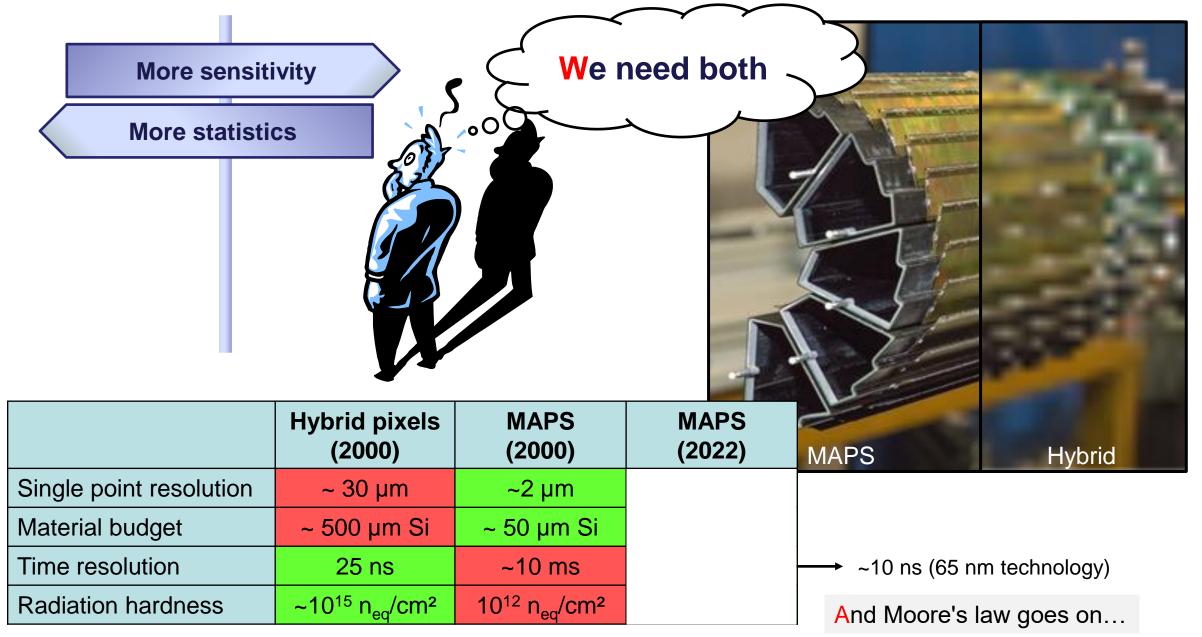
•

$$W = \oint_{\mathcal{O}} \sqrt{\frac{2 \varepsilon_s \left( U_{bi} - \mathbf{U} \right)}{e N_A}}$$

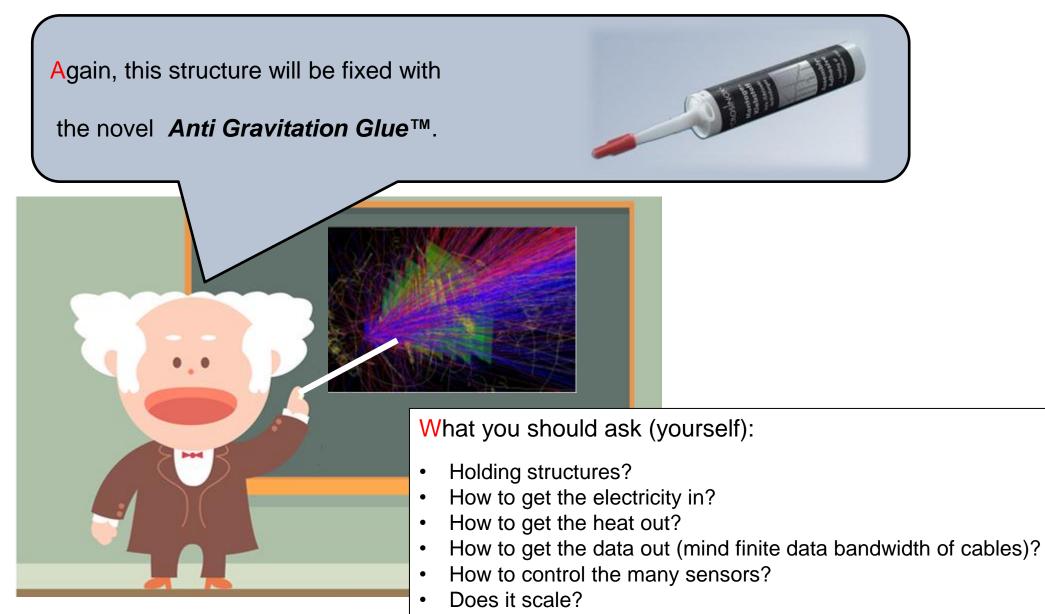


## **MAPS** – the hope and limitations





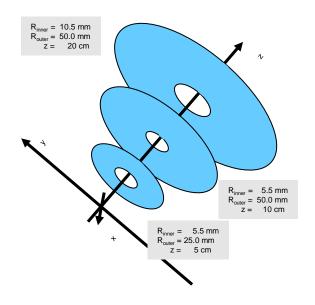


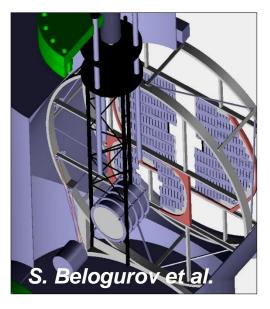


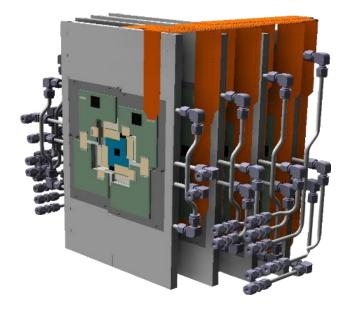
• Will it tolerate radiation (no standard ICs)?

## **Pictures of a detector project (CBM-MVD)**









2004

# 2007 (painting)

• Flying disks.

Fair GmbH | GSI GmbH D

- Technology unknown.
- No material estimate.
- Rough guess on technology.
- Rough guess on material.
- 2/4 stations missing.
- Simple digitizer model.

#### 2015

- Material gets realistic.
- Sensor models.
- 2 stations added to help tracking.

Used for many feasibility studies of CBM physics.

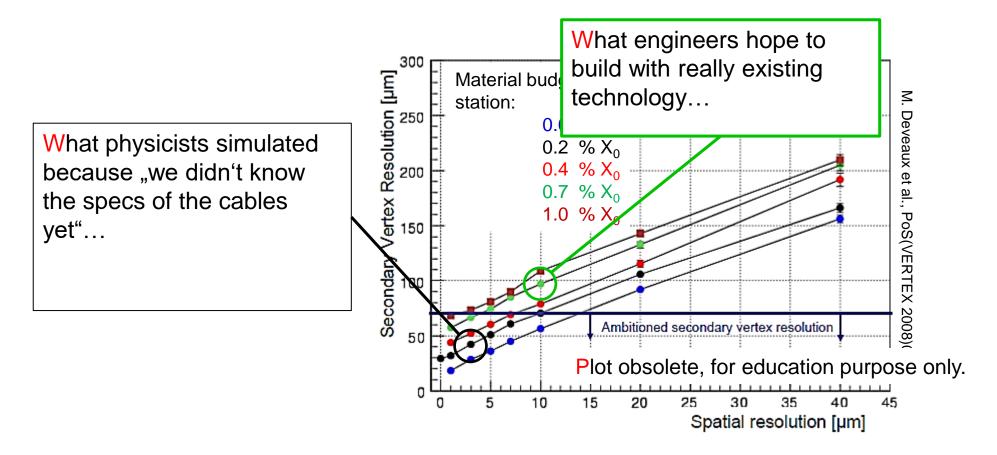
Inaccurate material may cause substantial uncertainties.

35

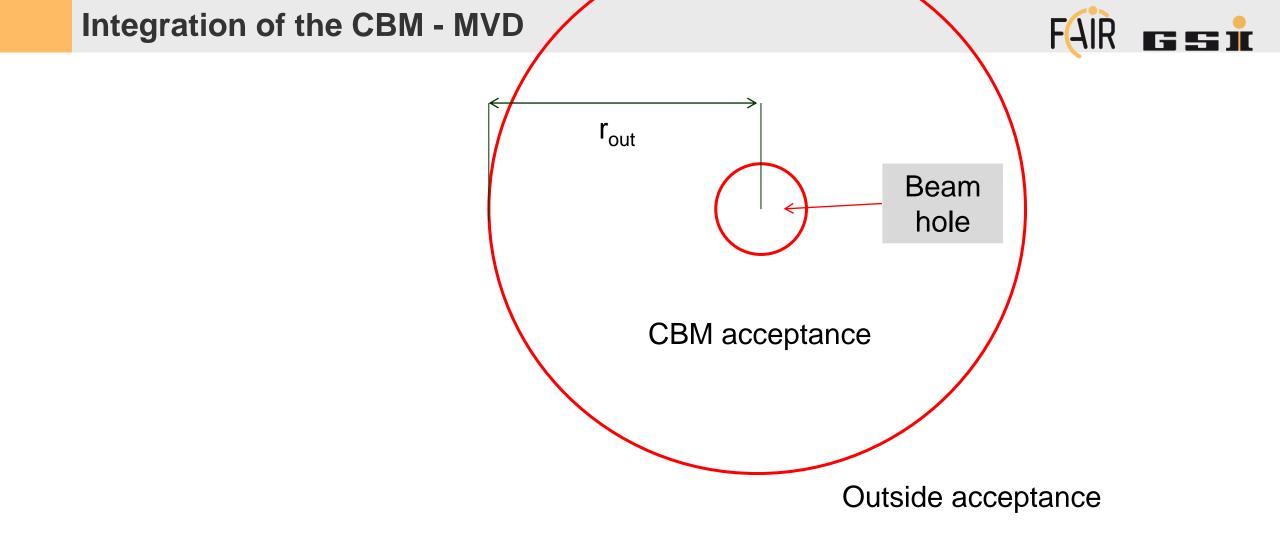
# Simulation vs. engineering

FAIR E S 1

CBM - MVD – secondary vertex resolution



Detector material budget is dominated by the infrastructure. Missing information turns often into too optimist physics simulations. Remain cautions, conservative: You see what you put.

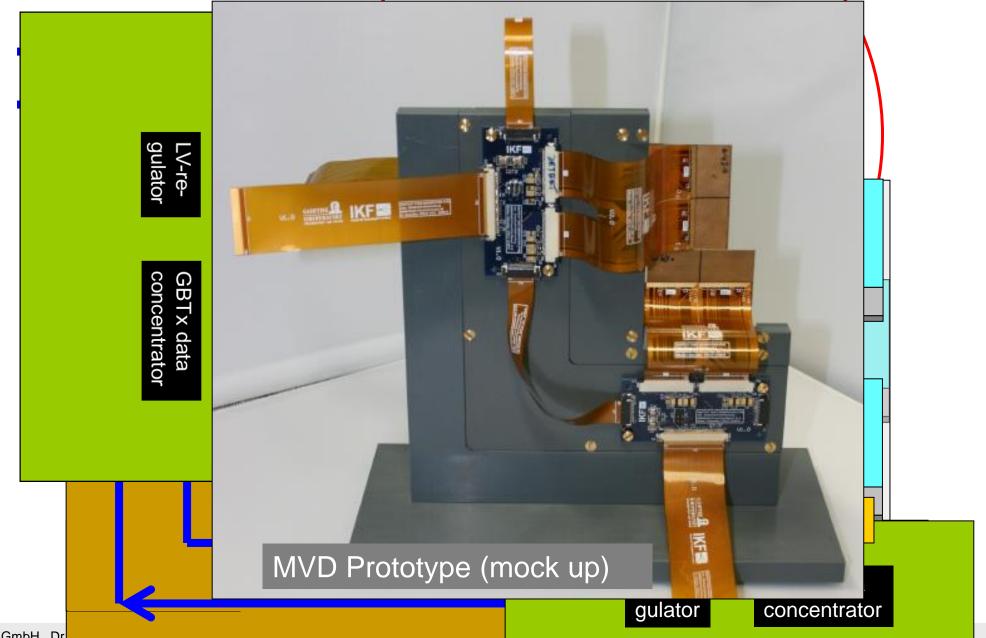


Vacuum operation requires actively cooled device.

- Use cooling support from diamond to move heat out of acceptance
- Put heat sink and FEE outside acceptance

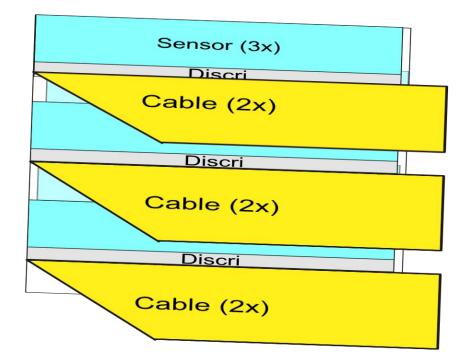
## Integration of the CBM - MVD





#### PRESTO:

Prototype of a quarter station incl. sensors (MIMOSA-26), cables, support etc.



Integration completed. Test:

- Vacuum compatibility
- Temperature cycling

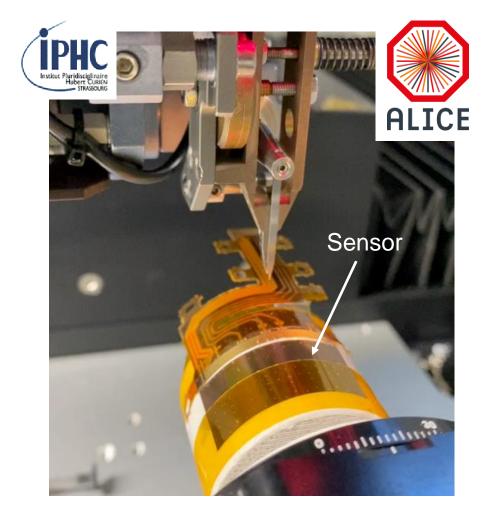
(More than) A spin-off: ≤ SQM2017, **Deveaux for NA61/SHINE** GOET UNIVER NA61/S. INE perspectives for Utrecht, open charm measurements Netherlands behalf of the NA61/SHINE co

FAIR

The NA61/SHINE vertex of detector uses (and tests) MVD prototype/PRESTO electronics

## **Outlook: The ALICE-ITS3 vision.**





ALICE ITS-3 program: Curved – Wafer detectors





CMOS Monolithic Active Pixel Sensors

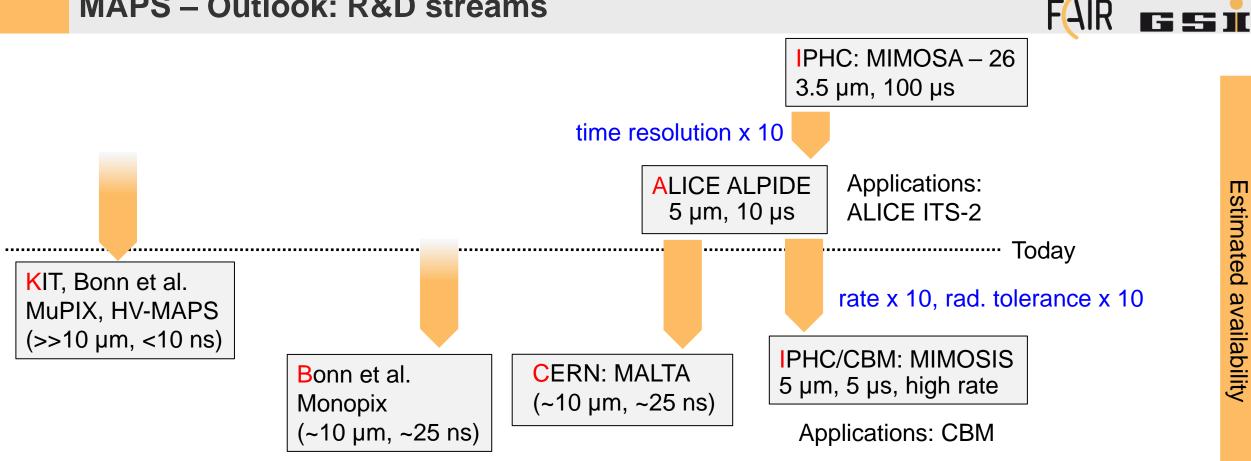
- Show lowest material budget together with highest granulartity.
- Integrate pixels and electronics on one system-on-a-chip.
- Can be mass produced with industrial CMOS processes at low cost.
- Are the coolest detectors ever made (my biased personal opinion).

When building detectors, consider that:

- the material budget and performance of detectors is determined by infrastructure.
  ⇒ Optimizing sensors wins the battle, optimizing cables and cooling wins the war.
- Being too optimist in simulations is mostly self-cheating.
  ⇒ Try to be conservative if you are missing detailed knowledge.

The performance of MAPS was improved by a factor 1000 during the past 20 years... ... and the story has just started.

## MAPS – Outlook: R&D streams



#### **Optimized: Time measurement**

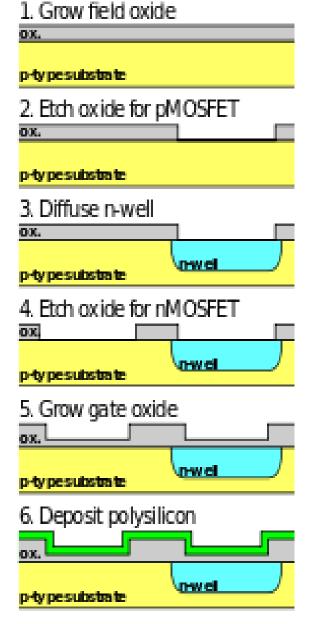
**Optimized: Position measurement** 

Toward new frontiers: Tower/Jazz 65 nm CIS technology (CERN, DESY, IPHC...) Estimated

availability

## Once again in slow...





<ol><li>Etch polysilicon and oxide</li></ol>
p-typesubstrate
8. Implant sources and drains
ox.
p-ty pesubstrate
9. Grow nitride
p-typesubstrate
10. Etch nitride
p-typesubstrate
11. Deposit metal
p-typesubstrate
12. Etchmetal
p-typesubstrate

CMOS production:

- Is highly complex (special companies needed).
- Works with lithography.
- Needs ~ 20 30 masks for modern processes.