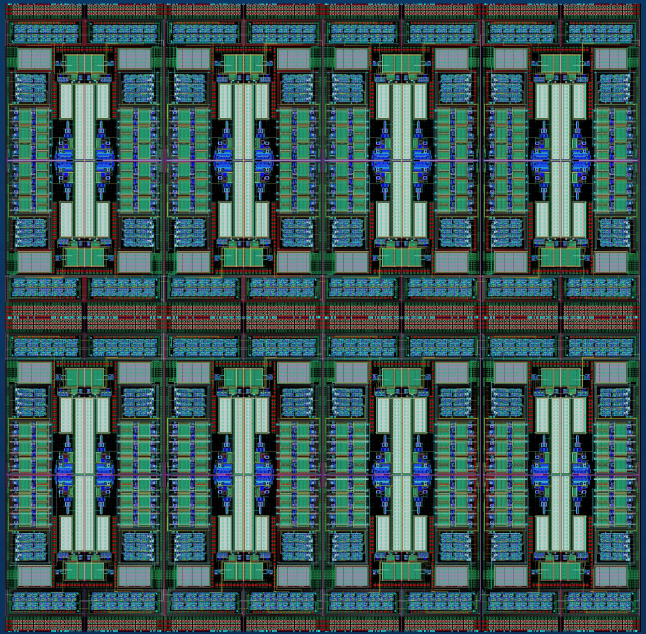
UNIVERSITÀ DEGLI STUDI DI BERGAMO | Dipartimento di Ingegneria e Scienze Applicate

INFN Istituto Nazionale di Fisica Nucleare

Front-end channels in 28 nm CMOS for future high energy physics detectors

EURIZON 2023 - Students presentation session



Layout detail of the prototype pixels matrix

Andrea Galliani

July 27th, 2023

Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

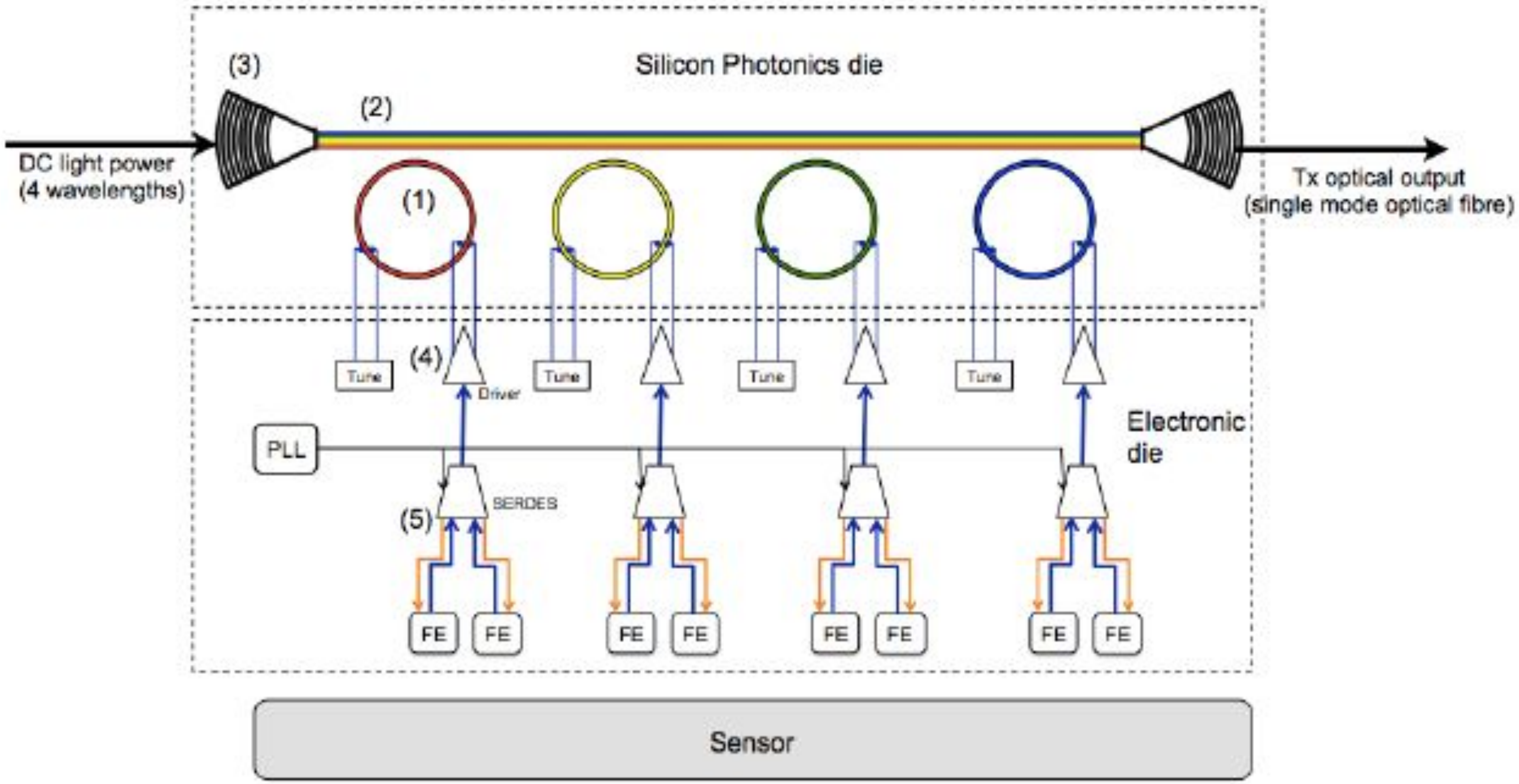
Falaphel

Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

Falaphel

Main goals:

- Deepen the 28nm CMOS technology
- Data rate > 100 Gb/s
- Radiation TID > 1 Grad (10 MGy)
- Total Fluence > 5 x 10^{16}n/cm^2
- **design and fabrication of a demonstrator by the end of 2024**

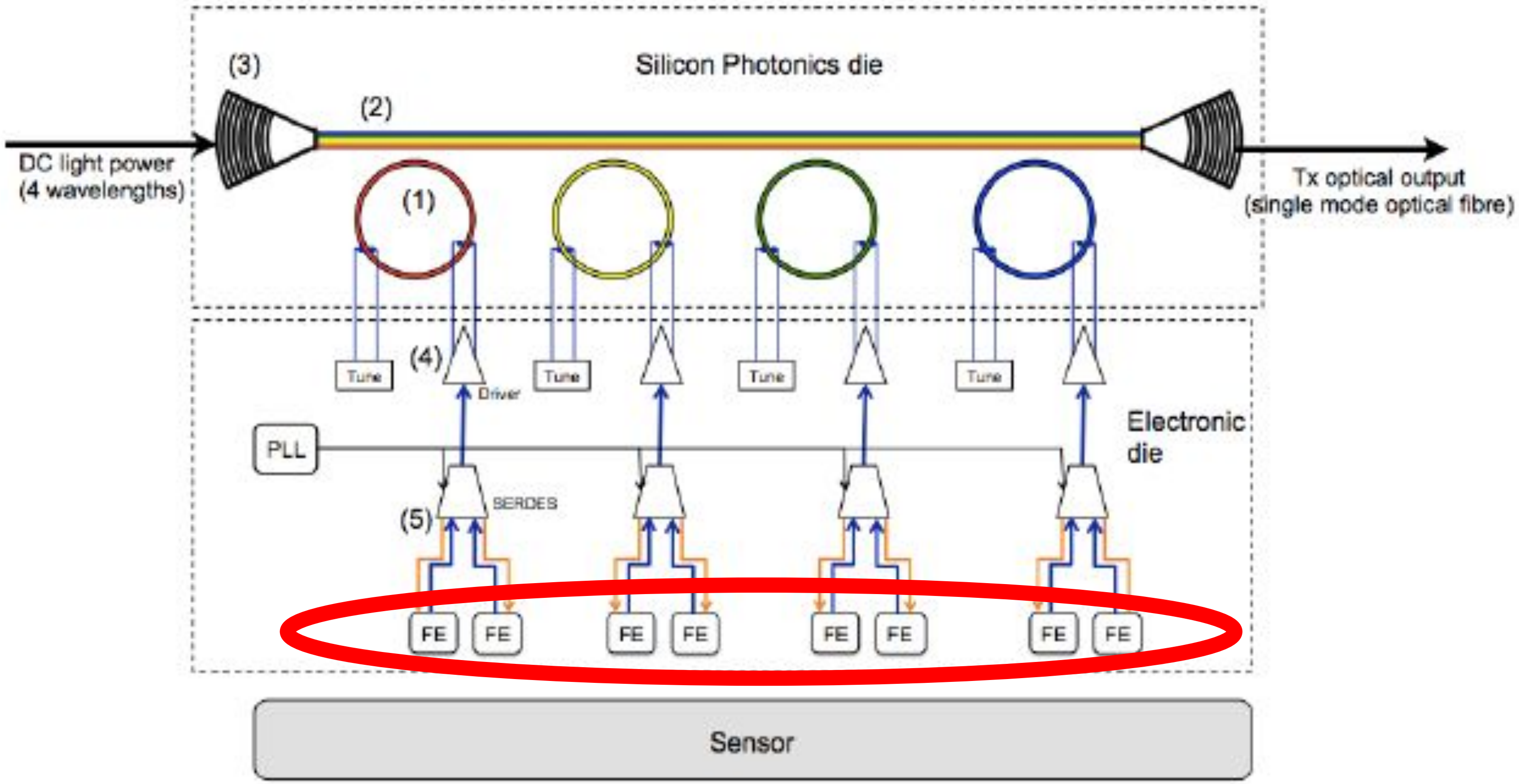


Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

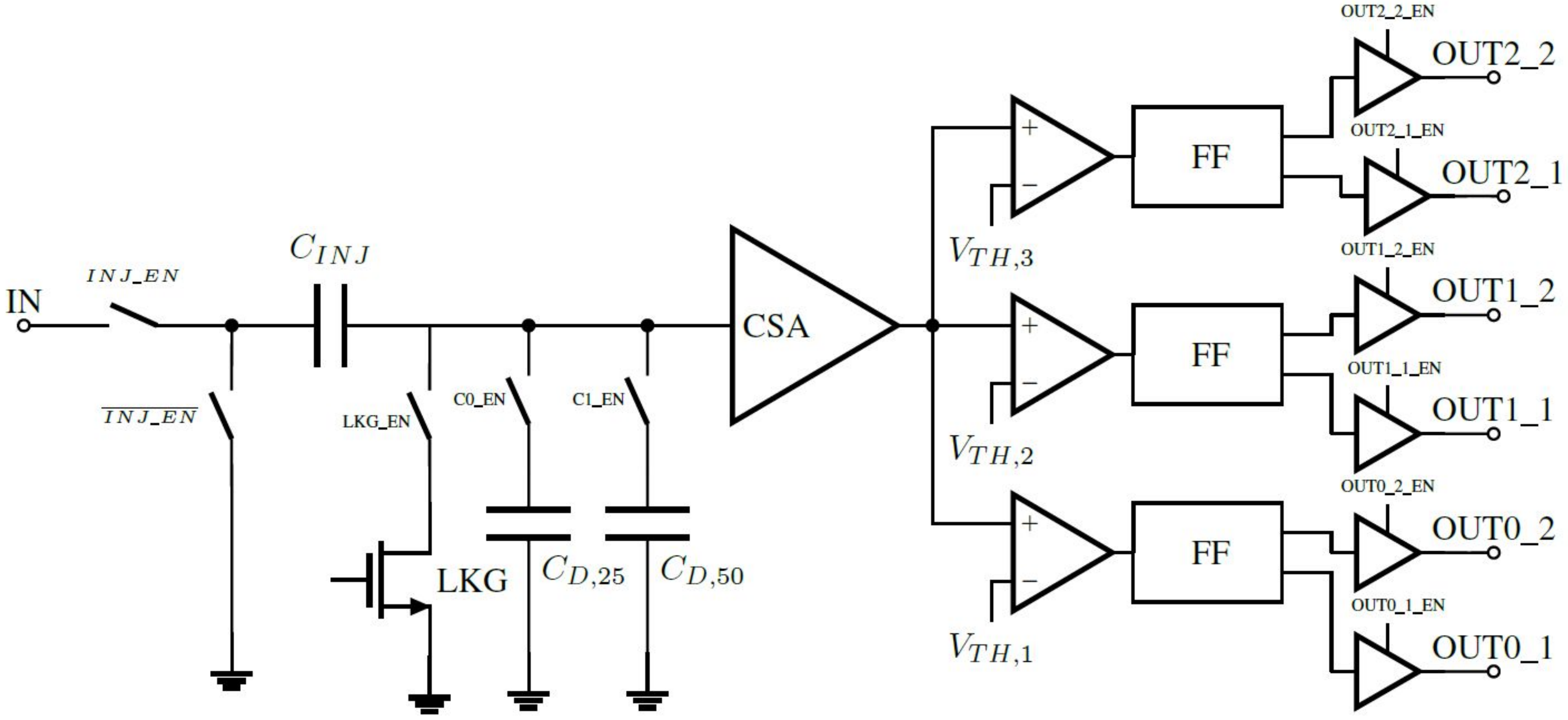
Falaphel

Main goals:

- Deepen the 28nm CMOS technology
- Data rate > 100 Gb/s
- Radiation TID > 1 Grad (10 MGy)
- Total Fluence > 5 x 10^{16}n/cm^2
- **design and fabrication of a demonstrator**

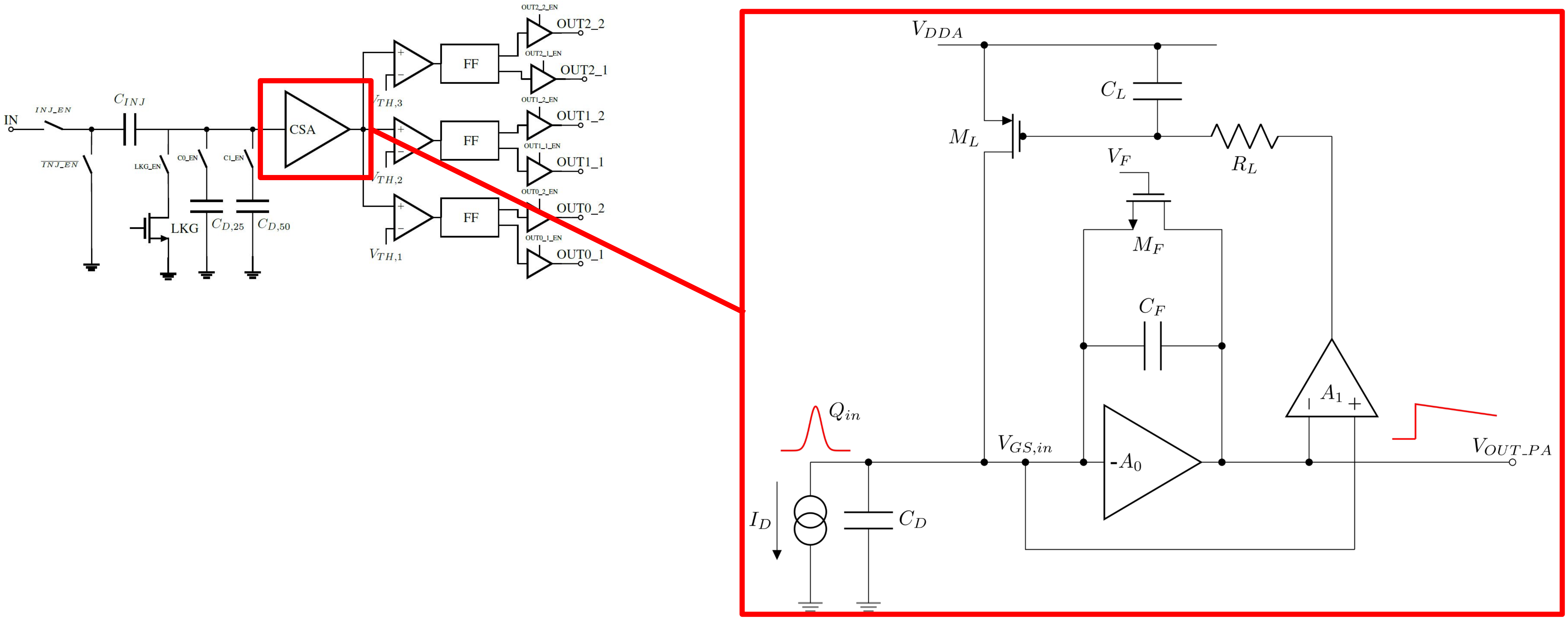


A first programmable FE channel has been designed

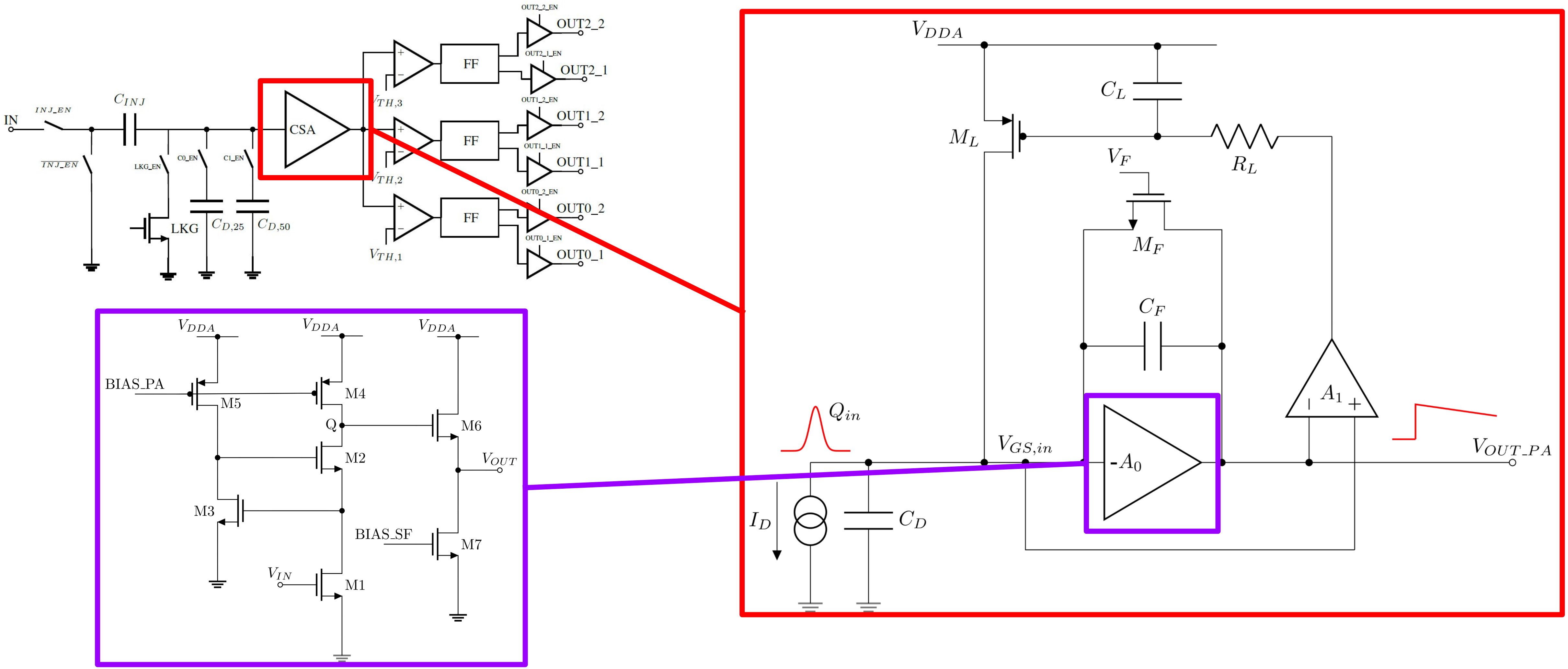


- based on a 2-bit, in-pixel flash ADC to digitize the read signal → **hit/no-hit response**
- **zero dead-time** behavior

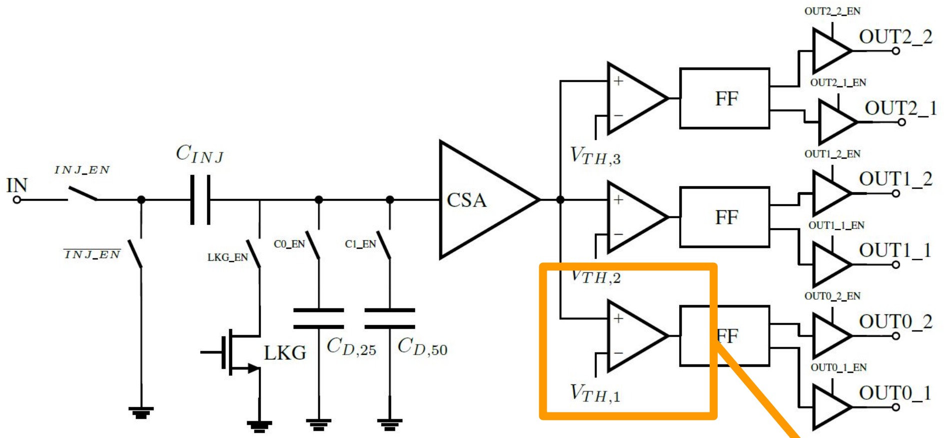
Building blocks inner structure is non-trivial



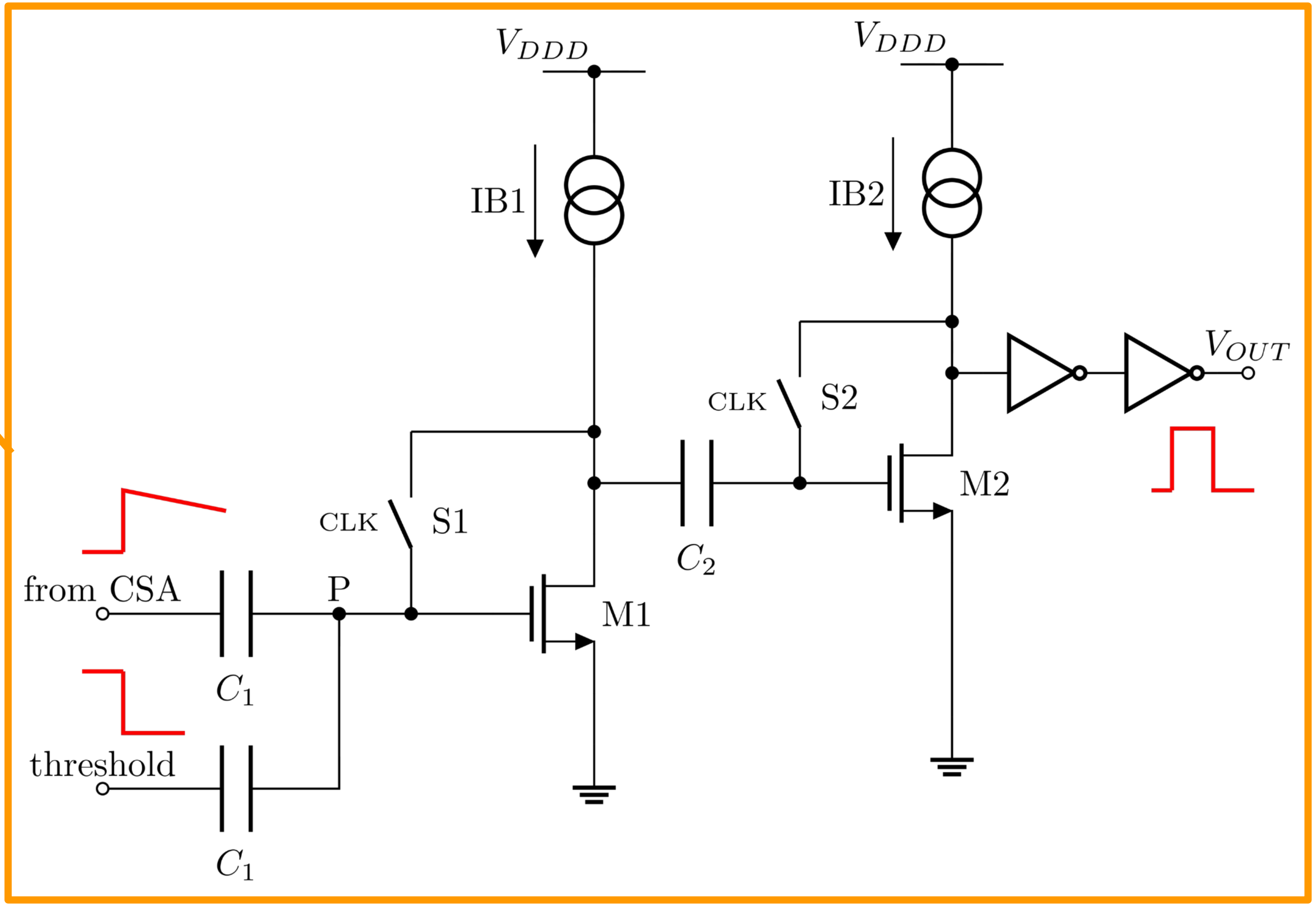
Building blocks inner structure is non-trivial



Building blocks inner structure is non-trivial



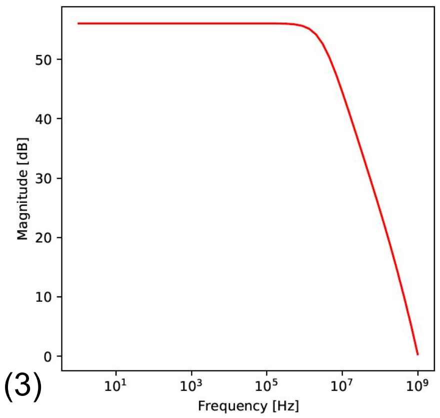
Investigate new architectures
→ this prototype integrates a "non-standard" discriminating stage



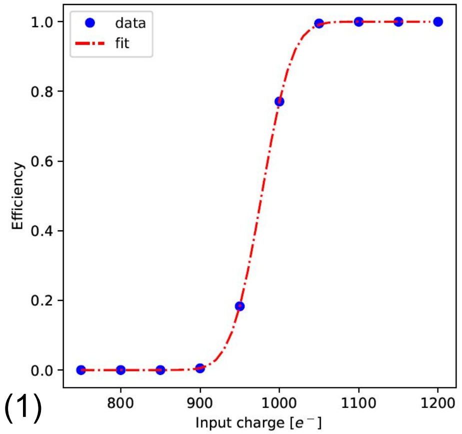
A well designed ASIC can take to extreme efficiencies

Simulations show:

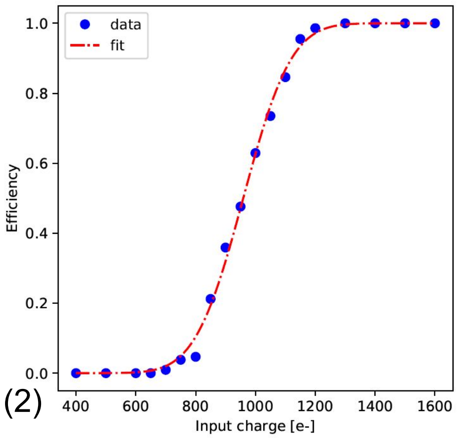
- **low power** → ~ 0.5 W/cm^2
- **low stable threshold** → ~ 800e-
- **low input referred noise**(1) → 67e- r.m.s. @ -20°C
- **low threshold dispersion**(2) → 30e- r.m.s.
- **stable operativity with detector:**
  - leakage < 20 nA
  - capacitance < 100 fF
- **noise occupancy** < 10^{-6}
- **performant gain stage**(3)**:**
  - Dominant pole @ 2 MHz
  - DC gain close ~ 58 dB
  - current consumption ~ 3μA



(3)

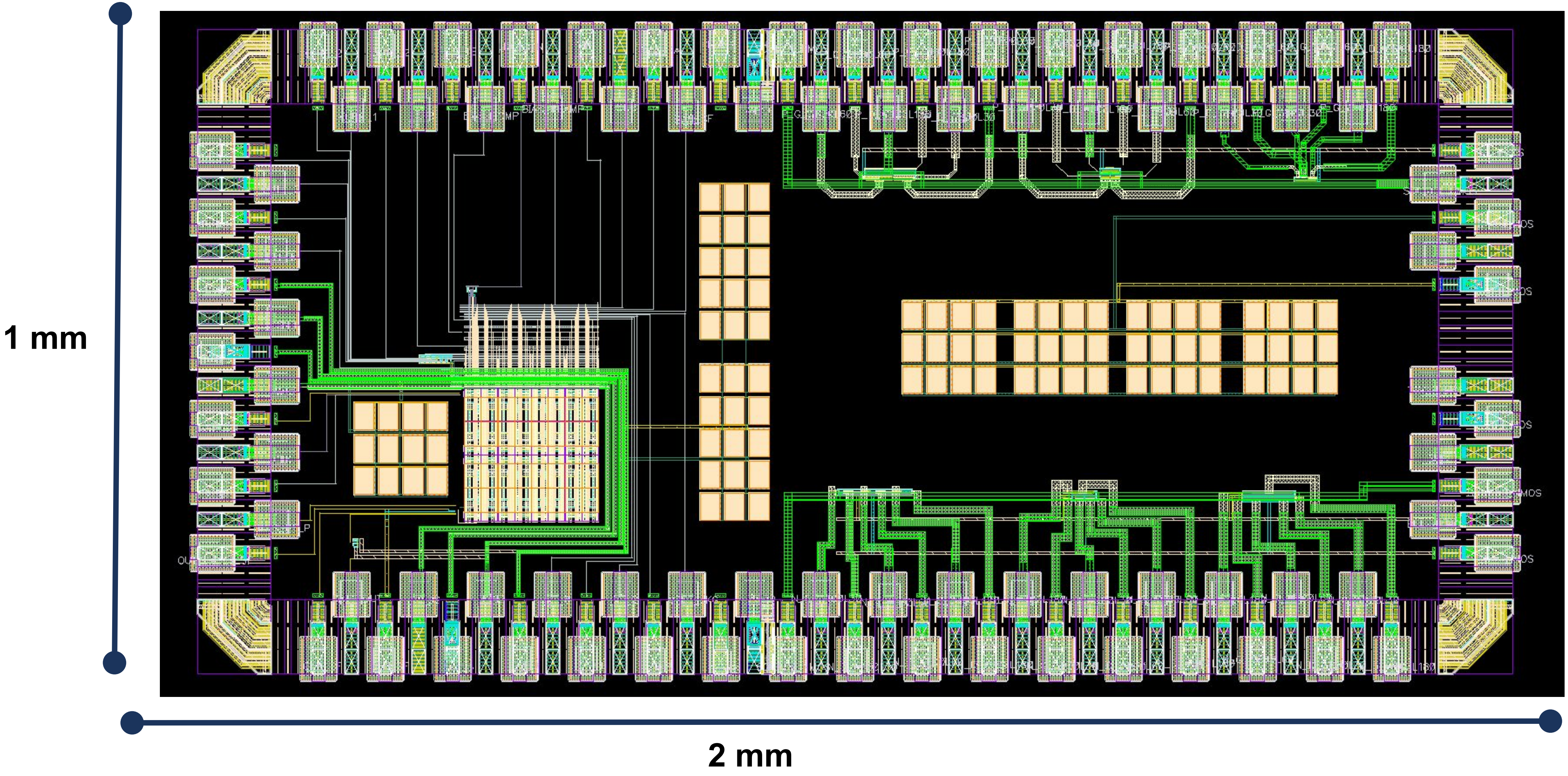


(1)



(2)

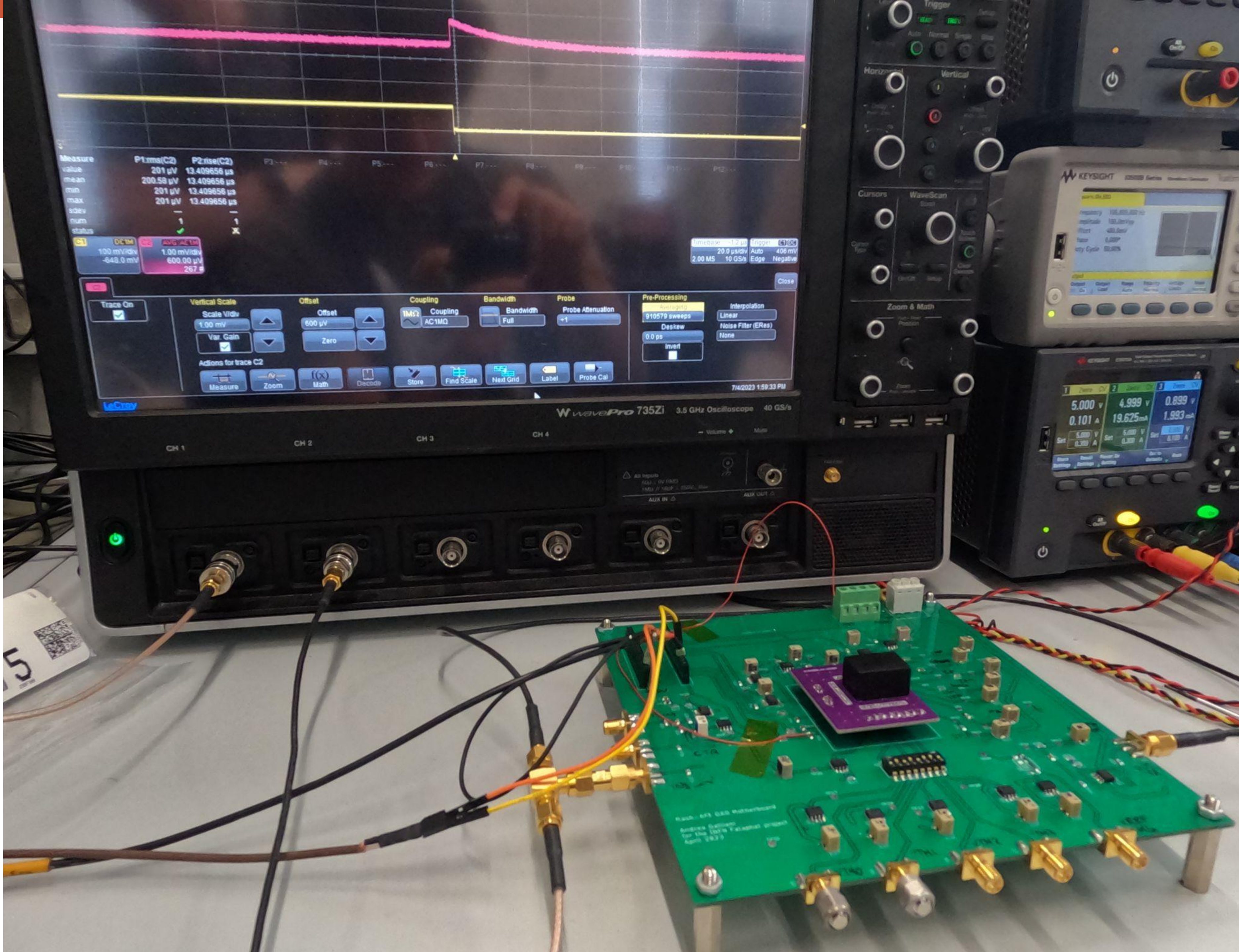
A Prototype Chip has been realized



Testing of the prototype in progress

The DAQ is completely self-designed and is composed of:

- motherboard + daughter board
- external data timing generator
- microcontroller for chip configuration
- graphical user interface on a pc for configuration and data acquisition management

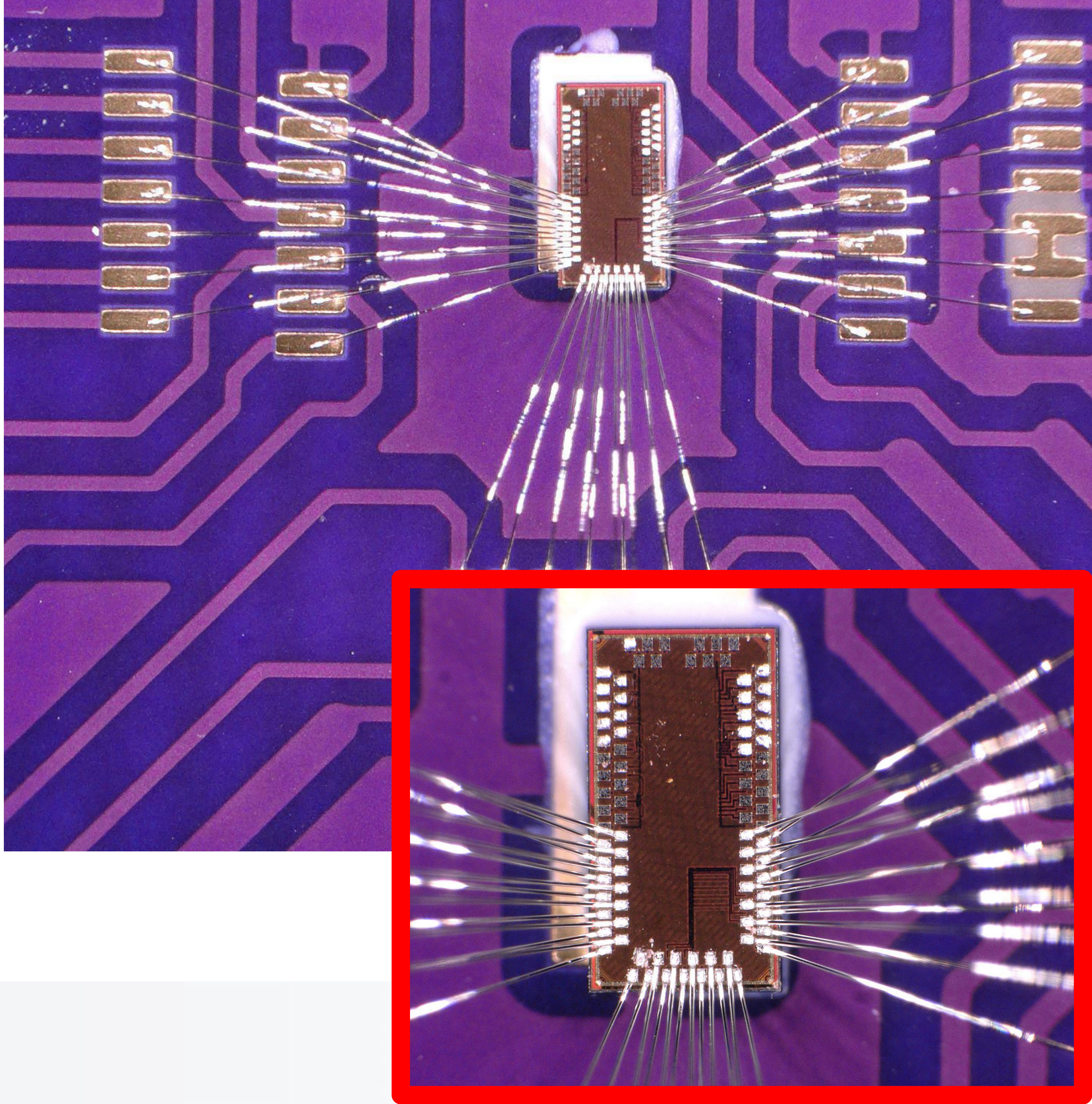


Conclusions

- **INFN** Falaphel project is working on a **28 nm** Silicon Photonics demonstrator for future physics experiments

- a first low power **front-end** prototype realized with very good simulated results

- data acquisition system designed and now used for **testing** the prototype chip



BACK-UP

The Gain Stage

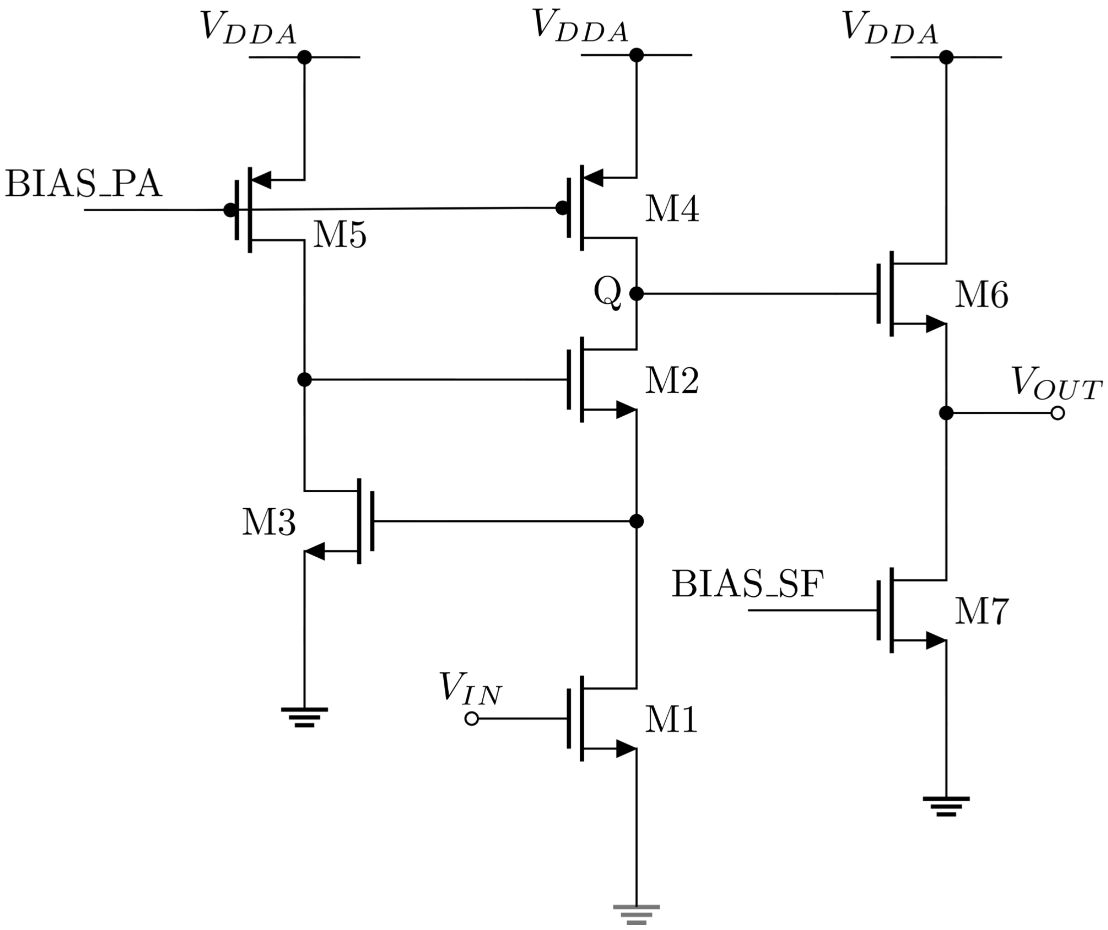
- **Regulated Cascode + Source follower**

Considering simplicistically a unitary gain for the Source Follower, the low frequency gain A_0 can be described as:

$$A_0 = g_{m1}\left\{\left[1+g_{m3}(r_{O3} \parallel r_{O5})\right]\cdot(g_{m2}r_{O2}r_{O1}) \parallel r_{O4}\right\}$$

In a first approximation it can be reduced to:

$$A_0 \sim g_{m1}r_{O4}$$



The Preamplifier

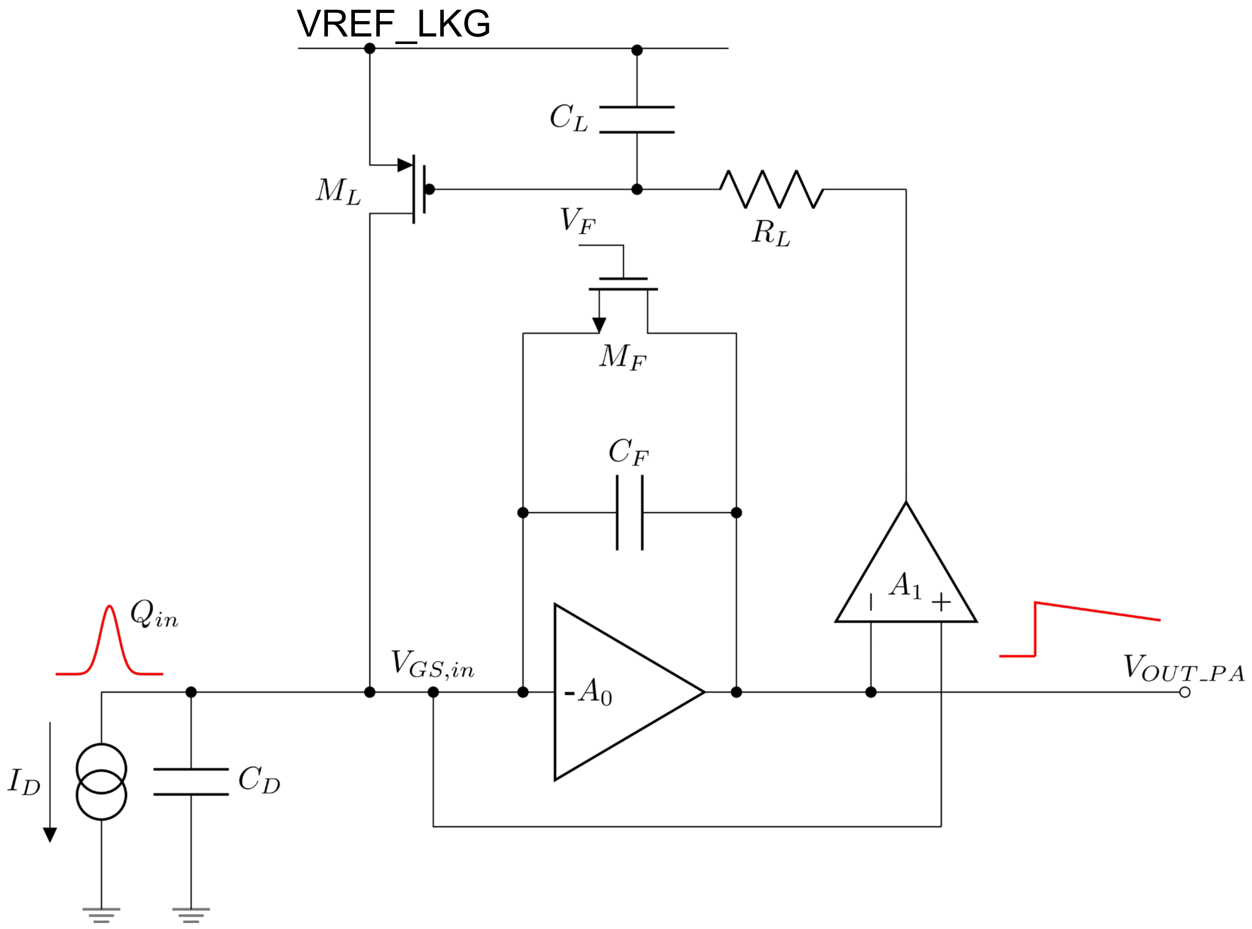
- Inverting forward gain stage A_0
- Fast negative feedback to manage the discharge current
- Slow negative feedback loop for leakage compensation

$$F(s) = -\frac{A_0}{1 + s\tau}$$

$$\tau = \frac{1}{R_{OUT} C_{EQ}}$$

$$R_{OUT} \sim r_{O4}$$

$$C_{EQ} \sim C_{DB2} + C_{GD6} + C_{GD4} + C_{GD2}$$



The Preamplifier

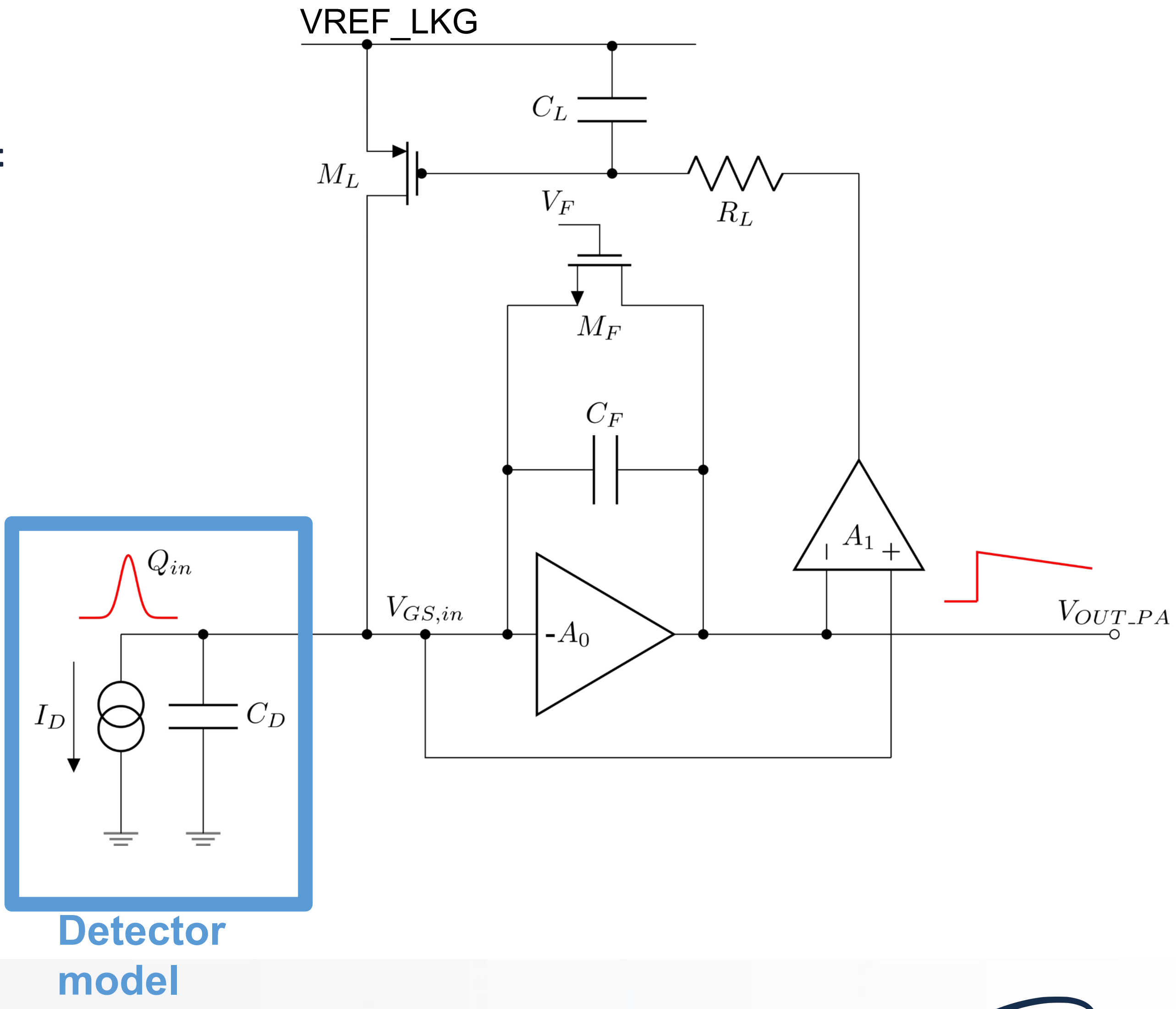
+ **Inverting forward gain stage A_0**
+ **Fast negative feedback to manage the discharge current**
+ **Slow negative feedback loop for leakage compensation**

$$F(s) = -\frac{A_0}{1+s\tau}$$

$$\tau = \frac{1}{R_{OUT}C_{EQ}}$$

$$R_{OUT} \sim r_{O4}$$

$$C_{EQ} \sim C_{DB2} + C_{GD6} + C_{GD4} + C_{GD2}$$



The Preamplifier

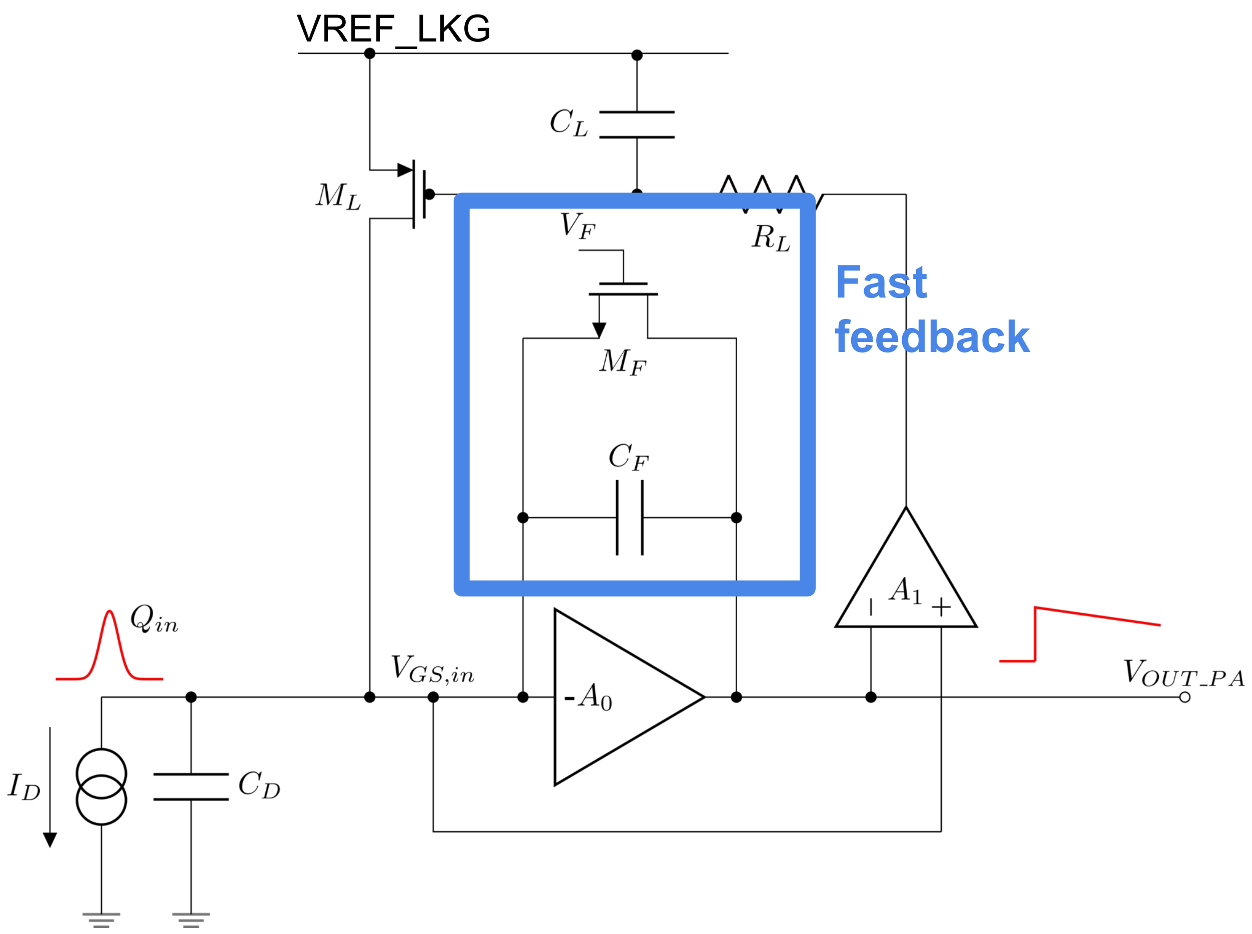
- **Inverting forward gain stage A_0**
- **Fast negative feedback to manage the discharge current**
- **Slow negative feedback loop for leakage compensation**

$$F(s) = -\frac{A_0}{1 + s\tau}$$

$$\tau = \frac{1}{R_{OUT} C_{EQ}}$$

$$R_{OUT} \sim r_{O4}$$

$$C_{EQ} \sim C_{DB2} + C_{GD6} + C_{GD4} + C_{GD2}$$



The Preamplifier

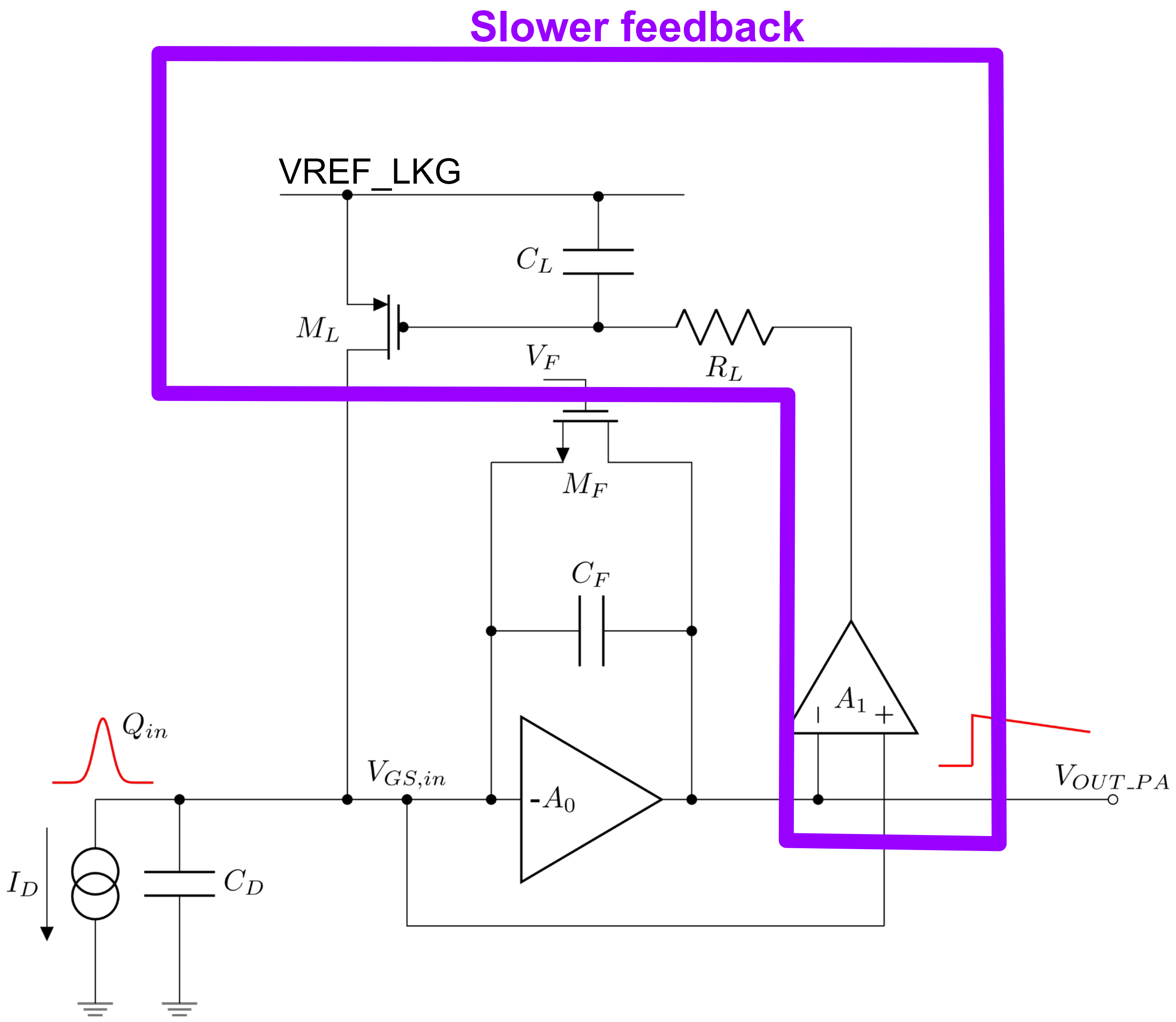
+ **Inverting forward gain stage A_0**
+ **Fast negative feedback to manage the discharge current**
+ **Slow negative feedback loop for leakage compensation**

$$F(s) = -\frac{A_0}{1 + s\tau}$$

$$\tau = \frac{1}{R_{OUT} C_{EQ}}$$

$$R_{OUT} \sim r_{O4}$$

$$C_{EQ} \sim C_{DB2} + C_{GD6} + C_{GD4} + C_{GD2}$$



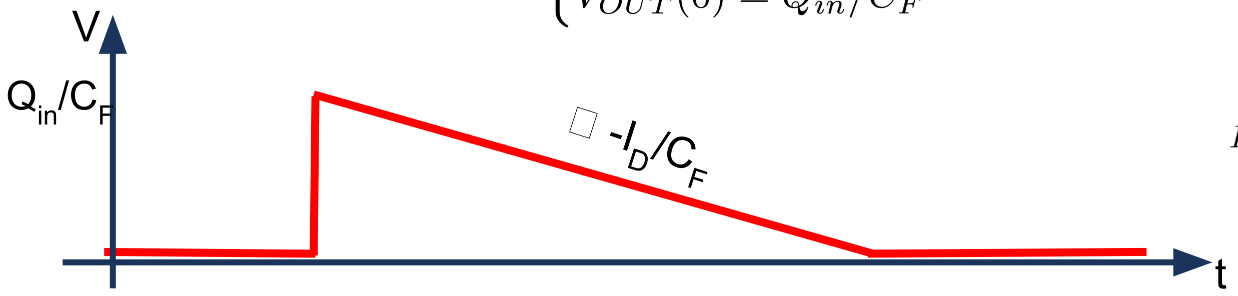
The Preamplifier

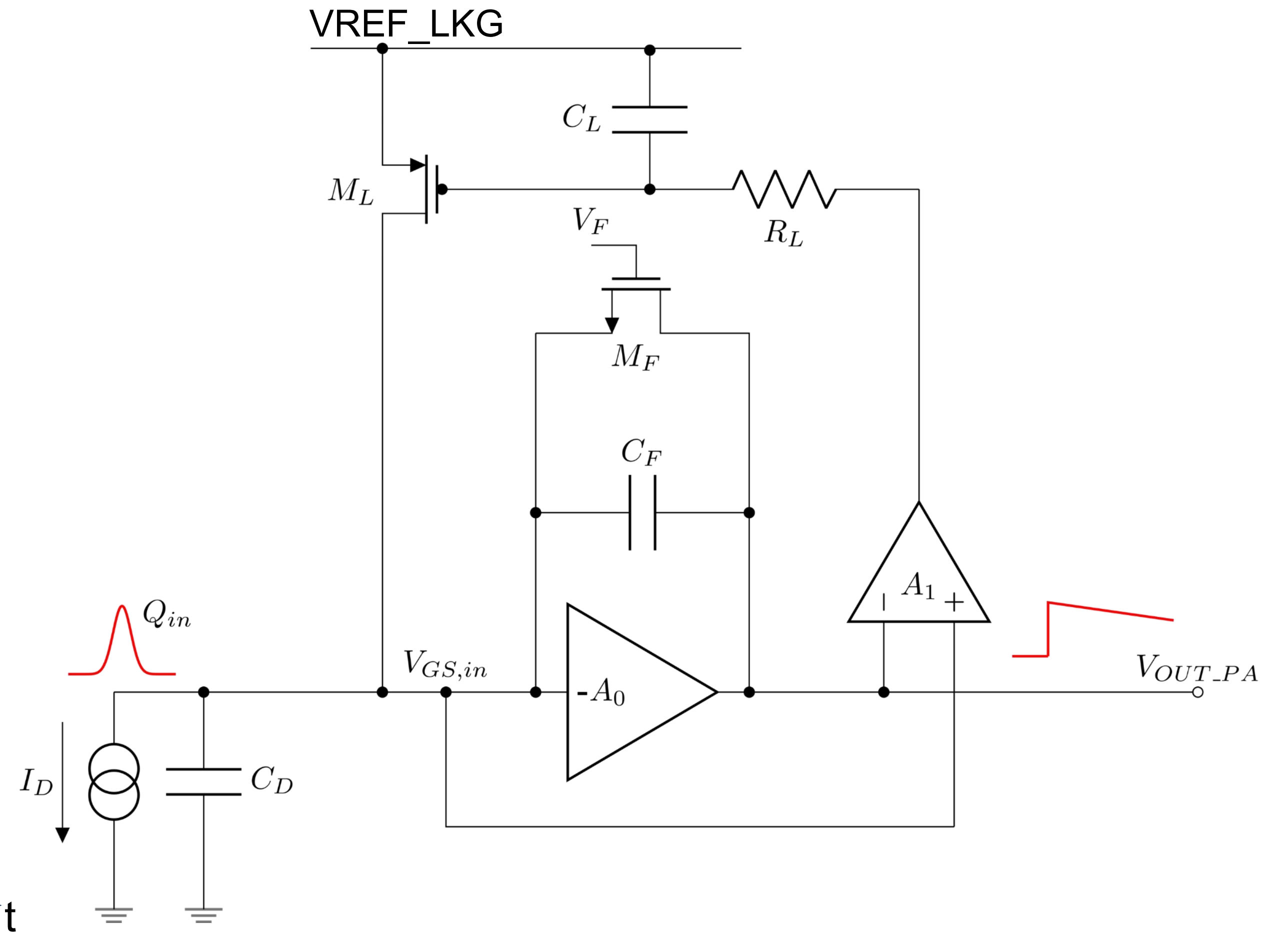
- **Inverting forward gain stage A_0**
- **Fast negative feedback to manage the discharge current**
- **Slow negative feedback loop for leakage compensation**

M_F weak inversion current $I_D = I_0 \frac{W}{L}(e^{\frac{V_{GS}-V_{TH}}{V_T}})(1 - e^{-\frac{V_{DS}}{V_T}})$

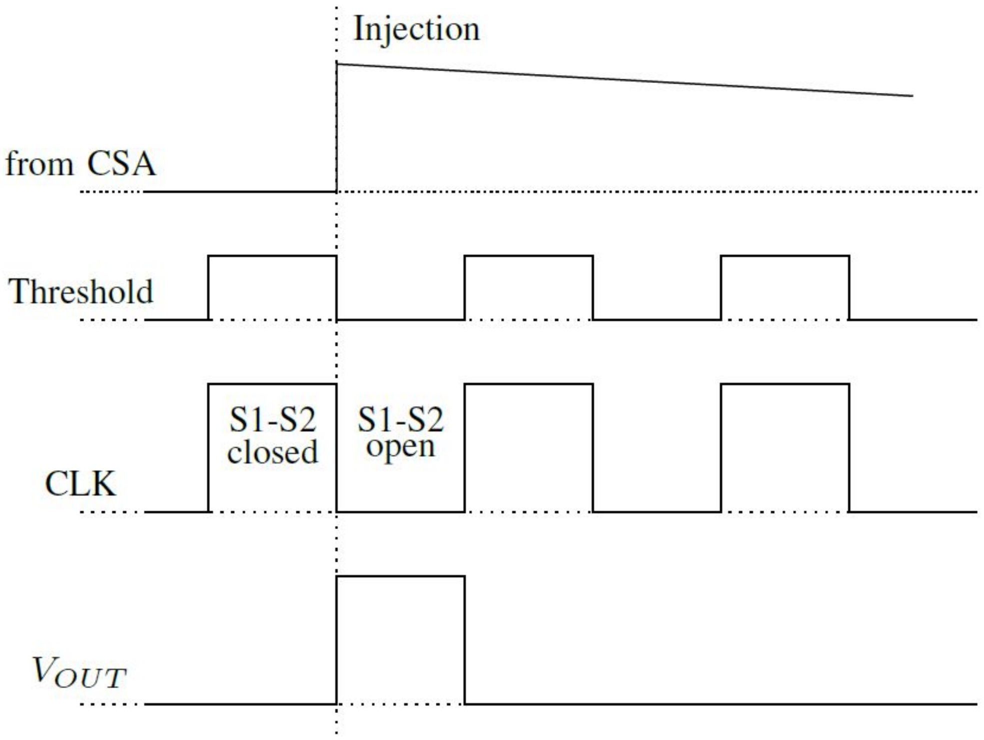
C_F discharge current: $I_D = K \cdot (1 - e^{-\frac{V_{OUT}}{V_T}})$

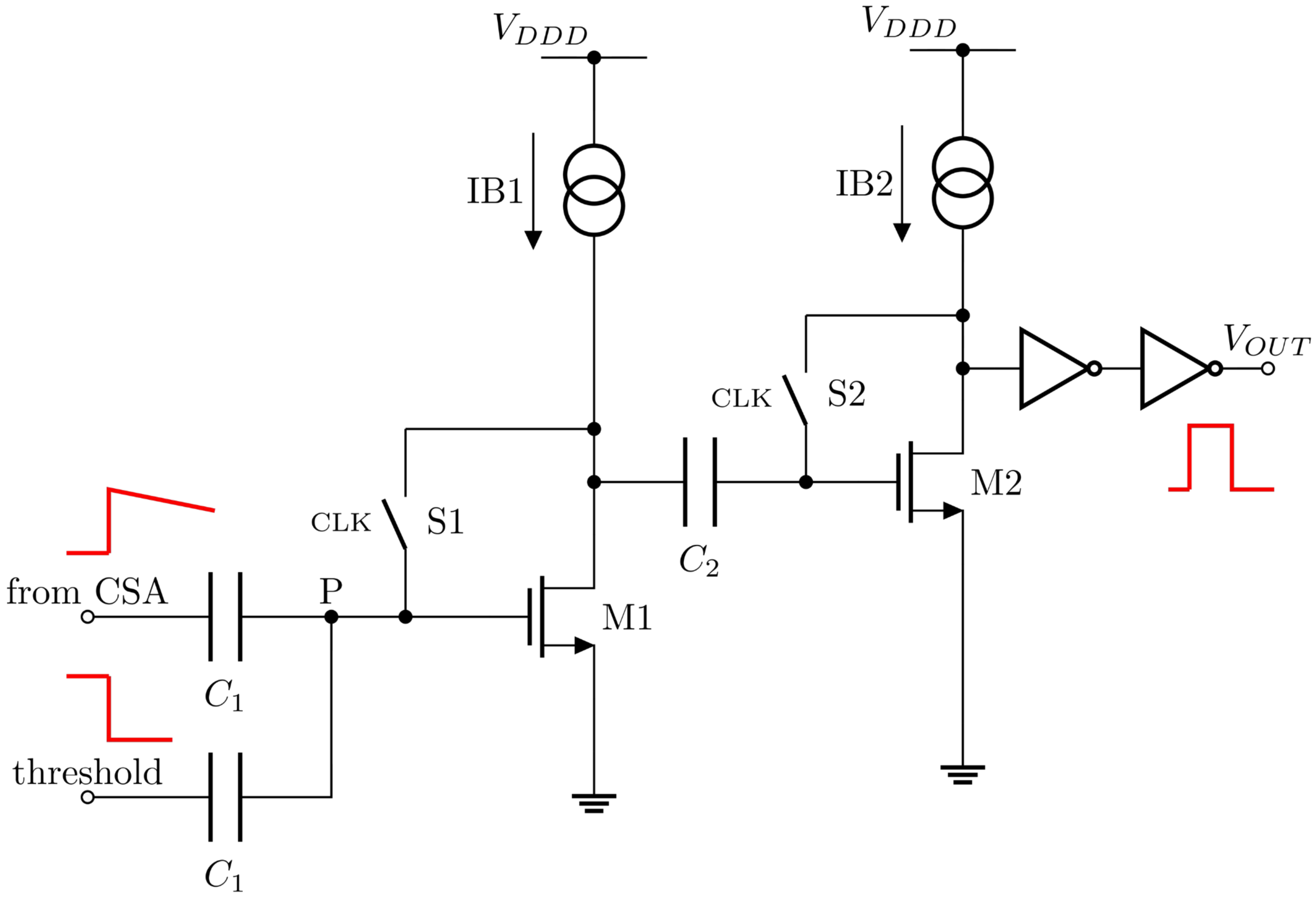
CSA return-to-baseline: $\begin{cases} I_D + C_F \cdot \frac{dV_{OUT}(t)}{dt} = 0 \\ V_{OUT}(0) = Q_{in}/C_F \end{cases}$





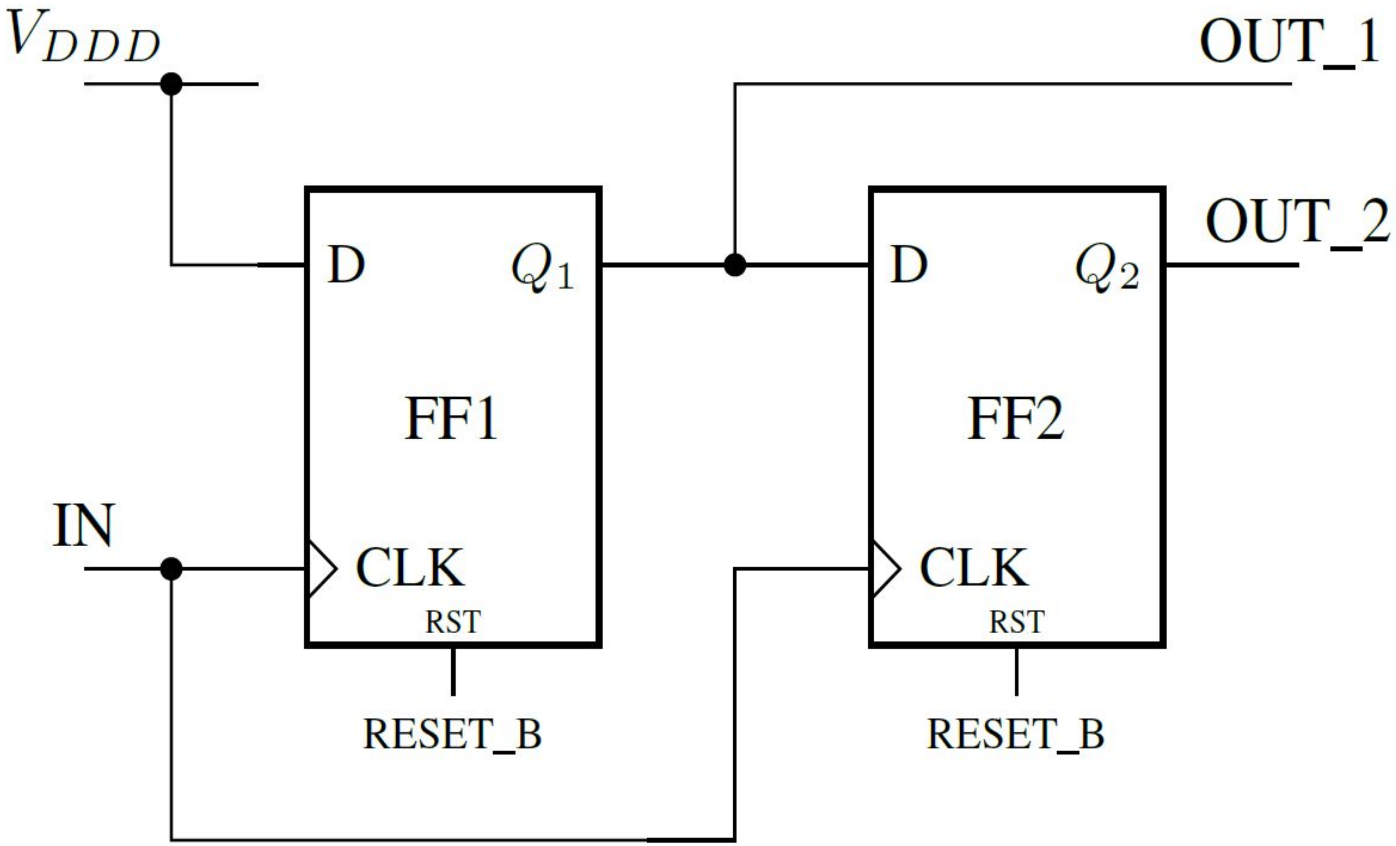
The Comparator



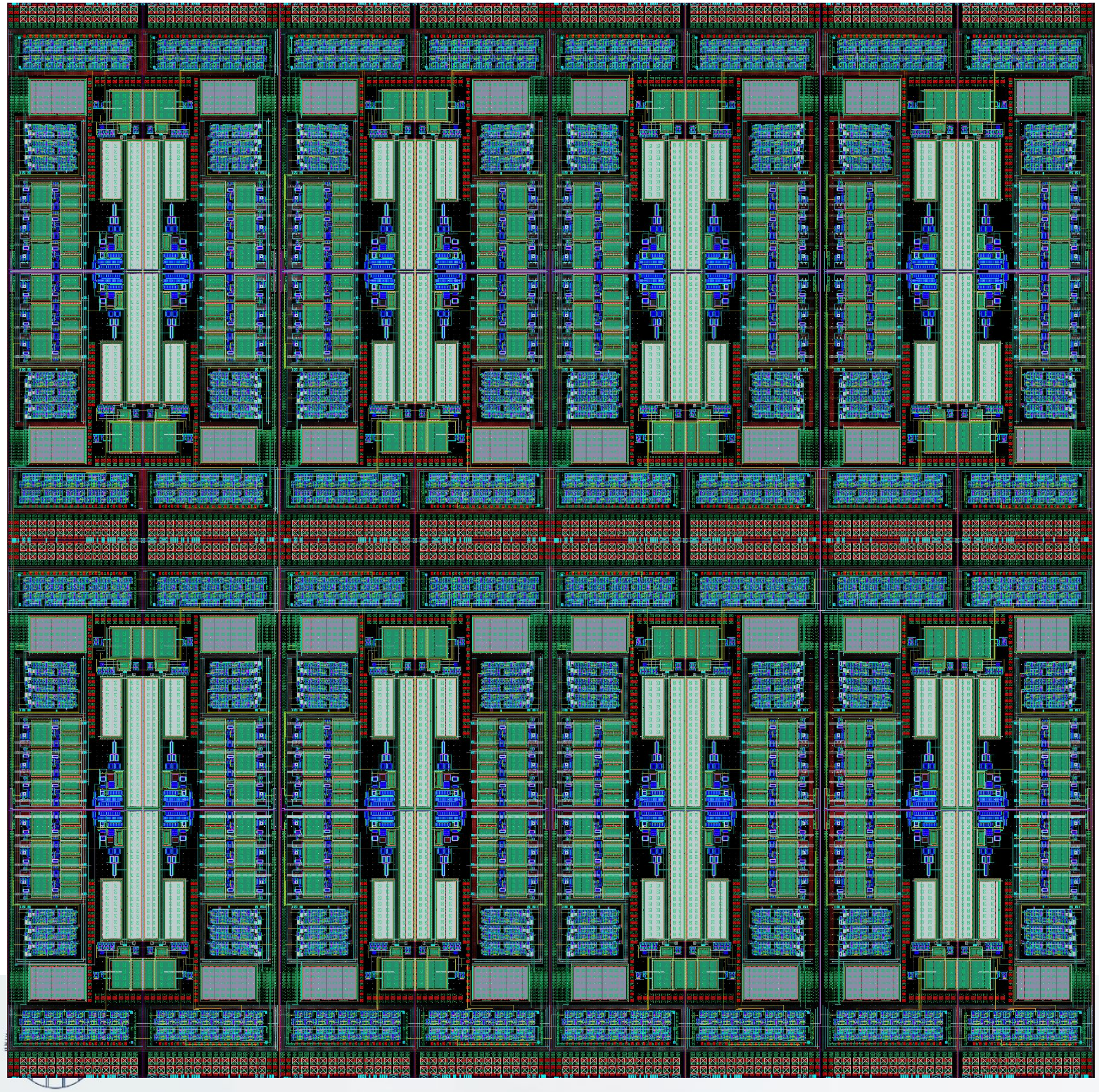


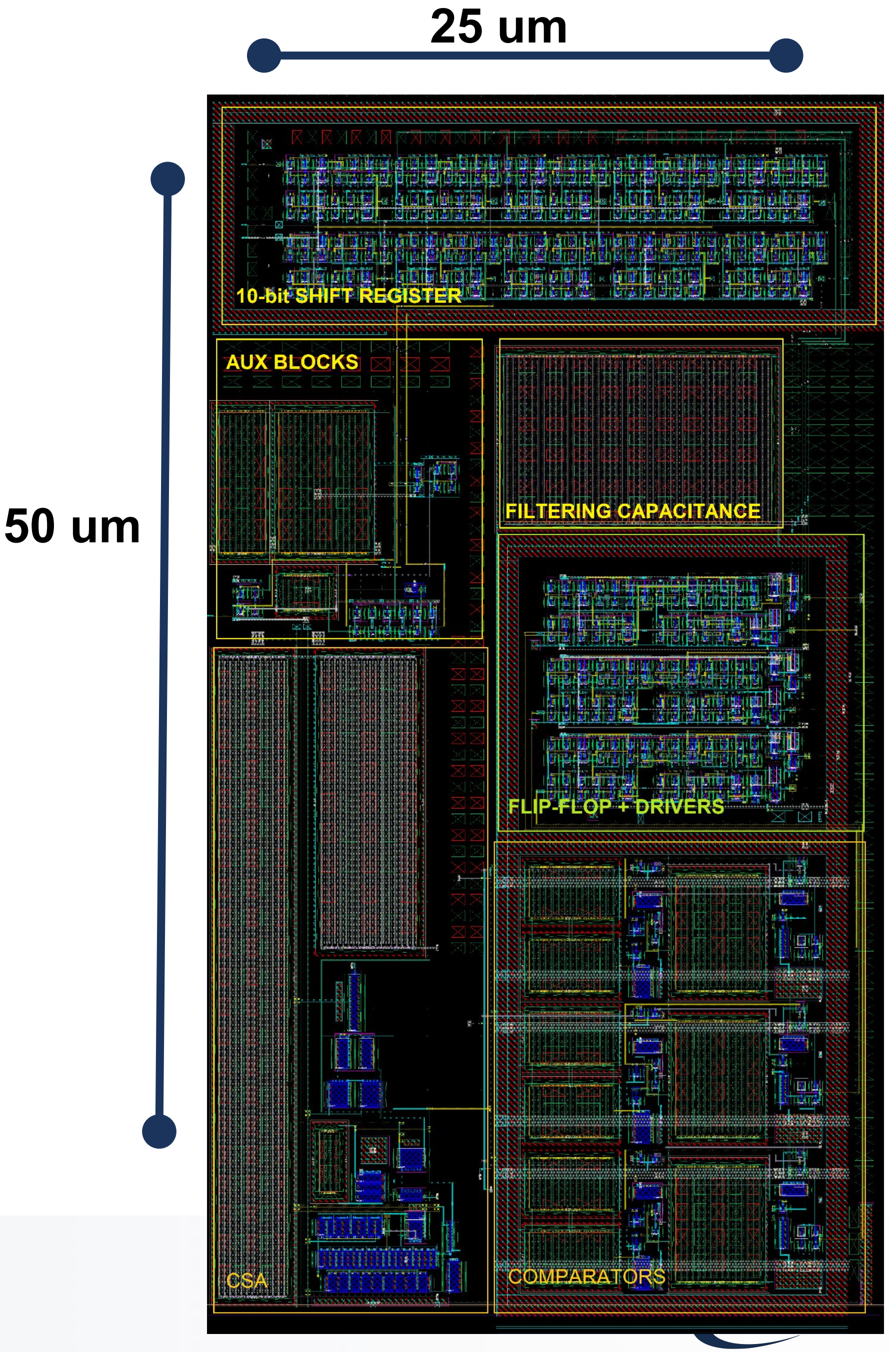
Double Hit Detection

1. IN = **LOW**
   → FF1 does not change Q1
   → OUT 1 = OUT_2 = Low
1. IN = **HIGH** for the **1st** time
   → FF1 changes Q1
   → OUT_1 = High; OUT_2 = Low.
   → FF2 is ready to change its state
1. IN = **HIGH** for the **2nd** time
   → FF2 changes its state
   → OUT1 = OUT2 = HIGH
1. RESET
   → OUT 1 = OUT 2 = LOW



Some layout details





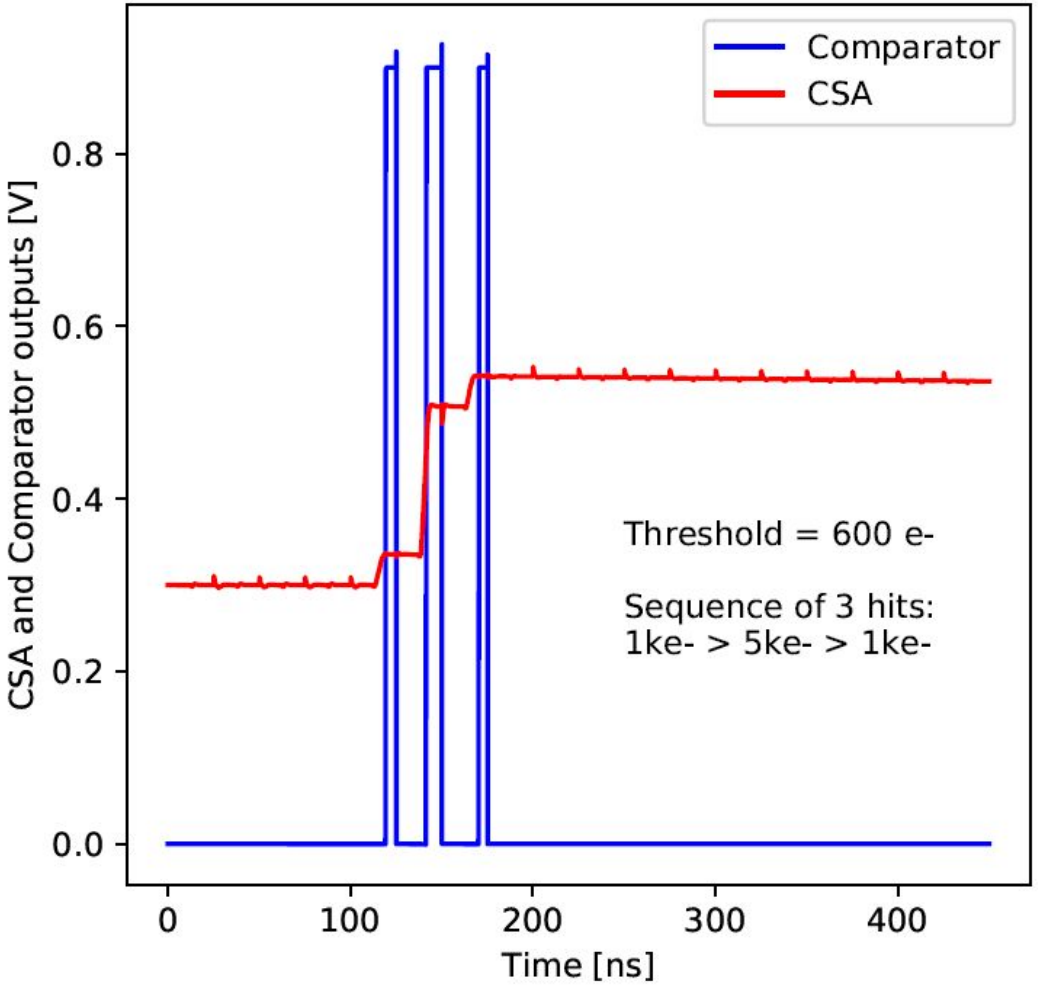
Post Layout Simulations

Zero dead-time behavior

Injections in sequential bunch crossing periods (25ns) with a 600e- threshold:

1000e- → 5000e- → 1000e-

The comparator successfully process the three consecutive signals

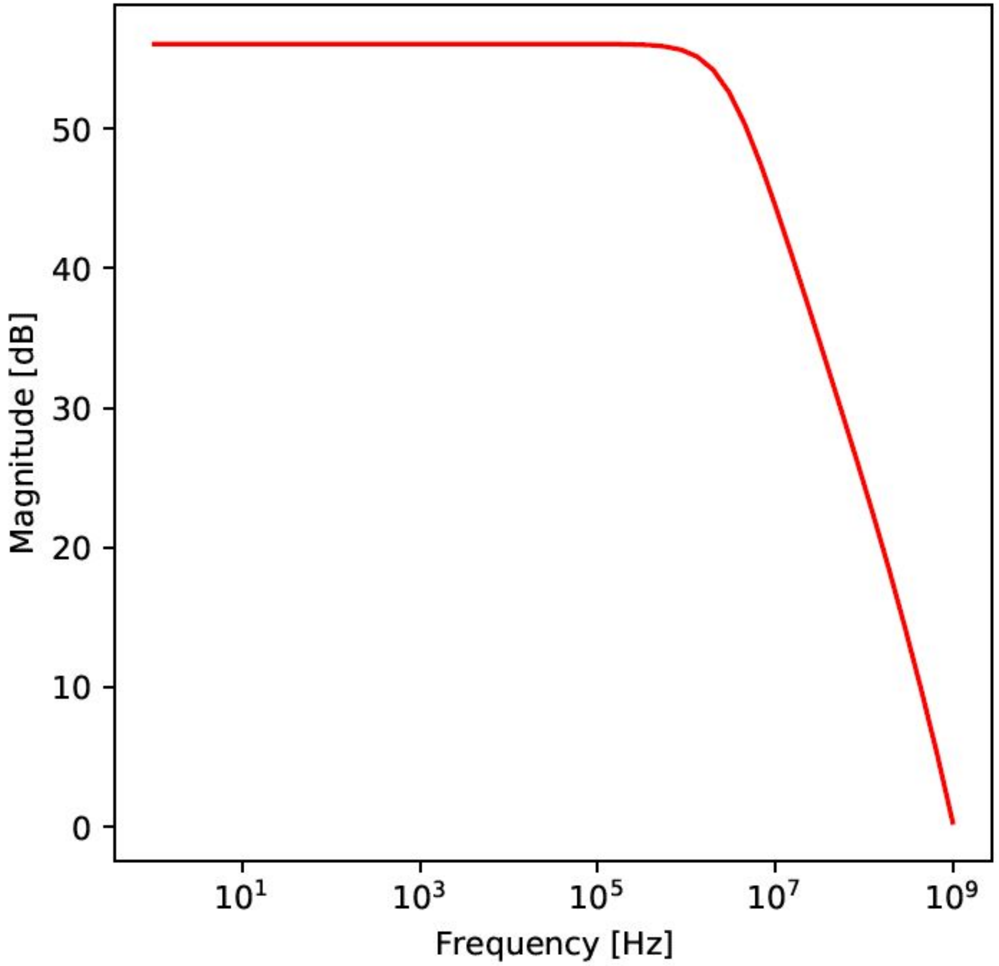


Post Layout Simulations

Dominant pole at 2 MHz

DC gain close to 58 dB

CSA current consumption ~ 3μA



Post Layout Simulations

Equivalent Noise Charge: input charge for which the front-end Signal-to-Noise ratio is equal to 1.

$$ENC = \frac{v_{n,out}}{G_Q}$$

$v_{n,out}$ → noise root mean square evaluated at the preamplifier output
G_Q → charge sensitivity

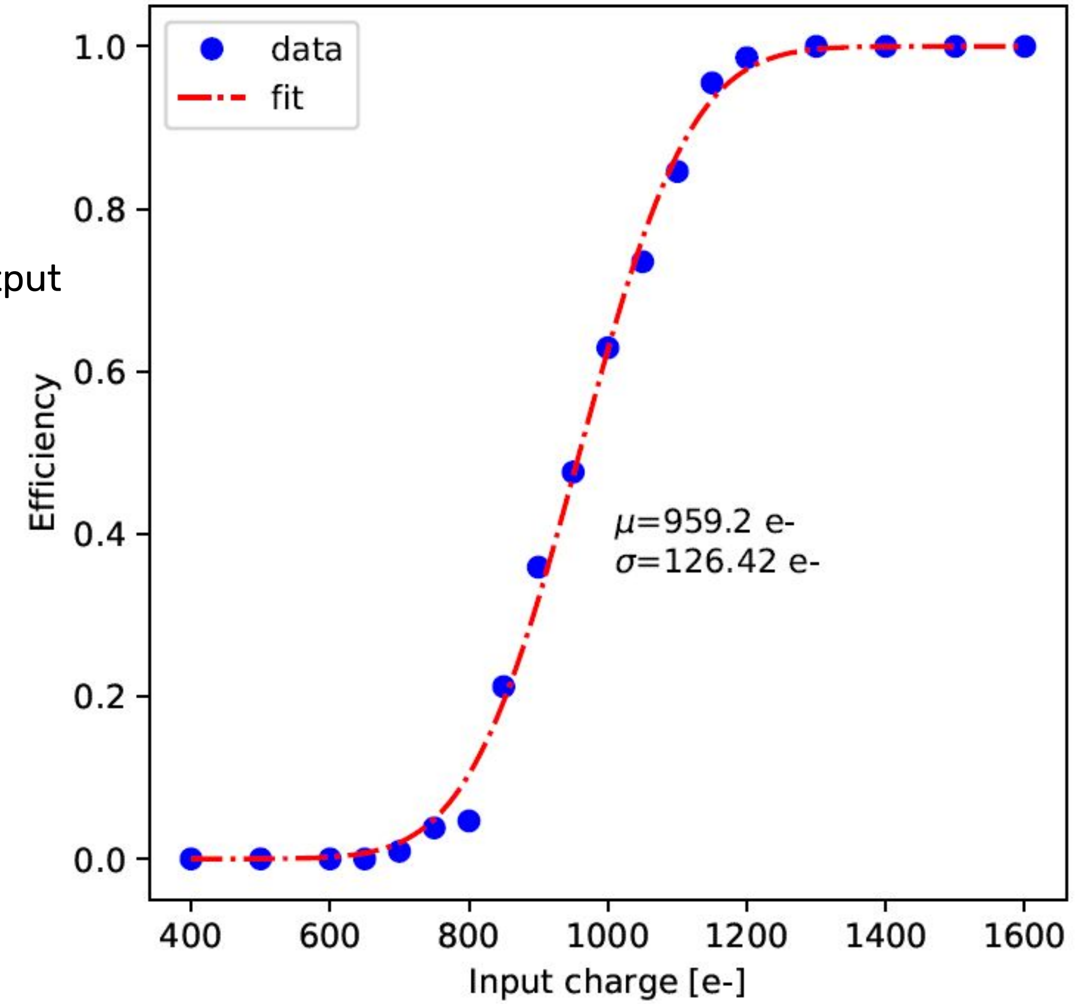
CSA ENC with 50fF detector capacitance

ENC ~ 73e- r.m.s. @ 27 °C

ENC ~ 67e- r.m.s. @ -20°C

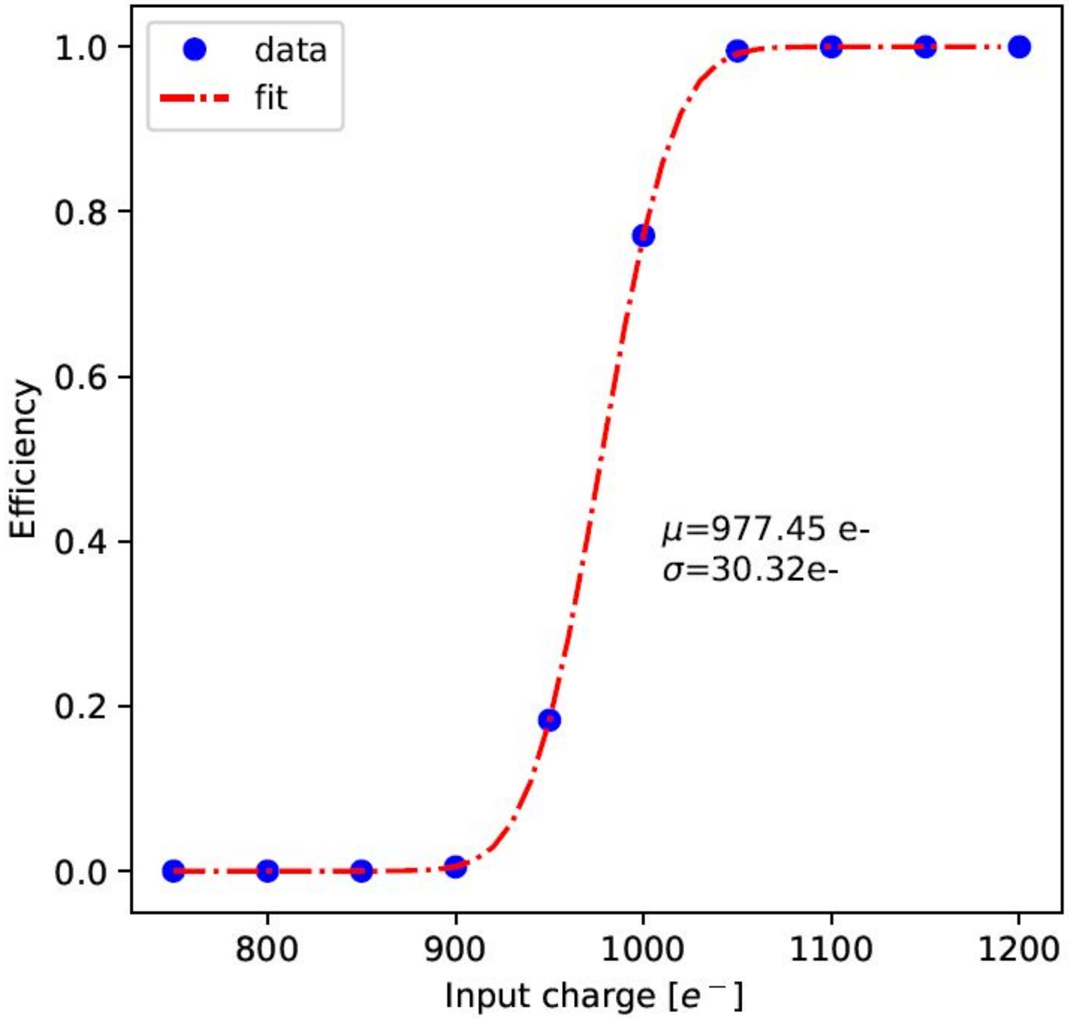
Comparator ENC
obtained through a set of 200 transient noise simulations

ENC ~ 126e-



Post Layout Simulations

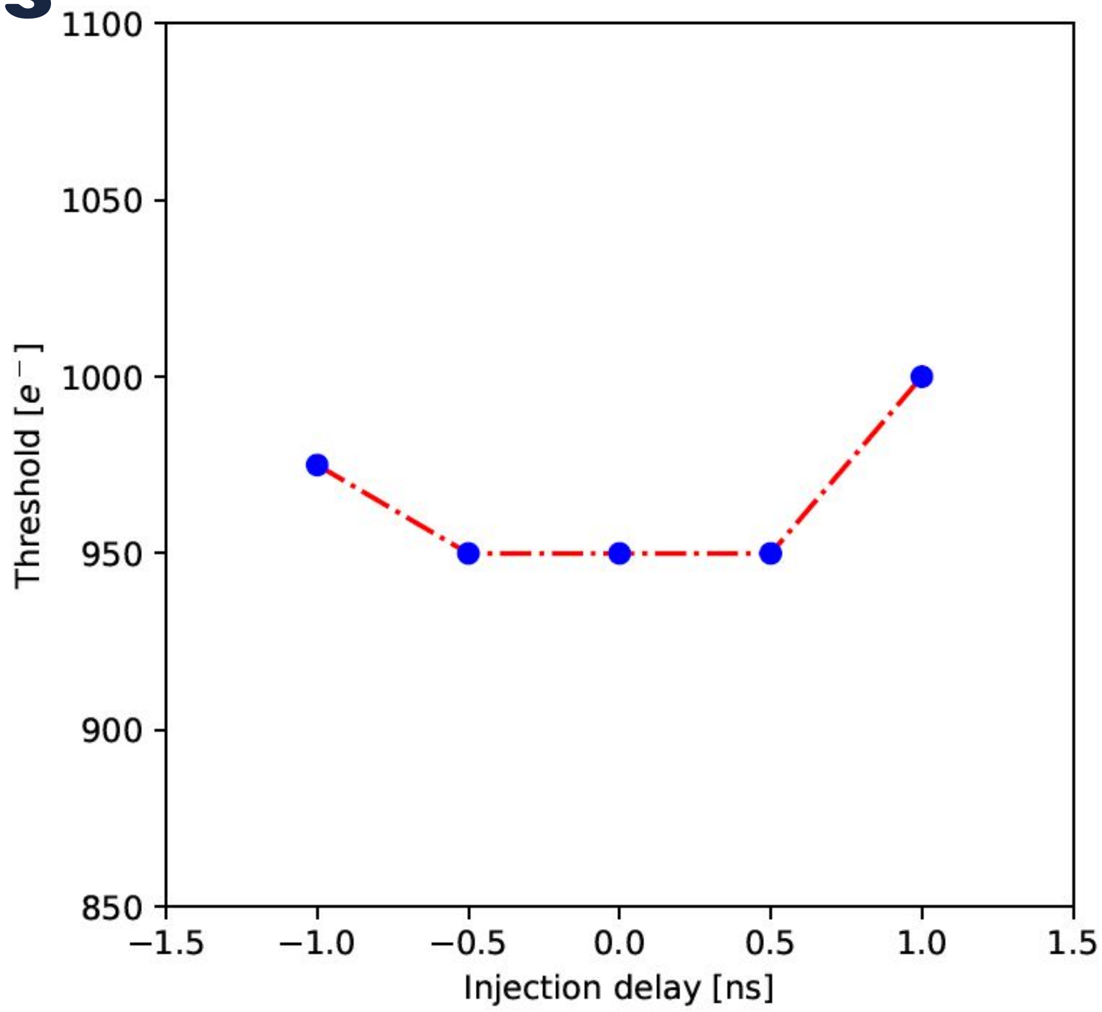
Threshold dispersion ~ 30e- r.m.s.



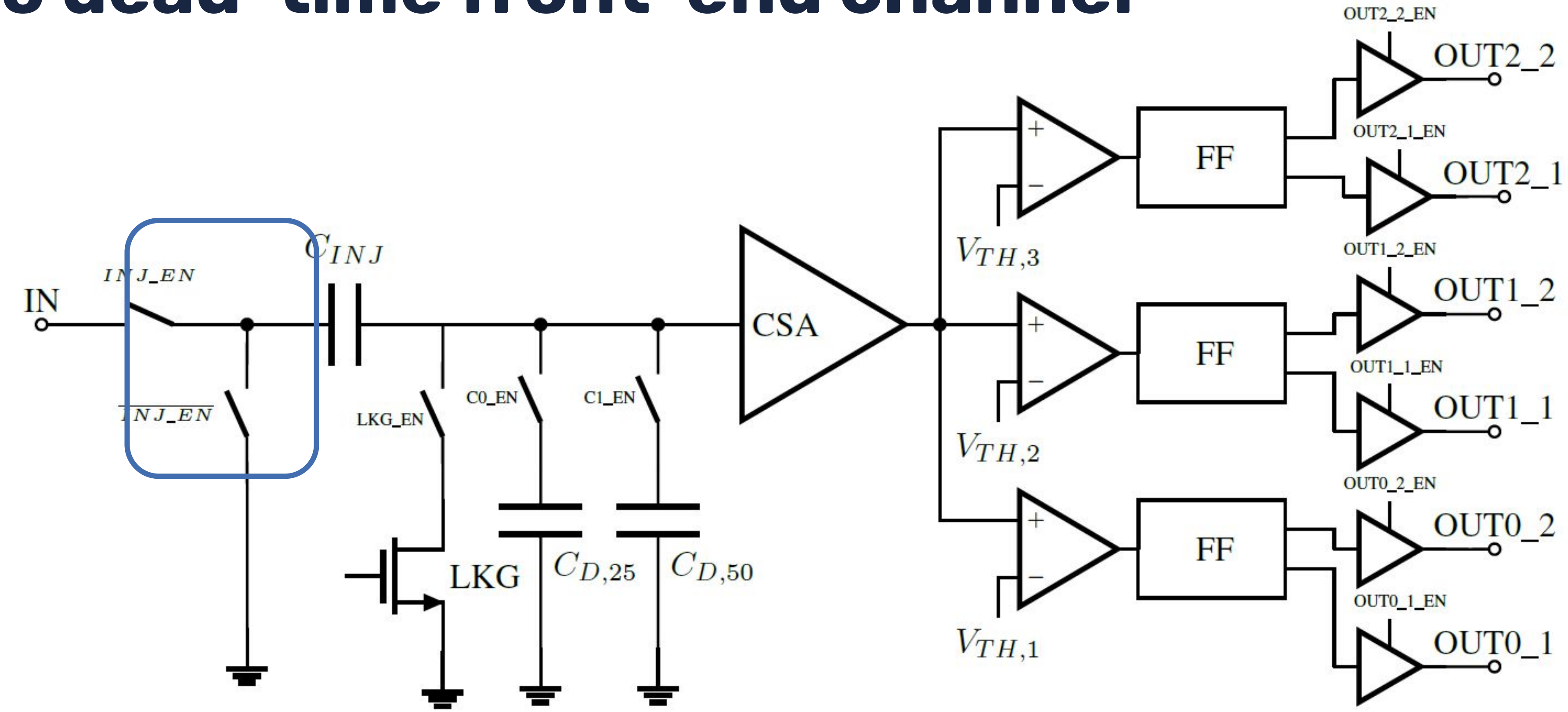
Post Layout Simulations

threshold is pretty **stable** with respect to injection delay (i.e. the time difference between injection and clock edge)

→ threshold variation < 50 e- against a delay from -1ns up to +1 ns

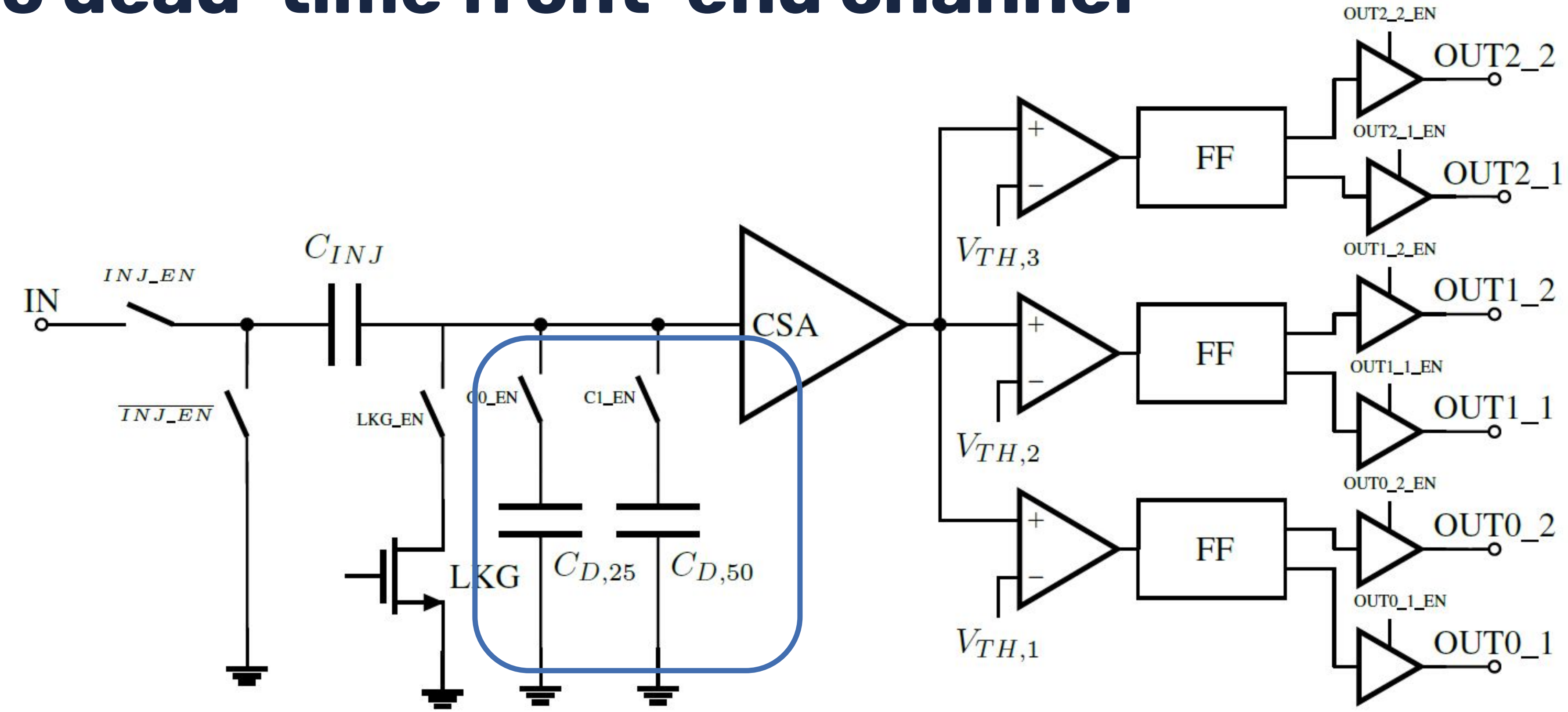


Zero dead-time front-end channel



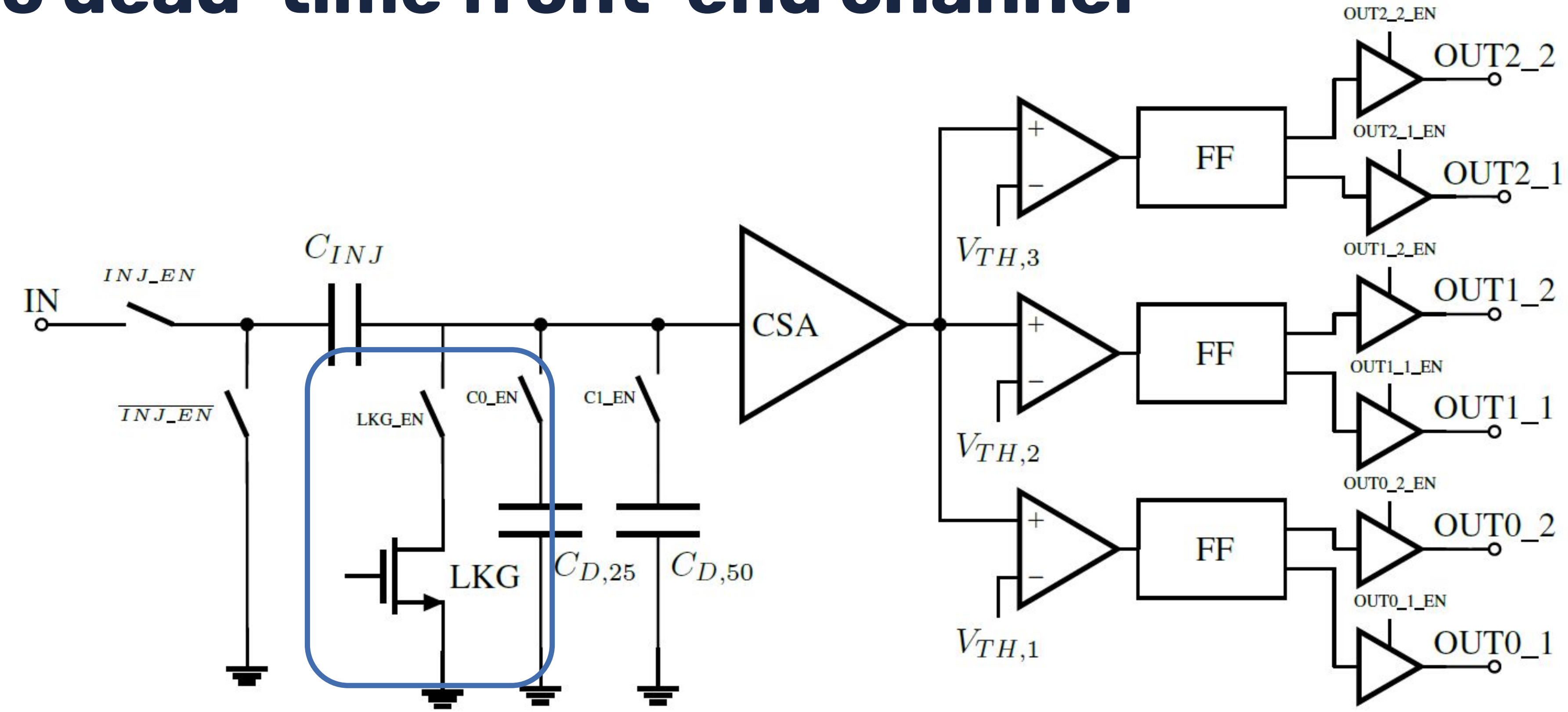
When disabled, the input is connected to ground, so that only the enabled pixel is tested with the injection signal and the other channels of the matrix are insensitive to possible swings on the injection bus.

Zero dead-time front-end channel



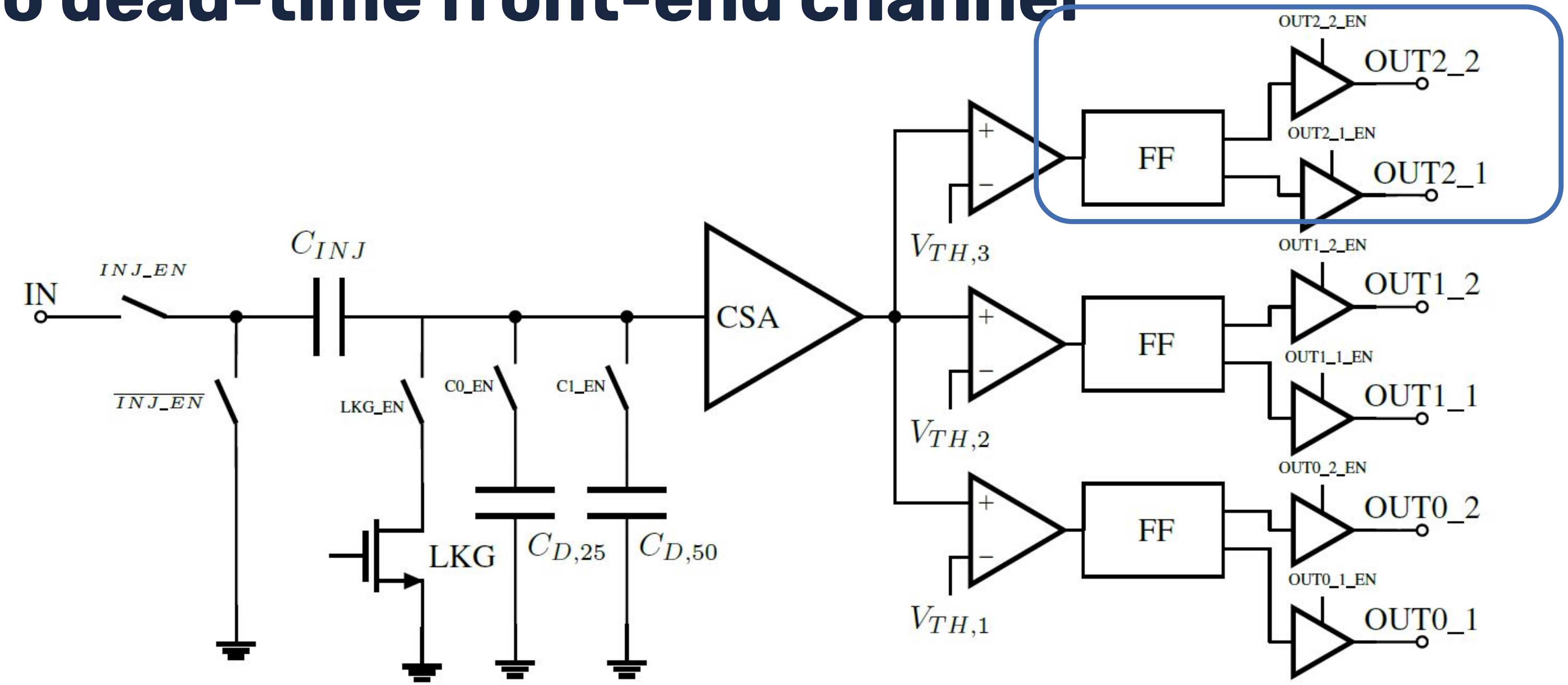
Detector capacitance emulation

Zero dead-time front-end channel



Leakage current simulation circuit

Zero dead-time front-end channel



Double hit detection stage with tristate buffer column driver

Data Acquisition System architecture