BWS LHC - Feasibility discussion to synchronise new LIU type acquisition with legacy mechanism for the run 2023

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LHC BWS Setup

LHC BWS BEAM 1 MOTION PART

LHC BWS BEAM 1 PMT PART
LIU type (right) OP type (left)

BEAM 1 LIU type (UA47)
Synchronization OP and LIU system

OP system US45
- LTIM (HW or SW)
- 1x Pot. Position (in mm with open gate ?)

LIU system UA43 & UA47
- LTIM (HW)
- Config event LTIM + flight time IN and OUT!

Independent ACQ UA43 & UA47
- OR
- LTIM (HW)
- 1 for IN, 1 for OUT

4x PMT DATA

NXCALS

SWAN script to correlate POSITION and 4x PMT bxb ?

App or FESA ?

App for OP ?
Modification proposal

• Operational system modification (HW / SW)
  - LTIM to trigger the scan
  - HW cable or is it enough to use an SW event?
  - Jitter with SW based interrupt for the SW motion trigger?

• LIU-based linear system modification (HW / SW)
  - LTIM HW is already on the drive => do we simply use the motion simulation mode
  - What about the acquisition window duration?
  - What about the different IN/OUT speed and delay….

=> Should we install a second VFC+ADC in parallel at the pre-amp's output and use an LTIM directly on the acq card?
Interaction (wire-beam) position estimation viewed from the motor resolver (in radian)

Stroke=133mm
Interaction point=66.5mm
Leadscrew=16mm/(2*pi)rad

Interaction point in rad: 66.5*2*pi/16 = 26.114 rad

Tested acquisition range: 0.02s (capture) * 0.5m/s = 10mm

How precise is the forks and wire installation?
**OP type:** Architecture, specification, and limitations (mechanism, electronics, control, acquisition)

**Limitations:**
- Architecture multiplexed
- Power stage failure
- Analog feedback
- CPU involved in the safety of the motion control
- Acquisition filter wheel
- Bellows lifetime (40kcycle)

**Actions:**
- SW FESA 2 -> 3 (2021)
- FPGA patch (2015)
- Lab testing (as much as possible)
- IST with dummy scanner (2x in 2022)
LHC hybrid prototype with LIU electronics

- Motion Controller Unit (MCU)
- Intelligent drive crate (IDC)
- Acquisition & Supervision crate
- LIN POT
- Wire, ESN, brake
- Position (Resolver)
- Power
- Ethernet
- Analog Interfaces FMC (AIF)
- VME FMC Carrier – High Density (VFC-HD)
- BWSVPA (V2) For powering the locking safety brake
  https://edms.cern.ch/item/EDA-03698-V2-0
- BWS LHC | Synch LIU ACQ and legacy mechanism | run 2023 | J.Emery