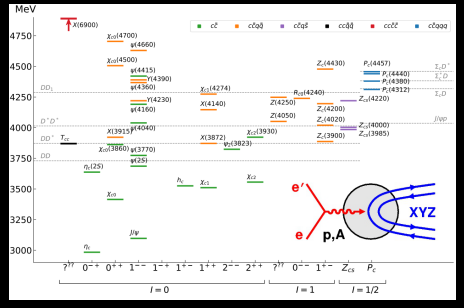
WP2 – Timepix

Glasgow: Simon Gardner, Derek Glazier, Ken Livingston, Dima Maneuski, ,Ross McGarrie
Daresbury: Mos Kogimtzis, James Lawson, Carl Unsworth

- Can we find a role for Timepix at EIC? Yes we can. It's the **Far Backward Tagger** (Low Q^2 Tagger).

Physics case - established



Design – well underway

Timepix4 for tracking

X. Llopart et al 2022 JINST 17 C01044

B. Bergmann, et al. NIM A, 2020. 978:164401

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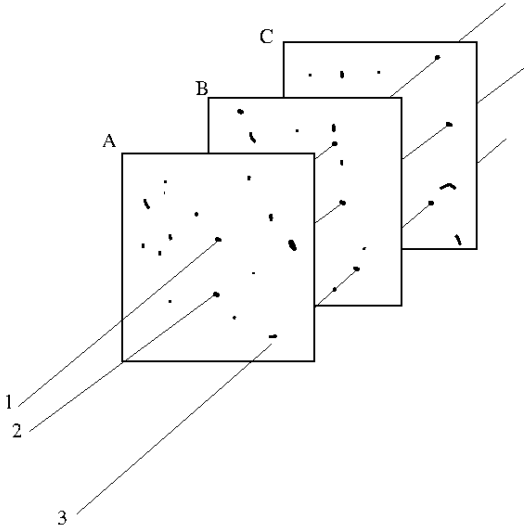
- **Calorimeter not required for Low Q^2 Tagger** – removed from simulation and design
- **What's required** of a pixel tracker?
- **Position resolution** good enough for physics needs (~50um adequate)
- **Segmentation** good enough to separate out tracks. (~50x50um pixels)
- **Vacuum compatibility**. Cooling. Readout. Beam impedance.
- **Rate capability**.
  - In a bunch crossing:
  - **~10 electrons tracks** from the interaction point almost all brem.
  - These are unrejectable! Need physics - exclusivity, kinematics …
  - 12ns between bunches => **pixel hit rate per layer = 2.5 GHz**
  - Assume same rate from synchrotron BG.
  - Total rate per layer = **5GHz**. At 64 bits per pixel = **320 Gb/s**. Very big. Timepix4 + SPIDR4 can do this.



  - Use **FPGA based clustering** to find MIPS. Store only MIPS clusters (x, y, time, energy, width) = 80 bits
  - 2 tagger, 4 layers, Trigger Rate 500kHZ => **Rate to DAQ = 3.2 Gb/s**. Very manageable.

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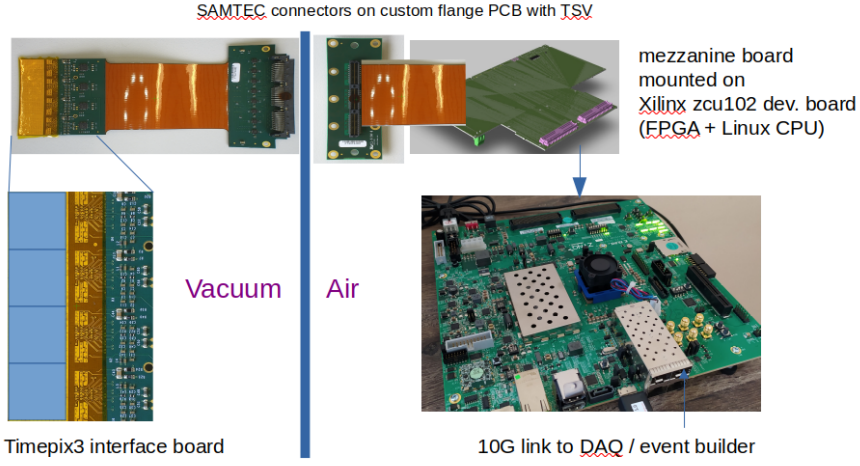
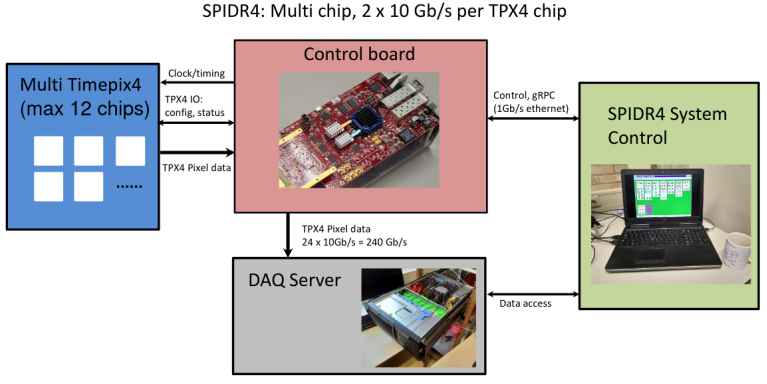
Timepix3



Developed by:
Glasgow Group: Ken Livingston, Dima Manuelski, Simon Gardner
Daresbury Group: Mos Kogimtzis, James Lawson, Carl Unsworth

Timepix4

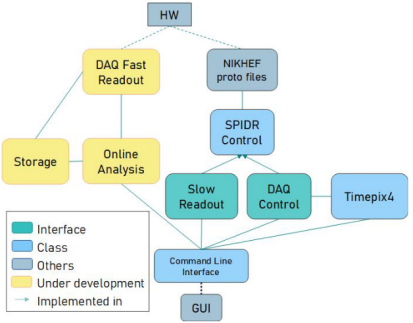


Martin Fransen (martinfr at nikhef.nl), Gridpix brainstorm April 2020 18

Availability of Timepix4 for tracking applications is driving hardware and software development.

SPIDR4 + DAQ tools look set to be the de facto standard
Closest to *off-the-shelf* technology

Build your own DAQ



You can use this software also with a hardware read-out system different from SPIDR4.
You only have to write the following 4 methods to:

- Read a Timepix4 Register
  - Operations to read a register through SC/I2C
  - Takes register address and returns vector of bytes
- Write a Timepix4 Register
  - Operations to write a register through SC/I2C
  - Takes register address and vector of bytes
- Configure the DAQ
  - Operations to configure the control board
  - Flexibility: desired configuration as xml file
- Read DAQ Monitoring Information
  - Operations to read back the control board
  - Flexibility returning configuration as xml file

N.V. Biesuz - Development of Readout Software for Timepix4-based Detectors - 16th November 2022 8

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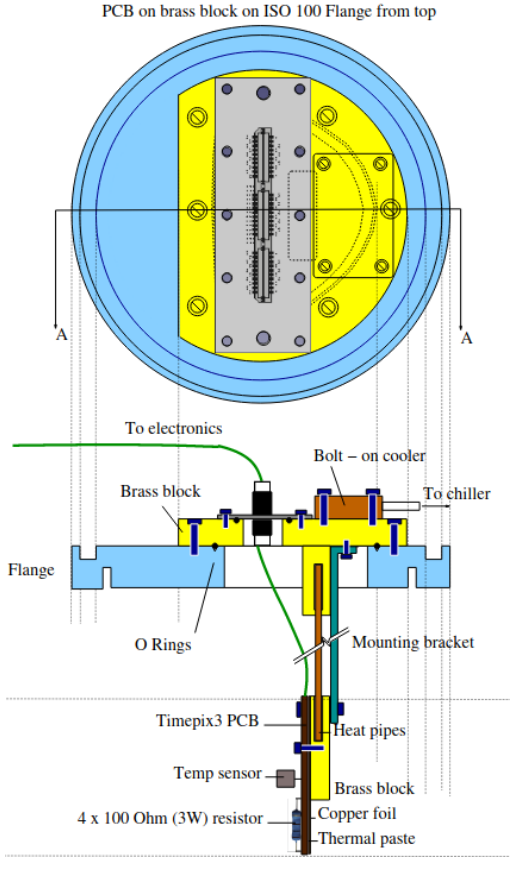
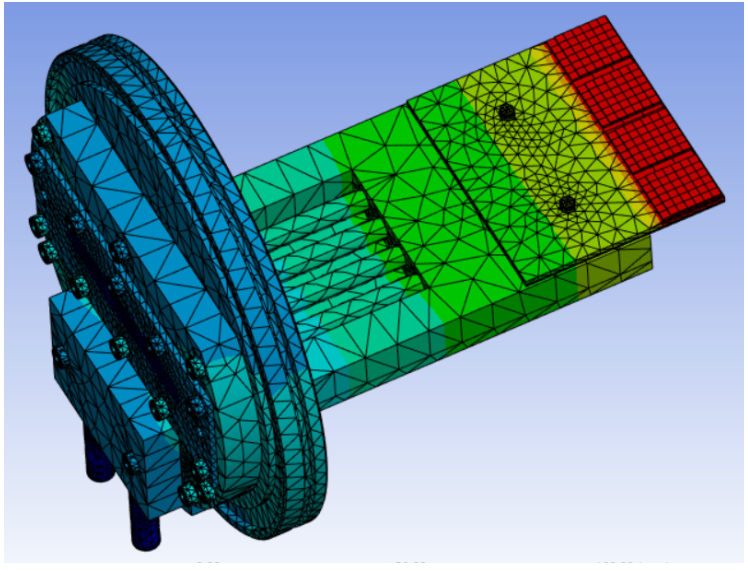
.. but timepix3 DAQ readout and test rig still essential for development



Real **connectors**, vacuum **feedthroughs**, **heat pipes**
PCB with **temp sensors**. **Resistors** to mock up ASIC heat.
Developed in CAD as **special flange** for ISO 100 mount.
Currently in Glasgow workshop.

To be tested in 10-5 mbar with **external mounted chiller**.
Cooling **modelled in ANSYS**.



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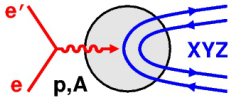
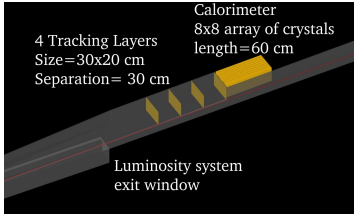
Summary

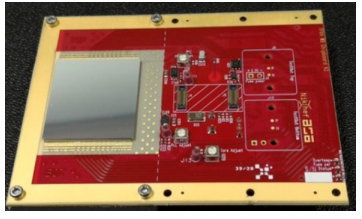
Strong physics case for low Q^2 tagger.



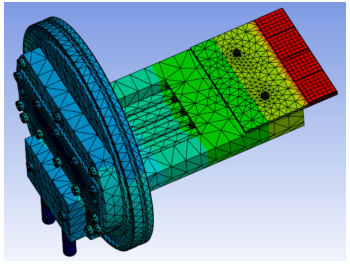
Design implemented needs more simulation and adjustment



Timepix4 + SPIDR4 looks like the best solution (but other options still being evaluated)



Development for structure, cooling, beamline
Continue with Timepix3 setup.



Links / Refs
Timepix4: X. Llopart et al 2022 JINST 17 C01044
SPIDR4: http://www.nikhef.nl/~s01/SPIDR4-MF-GP-apr2020.pdf
SPIDR4 DAQ: https://indico.cern.ch/event/1215762/contributions/5137274/