UNIVERSITY OF BIRMINGHAM

ePIC Vertex and Tracking Detector

L. Gonella

EIC UK Discussion Meeting

7 December 2022

Introduction

- The ePIC detector is evolving from the reference detector design though layout optimisations and technology updates.

- The ePIC vertex and tracking detector comprises silicon Monolithic Active Pixel Sensors (MAPS) closest to the interaction point and Micro-Pattern Gaseous Detectors (MPGD) further out.

- Two detector configurations have been prepared to be studied in the first ePIC simulations campaign that is ongoing.

- The Silicon Vertex and Tracking (SVT) detector is the same in both.
  - Different configuration of the MPGD layers, as well as of the systems beyond the tracker (calorimeters, PID, TOF).

Reference design and issues

- The reference detector was based on the ECCE proposal.

- A few issues were recognised early on for the vertex and tracking system:
  - 0.05% X/X0 assumed for sagitta layers at r = 21 and 23 cm, with 54 and 60 cm length, not feasible in practice.
  - Resolution and material budget for MPGD layers also not feasible in practice.
  - 1.5T magnetic field (BaBar magnet) not sufficient with realistic technology parameters.
  - Less than three hits per track at large eta in the electron going direction.
  - Lever arm in forward and backward regions could be larger.

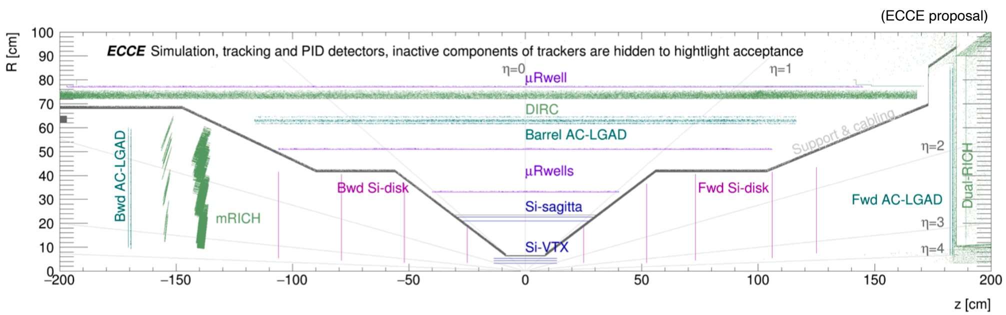


Figure 2.5: Schematic view of the ECCE tracker, including silicon, μRWELL, AC-LGAD, DIRC, mRICH and dRICH detector systems.

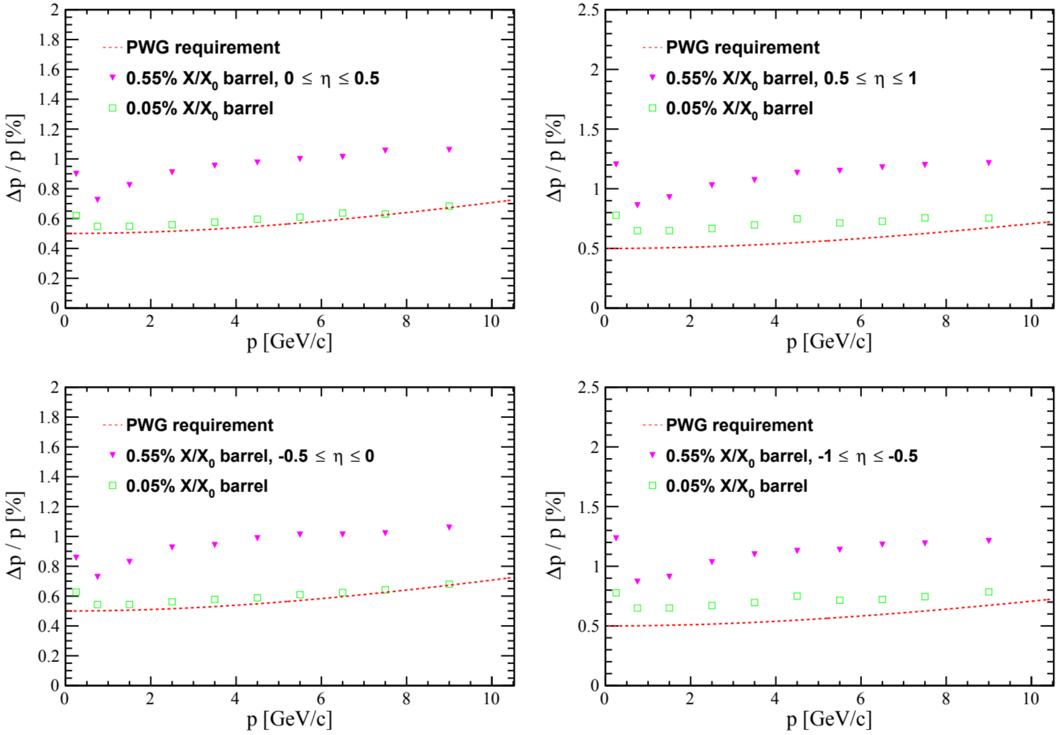
Barrel index	R (cm)	z_{min} (cm)	z_{max} (cm)
1	3.3	-13.5	13.5
2	4.35	-13.5	13.5
3	5.4	-13.5	13.5
4	21.0	-27	27
5	22.68	-30	30

H-endcap index	z (cm)	r_{in} (cm)	r_{out} (cm)
1	25	3.5	18.5
2	49	3.5	36.5
3	73	4.5	40.5
4	106	5.5	41.5
5	125	7.5	43.5

e-endcap index	z (cm)	r_{in} (cm)	r_{out} (cm)
1	-25	3.5	18.5
2	-52	3.5	36.5
3	-79	4.5	40.5
4	-106	5.5	41.5

Example of reference detector issues

- Reference detector with updated material estimates for sagitta layers.
  - 0.05 % → 0.55% X/X0, conservative estimate.
- Large dp/p degradation at central rapidity → Optimisations necessary to recover momentum resolution at mid-rapidity.

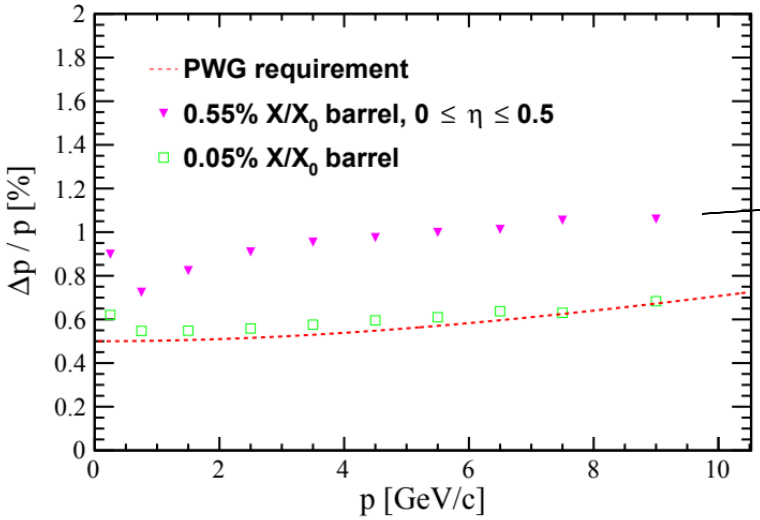


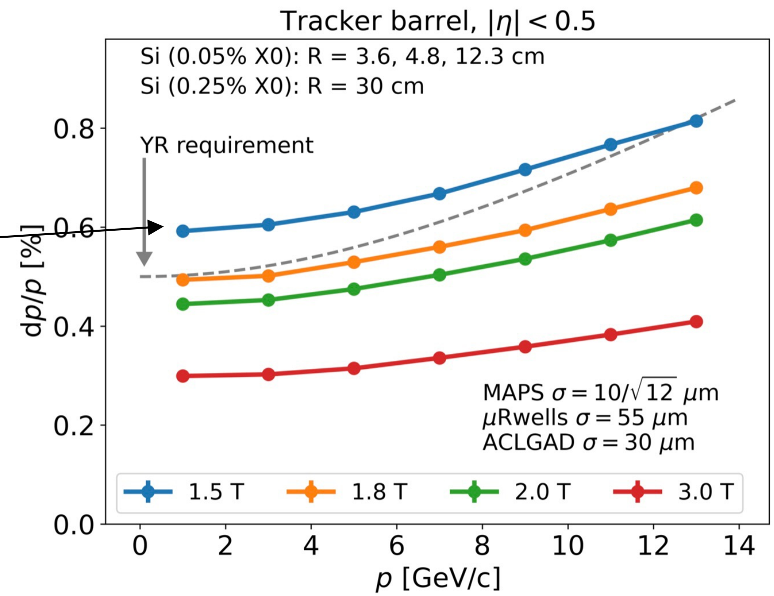
Plots by Stephen Maple (UoB)

Example of reference detector issues

- Some initial reconfiguration of the barrel layers showed momentum resolution could be regained with different radii and lengths but without a higher magnetic the YR requirement could not be satisfied.

- At this point the EIC project decided to design a new magnet that could go up to 1.7T.





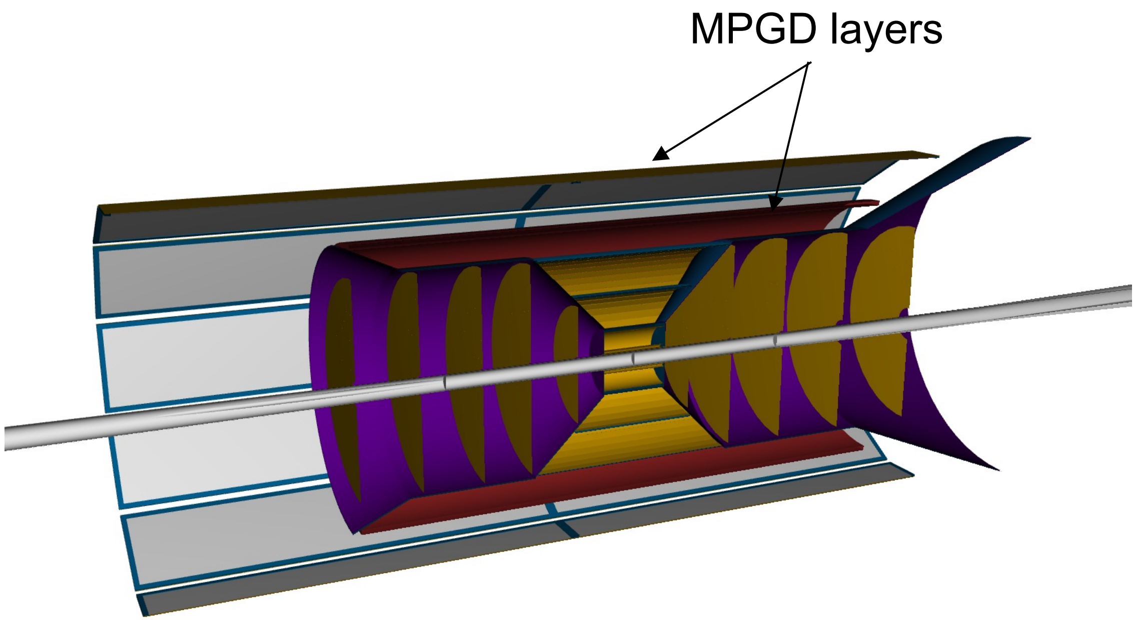
Plot by Rey Cruz-Torres (LBNL)

Current ePIC SVT configuration

- The ePIC SVT layout developed for the first simulation campaign has 5 barrel layers and 5 disks per side.

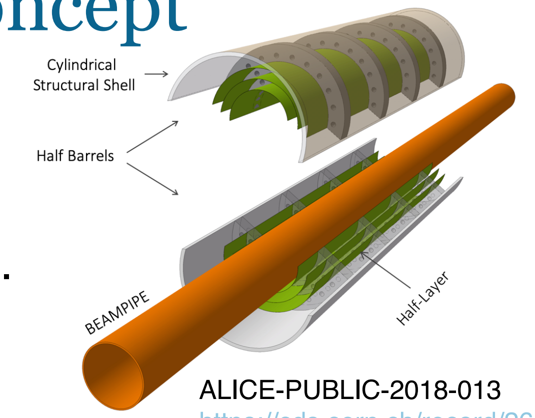
BARREL	r [mm]	l [mm]	X/X0 %
Layer 0	36	270	0.05
Layer 1	48	270	0.05
Layer 2	120	270	0.05
Layer 3	270	540	0.25
Layer 4	420	840	0.55

DISKS	+z [mm]	-z [mm]	X/X0 %
Disk 1	250	-250	0.24
Disk 2	450	-450	0.24
Disk 3	700	-650	0.24
Disk 4	1000	-900	0.24
Disk 5	1350	-1150	0.24



In between the MPGD layers there are a TOF layer and the DIRC, not shown here. Support cone shown in purple.

Reminder of the overall ePIC SVT concept



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611

- ePIC SVT detector concept based on 65 nm MAPS.
- Leading development of this technology: ALICE ITS3.
  - Truly cylindrical vertex detector with 0.05% X0.
  - Stitched, wafer scale sensors.
  - Thinned and bent around the beam pipe.
  - Mechanics and services outside active area.
  - Air cooling with low power sensor design in 65 nm.
- The EIC sensor requirements are in line with the ITS3 sensor specifications → The EIC sensor is based off the ITS3 sensor.

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	$< 10^{-7}$ event/pixel	$< 10^{-7}$ event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

- The ultra low mass ITS3 vertex layers concept is very attractive for the EIC.
- The timelines of the two projects are well aligned. ITS3 TDR schedule and EIC CD-2/3A review schedule on the same timescale.

Reminder of the overall ePIC SVT concept

- ITS3-like vertexing layers.
  - Re-use ITS3 sensor as is.
  - Adapt ITS3 detector concept to the EIC radii.
    - Mechanics of bent layers needs specific development for EIC.

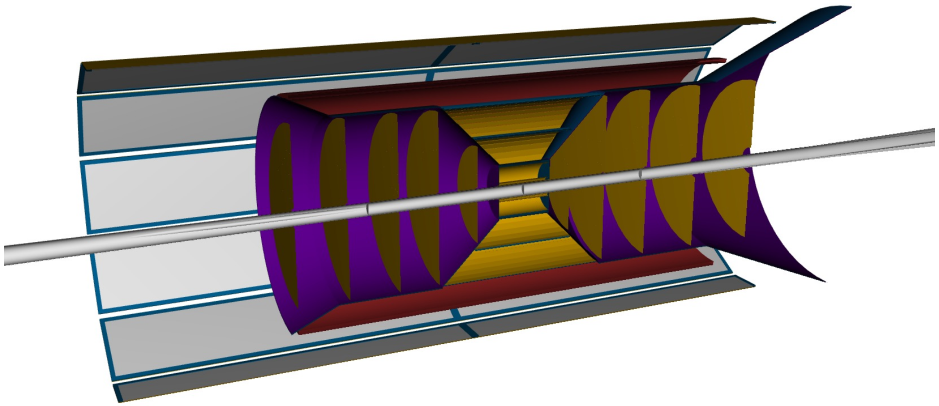
- EIC variant for the staves and disks.
  - EIC Large Area Sensor (LAS), i.e. ITS3 sensor size optimised for high yield, low cost, large area coverage.
    - EIC LAS will be stitched, but not wafer scale. Functionality and interfaces stay the same as the ITS3 sensor.
    - Size(s) of the EIC LAS to be defined based on yield of stitching process and requirements for full coverage.
  - Convectional carbon fibre support structures with integrated cooling.

Vertex and sagitta layers optimisations

- Vertex layers:
  - Radii of two innermost vertex layers optimised for beam pipe bake out (5 mm clearance required) and ITS3 sensor size.
  - 3rd vertex layer moved at r = 120 mm, dual purpose vertexing & sagitta layer, without increase in material (i.e. 0.05% X/X0, bent layer).

- Sagitta layers:
  - Moved at larger radii to increase lever arm with high precision measurements to improved momentum resolution.
  - Layer at 27 cm to be constructed in two halves of 0.25% X/X0.

BARREL	r [mm]	l [mm]	X/X0 %
Layer 0	36	270	0.05
Layer 1	48	270	0.05
Layer 2	**120**	270	**0.05**
Layer 3	**270**	540	**0.25**
Layer 4	**420**	840	0.55

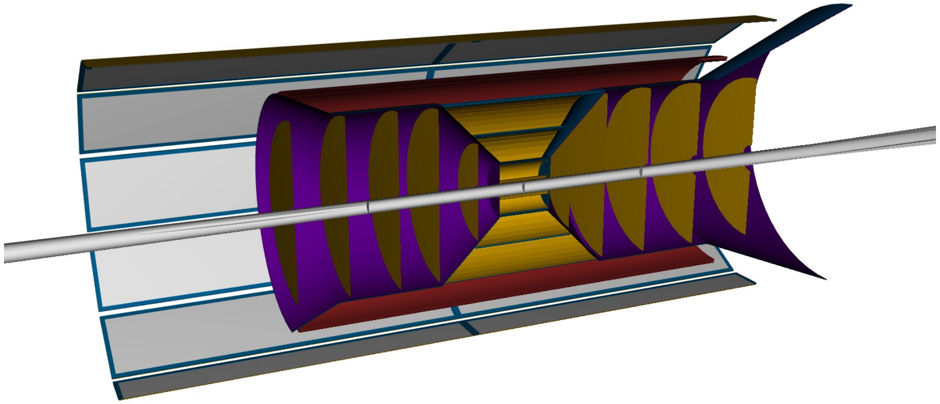


Disks optimisations

- Number of disks in the electron direction increased to improve acceptance at high eta/increase number of points on track.
  - At |eta| >= 3 in the electron going direction, hits on three disks only in reference detector. Insufficient considering noise and inefficiency.

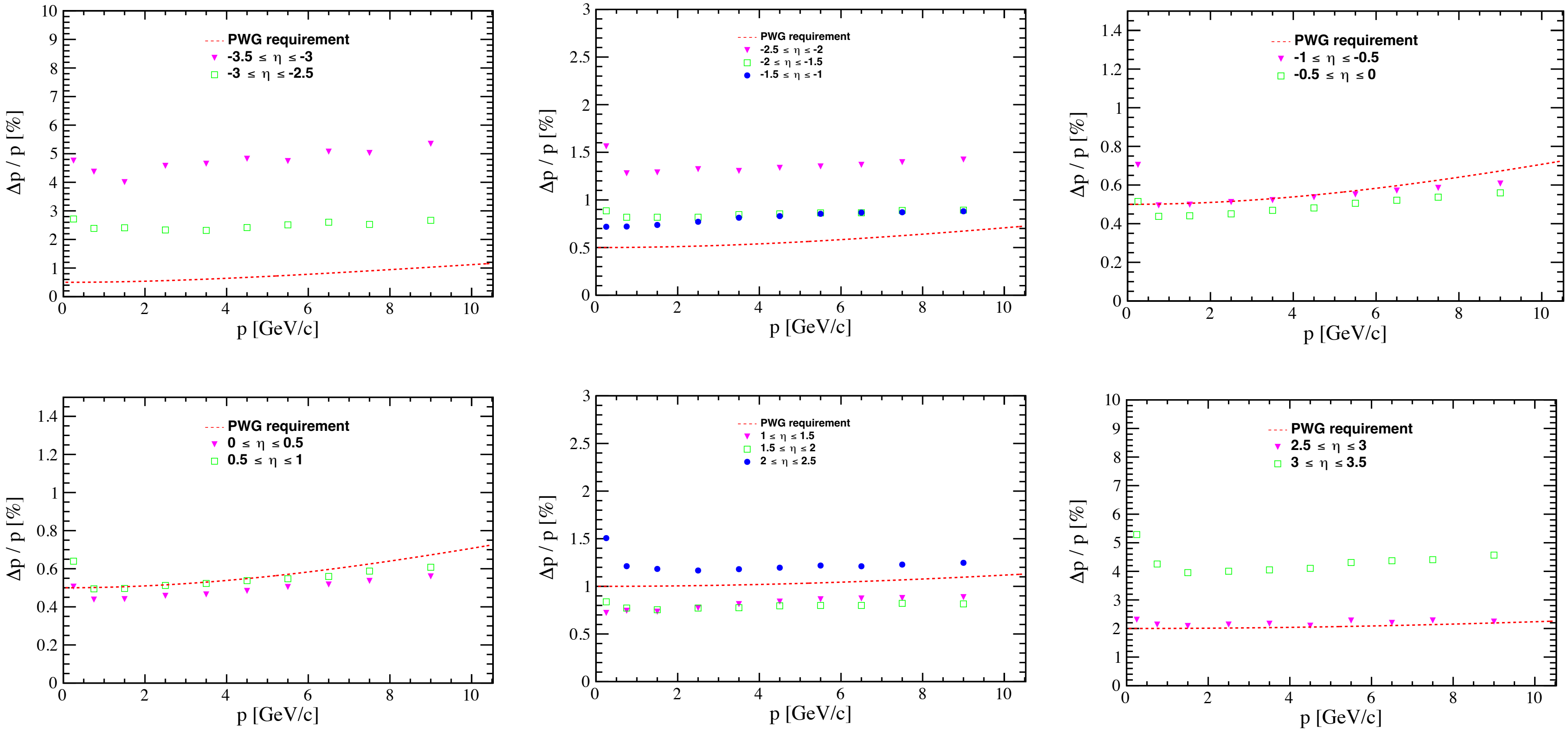
- Use all available space in z to increase lever arm.
  - The table below show the current layout implemented in simulation. This is the envelop assuming the pfRICH in the electron going direction. The disk design can be symmetric if the mRICH is used (i.e. envelop on electron side up to ~1350 mm).

DISKS	+z [mm]	-z [mm]	X/X0 %
Disk 1	250	-250	0.24
Disk 2	450	-450	0.24
Disk 3	700	-650	0.24
Disk 4	1000	-900	0.24
Disk 5	**1350**	**-1150**	0.24



Momentum resolution

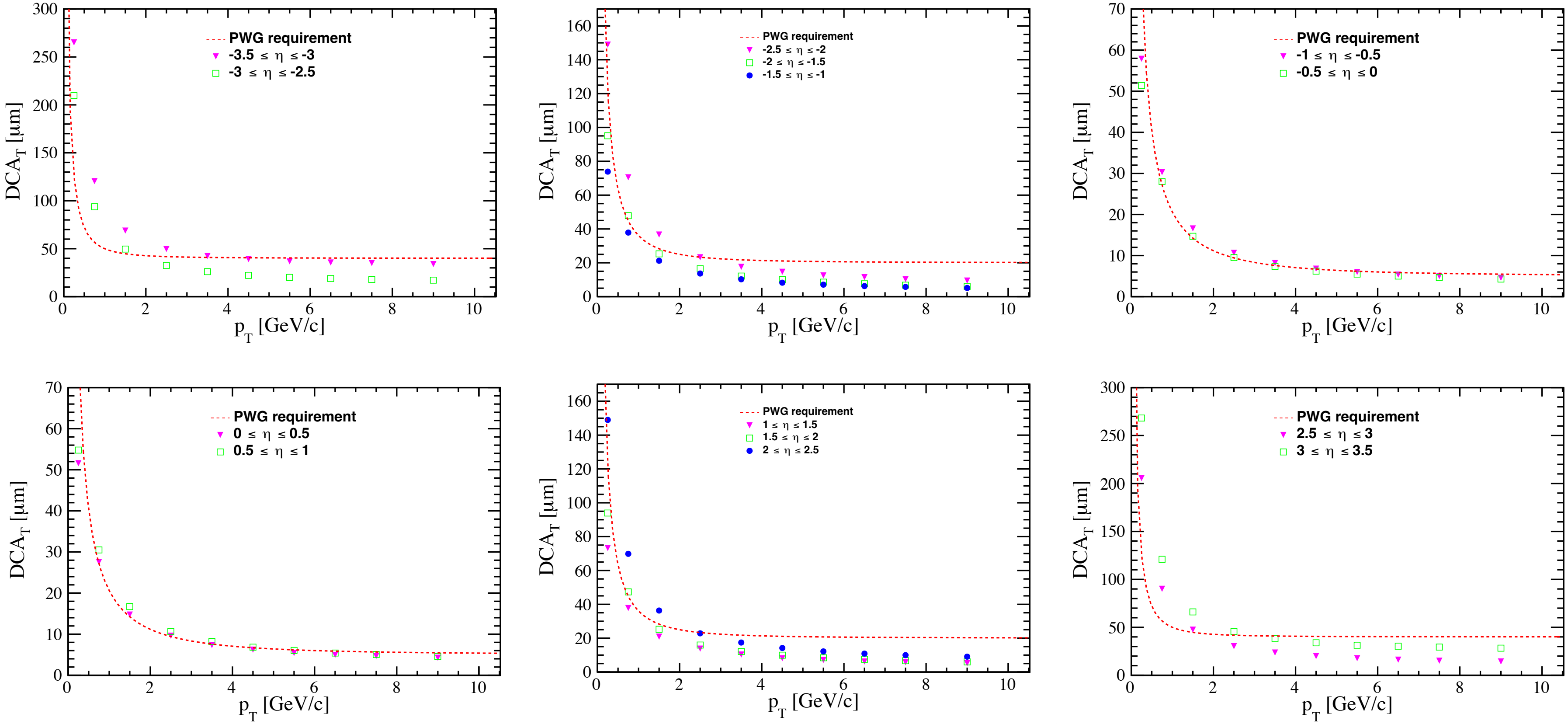
- Momentum resolution met in central and most of the forward eta regions; still challenging in the backward regions.



Plots by Stephen Maple (UoB)

Vertex resolution

- Vertex resolution (quantified with transverse DCA here) met at p_T > ~3 GeV everywhere.
- At low momenta, requirements not met at large pseudorapidity in both directions.



Plots by Stephen Maple (UoB)

ePIC SVT R&D programme

- R&D for the EPIC detector is carried out by the EIC Silicon Consortium in the framework of EIC project directed eRD104, eRD111, eRD113 activities.

- eRD104 Services reduction – Investigate methods to significantly reduce the services load for an EIC MAPS based tracking detector.
  - Powering system → **UK participation in-kind.**
  - Readout system.

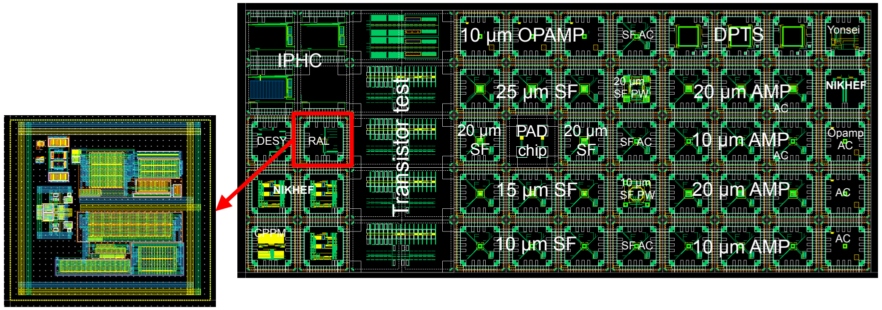
- eRD111 Si tracker – Development of a full tracking detector solution composed of next generation 65 nm MAPS sensors.
  - Forming modules from stitched sensors.
  - Barrel & discs → **UK participation in-kind.**
  - Mechanics, integration, & cooling.
- eRD113 Sensor – Development of the EIC MAPS sensor – **NEW IN FY23.**
  - Sensor design → **UK participation in-kind.**
  - Sensor characterisation → **UK participation in-kind.**

Highlights of UK R&D activities

MLR1 designs from RAL (Q4 2021)

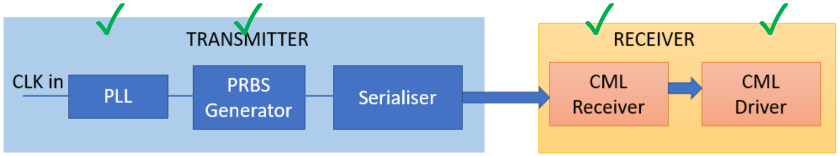
- First submission in TPSCo 65 nms, scoped within CERN EP R&D WP1.2
- Significant drive from ITS3, contributions from several groups
- Technology exploration and prototype circuit blocks for future sensors

RAL: LDVS receiver and CML transmitter



ER1 designs from RAL (Q4 2022)

- Functional blocks for high-speed data transmission (PLL dual mode 1 GHz/ 7 GHz PRBS Generator, CML Receiver)



- I2C block for on-chip data transmission
- Plus, redesigned standard cells for DFM

ER2 Plans

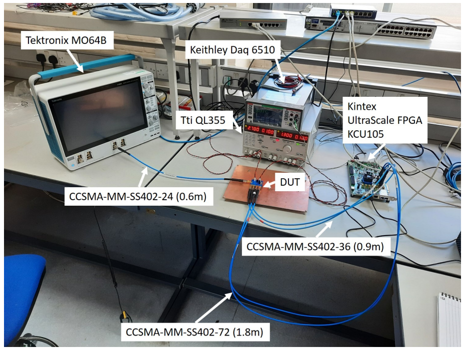
- Port Serialiser design in 180 nm to 65 nm
- Developing regulators to explore serial and DC-DC based powering options

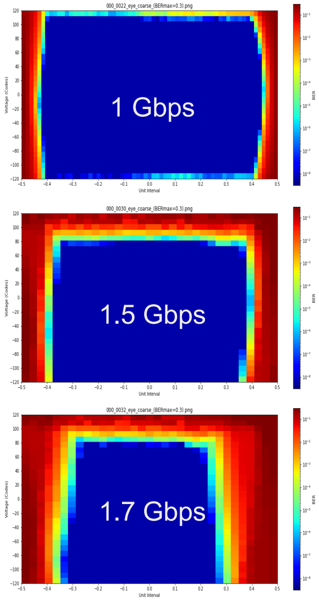
RAL is the only EIC designer group working on sensor design so far.

Highlights of UK R&D activities

MLR1 – RAL IP Block

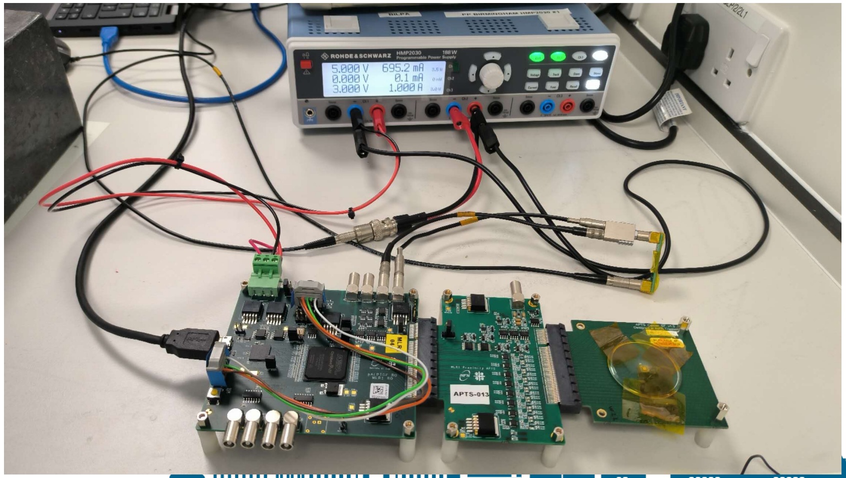
- New test setup developed by DL/RAL TD.
- Chips bonded at BHM/LIV, tested at BHM/DB.
- Circuit works up ~1.5 Gbps.
- X-ray irradiations carried out at CERN up to ~10 Mrad at two dose rates (Sep 22)





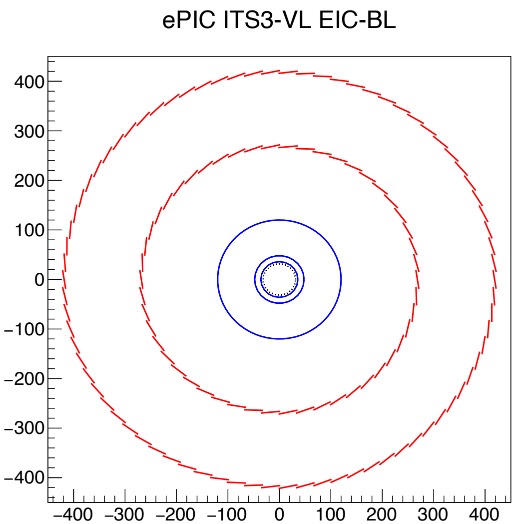
MLR1 – APTS / DPTS

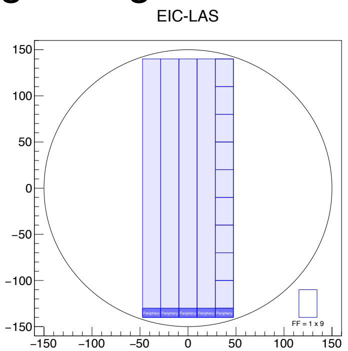
- MLR contains Analogue Pixel Test Structures (APTS) and Digital Pixel Test Structures (DPTS) designed by ITS3 groups.
- BHM/LIV contributing to APTS to bonding of chips for ITS3 institutes.
- Both institutes have now received and commissioned APTS test setups.
- Expect to receive DPTS test setups for DL and RAL next year.

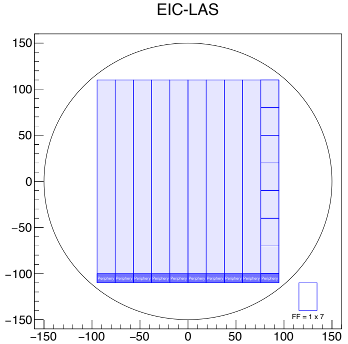


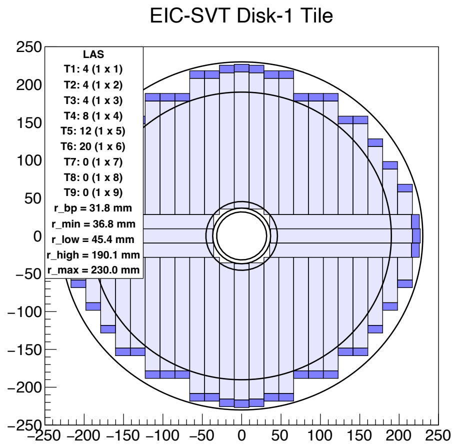
Highlights of UK R&D activities

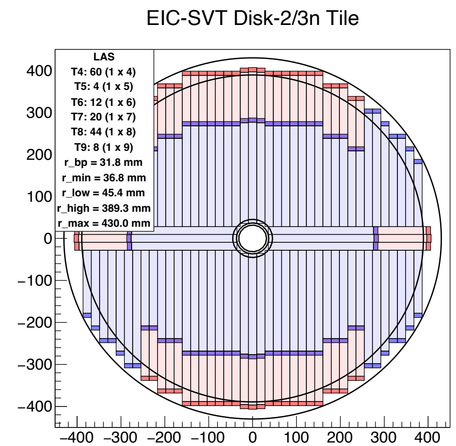
- Conceptual study of LAS size for staves and disks well advanced → Baseline configuration for ePIC SVT defined based off these studies and the current ePIC layout (see https://indico.bnl.gov/event/17713/)
  - Tiling of vertex and barrel layers considers re-use of ITS3 sensor and maximisations of wafer surface usage.
  - Macro developed to study best LAS configuration for disks. Multiple sensor formats needed, requiring changes to stitching plan & organisation of the digital periphery.











Conclusion

- The ePIC detector configuration is evolving from the reference design with inputs from performance simulations and R&D.

- The ePIC SVT has currently reached a first optimised implementation to be studied in the ePIC first simulation campaign and to kick-off R&D activities.

- R&D activities on sensor development, engineering aspects and conceptual designs expected to take off and progress significantly in FY23.

- **Significant UK contributions, well aligned with the programme and visible in the collaboration.**

Backup

Current ePIC detector configurations

detector region	option A	option B	notes
all	"standard" Si tracker system (layers: 5 in barrel; 5 disks in FW; 5 disks in BW)		if possible, converge towards 1 single configuration with 1 single envelop
barrel	2 MPGD layers (1 behind DIRC; first layer at 55 cm)	1 MPGD layer (in front of the DIRC)	option B more consistent with imaging Ecal
FW	no MPGD behind the RICH		
barrel	"standard" DIRC		
FW	"standard" dRICH		not realistic to elaboirate two different optics by mid October
BW	mRICH	pfRICH	pfRICH shorter than in ATHENA: ~45 cm in total
FW/BW	standard Ecal and Hcal	standard & insert in the FW Ecal	status of implementation in gloal simulation: advanced; about inseret, to be used in October simulation if a preliminary mechanical support will be designed
barrel	SciGlass Ecal	imaging Ecal (same inner radius, 21 X0)	thicker imaging Ecal if supported by preliminary studies
barrel	HCAL outside	HCAL outside	implementation in progress
BW	no		BW ToF layer simulated if intregration in the the detector layout possible (second priority)
FW	ToF layer (15 cm; 8% X0; pixel 0.5*0.5 mm^2)		X0 correlated to resolution
barrel	ToF layer (1 % X0; strips)		X0 correlated to resolution
FFW/FBW	"standard"		implementation advanced; some open points in B0; ZDC is the "ATHENA" one;
field map	1.7 T scaled from BaBar magnet		

Vertex and tracker system

PID detectors

Calorimeters

TOF system

Far forward/backward detectors

Magnetic field

Where is the ePIC SVT work done?

- ePIC tracking WG: detector layout optimisation via simulations.
  - Weekly meetings on Thursday at 4:00 pm UK time.
  - Indico https://indico.bnl.gov/category/404/
  - Mailing list https://lists.bnl.gov/mailman/listinfo/eic-projdet-tracking-l

- EIC Silicon Consortium: technology development.
  - By-weekly meetings on Monday at 5:30 UK time.
  - Indico https://indico.bnl.gov/category/386/
  - Mailing list https://lists.bnl.gov/mailman/listinfo/eic-rd-silicon-l

EIC Silicon Consortium

- The overarching goal of the EIC Silicon Consortium is the development and construction of a full tracking and vertexing detector subsystem for the EIC detector(s) based on 65 nm MAPS sensors.

- The EIC silicon consortium grew out of the "eRD25: Silicon Tracking and Vertexing Consortium" project (LBNL/RAL/UoB), part of the former EIC Generic Detector R&D program (2011- 2021).
  - Expand scope of the work and build the critical mass to deliver the EIC SVT.

- R&D for the EPIC detector is carried out by the EIC Silicon Consortium in the framework of EIC project directed eRD104, eRD111, eRD113 activities.
  - This programme started in FY22 (note: US financial year Oct. to Sept.).

- Note: the EIC SC also works on generic R&D for EPIC upgrades/further optimisations and/or for a second detector.
  - Proposal submitted to the new Generic EIC-related Detector R&D Program starting this year (FY23).

EIC SC institutes

eRD104

Table 1: Institutions involved and institutional contacts

Topic	Institute	Institutional contact
Powering System	Birmingham	Laura Gonella
	RAL	Fergus Wilson
Readout System	ORNL	Jo Schambach
	BNL	Grzegorz Deptuch

eRD111

Topic	institute involved	institute contact
modules	INFN groups UK institutes (Birmingham, Daresbury, Lancaster, Liverpool)	Giacomo Contin Roy Lemmon, Peter Jones
barrel & discs	LANL LBNL ORNL UK institutes (Birmingham, Daresbury, Lancaster, Liverpool)	Walter Sondheim Nicole Apadula Ken Read Roy Lemmon, Peter Jones
mechanics, infrastructure, & cooling	LANL LBNL ORNL	Walter Sondheim Nicole Apadula Ken Read

eRD113

Table 4: Institutions involved and institutional contacts

Topic	Institution	Institutional contact
Sensor Development	RAL	Iain Sedgwick
	BNL	Grzegorz Deptuch
	LBNL	Carl Grace
Sensor Characterization	INFN	Domenico Elia
	UK institutes	Laura Gonella
	LBNL	Yuan Mei
	ORNL	Jo Schambach
	LANL	Xuan Li

Status of R&D

- EIC SC activities have so far progressed quite slowly for a number of reasons.
  - Lack of/delayed funding in the US.
  - A number of unknown about the detector layout and sensor technology.
  - UK funding available earlier but long recruiting time, critical mass only just established.

- The plan for FY23 includes the rollover of the FY22 activities with expansion to account for the accelerated timeline in preparation for the project TDR.
  - R&D activities are expected to take off at US labs with significant funding arriving soon for FY23.
  - Baseline configuration for ePIC SVT defined to kick off all activities.

- The combined aim of eRD104/111/113 for FY23 is to
  - Be ready to design the LAS sensor in FY24.
  - Reach a mature conceptual design of all items of the ePIC SVT (supported by prototyping/testing of components).

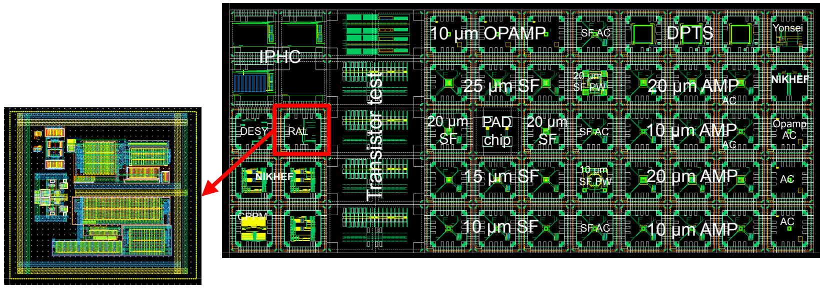
eRD113 - Sensor development

- Sensor development done by EIC groups in collaboration with ITS3.

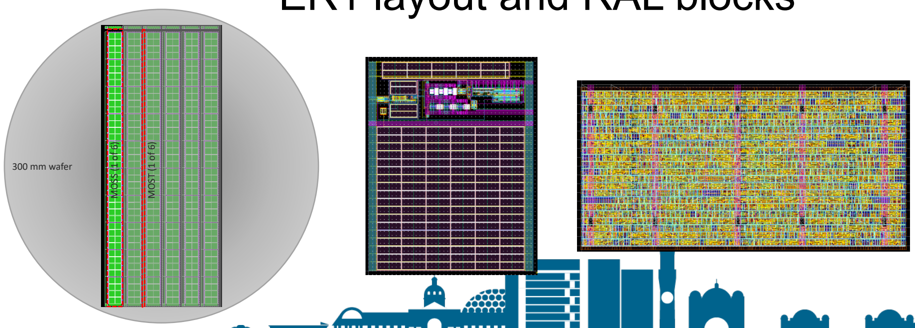
- Sensor design **(Iain, Soniya)**
  - RAL contributed IP blocks to both MLR1 (Q4 2021) and ER1 (Q4 2022).
  - RAL is the only EIC designer group working on sensor design so far.

- Sensor characterisation **(James, Jian, Jonathan, Long, Marcello)**
  - MLR1 APTS and DPTS testing starting at EIC institutes. Setups received at BHM, LIV, LBNL, ORNL, INFN.
  - MLR1 IP block tested by BHM, DB, RAL.
  - MLR1 and ER1 setup development planned at LBNL and ORNL.

MLR1 layout and RAL block



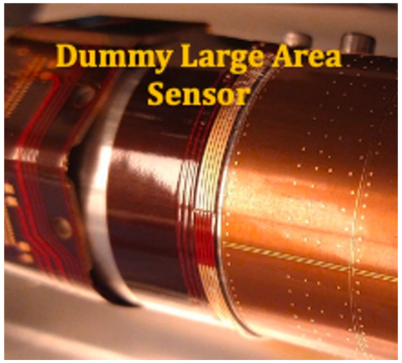
ER1 layout and RAL blocks

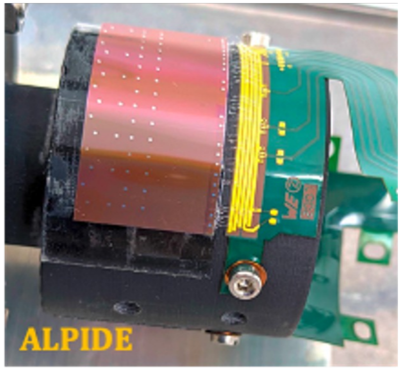


eRD111 – Modules, barrel & disks, mech & cooling

- Conceptual study of LAS size for staves and disks well advanced **(Peter)** → Baseline configuration for ePIC SVT defined based on these studies and the current ePIC layout.
  - To be released to the EIC SC at the general meeting on Mon 7 Nov.

- Mechanical studies on single-reticule sensors & large-size MAPS at INFN.
  - Bending, thinning, & interconnection.
  - Characterization in flat & curved geometries.
  - Bending & wire-bonding have been successfully exercised at EIC vertex radii.



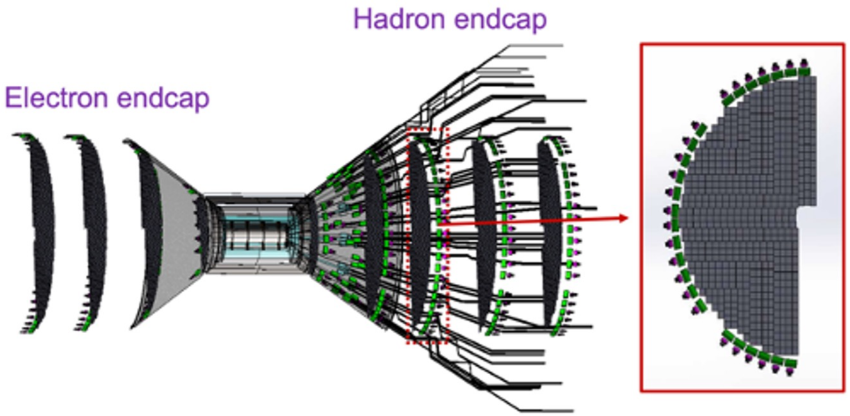


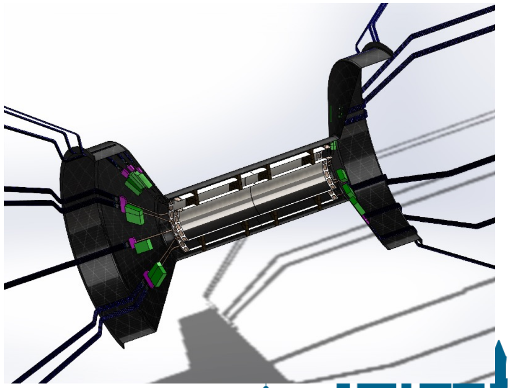
eRD111 – Modules, barrel & disks, mech & cooling

- Initial study of (internal) air cooling as an option for staves & discs at LBNL.
  - Summer student project.
  - Different carbon foam types/thicknesses under evaluation.

- Starting assessment of materials for making discs & supports at LANL.

- CAD modelling continues following on from detector proposals at LANL and JLAB.
  - CAD also used to explore different sensor & stave configurations and to study minimization of material minimization.





eRD104 – Powering & readout systems

- Powering work by UK groups **(Fergus, Iain, Laura, Soniya)**
  - Review of existing serial powering and DC-DC converter based powering schemes completed based on large experience within ATLAS.
  - Serial powering and DC-DC conversion with integrated regulator identified as the most promising candidates for the EPIC SVT.

- Readout work at ORNL.
  - Possible candidates for radiation tolerant FPGA and optical interconnect, and electrical/optical interface identified.
    - Microchip PolarFire FPGA, CERN “lpGBT”, Samtec optical “FireFly”.
  - An initial exercise to estimate number of hits and links in the detector has started to be updated in line with the evolving EPIC configuration.