CMOS sensors for vertex detectors

Francesca Carnesecchi

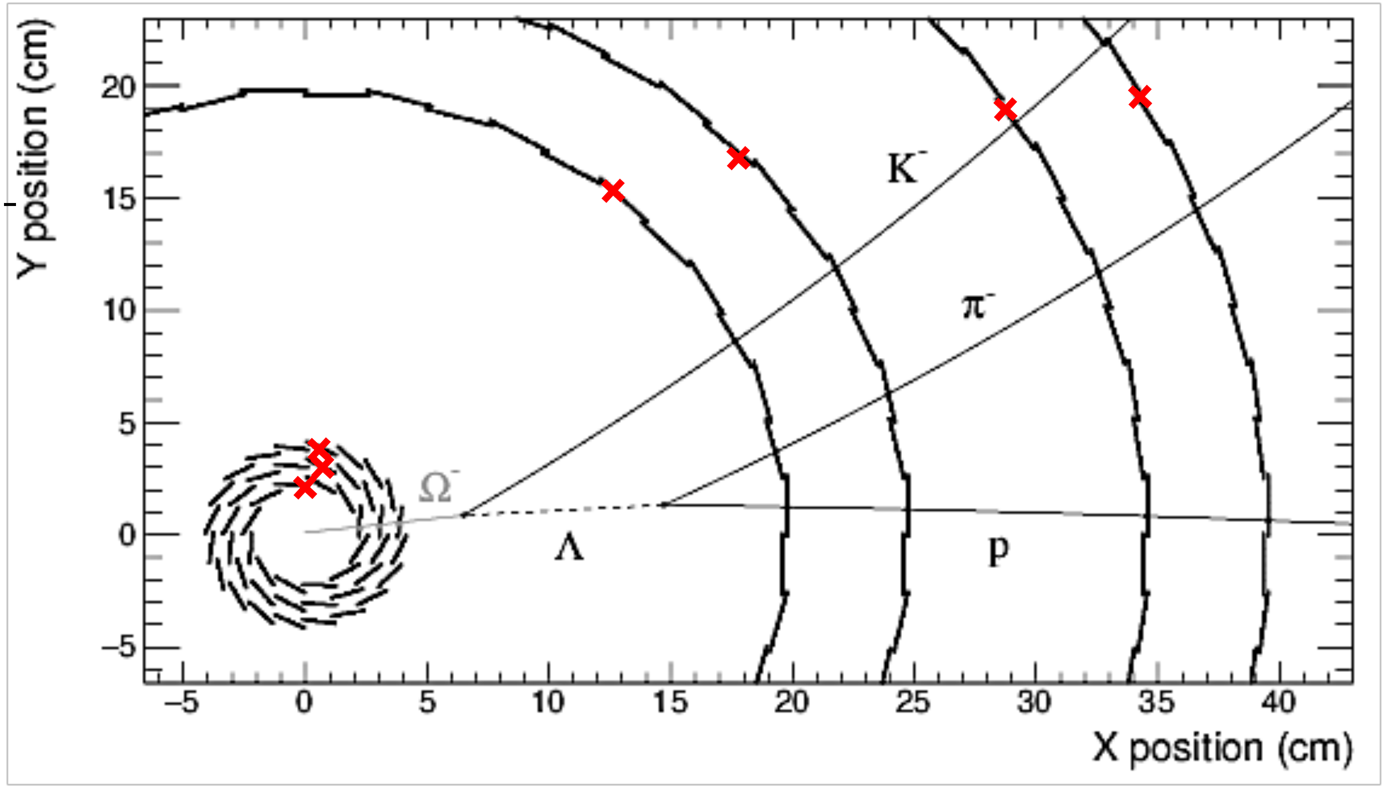
24th April 2023, Zurich

Reconstruct a charged particle track

Reconstruct a charged particle track to understand underlying physics processes in HEP, for precise studying or seeking signs of new physics.

In HEP experiments:

1. **Trajectory of charged particles:**
   - pattern recognition and identification of particle tracks at large background and pile-up levels



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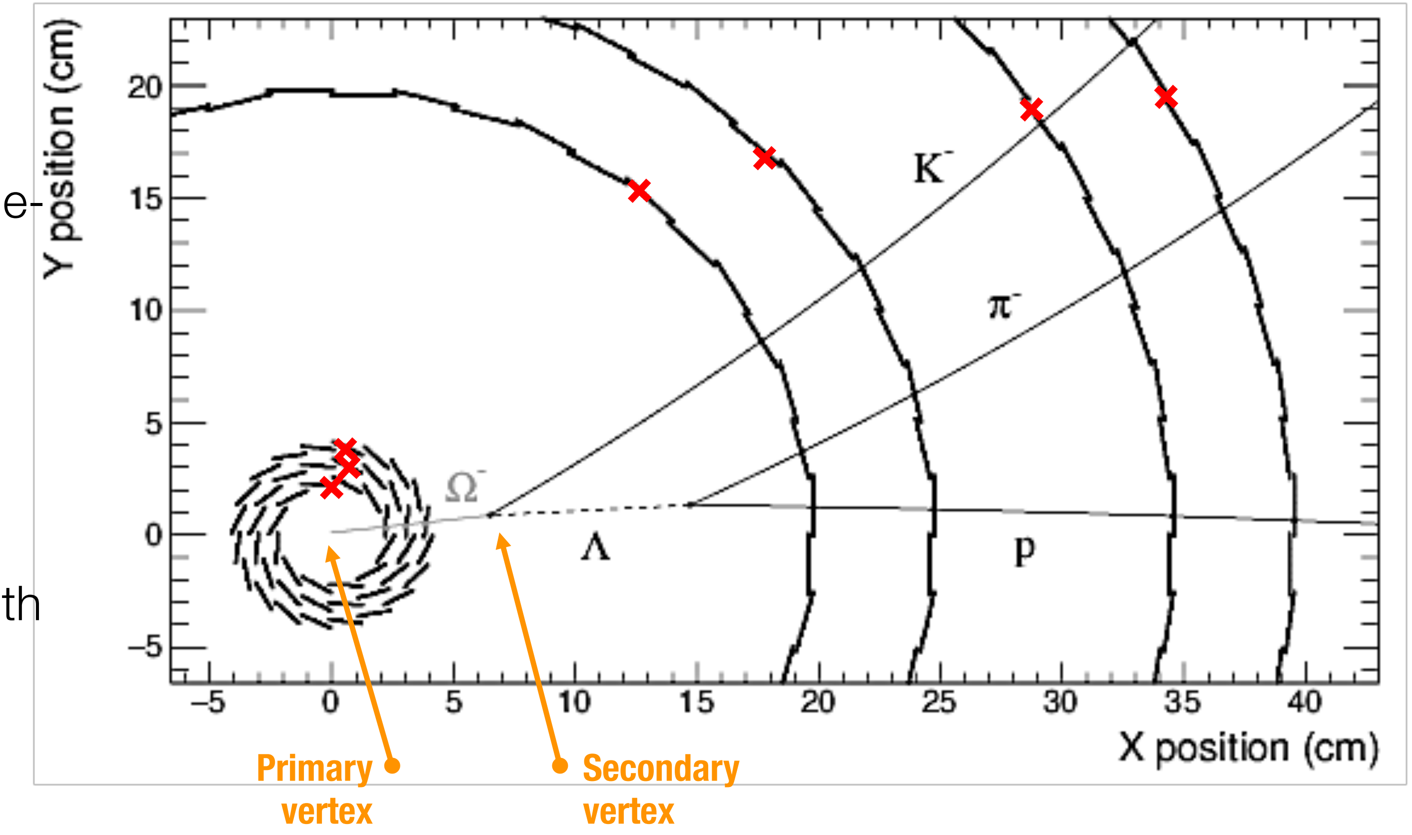
2. **Extrapolate tracks to the origin**
   - **Primary vertices** position
   - Find **secondary vertices**
3. **Momentum measurement of particles** (resolution depends on detector space resolution, number of tracking layers, total length of tracker, bending field and material budget)
4. Measurement of specific ionization



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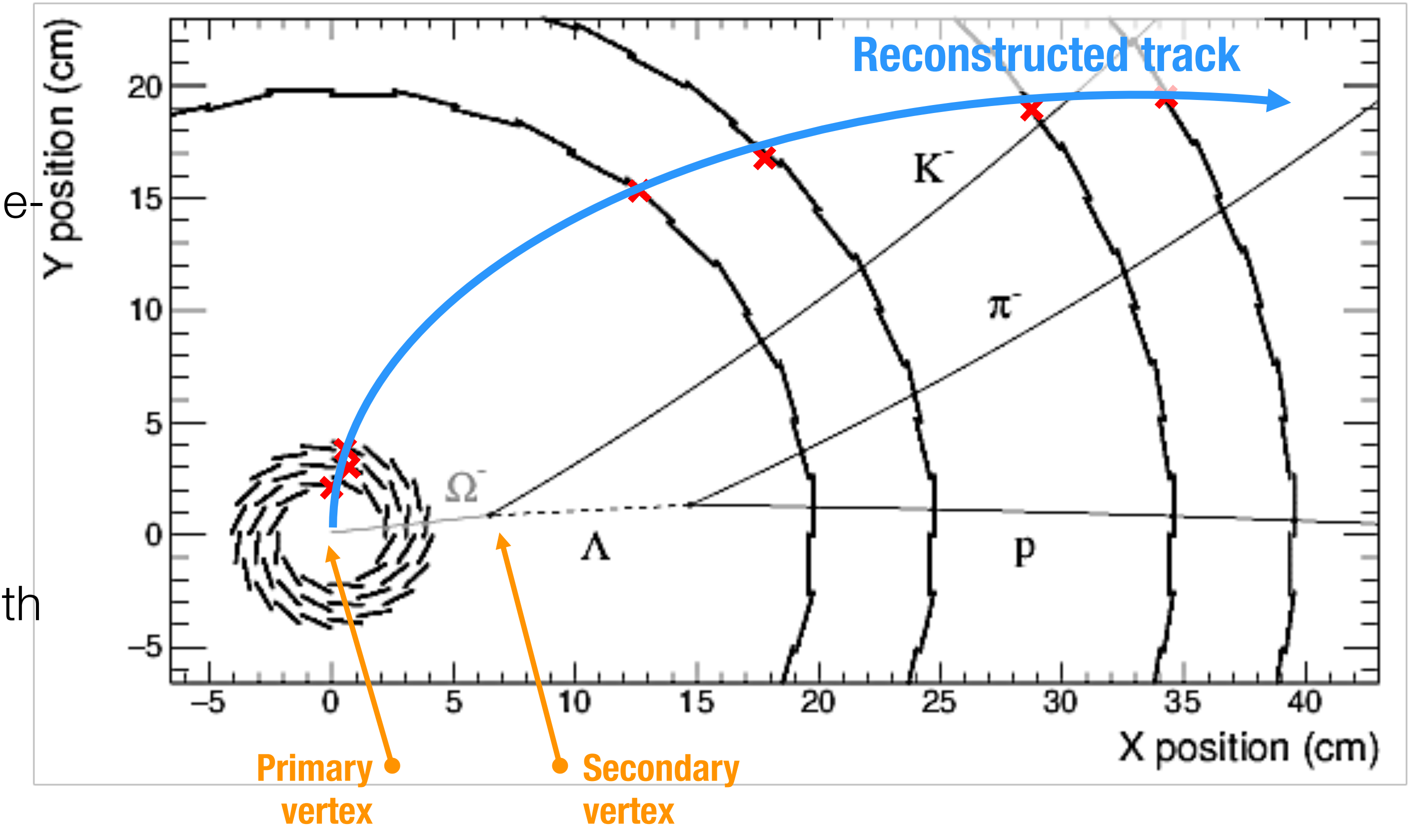
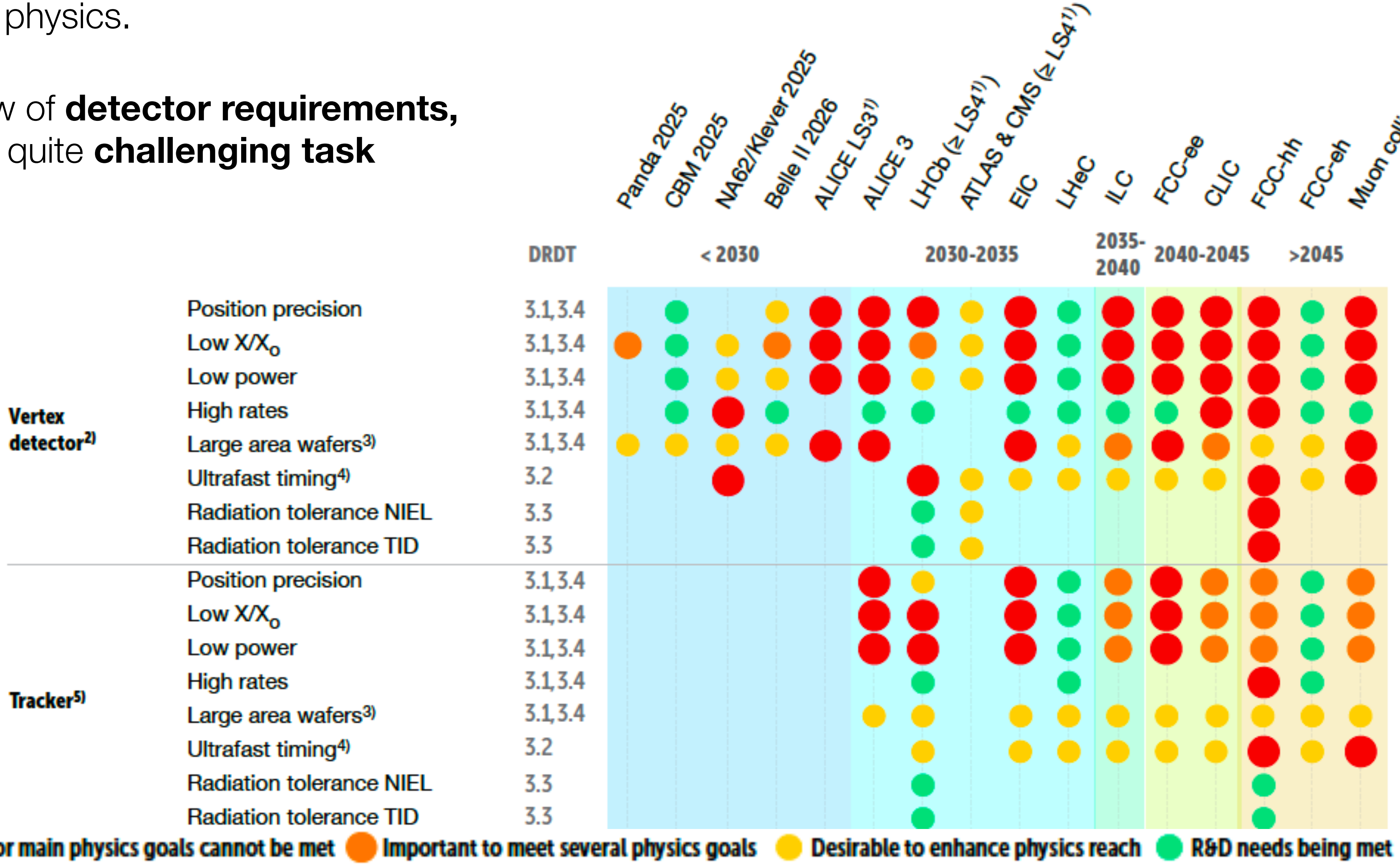


Reconstruct a charged particle track

Reconstruct a charged particle track to understand underlying physics processes in HEP, for precise studying or seeking signs of new physics.

From the point of view of **detector requirements,** **finding vertices** is a quite **challenging task**



		DRDT	Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3$^{1)}$	ALICE 3	LHCb (≥ LS4$^{1)}$)	ATLAS & CMS (≥ LS4$^{1)}$)	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
			< 2030					2030-2035					2035-2040	2040-2045		>2045		
Vertex detector$^{2)}$	Position precision	3.1, 3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X$_0$	3.1, 3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1, 3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1, 3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers$^{3)}$	3.1, 3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing$^{4)}$	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker$^{5)}$	Position precision	3.1, 3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X$_0$	3.1, 3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1, 3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1, 3.4							🟢			🟢				🔴	🟢	
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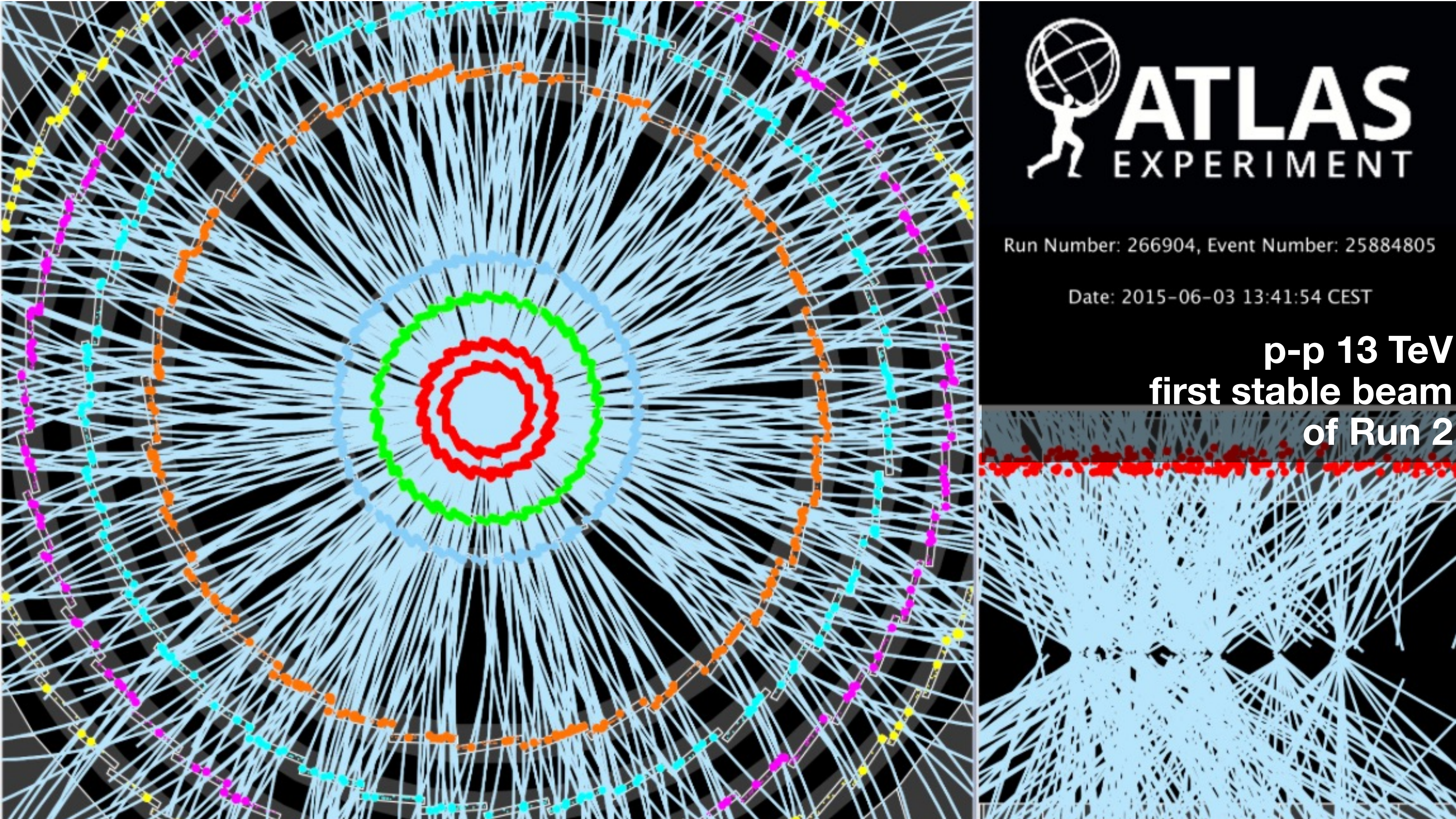
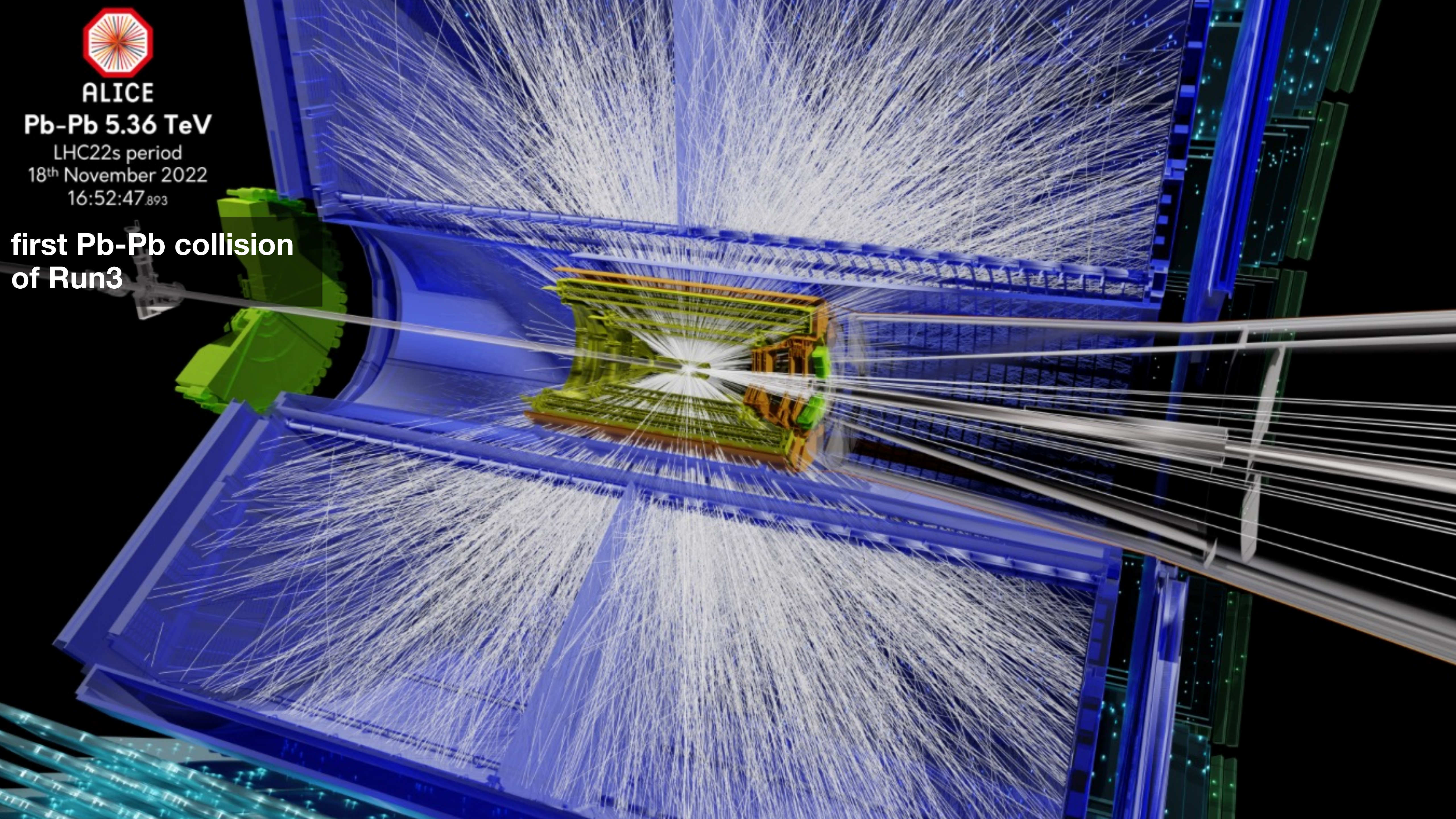
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		

🔴 **Must happen or main physics goals cannot be met** 🟠 **Important to meet several physics goals** 🟡 **Desirable to enhance physics reach** 🟢 **R&D needs being met**

ECFA Roadmap
http://dx.doi.org/10.17181/CERN.XDPL.W2EX



p-p 13 TeV
first stable beam
of Run 2



first Pb-Pb collision
of Run3

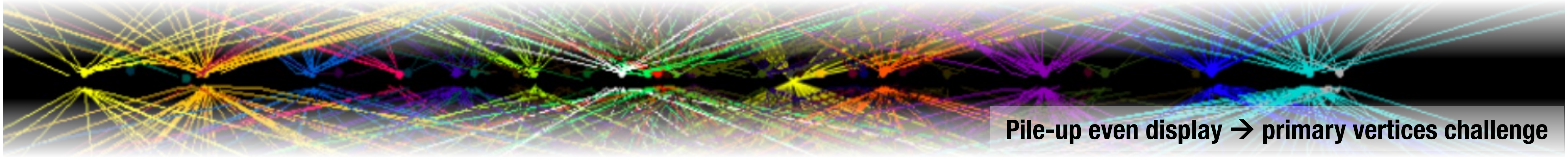
Finding vertices

Reconstruction of primary vertices

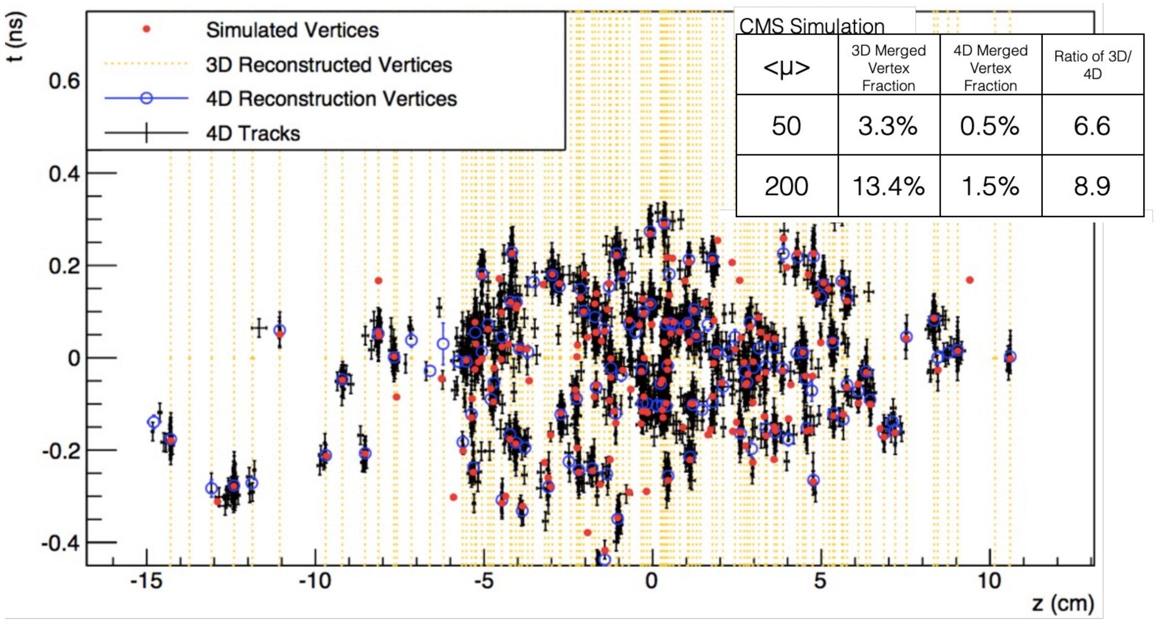
Often multiple interactions within single “Event” (pile-up interactions).

Understanding which tracks originate from a given interaction/process requires reconstruction of the vertex

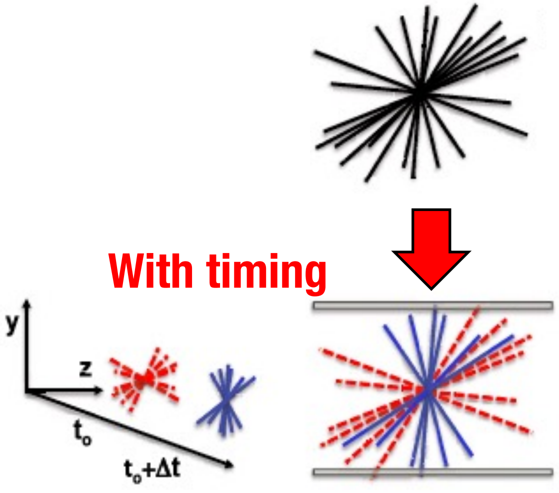
- Huge R&D to add time resolutions ~10–100 ps → timing layer or 4D tracking



Pile-up even display → primary vertices challenge



<μ>	3D Merged Vertex Fraction	4D Merged Vertex Fraction	Ratio of 3D/4D
50	3.3%	0.5%	6.6
200	13.4%	1.5%	8.9



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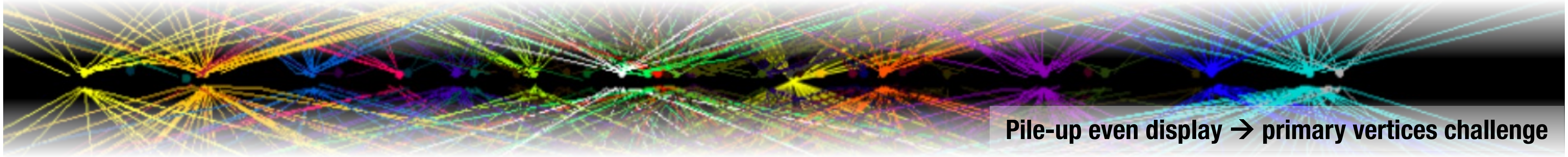
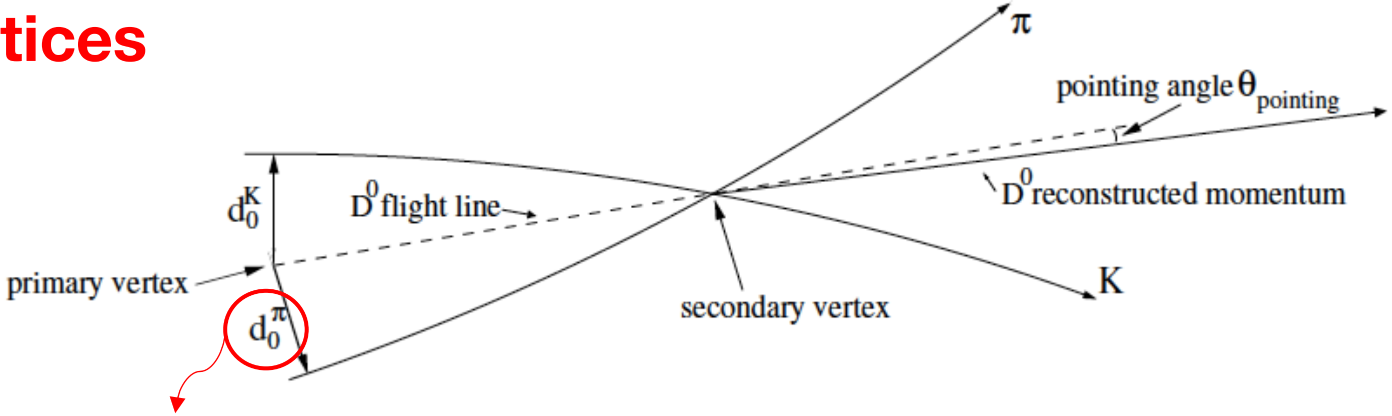


Pile-up even display → primary vertices challenge

Reconstruction of secondary vertices

Decays vertex of short-lived particles:

- Interactions with detector material
- photon conversions or hadronic interactions



d_0 track impact parameter

Typical (proper) decay length of charm and beauty hadrons: ≈100µm and ≈500µm respectively

Finding vertices

d_0 resolution (pointing resolution) → detector capability to **separate secondary vertex**

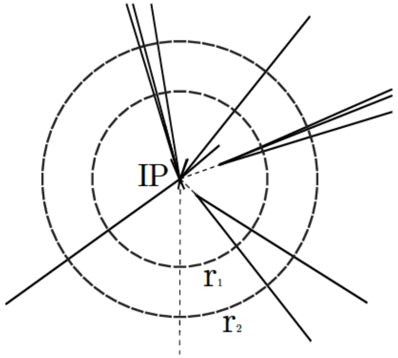
$$\sigma^2_{d0} = \boxed{\sigma^2_{sp}} + \boxed{\sigma^2_{ms}}$$

Uncertainty due to multiple coulomb scattering (in beam pipe and detector layers)

$$\sigma_{ms} \approx r_1\theta_{RMS} \approx r_1 \frac{\sqrt{x/X_0}}{\beta cp}$$

Resolution of the extrapolation from the measured points to the Interaction Point. **Considering 2 layers:**

$$\sigma_{sp} = \sqrt{\left(\frac{r_2}{r_2 - r_1}\sigma_1\right)^2 + \left(\frac{r_1}{r_2 - r_1}\sigma_2\right)^2}.$$



d_0 resolution improves with:

- **Lower** material budget **x/X_0** (in particular for the first layer)
- Get **closer to IP** for r_1 (and r_2 , but keeping r_2 as far away as possible from r_1)
  → limited by beam pipe size, radiation, particle density and bkg (r_2 by the cost)
- **Better** detector **spatial resolution** (in particular for the first layer, σ_1)

Finding vertices

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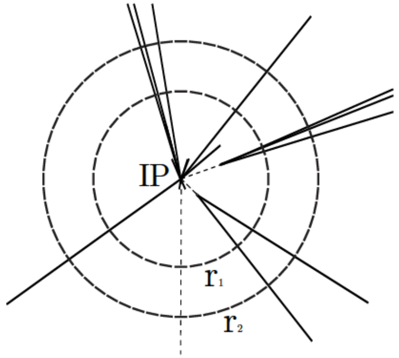

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Spatial resolution for a binary readout, p=pitch

$$\sigma^2 = \frac{1}{p}\int_{-p/2}^{p/2} x^2 dx = \frac{p^2}{12} \Rightarrow \sigma = \frac{p}{\sqrt{12}}$$

For an analogue readout $\sigma \sim \dfrac{p}{1.5 * S/N}$

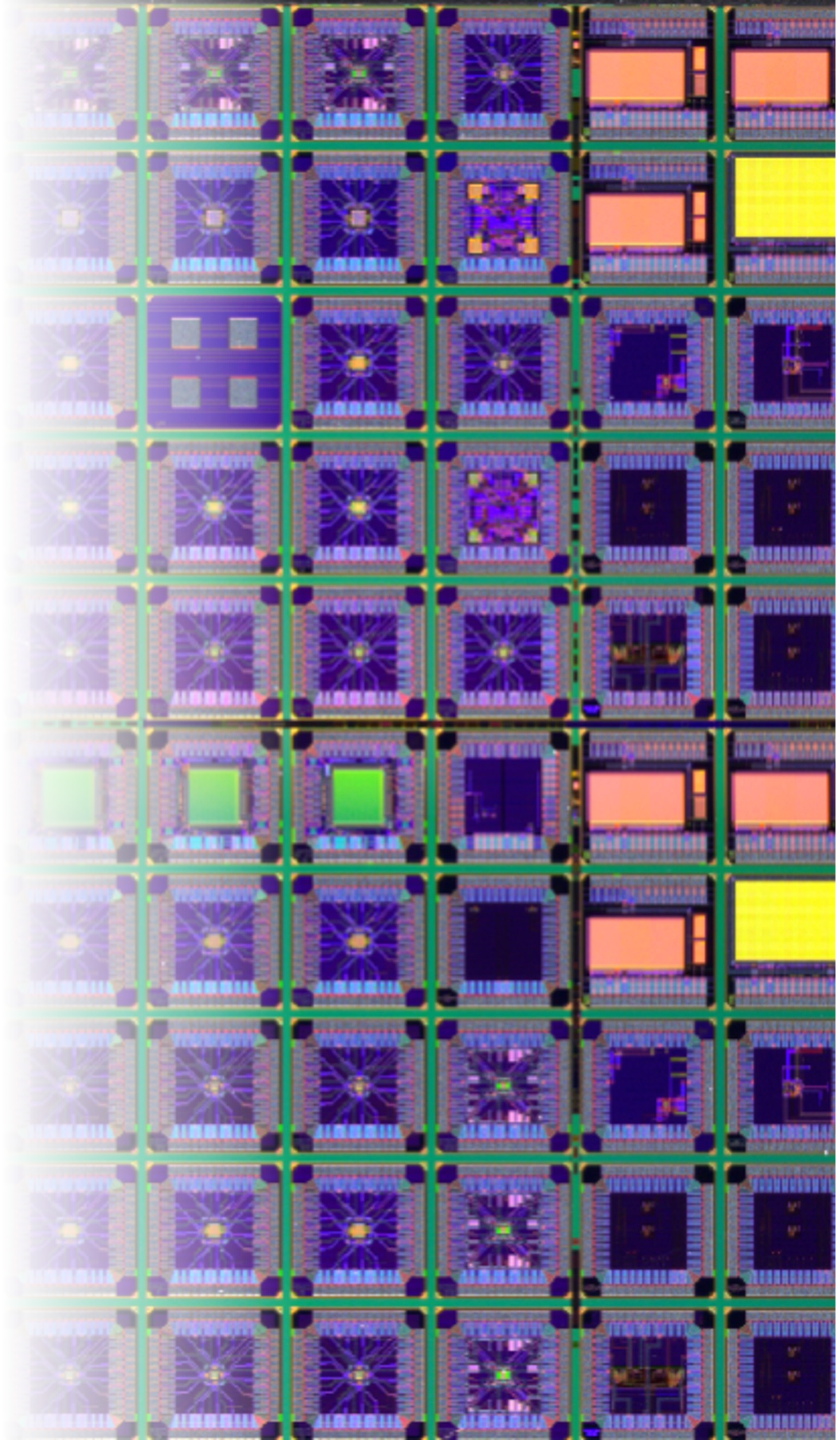
Spatial resolution improves with:

- **Smaller pitch**
- **Higher S/N**
- **Charge sharing** between more pixels/strips (Caveat: if too large might be excessive…)

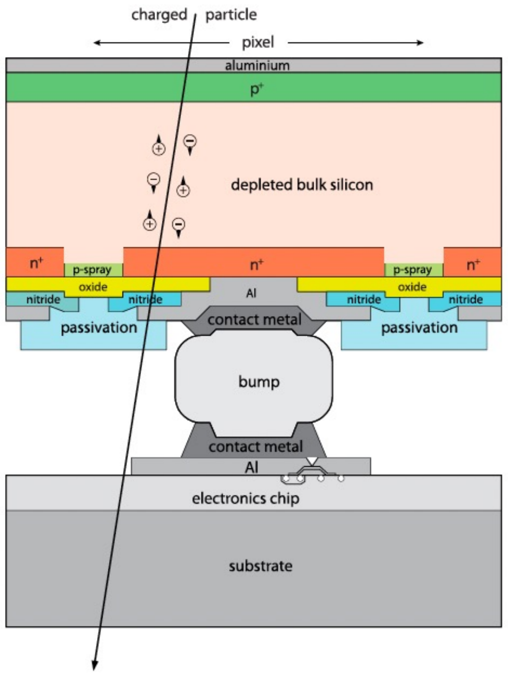
Depends also on several factors: en.loss fluctuation, diffusion, charge trapping, …

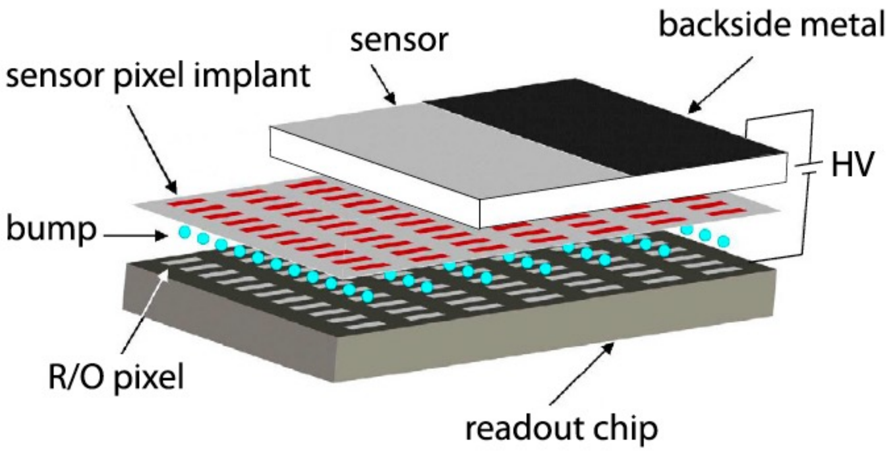
CMOS MAPS

past, present and future



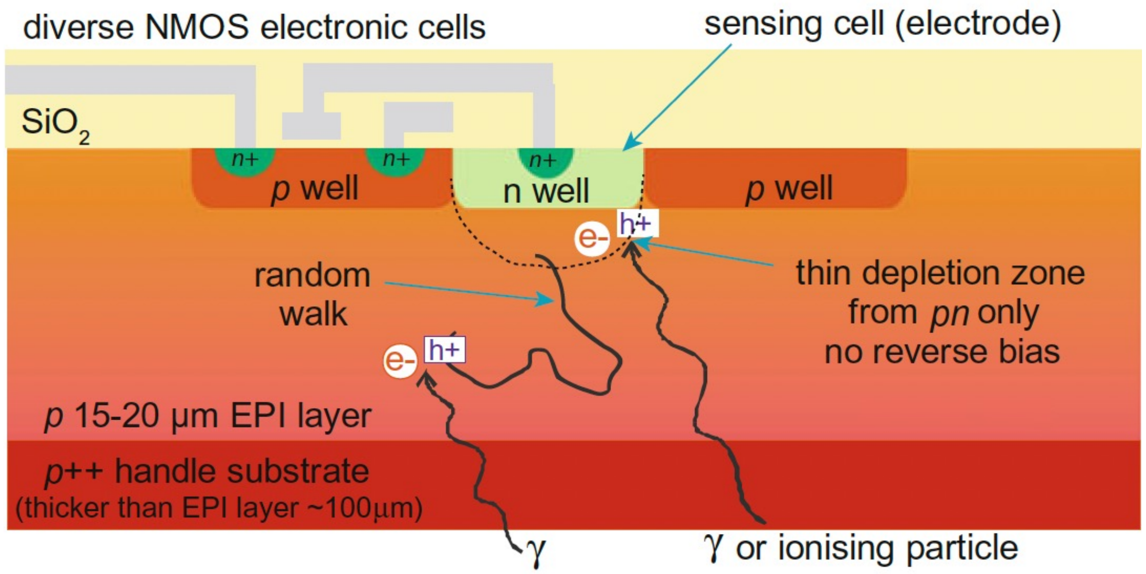
Hybrid vs MAPS





Hybrid : sensor and readout chip as separate entities → need to be interconnected

- Majority of presently installed systems
- Spin-off from HEP developments
- 100 % fill factor easily obtained
- Sensor and ASIC can be optimized separately



Monolithic Active Pixel Sensor : integrate sensor and all electronics chain in one chip

- Easier integration
- Commercial process, lower cost
- Very low capacitance → low power
- Lower material budget
- Small pixel pitch

Traditionally worse for speed, S/N, rad hard
BUT last years large improvements

CMOS MAPS – evolution and applications

Qualitative timeline…

1969

Digital imaging → with the invention of the **C**harge-**C**oupled **D**evice (**CCD**) ,
→ Start of the the digital imaging **revolution**

Improved commercial and consumer products for decades and is one of the most important technological innovations of the past half-century
Continuously improvements in CCDs

Early 1990s

Emergence of **C**omplementary **M**etal-**O**xide **S**ilicon (**CMOS**) Image Sensor technology

2009

Nobel Prize in Physics
Willard S. Boyle and George E. Smith
"for the invention of an imaging semiconductor circuit - the CCD sensor"

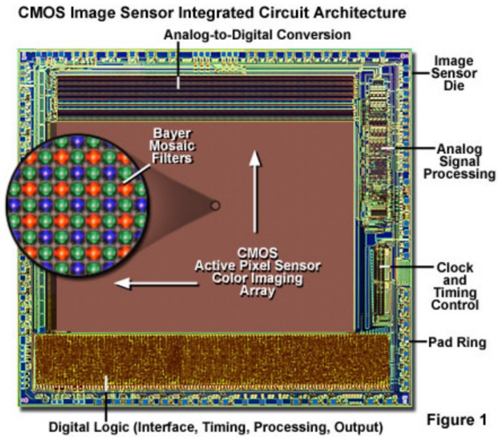
Since more than 10 years

Since more than 10 years CMOS
→ leading imaging technology

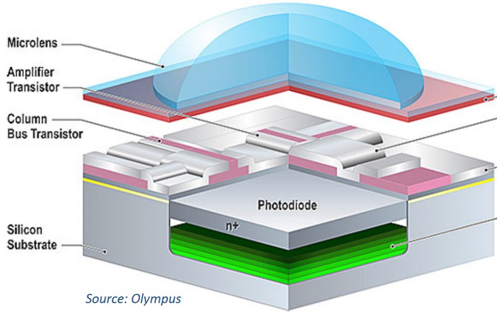
Today

CMOS used in **camera phones**, vehicles, machine vision, human recognition and security systems

- most widespread implementation of image sensors
  → main advantage: price
- need to increase sensitive area to 100%
  (no focussing lenses for charged particles, only for photons)



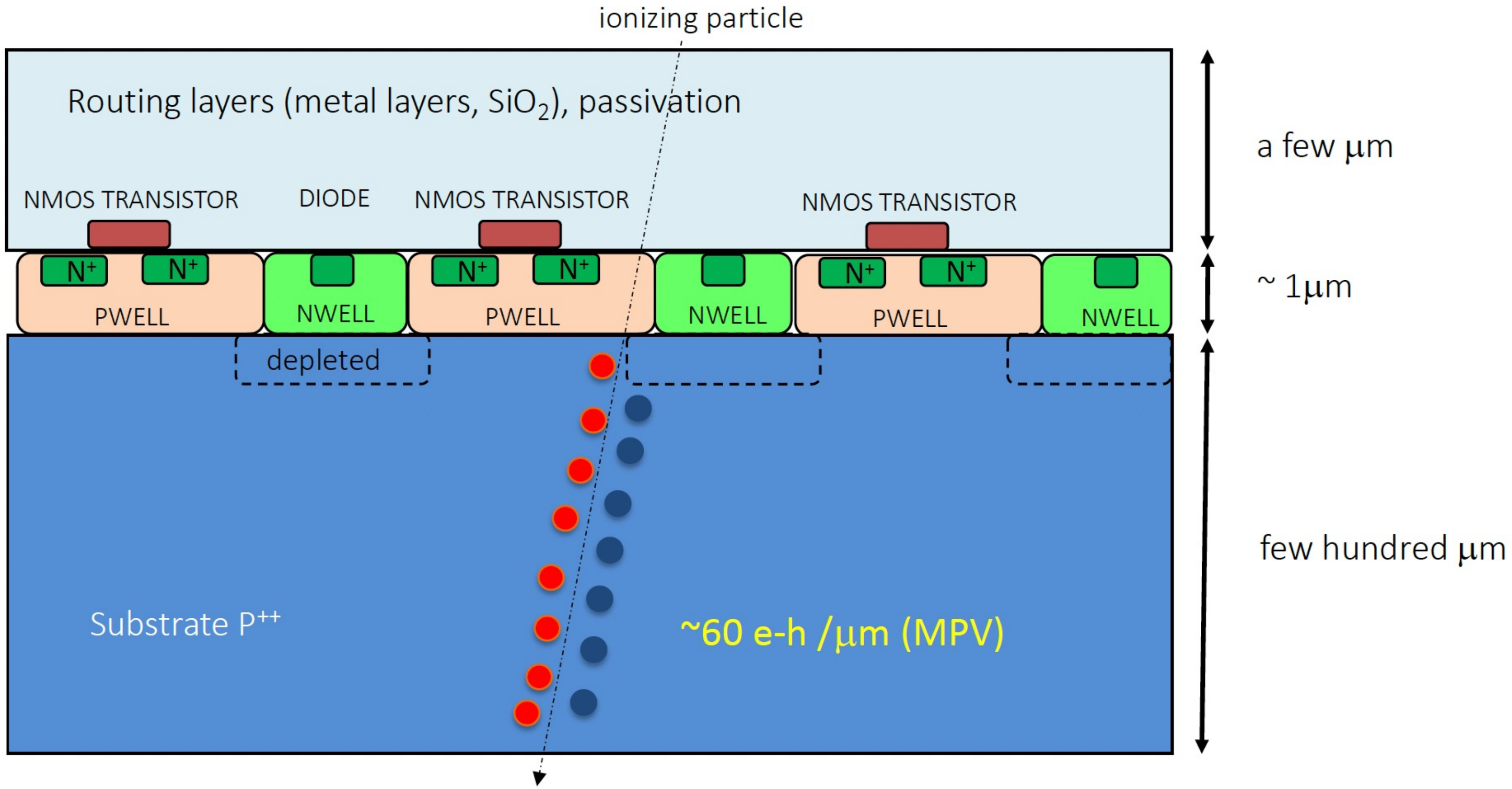
Source: Olympus (optical microscopy)



Source: Olympus

CMOS MAPS – evolution for charged particles

At the beginning, standard CMOS → **low-resistivity silicon**



Shallow depletion region
→ low charge collection efficiency

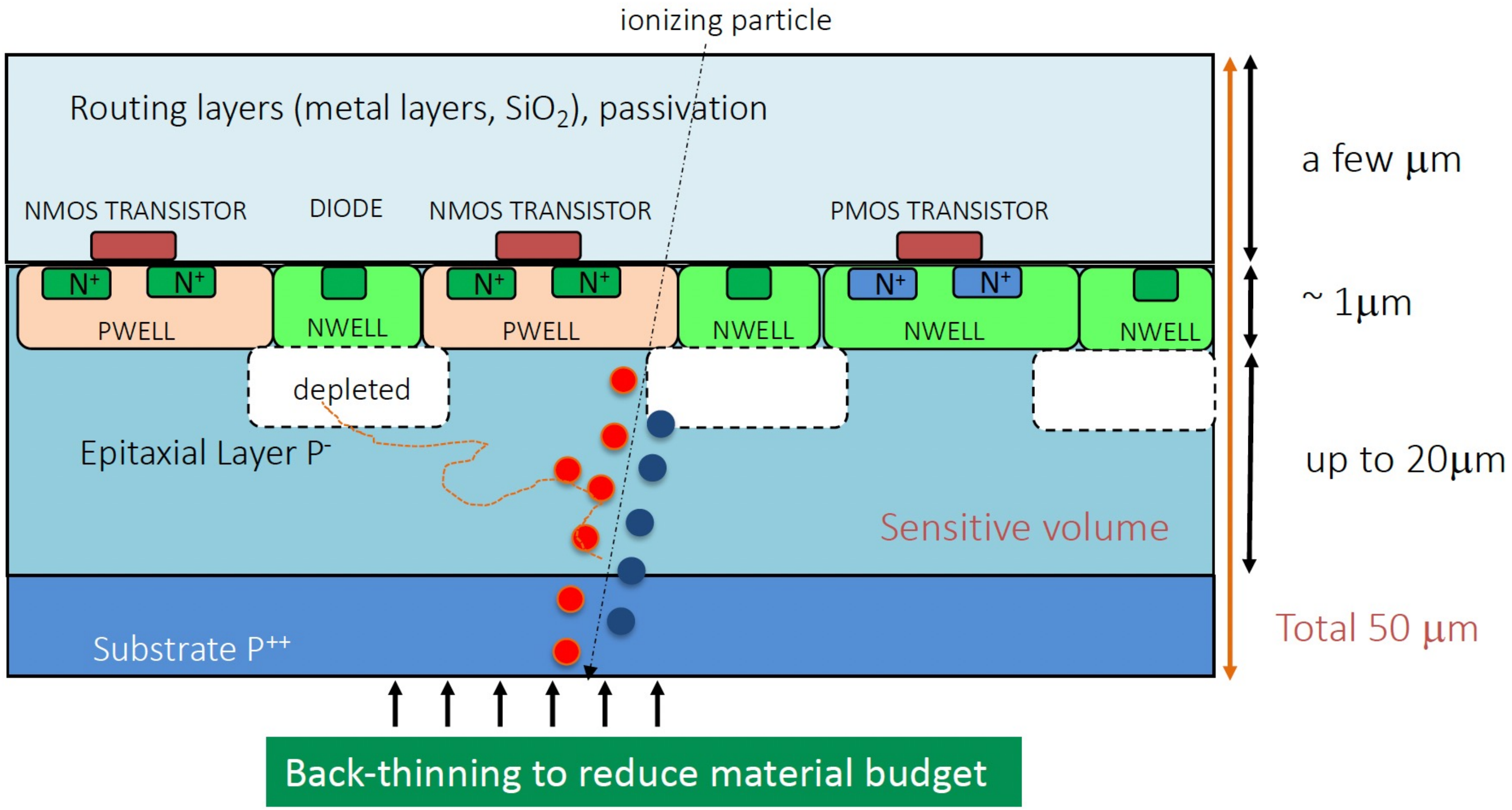
Detector element covers only a small fraction of the pixel area

→ **NOT ok for charged particles detection**

N.B. **NMOS transistors in a pwell** → to shields the source and drain junctions from the epitaxial layer
→ **essential**, otherwise these sources and drains would act as collection electrodes
→ would prevent the nwell from collecting all the signal charge.

CMOS MAPS – evolution for charged particles

In order to properly detect charged particles → **high resistive epitaxial layer**, with doping few order of magnitude smaller than one of the p++ substrate



Epitaxial layer partially depleted
Minority carriers **diffuse** in the epi layer…

…potential barriers at its boundaries which keep minority carriers confined in epi…

… till they reach the depleted region → **drift**

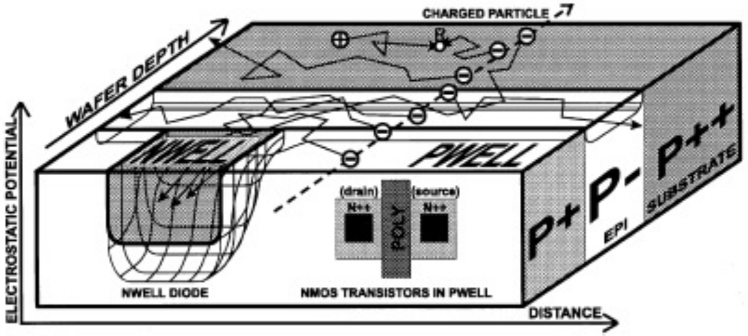
$$V_1 = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}}$$

$$V_2 = \frac{kT}{q} ln \frac{N_{PWELL}}{N_{epi}}$$

Monolithic detectors offer advantages in terms of detector assembly, production cost and input capacitance
→ promising for pixel detectors and full tracking detectors

STAR – first application in HEP

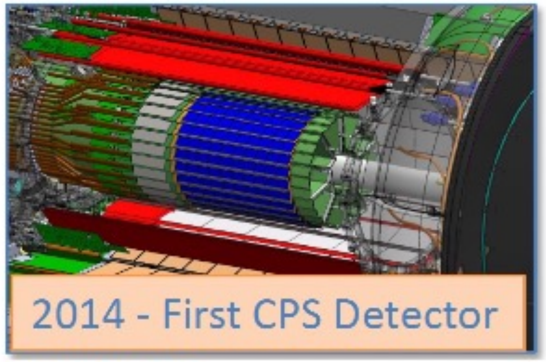
Full detector in 2014



MIMOSA-1 chip unit

2001, https://doi.org/10.1016/S0168-9002(00)00893-7

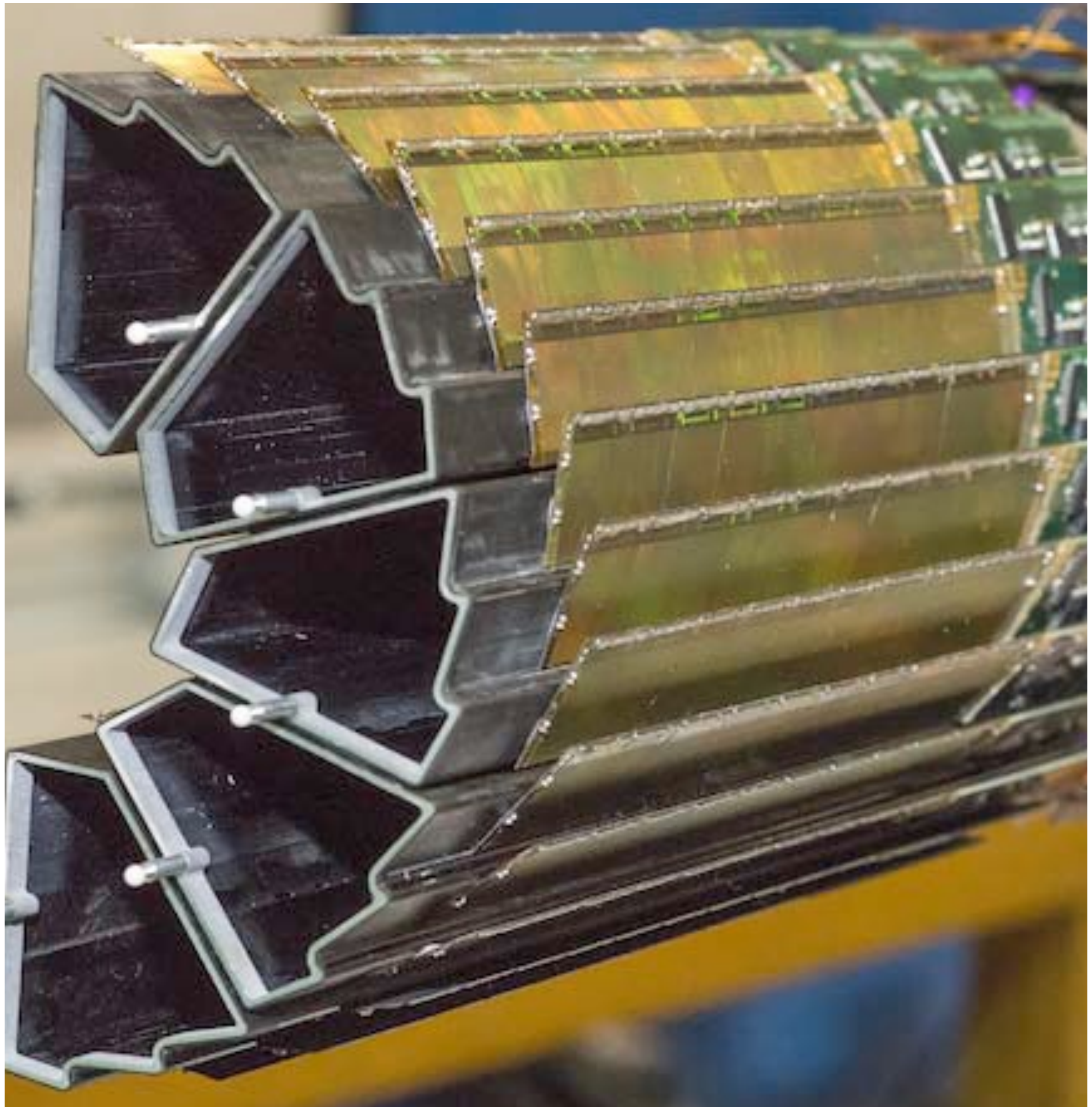
Early versions with thin and low resistivity epi-layer



STAR HFT

Physics Runs in **2015-2016**

- **2 layers at 2.8 and 8 cm**
- 400 sensors of **MIMOSA-28** as brick
- 0.16 m^2
- 356 MPixels

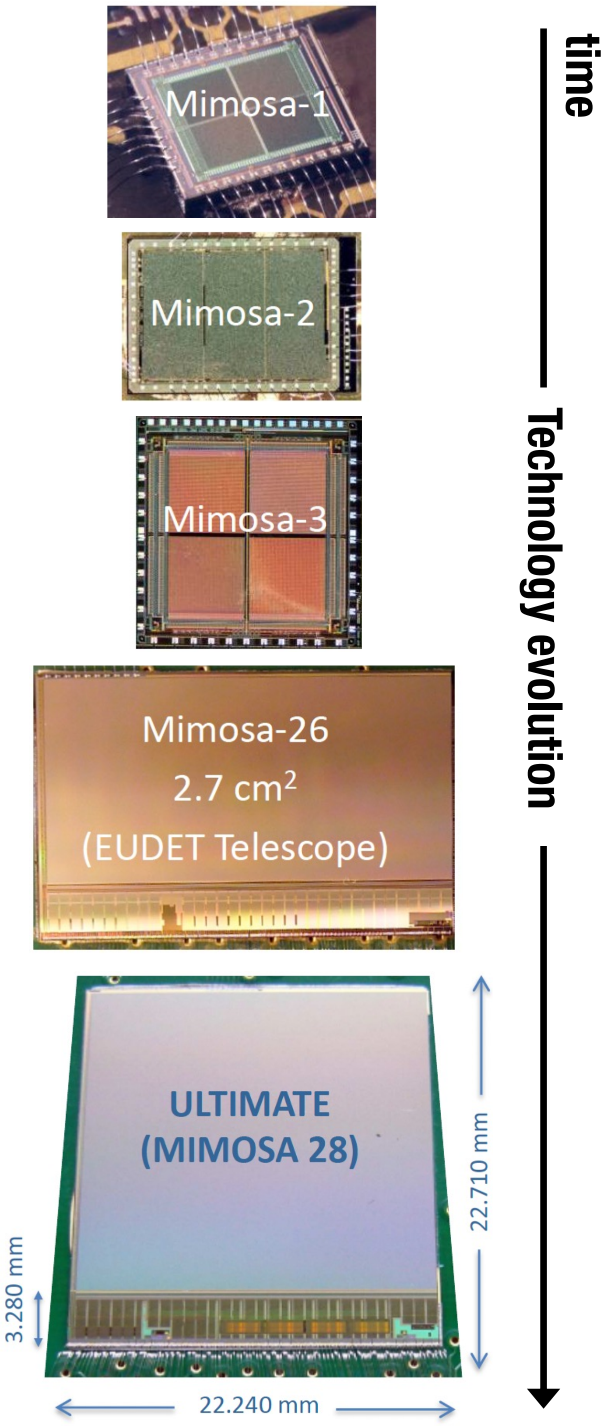


STAR – first application in HEP

Full detector in 2014

Final chip chosen → Ultimate (aka **MIMOSA 28**)

- technology node **0.35 µm CMOS**
- **power ~ 150 mW/cm^2**
- 20 µm high-resistivity p-epi layer **not fully depleted and no reverse bias**
  - Charge collected (mostly) by diffusion
  - Typical charge collection time < 100ns
  - up to ~**10^{12} 1MeV n_{eq}/cm^2**
- Radiation length (1st layer): **x/X_0 = 0.39%**
- **in-pixel simple circuit**: 2T structure
- Integration time 190 µs
- **18.4 µm pitch**
- 576 x 1152 pixels, 20.2 x 22.7 mm^2



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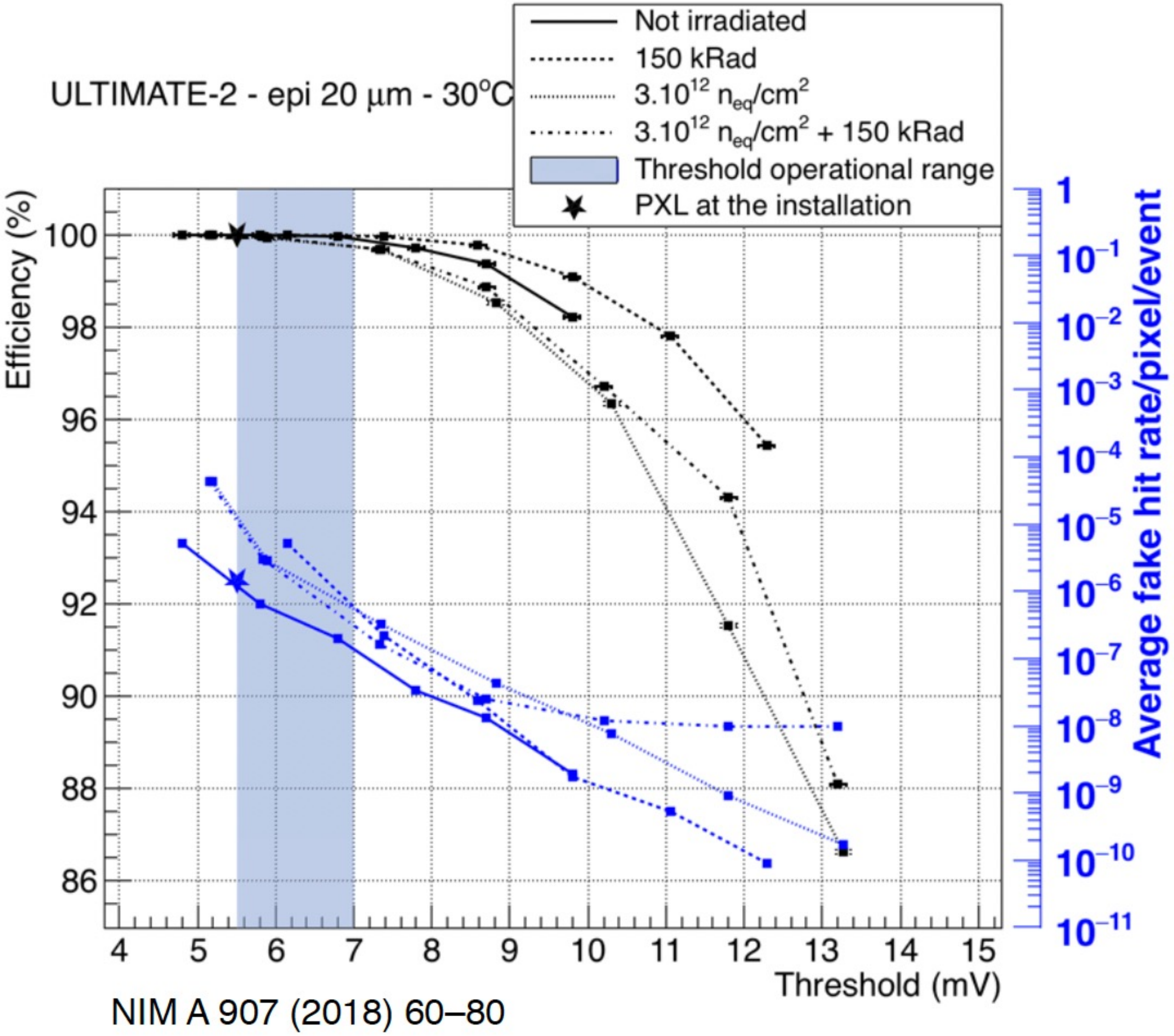
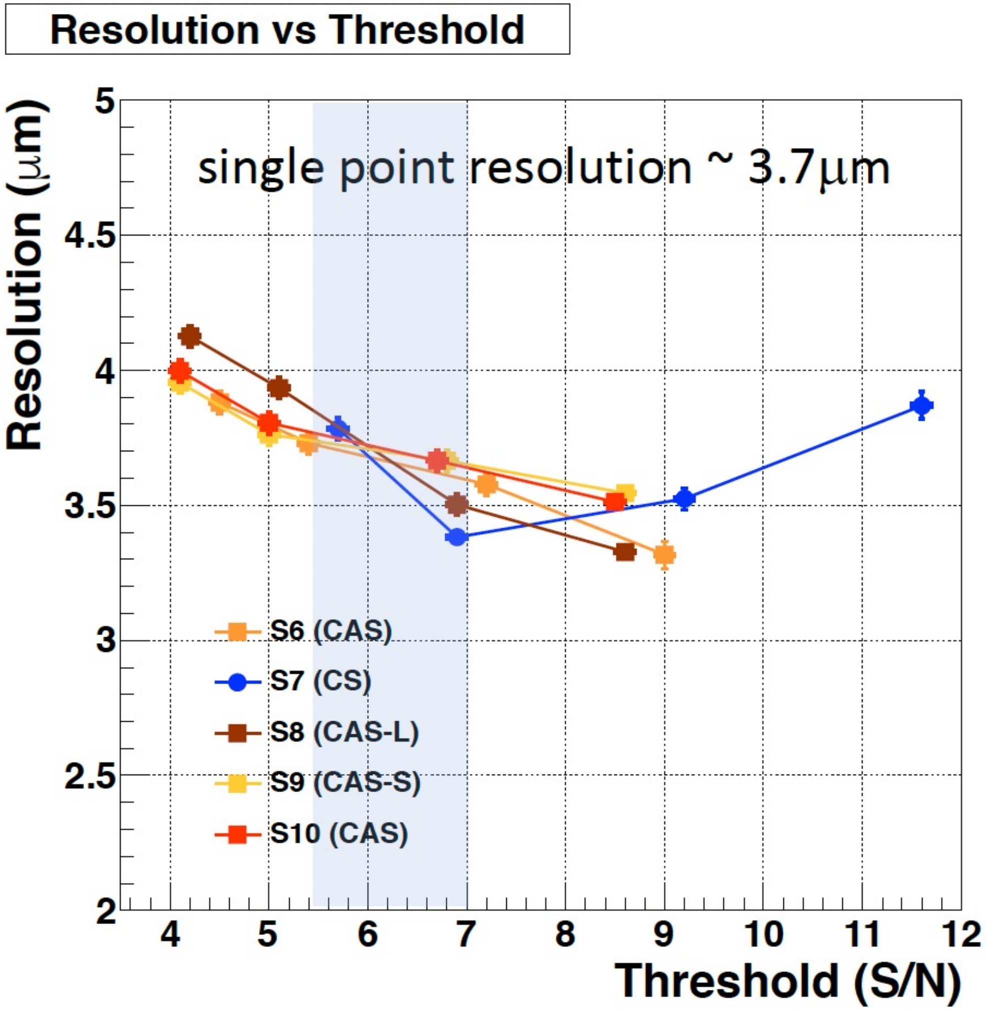


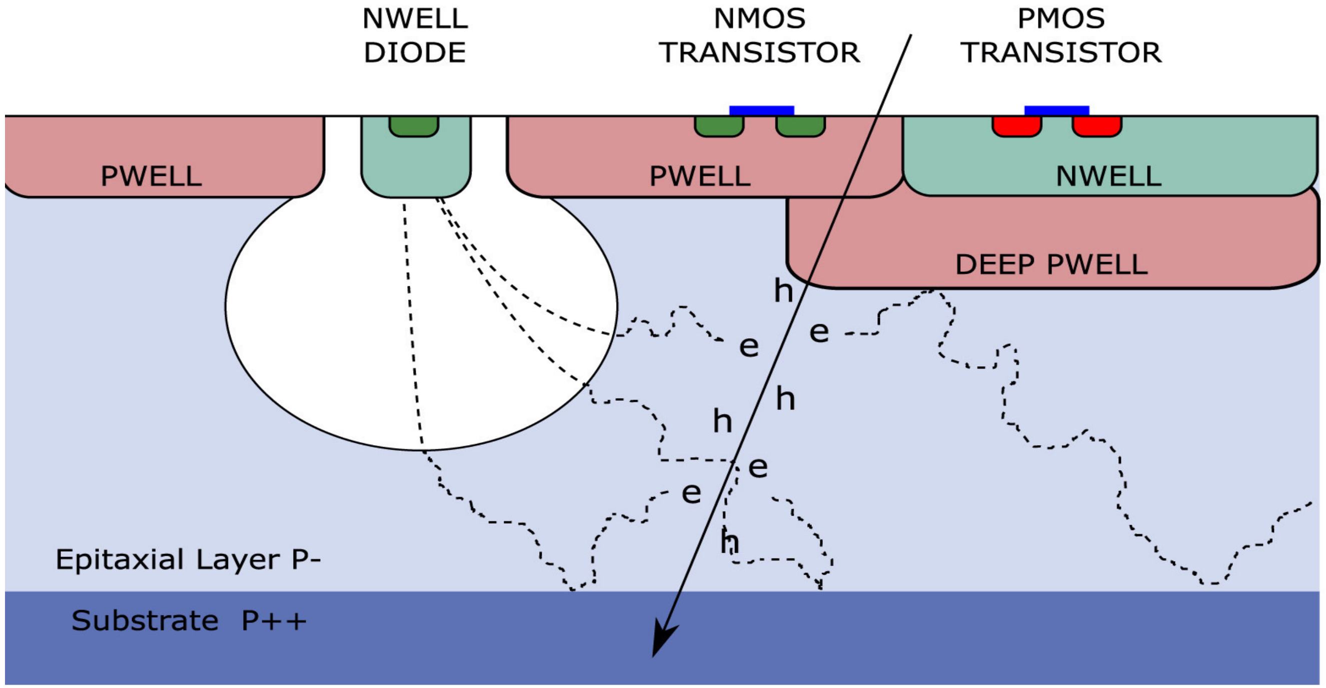
NIM A 907 (2018) 60–80



The INMAPS process

2008, https://doi.org/10.3390/s8095336
STFC development, in collaboration with
TowerJazz

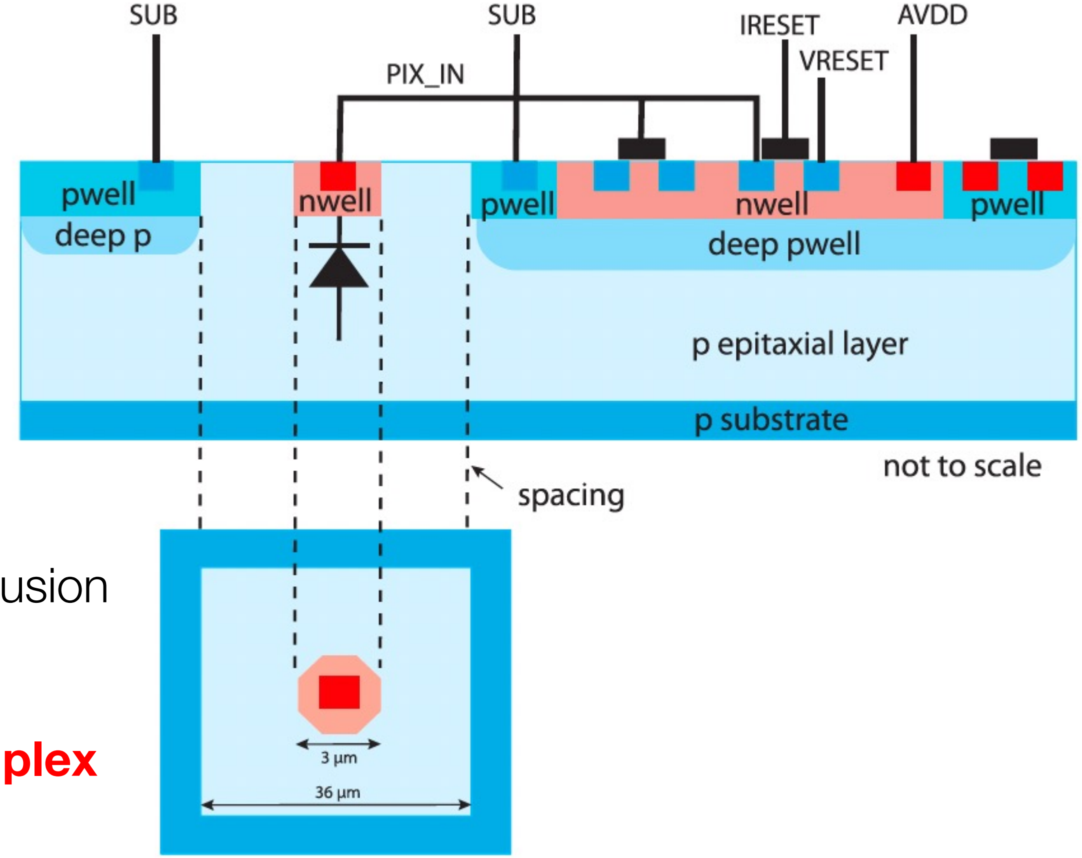
Standard CMOS with additional deep P-well implant → Quadruple well technology



In-pixel: Amplification, Discrimination

Additional **deep P-well** :

- **100% efficiency**
- **CMOS electronics in pixel**
- **faster**



Before
limitation of in-pixel circuitry (only NMOS), charge collection by diffusion

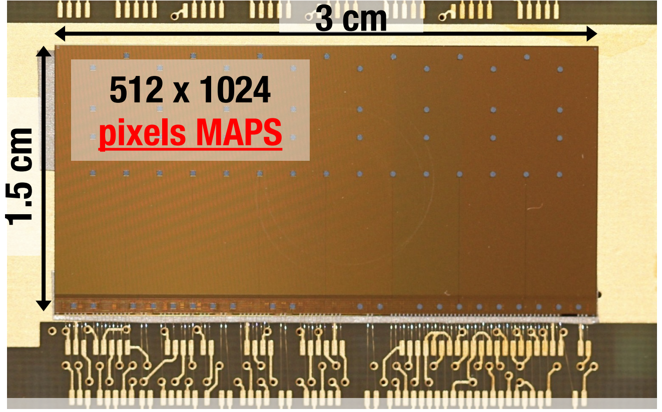
Now
new generation of CMOS APS for scientific applications with **complex CMOS circuitry inside the pixel** (TowerJazz CIS 180nm)

ALPIDE in ALICE – ITS2

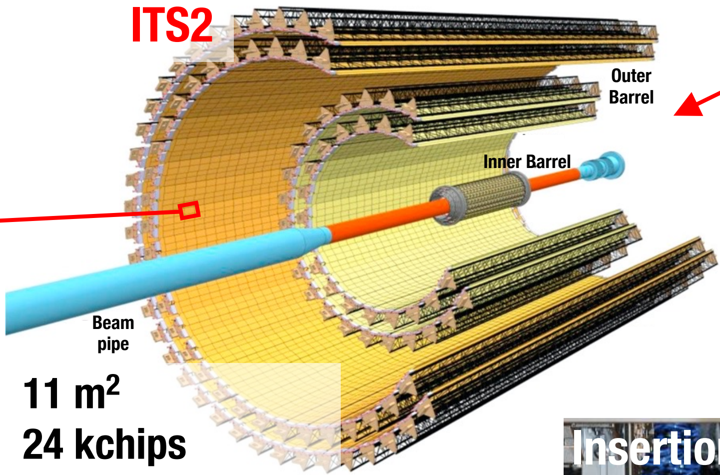
First MAPS in HEP with sparse readout similar to hybrid sensors

Inner Tracking System 2 (ITS2) upgrade – installation during 2021 (LS2)

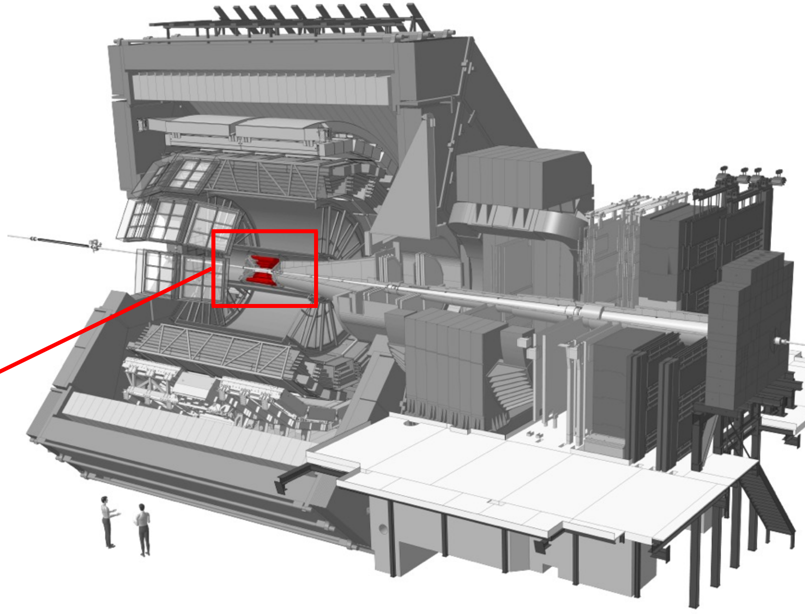
Single ALPIDE chip



In-pixel: Amplification, Discrimination and Multi event buffer



- $11\ m^2$
- 24 kchips
- 12.5 Giga-Pixels



ITS2, Closer, thinner, better:

- 23 mm from IP
- 0.36% x/X_0 per layer, Inner Barrel
- pixel size ~ $27 \times 29\ \mu m^2$

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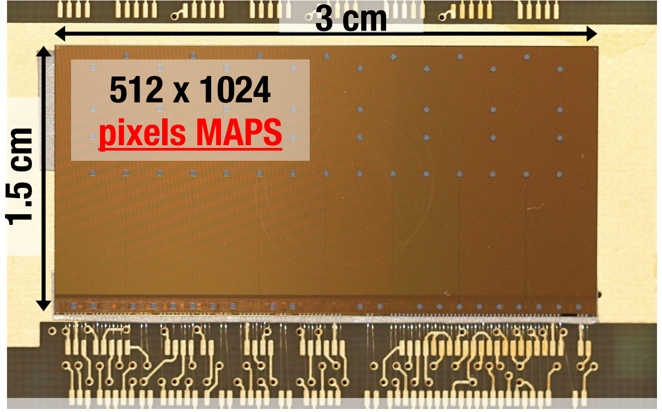

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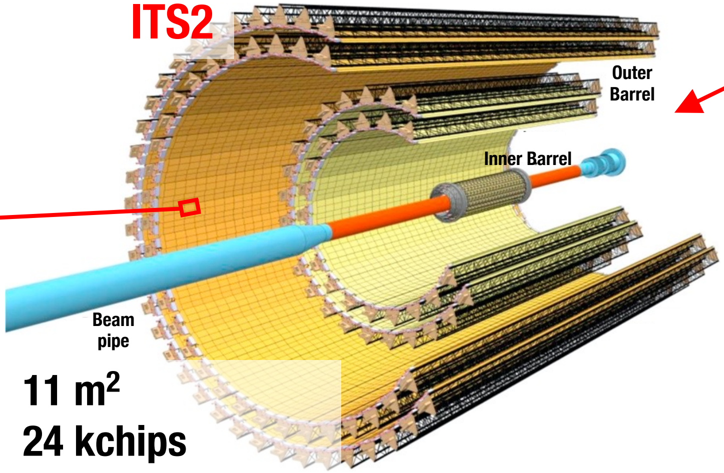

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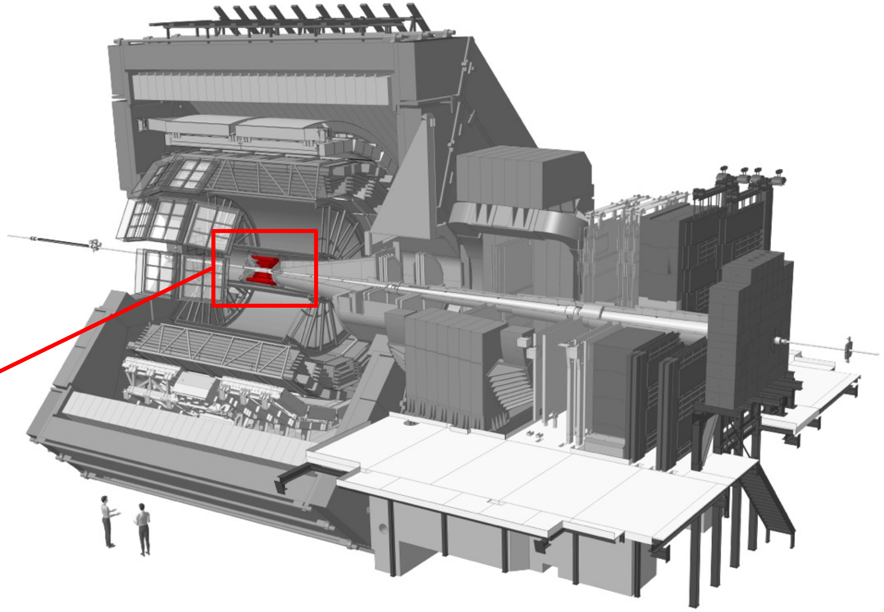

ITS2, Closer, thinner, better:

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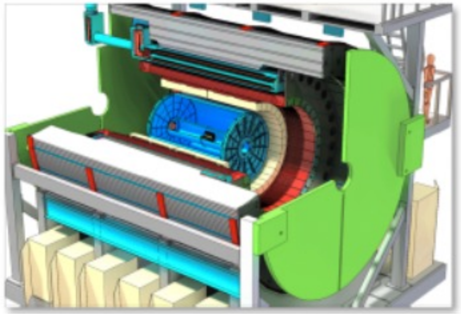
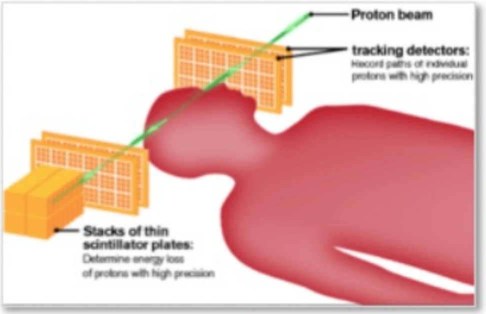
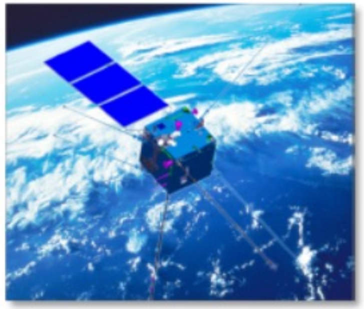
ALPIDE also for several other physics experiments, in space and for medical applications



sPHENIX



Proton CT (tracking)

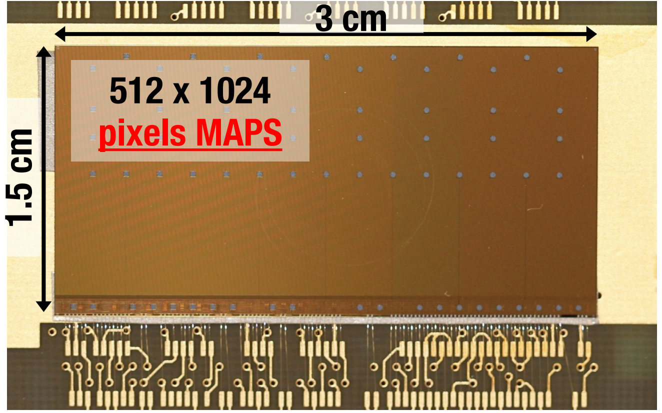


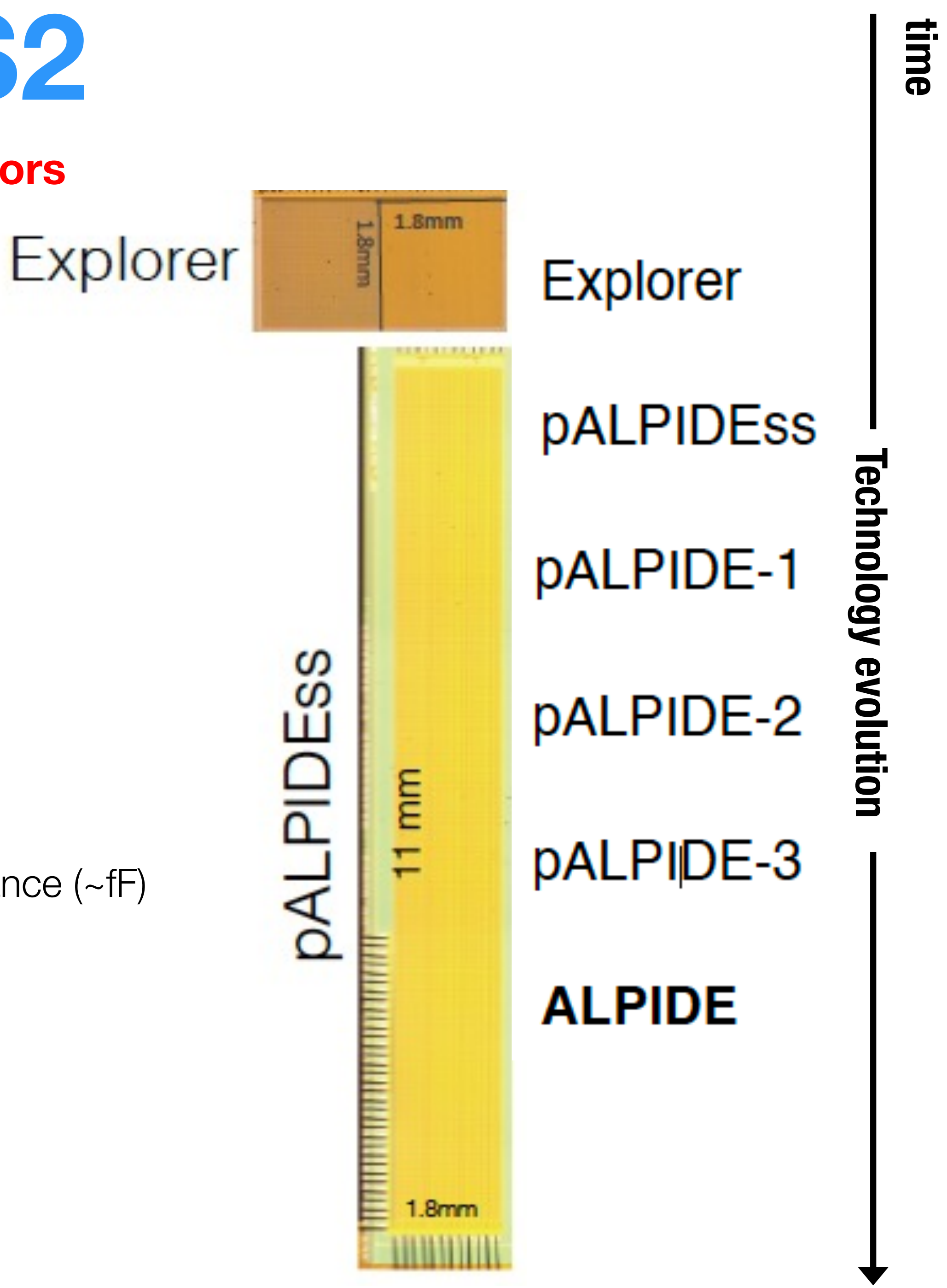
CSES – HEPD2

ALPIDE in ALICE – ITS2

First MAPS in HEP with sparse readout similar to hybrid sensors

Single ALPIDE chip → used as brick in ITS2





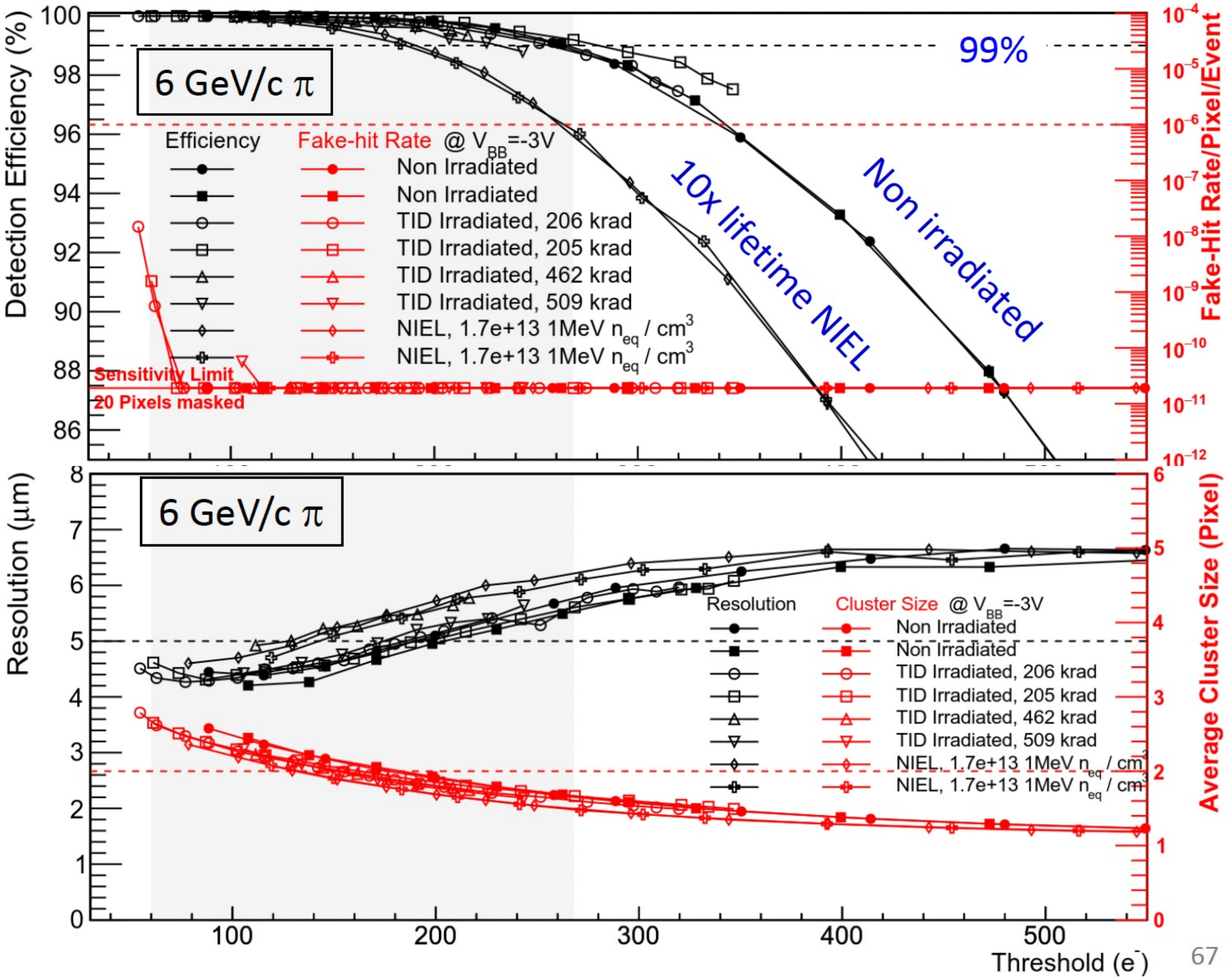
TJ CMOS 180 nm INMAPS imaging process (TJ)

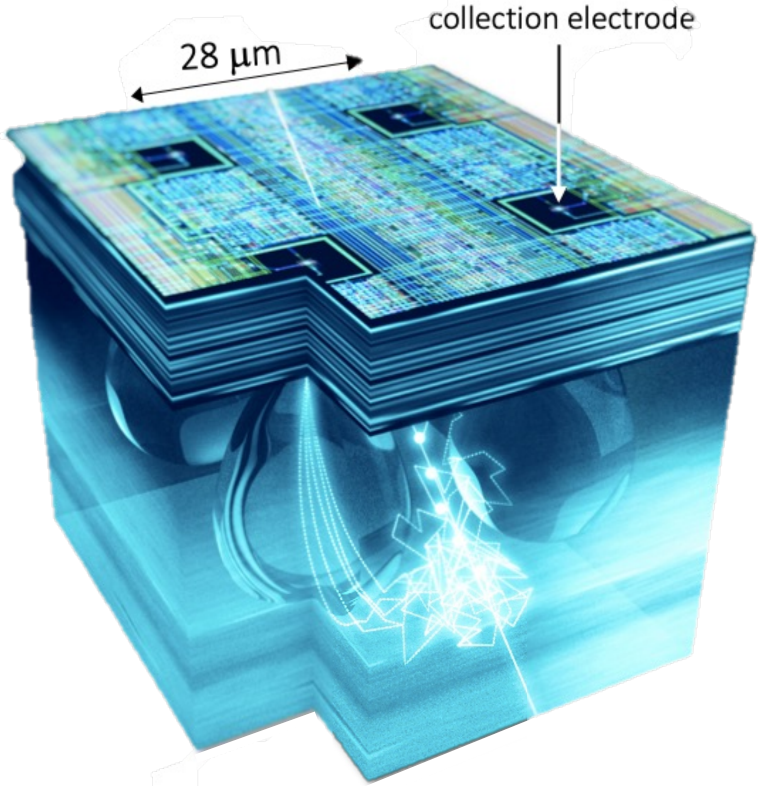
High-resistivity (> 1kW cm) p-type epitaxial layer (25µm) on p-type substrate

- **Small n-well diode** (2µm), ~10 times smaller than pixel => low capacitance (~fF)
- Qin (MIP) ≈ 1300 at ≈ 40mV
- **Reverse bias voltage** (-6V < Vbb < 0V) to substrate
- but **no full depletion** -> NIEL up to ~**10^{13-14} 1 MeV n_{eq}/cm^2**
- **INMAPS** process → Deep PWELL shields NWELL of PMOS transistors
- charge collection time <30ns (Vbb = -3V)
- **power**: 300 nW /pixel **(<40 mW/cm^2, in matrix ~6 mW/cm^2**)

ALPIDE in ALICE – ITS2

First MAPS in HEP with sparse readout similar to hybrid sensors



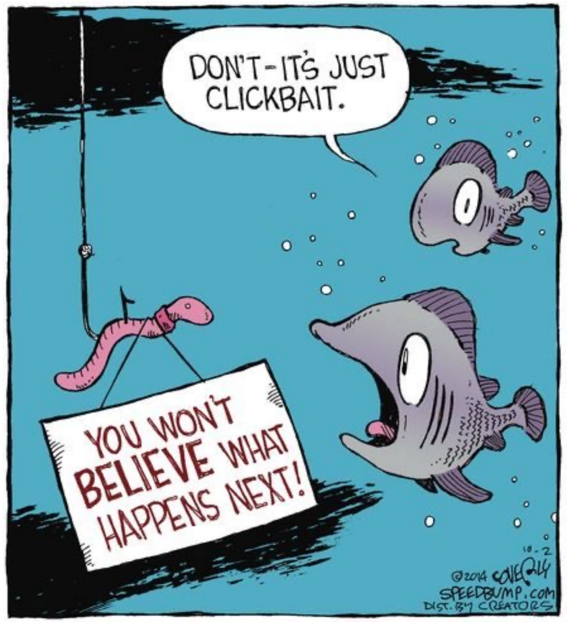


…and currently working (since 2 years):

- with stable operation of all the 24k ALPIDEs
- >99% functional pixels
- Very low FHR

What next?

What do we need further in HEP?



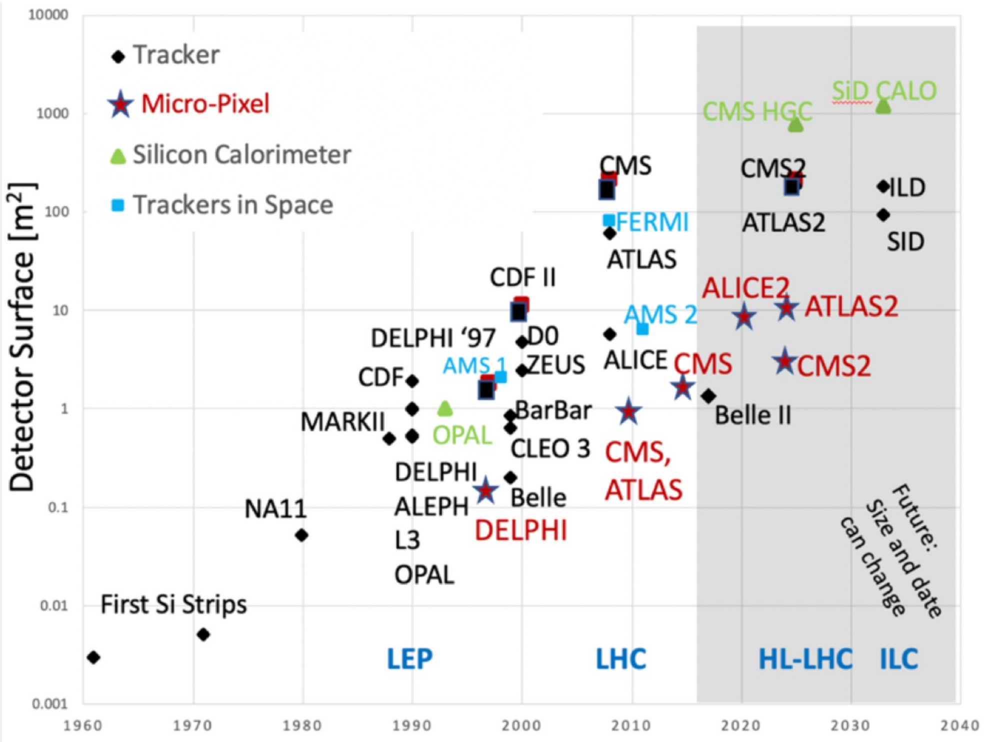
CMOS MAPS in HEP - summary and requirements

CMOS MAPS used in several applications

- In **HEP several experiments used/will use CMOS**: STAR,ALICE,DEPFET in Belle,CBM,MPD,sPHENIX, Mu3e,…

More and more **future applications** are **demanding to improve among several aspects**:

- Increase **radiation tolerance**
- Improve **time resolution** (0.05 ns - μs)
- Scalability (larger and **larger areas**)
- Reduce the **power consumption**.
  - 20-40 mW/cm^2 (30 μm pixels)
  - Analog power consumption $P \sim (Q/C)^{-m}$, m=2 usually → Q/C key parameter
  - Input capacitance: O(1-5 fF), also to reduce noise
- Improve even further the impact parameter, and as a consequence:
  - **Position resolution** (~5 μm, pixel pitch ~ 10-30 μm)
  - Move to **deeper sub micron tech. node** (65 nm node)
  - Reduce **material budget** (from $x/X_0 \simeq 0.3\%$ down to ~0.05%)
  - **Larger wafers**: at the moment we are stuck in 90s, with 200 mm (8”) → needed o increase to 300 mm (12”) for next upgrades
  - **Stitching**



From F. Hartmann, HST2017

CMOS MAPS in HEP - summary and requirements

CMOS MAPS used in several applications

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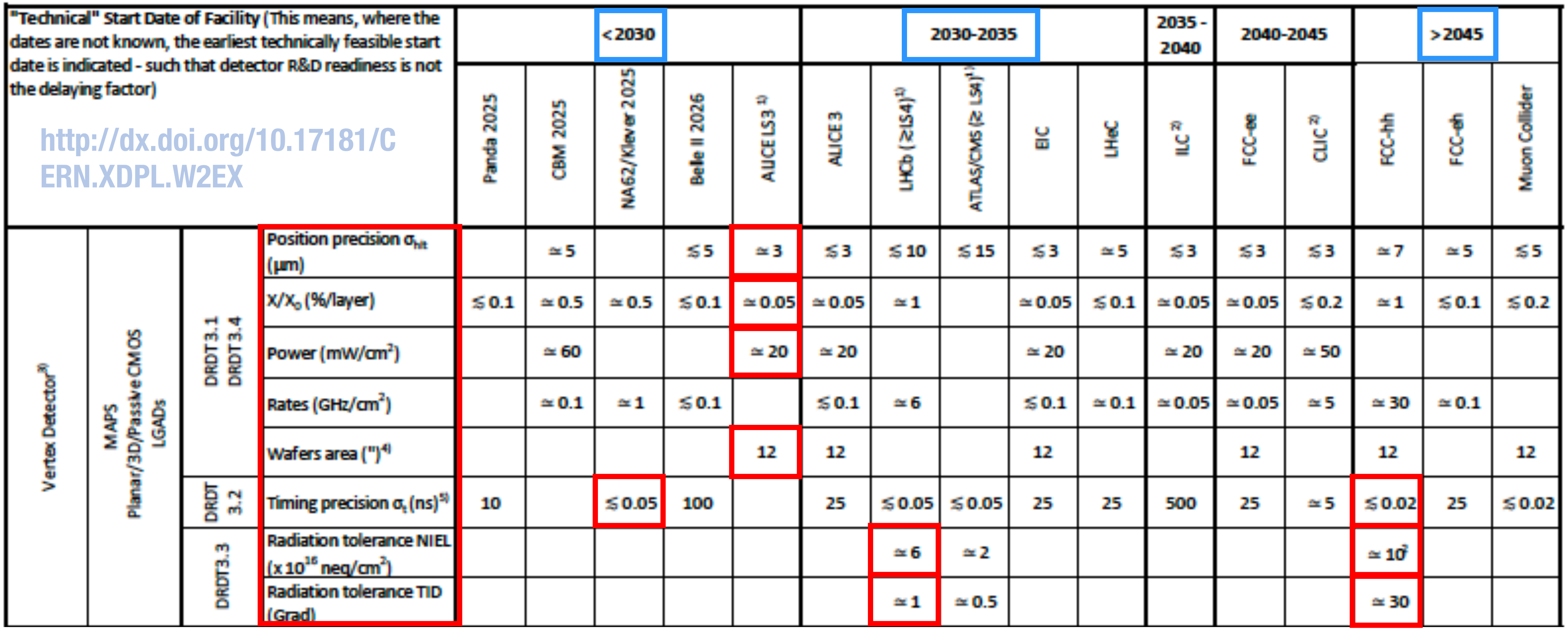


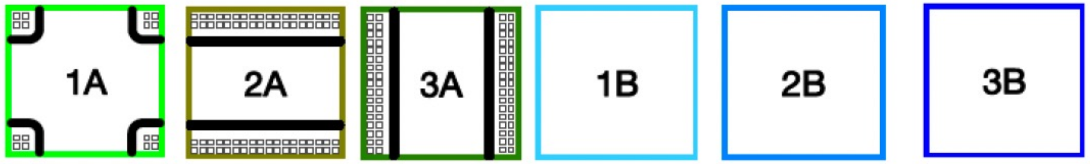
"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				<2030					2030-2035					2035 - 2040	2040-2045		>2045		
http://dx.doi.org/10.17181/CERN.XDPL.W2EX				Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 1)	ALICE 3	LHCb ($\gtrsim$LS4) 1)	ATLAS/CMS ($\gtrsim$ LS4) 1)	EIC	LHeC	ILC 2)	FCC-ee	CLIC 2)	FCC-hh	FCC-eh	Muon Collider
Vertex Detector 3)	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)		$\simeq 5$		$\lesssim 5$	$\simeq 3$	$\lesssim 3$	$\lesssim 10$	$\lesssim 15$	$\lesssim 3$	$\simeq 5$	$\lesssim 3$	$\lesssim 3$	$\lesssim 3$	$\simeq 7$	$\simeq 5$	$\lesssim 5$
			X/X_0 (%/layer)	$\lesssim 0.1$	$\simeq 0.5$	$\simeq 0.5$	$\lesssim 0.1$	$\simeq 0.05$	$\simeq 0.05$	$\simeq 1$		$\simeq 0.05$	$\lesssim 0.1$	$\simeq 0.05$	$\simeq 0.05$	$\lesssim 0.2$	$\simeq 1$	$\lesssim 0.1$	$\lesssim 0.2$
			Power (mW/cm^2)		$\simeq 60$			$\simeq 20$	$\simeq 20$			$\simeq 20$		$\simeq 20$	$\simeq 20$	$\simeq 50$			
			Rates (GHz/cm^2)		$\simeq 0.1$	$\simeq 1$	$\lesssim 0.1$		$\lesssim 0.1$	$\simeq 6$		$\lesssim 0.1$	$\simeq 0.1$	$\simeq 0.05$	$\simeq 0.05$	$\simeq 5$	$\simeq 30$	$\simeq 0.1$	
			Wafers area (") 4)					12	12			12			12		12		12
		DRDT 3.2	Timing precision σ_t (ns) 5)	10		$\lesssim 0.05$	100		25	$\lesssim 0.05$	$\lesssim 0.05$	25	25	500	25	$\simeq 5$	$\lesssim 0.02$	25	$\lesssim 0.02$
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							$\simeq 6$	$\simeq 2$						$\simeq 10^7$		
			Radiation tolerance TID (Grad)							$\simeq 1$	$\simeq 0.5$						$\simeq 30$		

(Detour parenthesis about stitching)

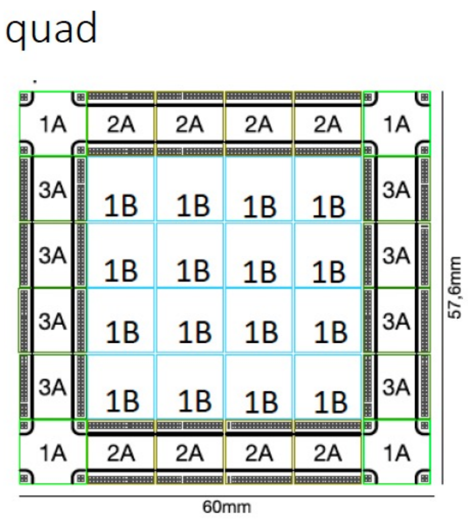
Reticle stitching:

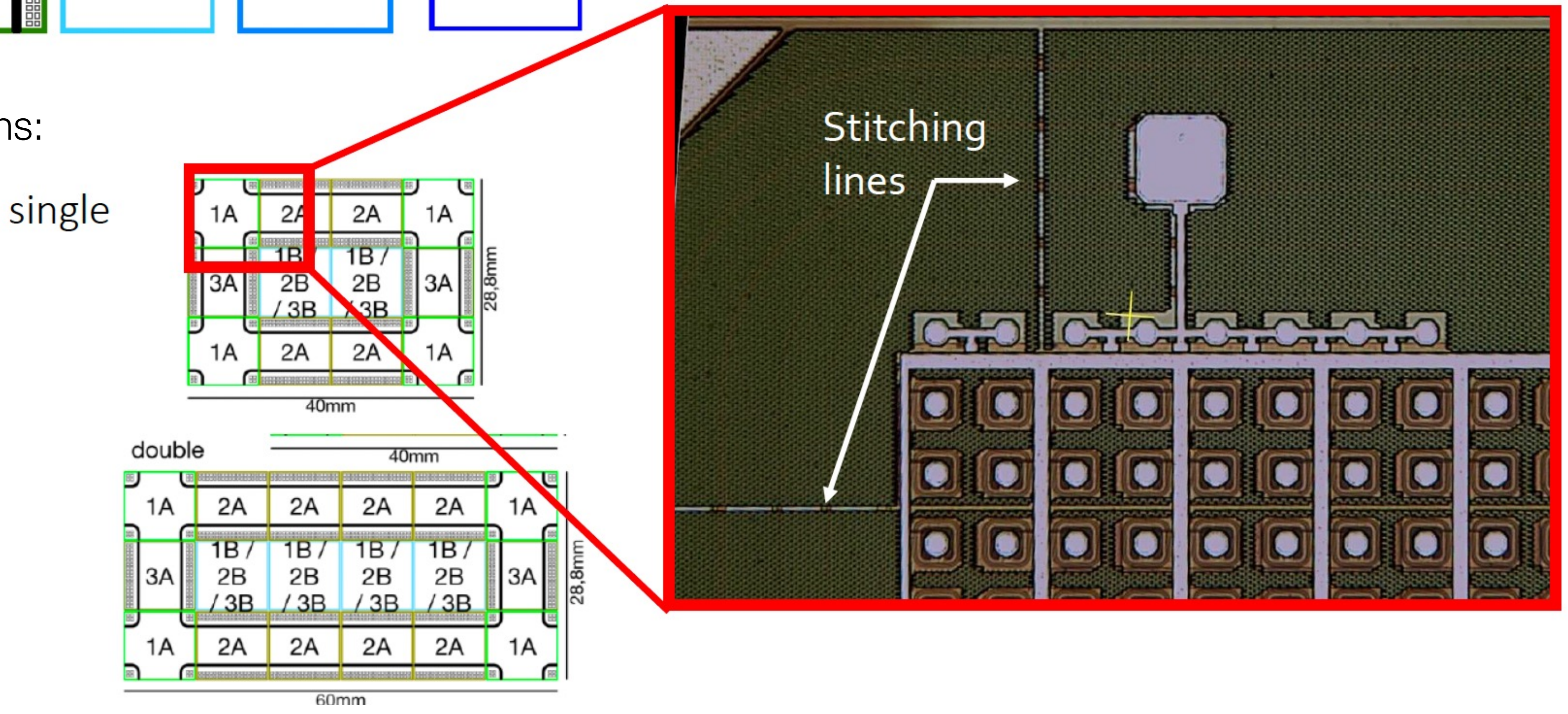
- Needed if sensor size > reticle size, 26mm x 32 mm
- Reticule made of blocks
- Printing only individual blocks at each step with a tiny well-defined overlap
- Different sub-reticle (~1cm x 1cm) for edge and active ares

- Will be fundamental to move to larger sensor size → no limit (if not the wafer size itself)
- New technique, never tested in HEP yet



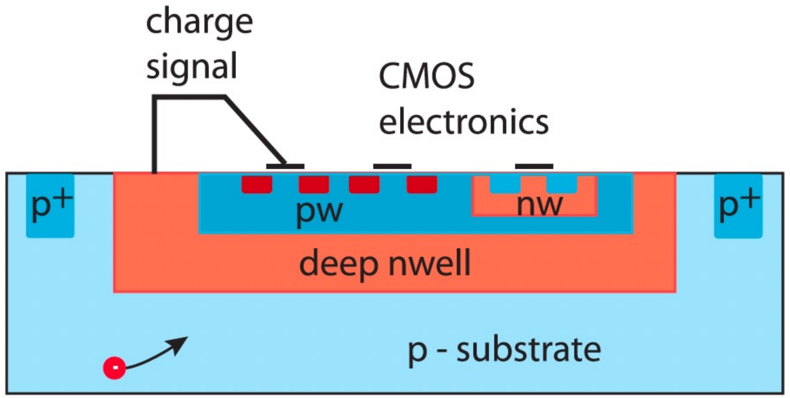
Repeat for different designs:

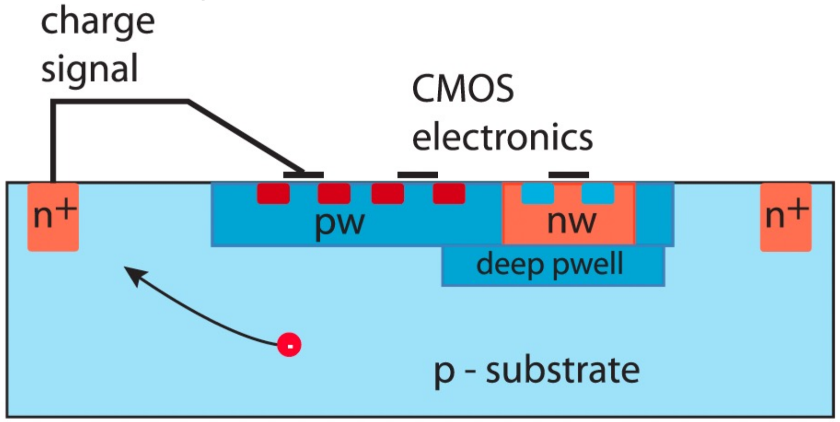




Depleted MAPS, DMAPS

A common path in order **to face the radiation tolerance and to improve the time resolution is to try to realize a first full depletd CMOS MAPS**. **Two** different **ways** could bring to this results:





Electronics inside charge collection well

large collection electrode

- → C~300 fF → higher noise O(100 e-) and speed/power penalty
- high and homogeneus electric field
- homogeneous weighting field
- on average short(er) drift paths
- Large depletion depth
- less trapping -> **radiation hard**
- possible cross-talk (digital to sensor)

E.g. MUPIX, RD50, MONOLITH, LF MONOPIX, ATLASPIX
For timing: very uniform, small wf but larger landaus

Electronics outside charge collection well

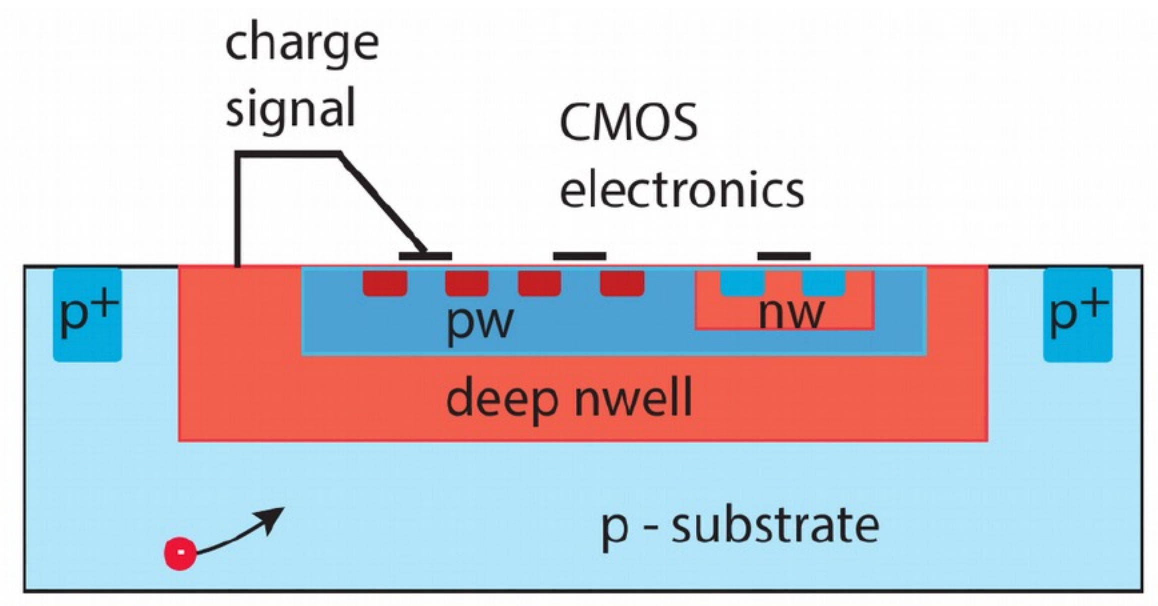
small collection electrode

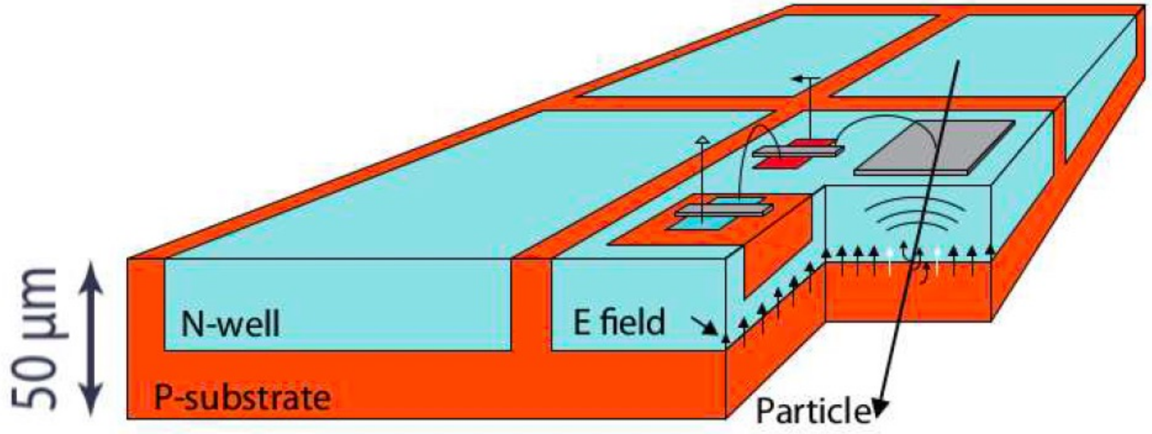
- → C~3fF → reduced noise O(10 e-) and lower analog power budget (noise, speed)
- potentially low field regions
- Less homogeneus weighting field
- on average long(er) drift distances
- smalller depletion depth, **needs process modification**
- radiation hardness **needs process modification**
- less prone to cross-talk

E.g. MALTA, TJ MONOPIX. CLICTD, FASTPIX, ALICE, ARCADIA
For timing: large wf, small landaus

ATLAS and Mu3e

Large collection electrode to fully deplete

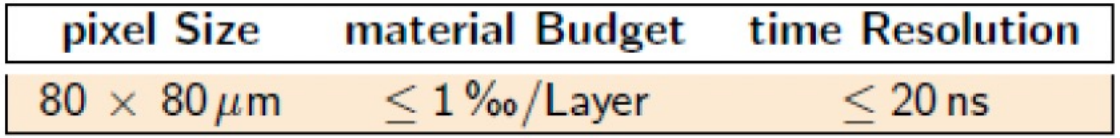




The **collection diode occupies a large part of the pixel**

- Electronic circuits inside deep n-well
- HV O(60 – 120V) contacts at the top side
- MUPIX8 pixel: 80x81 µm2
- Circuitry in the collection diode introduces additional sensor capacitance
- Keep pixel circuitry as simple as possible
- Confine digital circuitry at the periphery

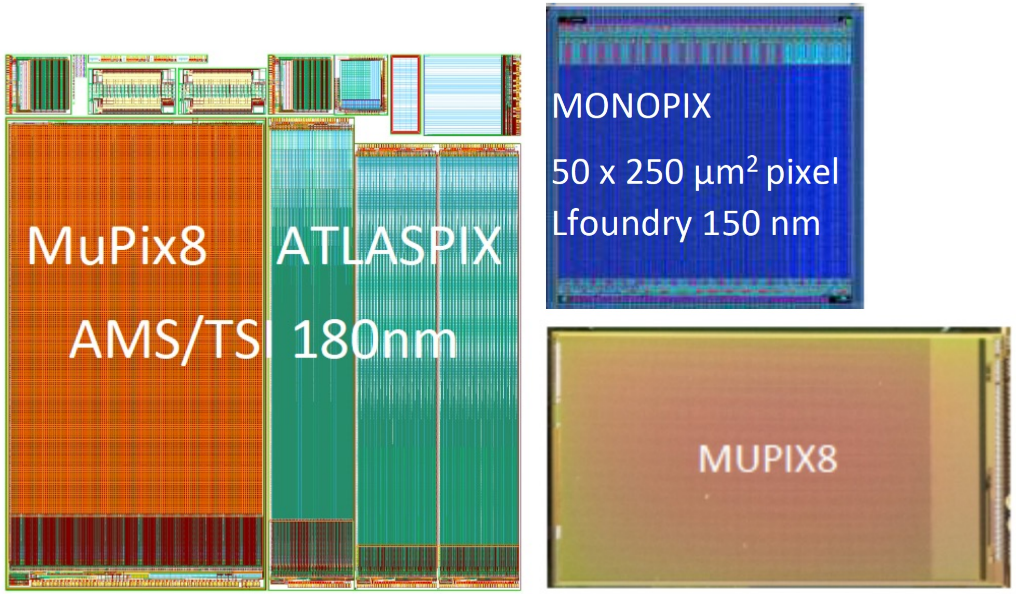
Mu3e

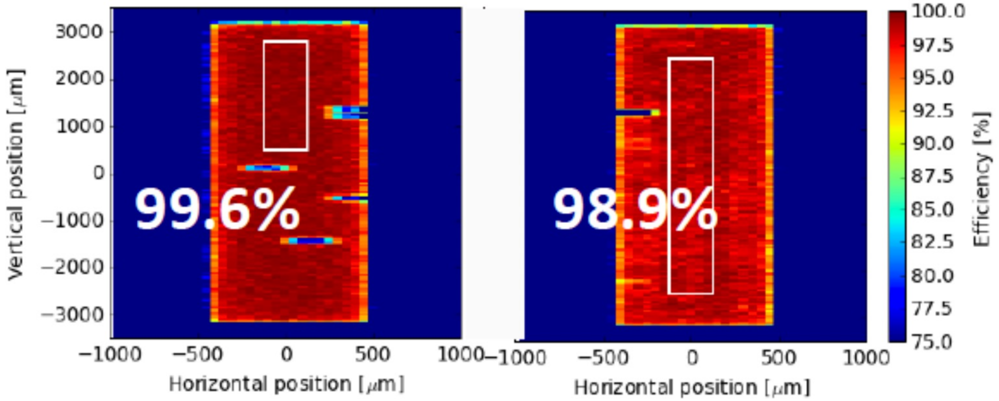


pixel Size	material Budget	time Resolution
$80 \times 80\,\mu m$	$\lesssim 1$ ‰/Layer	$\lesssim 20$ ns

ATLAS and Mu3e

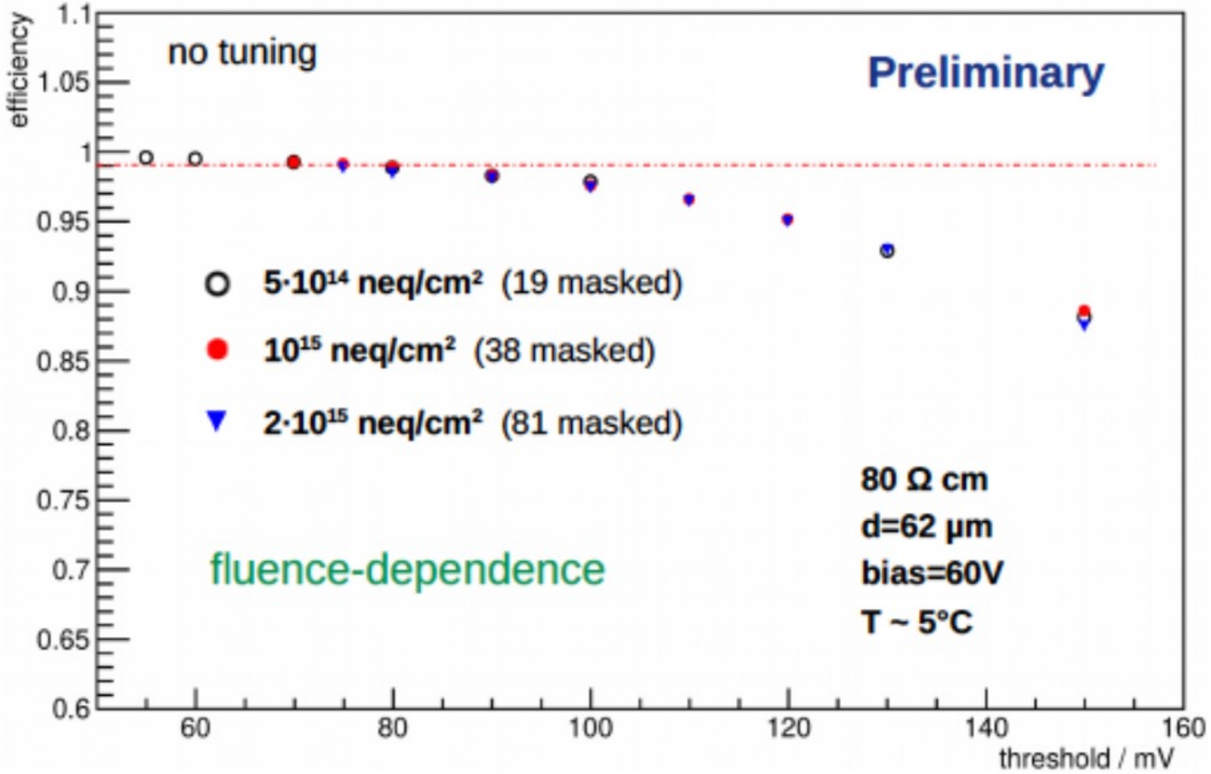
Large collection electrode to fully deplete




Efficiency non-irradiated after 1.14 E15 n_{eq}/cm^2

T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

Better sensor radiation tolerance and timing:
rad hard, but large C (100fF or more)



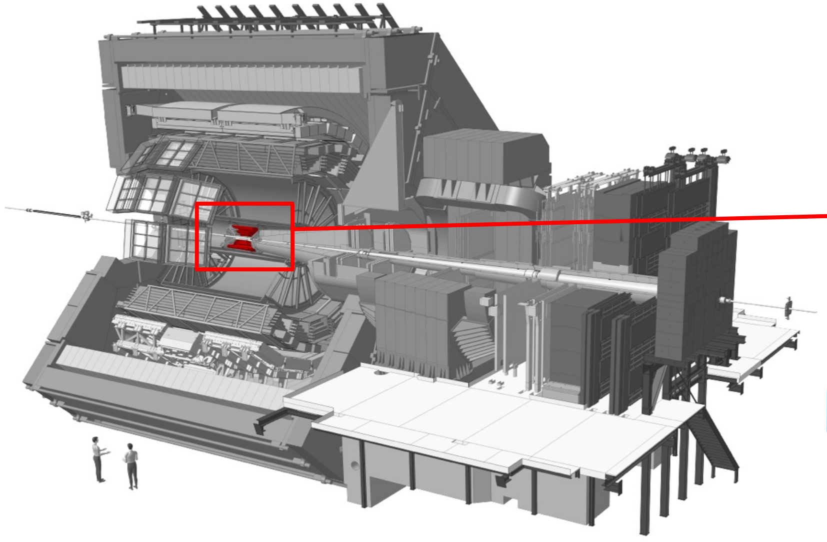
Courtesy I.Peric and A. Schoening

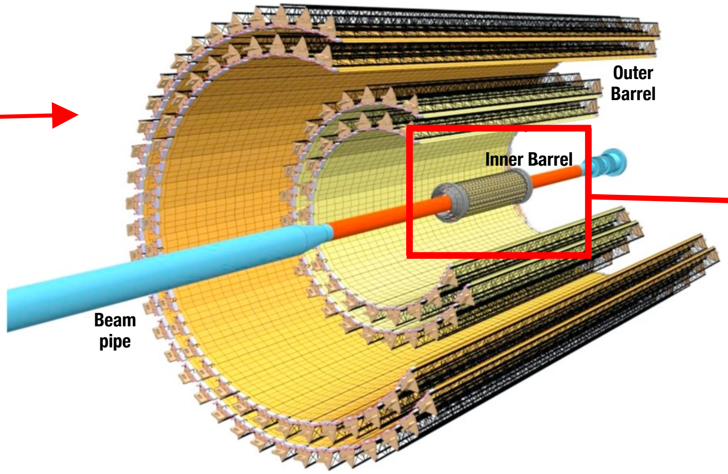
ALICE

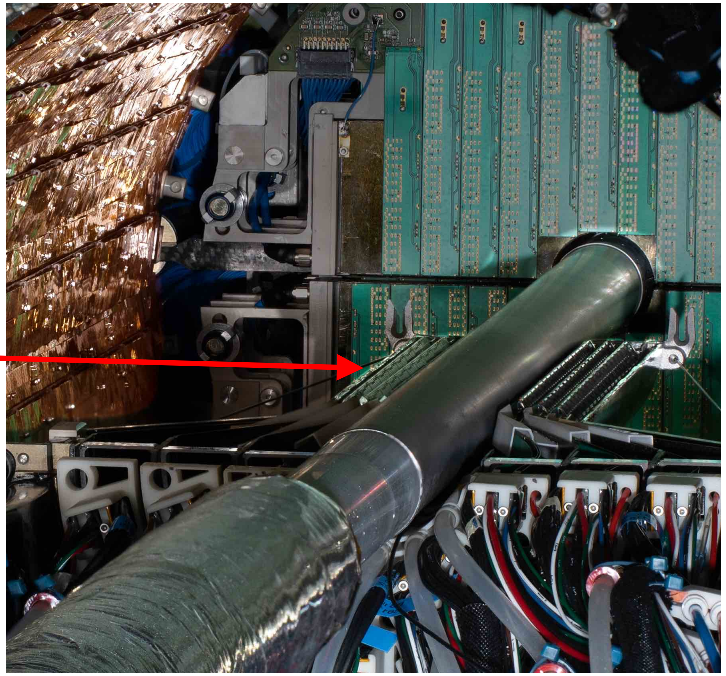
How can we further improve the ITS2 performance?

LHC LS3, 2027/28

ITS2 → **ITS3**







Q. **Can we further improve the ITS2 performance?** → A. **Yes, replacing the 3 innermost layers** with new ultra-light, truly cylindrical layers

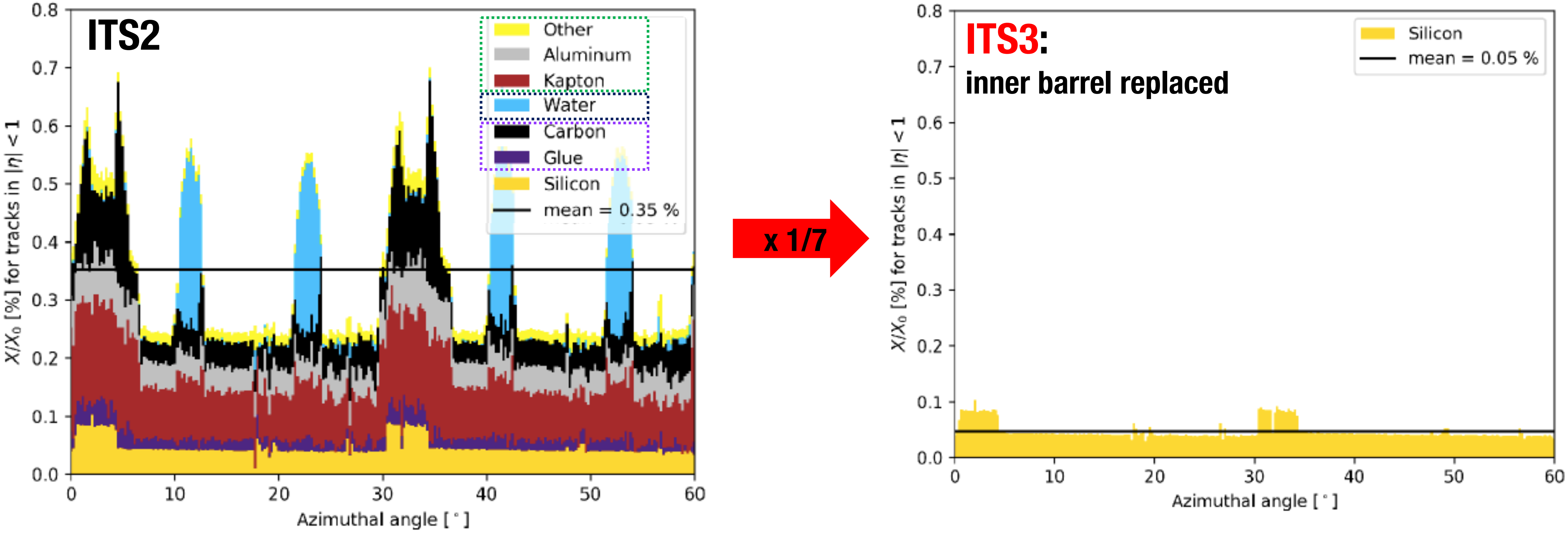
N.B. Important similarities between vertex detector requirements for **FCC$_{ee}$** factories and for ALICE upgrades & **EIC**

ALICE ITS3

LHC LS3, 2027/28

How can we further improve the ITS2 performance?

Replacing the 3 innermost layers



- **Circuit board** → not required if integrated in circuit (stitching)
- **Water cooling** → not required if power consumption < 20 mW/cm^2
- **Mechanical support** → not required if self supporting arched structure

ALICE ITS3: 6 truly cylindrical wafer-scale MAPS

From 432 flat to 6 bent sensors

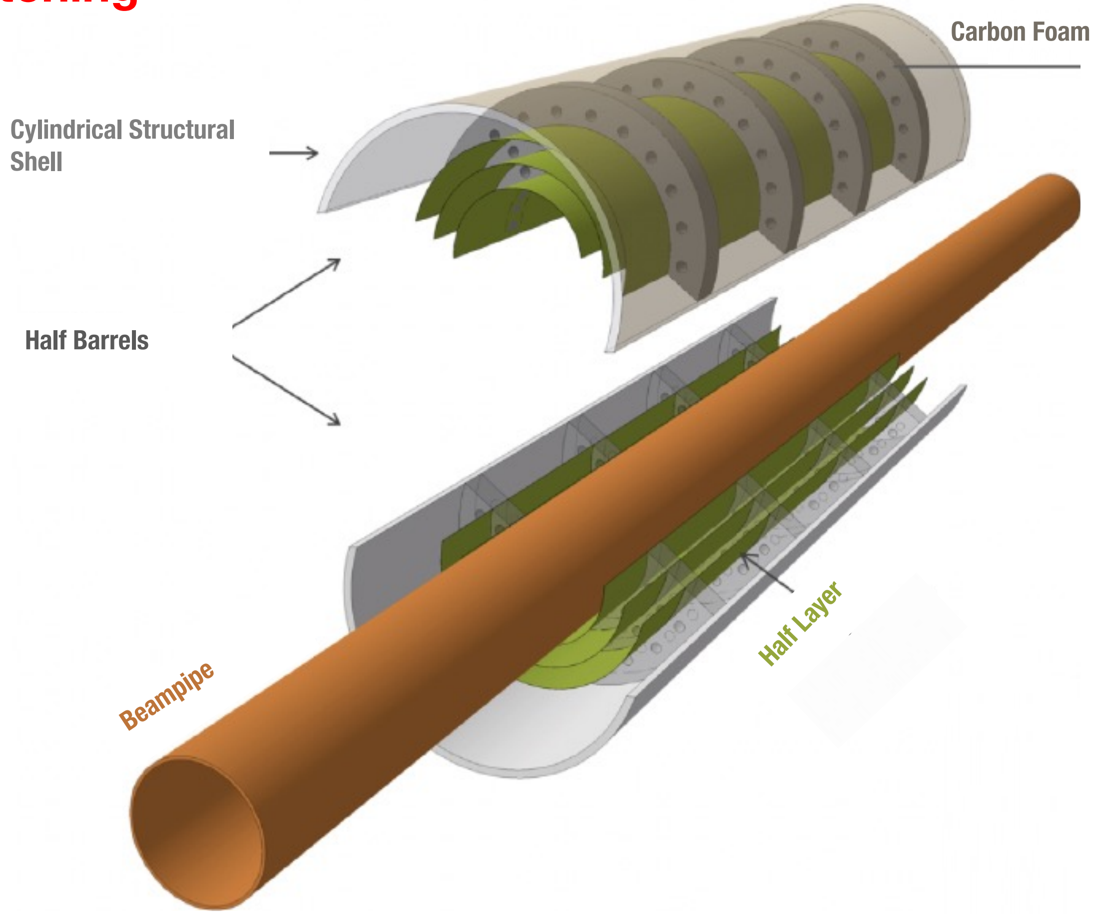
Key ingredients:

- **300 mm wafer-scale MAPS sensors**, fabricated using **stitching**
- **thinned down** to 20-40 μm, making them flexible
- **bent** to the target radii
  (L_0 23 mm → 18 mm, **closer** to the interaction point thanks to the new beampipe at 16 mm)
- mechanically held in place by carbon foam ribs
- cooled down by air

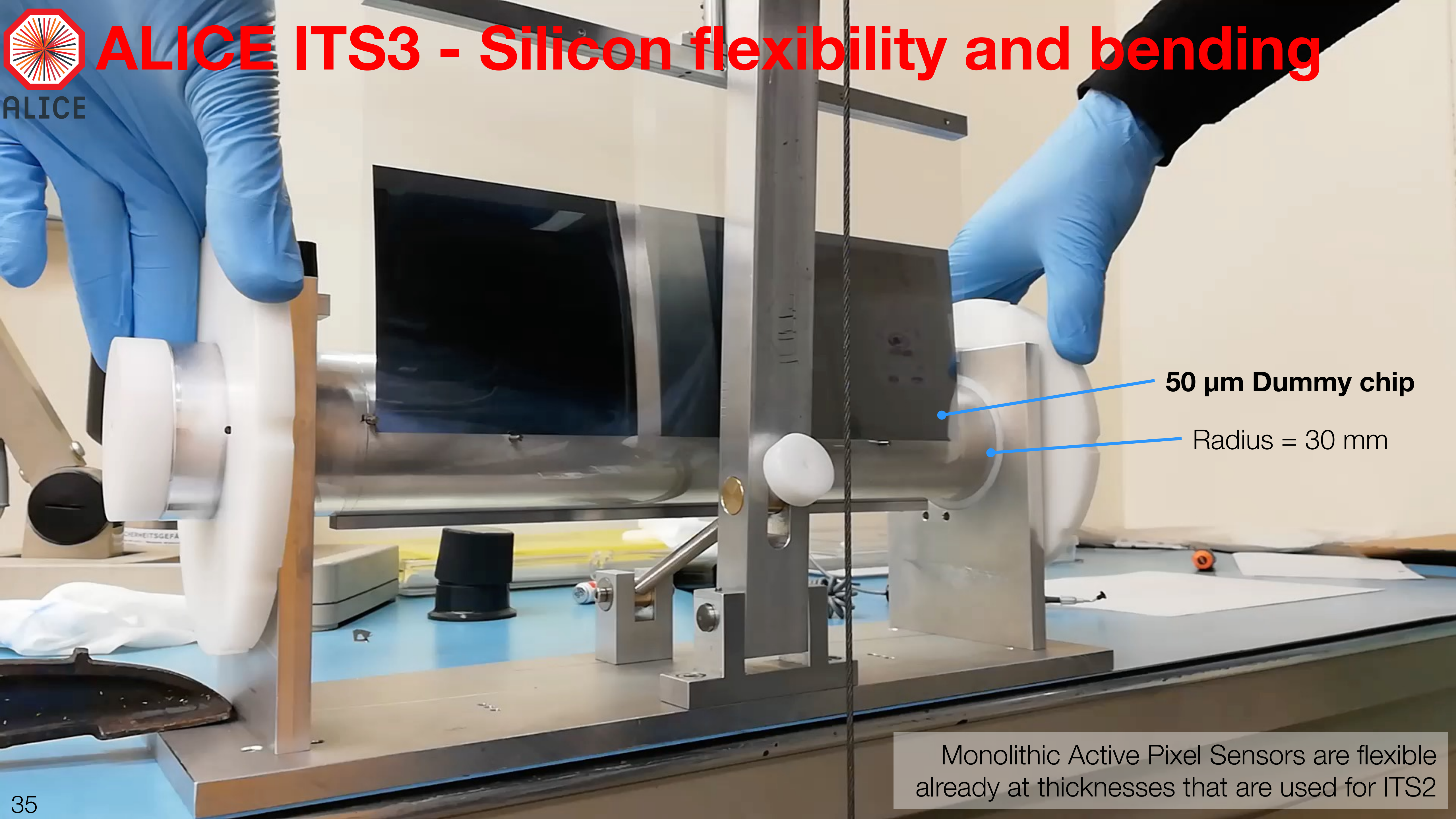
Key benefits:

- extremely **low material budget**: 0.02-0.05% X_0
  (beampipe: 500 μm Be, 0.14% X_0)
- **homogeneous** material distribution: negligible systematic error from material distribution

Detector concept

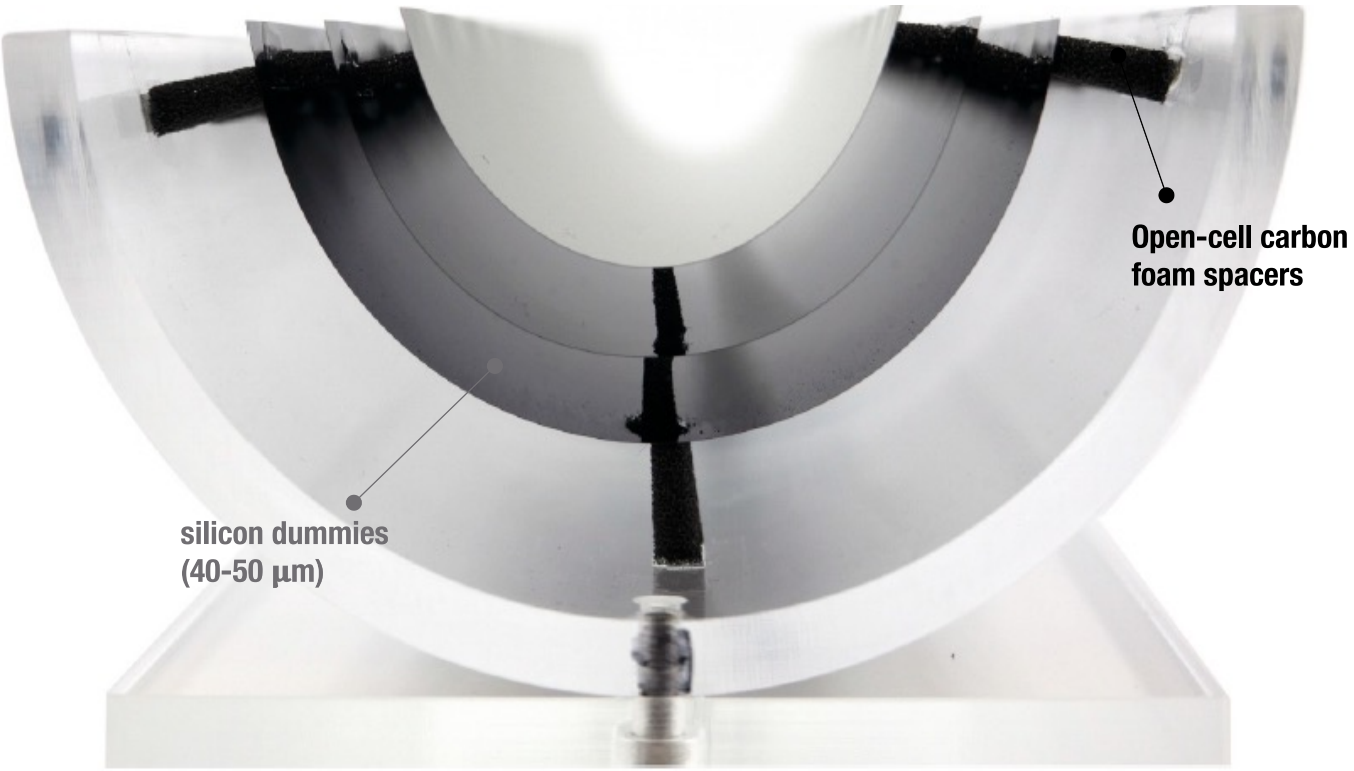


ALICE ITS3 - Silicon flexibility and bending



Monolithic Active Pixel Sensors are flexible already at thicknesses that are used for ITS2

ALICE ITS3 - Silicon flexibility and bending



Mechanical mockup of 3 truly cylindrical dummy layers
Radii: 18 mm, 24 mm, 30 mm

Final aim → turn these **dummy silicon** chips into a true single die monolithic pixel sensor

ALICE ITS3 – Sensor design

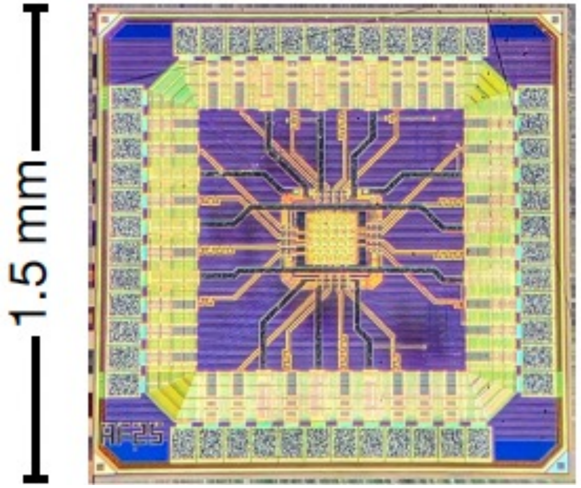
First submission in the Tower Partners Semiconductor (**TPSCo**) **65 nm technology**

Small collection electrode

Verification of the technology for charge collection efficiency, detection efficiency, radiation hardness:

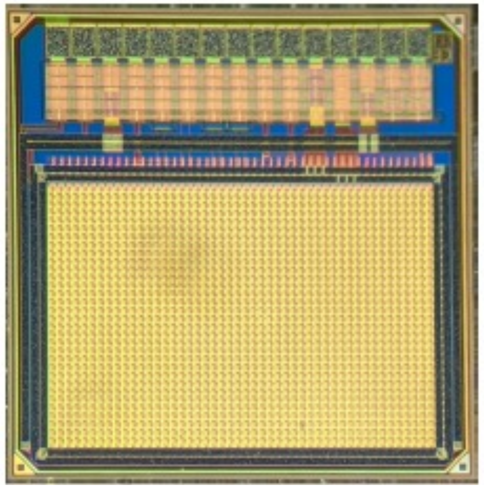
- larger wafers: 300 mm (instead of 200 mm), single “chip” is enough to equip an ITS3 half-layer
- smaller structure sizes to: lower power consumption, increase spatial resolutions, increase in-pixel circuitry, increase yield

APTS



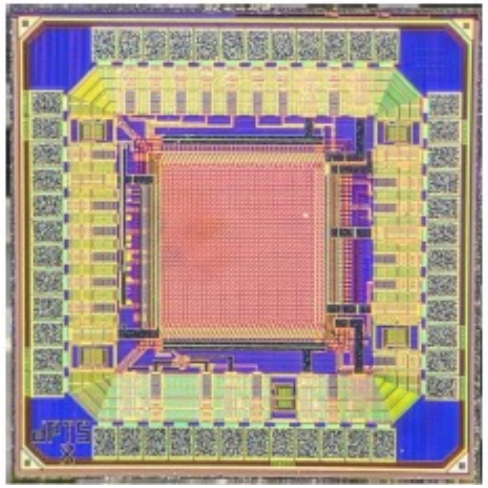
- **matrix**: 6x6 pixels
- **readout**: direct **analogue** readout of central 4x4
- **pitch**: 10, 15, 20, 25 μm
- **process**: 3 variants
- **design**: different nwell/pwell

CE65



- **matrix**: 65x32, 48x32 pixels
- **readout**: rolling shutter analog
- **pitch**: 15, 25 μm
- **process**: 3 variants

DPTS



- **matrix**: 32x32 pixels
- **readout**: async. **digital** with ToT
- **pitch**: 15 μm
- **process**: 1 variant

R&D - Process modification

First submission in the Tower Partners Semiconductor (TPSCo) 65 nm technology

Small collection electrode

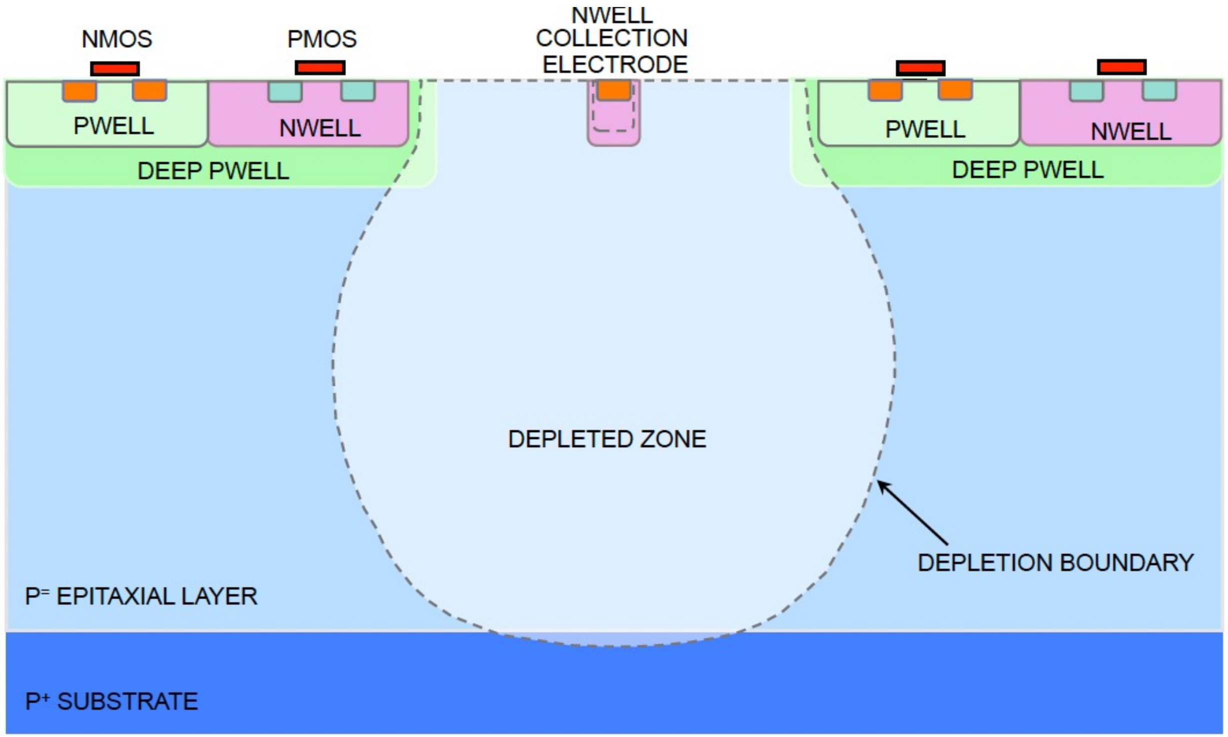
ALICE received **3 variants processes**, indeed spherical junction depletion thickness → proportional only to cubic root of reverse bias, inner radius R1 to be kept small for low capacitance → Deep pwell and substrate limit extension of the depletion layer

Planar junction, delpetion width

$$w \simeq x_n \simeq \sqrt{\frac{2\epsilon V}{eN_D}}$$

Spherical junction, outer depleation radius

$$\sqrt[3]{\frac{2\varepsilon|V|}{qN_A}\frac{3R_1}{2}}$$



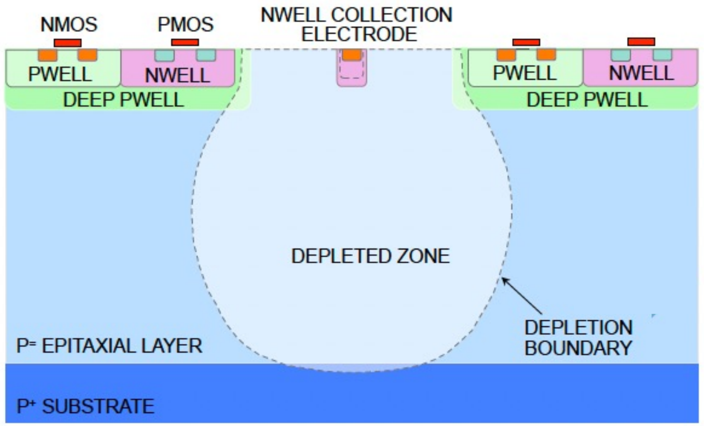
Need process modification:

→ **development in MALTA, Monopix, ALICE, CLICpix, … :**

move junction away from the collection electrode to create a planar junction and deplete the epitaxial layer

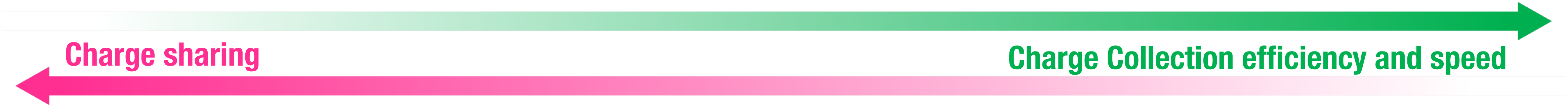
https://doi.org/10.3390/s8095336

R&D - Process modification

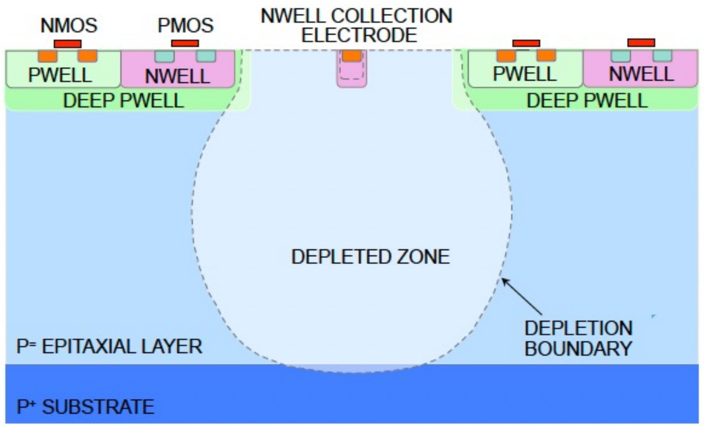


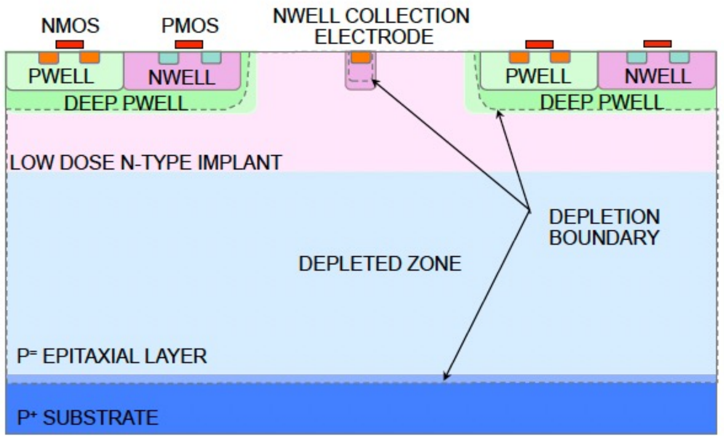
Standard ALICE ITS2 type

- High res. p-type epi. (> 1 kΩ.cm)
- INMAPS process
- Reverse bias typ. -3 V
- enhanced (but not yet full) depletion
- some charge collected by diffusion only → slow
- Operation up to 10^{14} n_{eq}/cm^2



R&D - Process modification





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Modified implement a planar junction (N implant) separate from the collection electrode

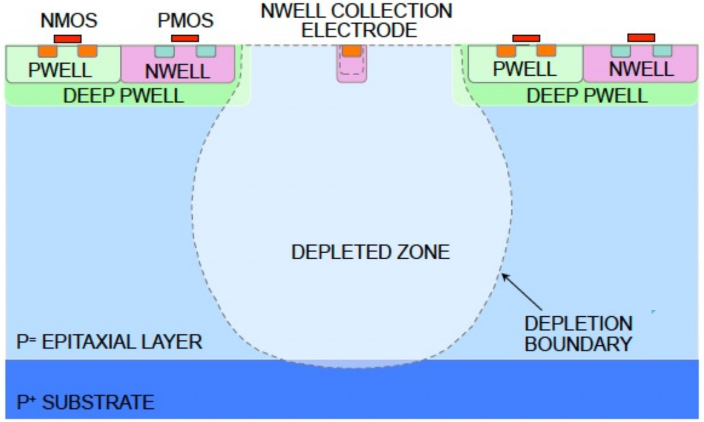
- **full volume can be depleted**
- Charge collection time < 1 ns
- Operational up to 10^{15} n_{eq}/cm^2
- better charge collection in lateral direction
- Maintain small capacitance
- No significant circuit/layout changes

https://dx.doi.org/10.1016/j.nima.2017.07.046

Charge sharing

Charge Collection efficiency and speed

R&D - Process modification



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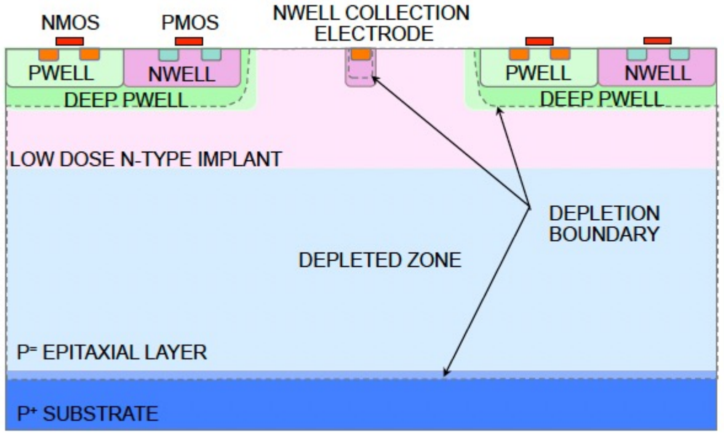

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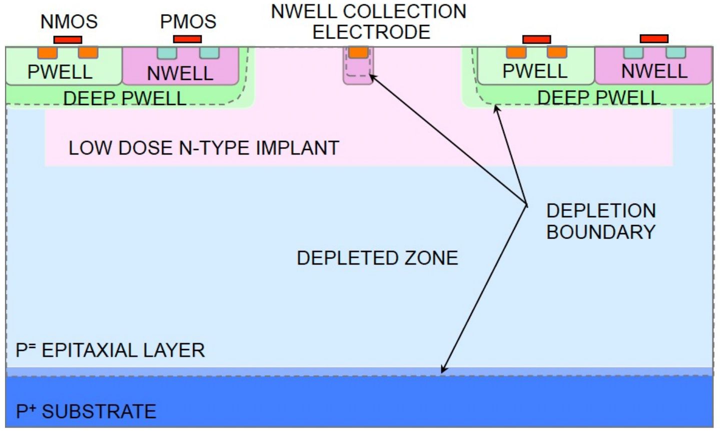
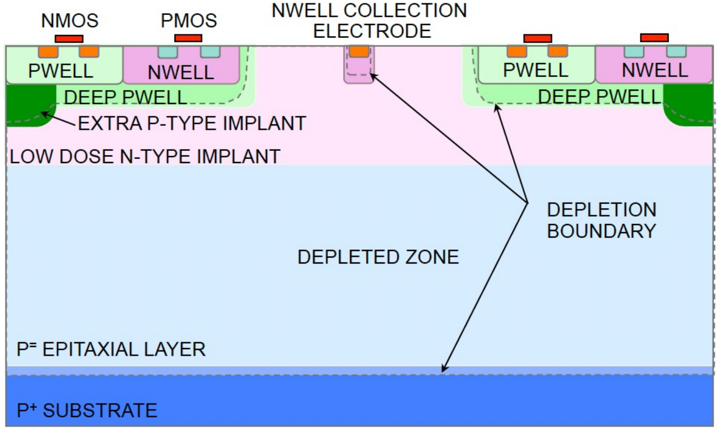


Modified with gap Additional gap in the low dose n-type implant

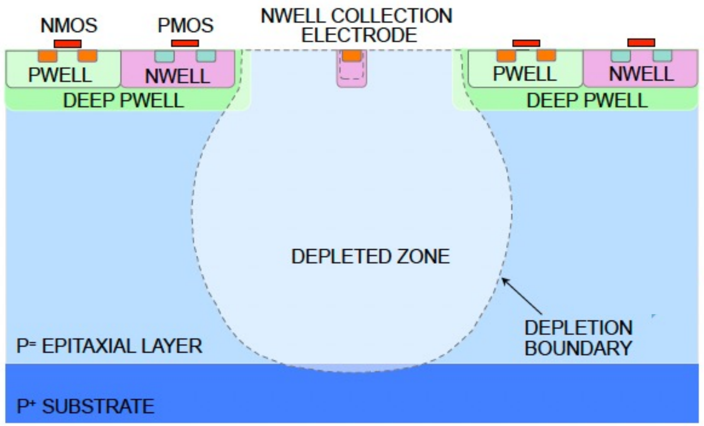


Modified extra implant Additional deep p-type implant in the low dose n-type implant

Charge sharing

Charge Collection efficiency and speed

R&D - Process modification



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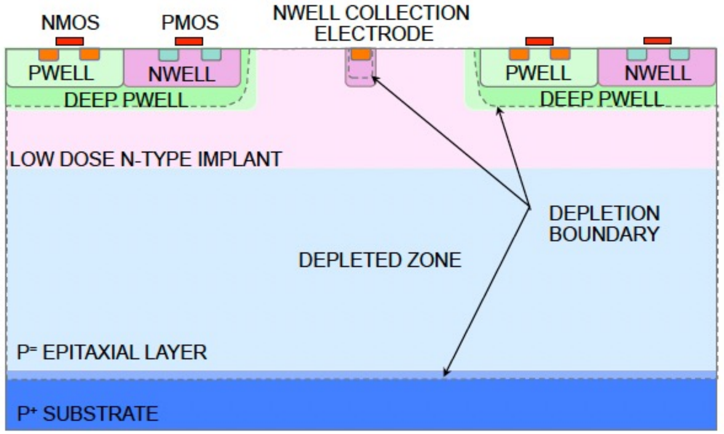

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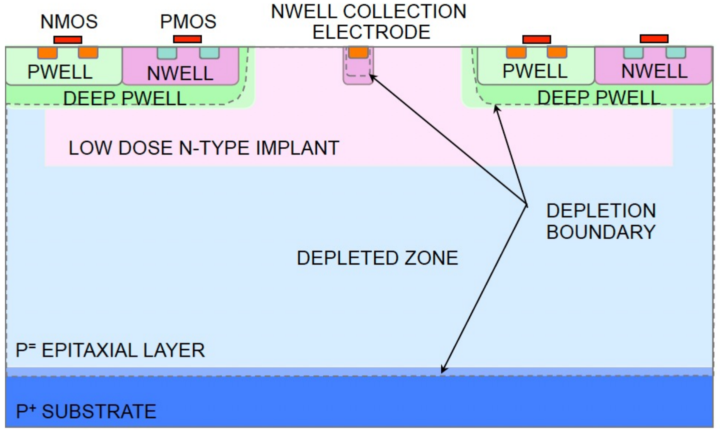
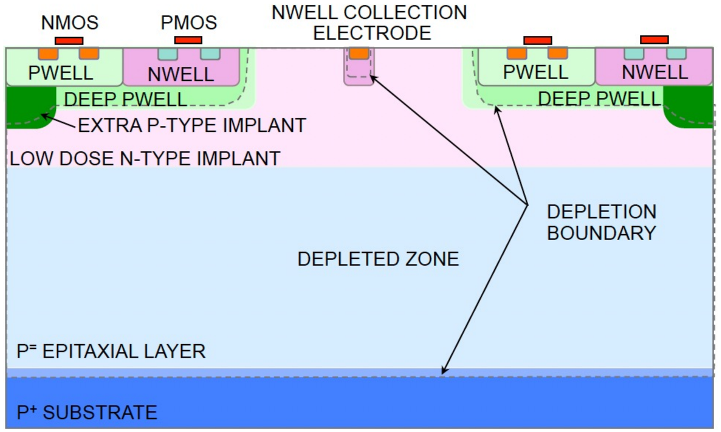
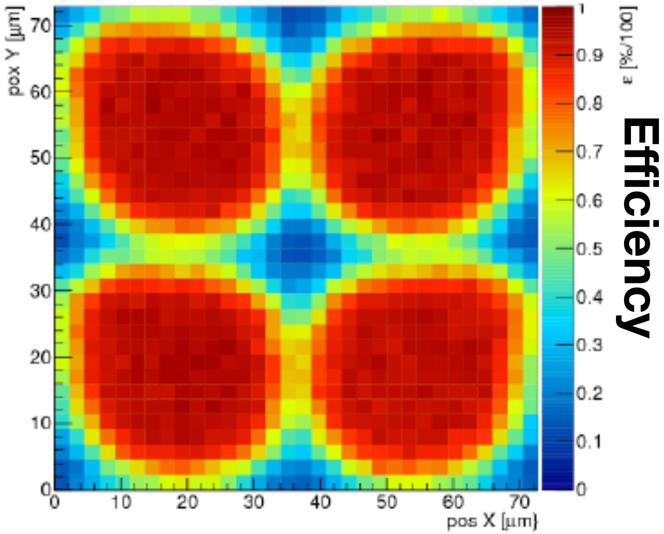


Modified with gap Additional gap in the low dose n-type implant



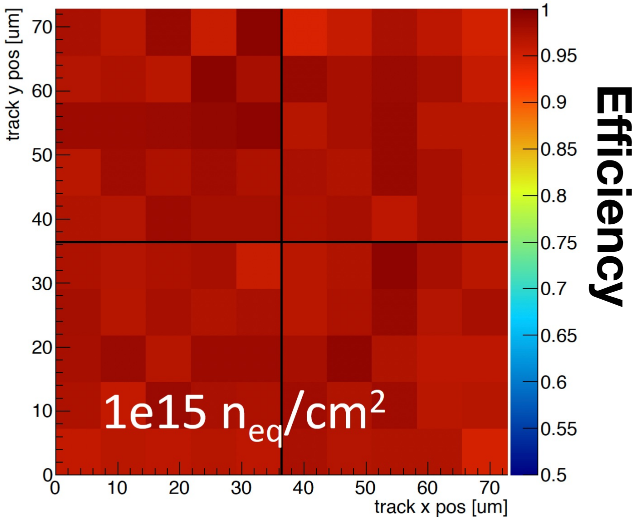
Modified extra implant Additional deep p-type implant in the low dose n-type implant

Modified

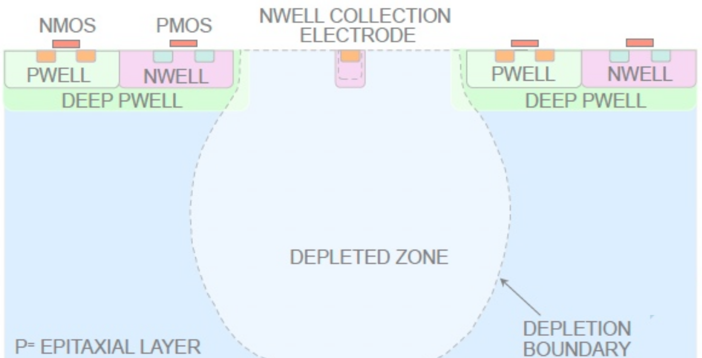


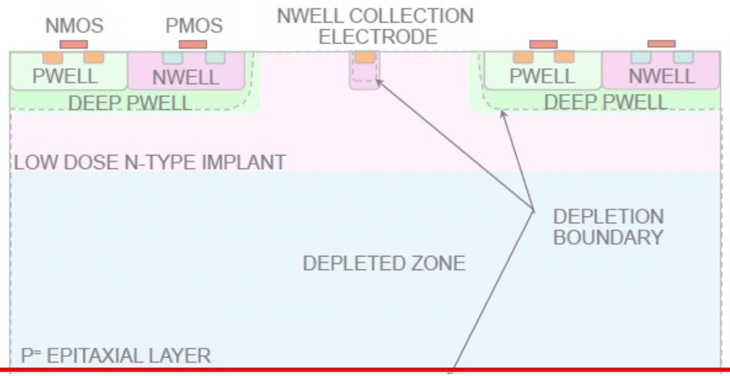
Modified with gap or extra implant

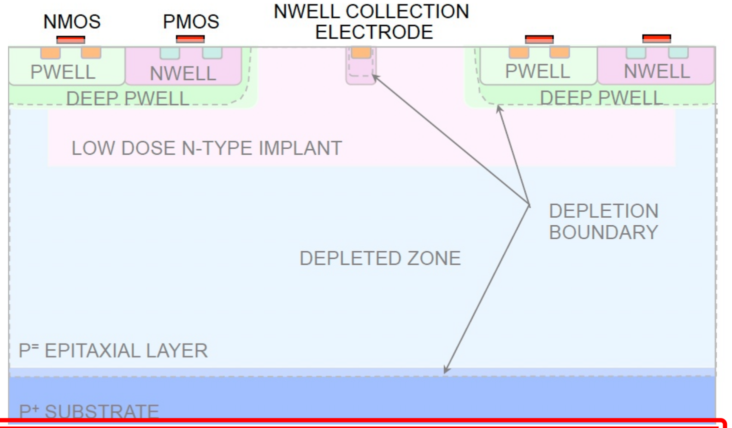
miniMalta in pixel efficiency, sector 1



R&D - Process modification







Disclaimer: just one among similar developments for full depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483

H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027

S. Kawahito et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027

L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027

C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

And other project names; FASTPIX ATTRACT, SEED, ARCADIA

"I need a simple fix. No one asked you to reinvent the wheel."

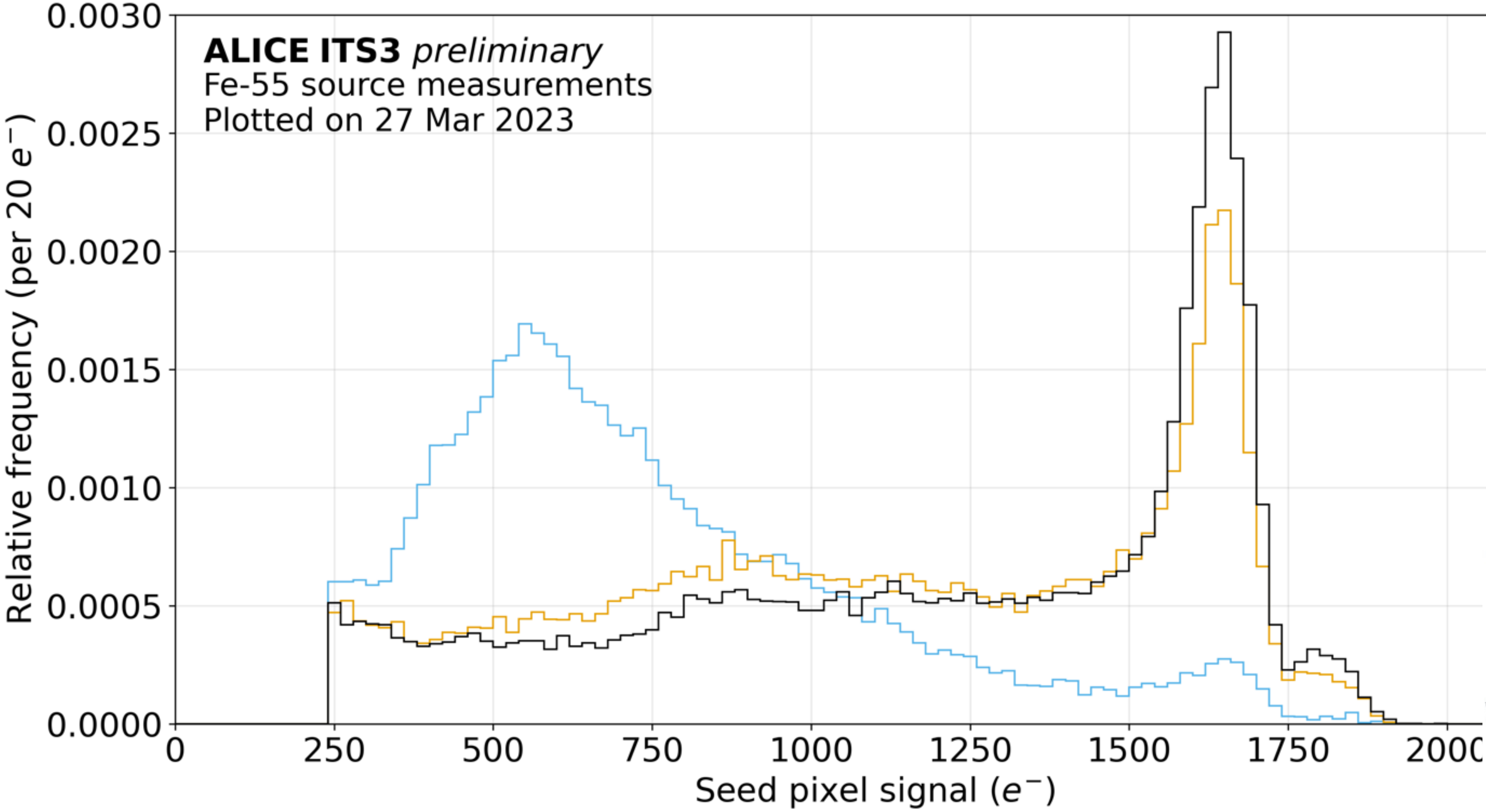
Modified extra implant Additional deep p-type implant in the low dose n-type implant

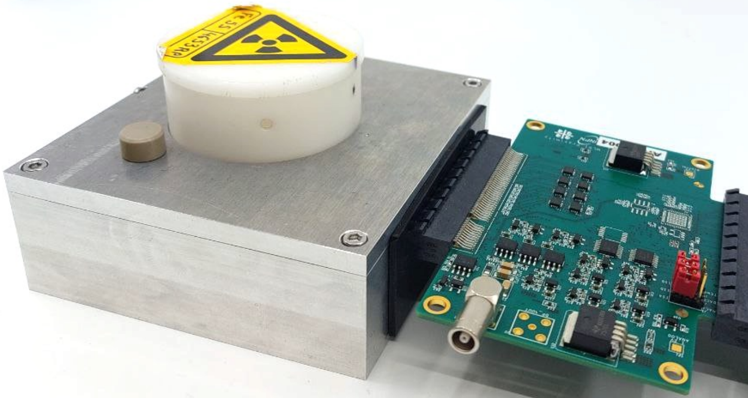
ALICE ITS3 – Sensor design

First submission in the Tower Partners Semiconductor (TPSCo) 65 nm technology

Small collection electrode

→ Process modification in 65 nm, 3 variants processes: standard, modified and modified with gap





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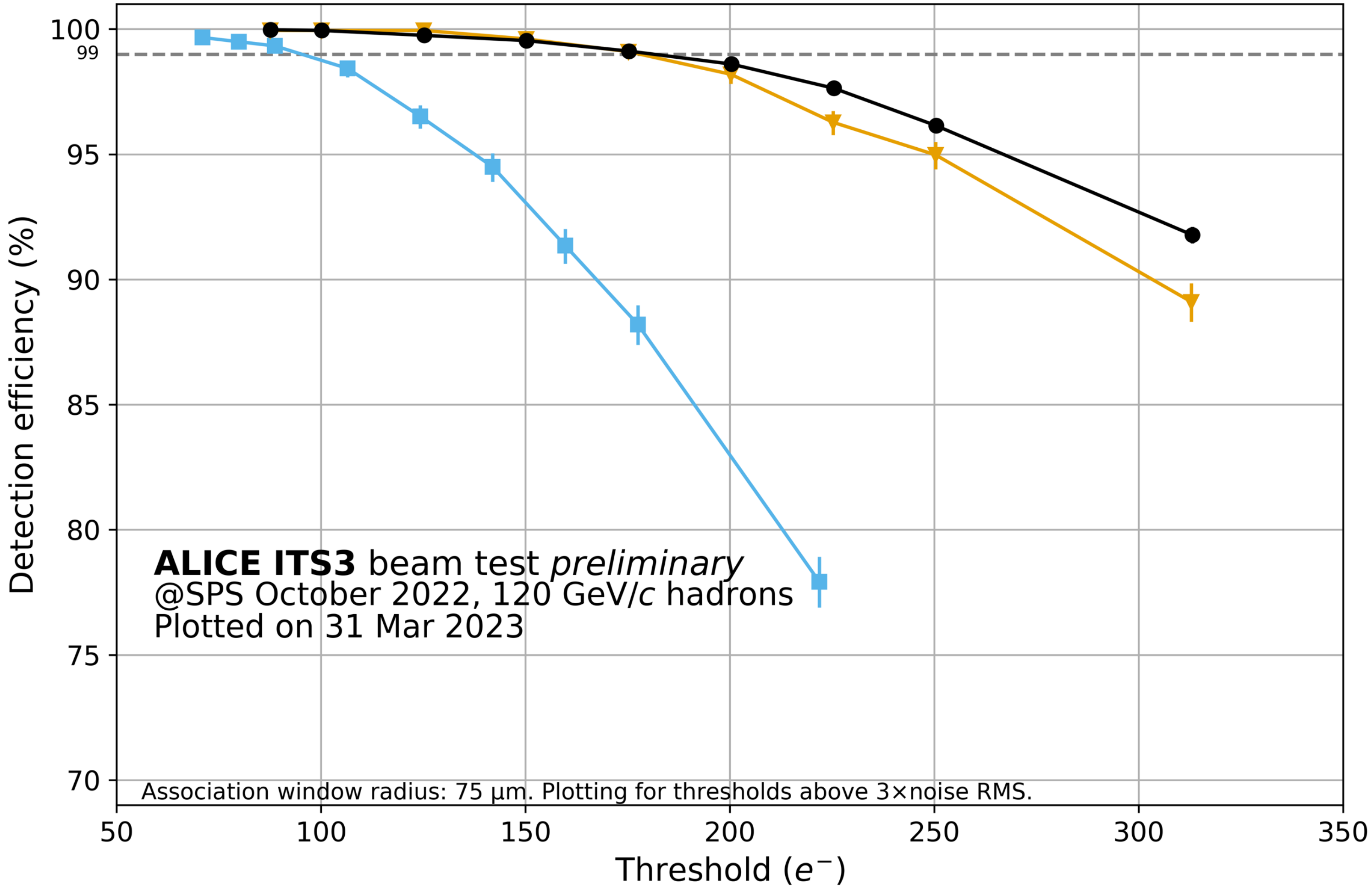
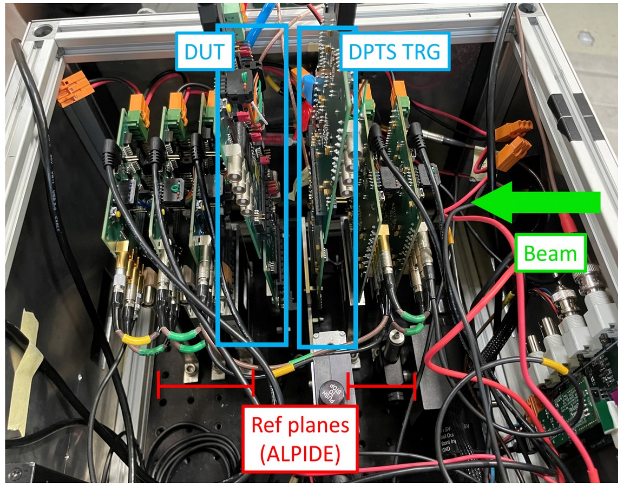


APTS SF
Non-irradiated
pitch: 15 µm
split: 4
I_{reset} = 100 pA
I_{biasn} = 5 µA
I_{biasp} = 0.5 µA
I_{bias4} = 150 µA
I_{bias3} = 200 µA
V_{reset} = 500 mV
$V_{pwell} = V_{sub}$=-1.2 V
T = 20 °C



ALICE ITS3 – Sensor design

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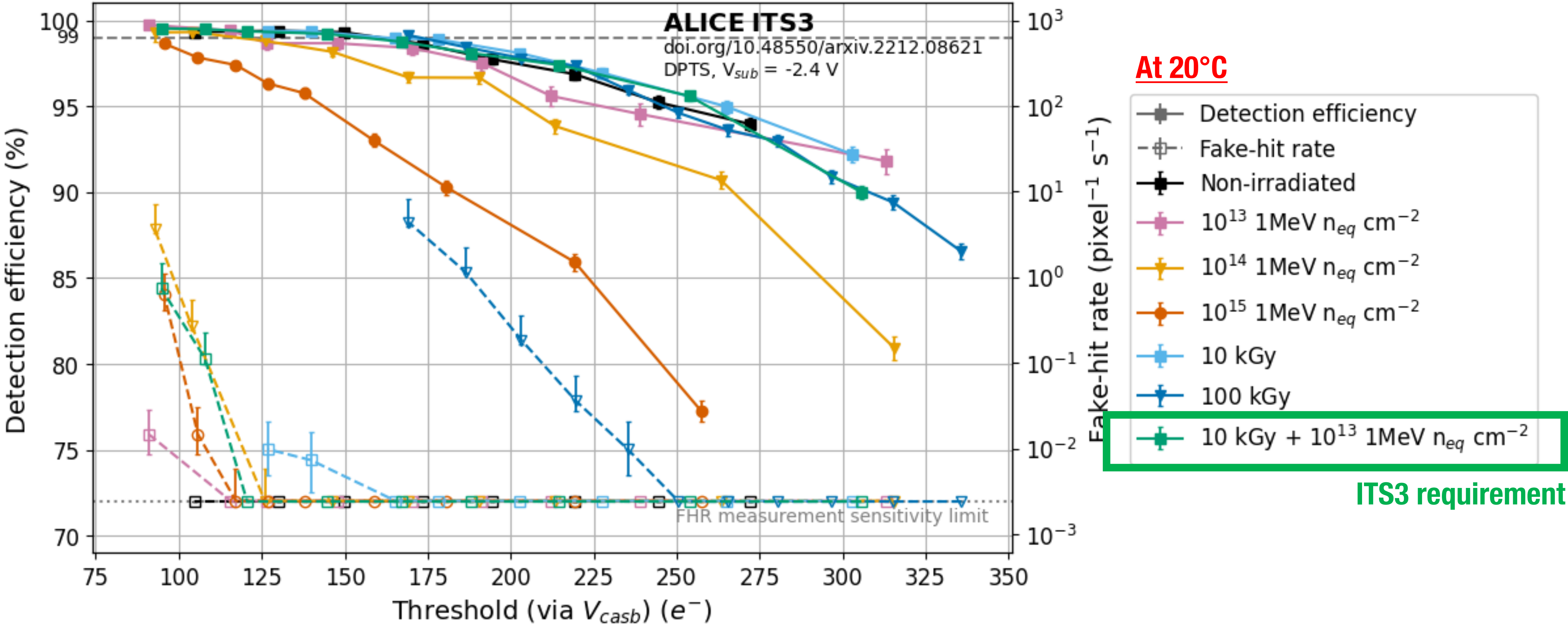
Small collection electrode



ALICE ITS3 – Stitching

our target: ~**280 x 94 mm**

For such large area → stitching needed:
aim at a realization of **a true single wafer scale sensor**

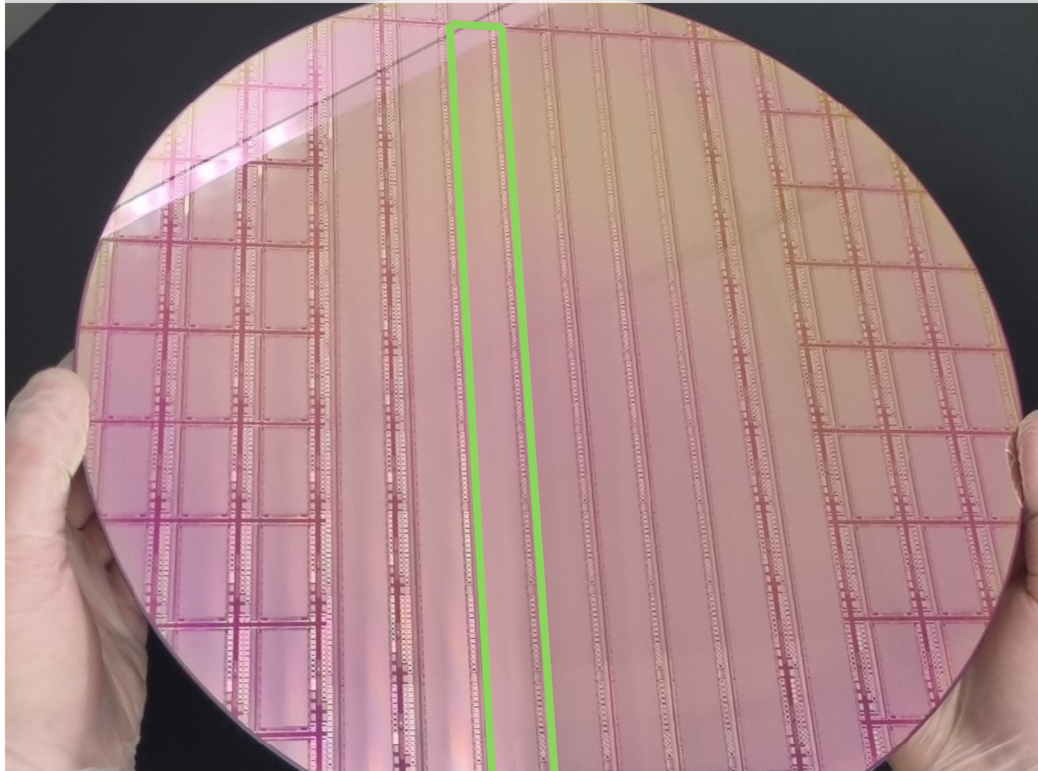
Required dedicated design effort:

- understanding **stitching** rules to make a particle detector
- redundancy, fault tolerance

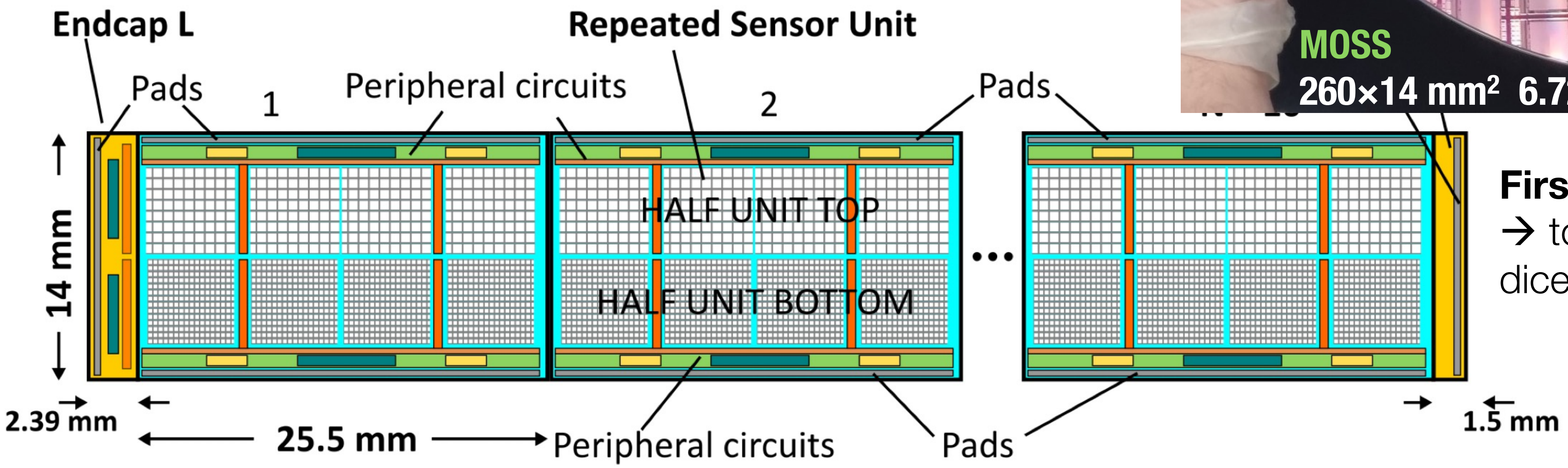
Crucial exercise to understand:

- **yield**
- **uniformity**

First MAPS for HEP using stitching



MOSS
260×14 mm² 6.72 Mpixels

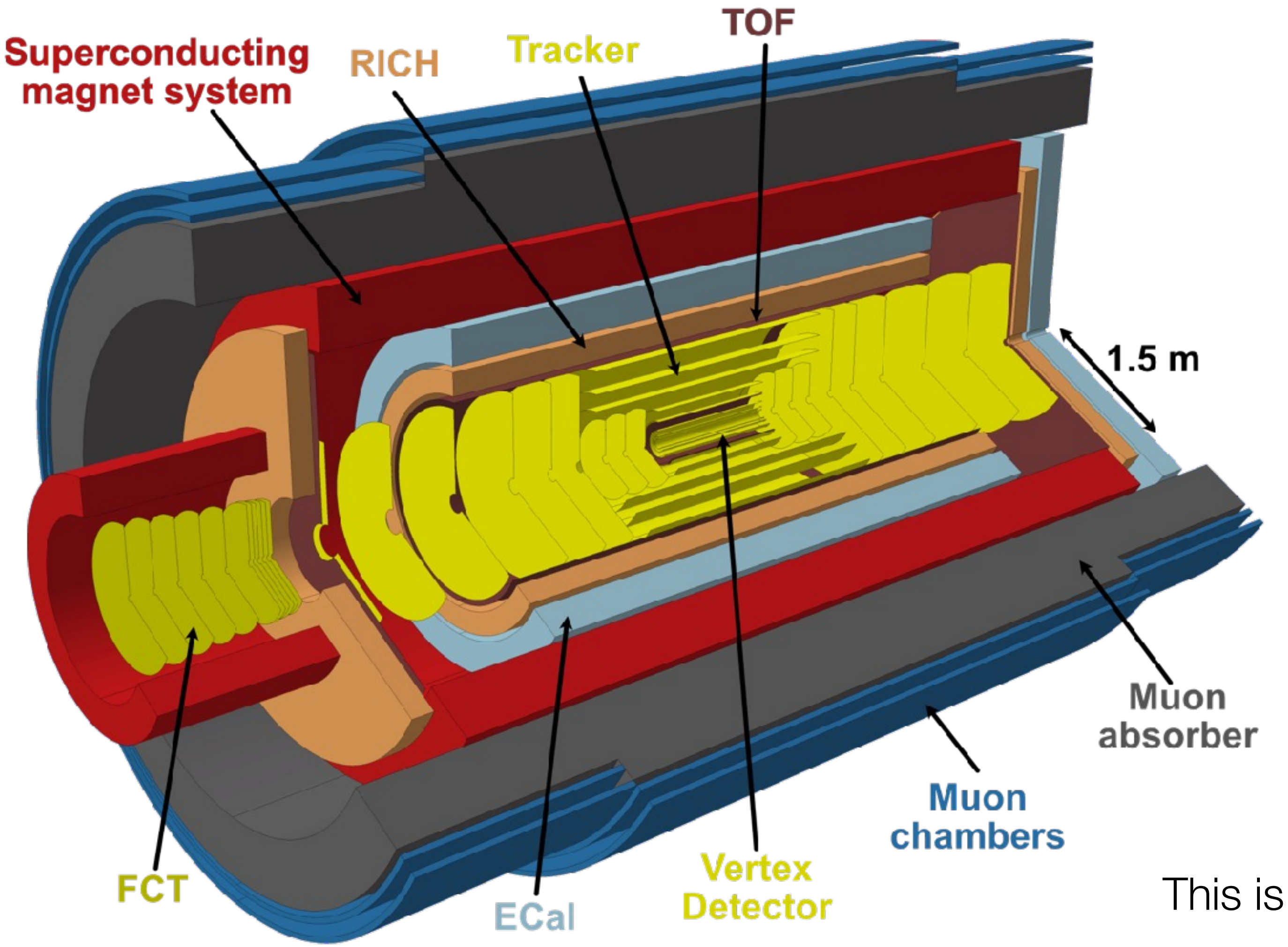


First wafers just received
→ to be thinned,
diced…and testet

ALICE3

LHC-LS4 2033/34, to start in Run5

a next-generation LHC heavy-ion (soft QCD) experiment



around a **60 m² MAPS** tracker:

- **outer tracker** will be **ITS2 like** (**but** order of magnitude **larger**)
- innermost layers (**vertex detector**) will be based on wafer-scale Silicon sensors "iris tracker", **ITS3 like** (**but in vacuum**)

This is the next big and concrete step for CMOS MAPS

ALICE3 – vertex detector

Unprecedented performance figures

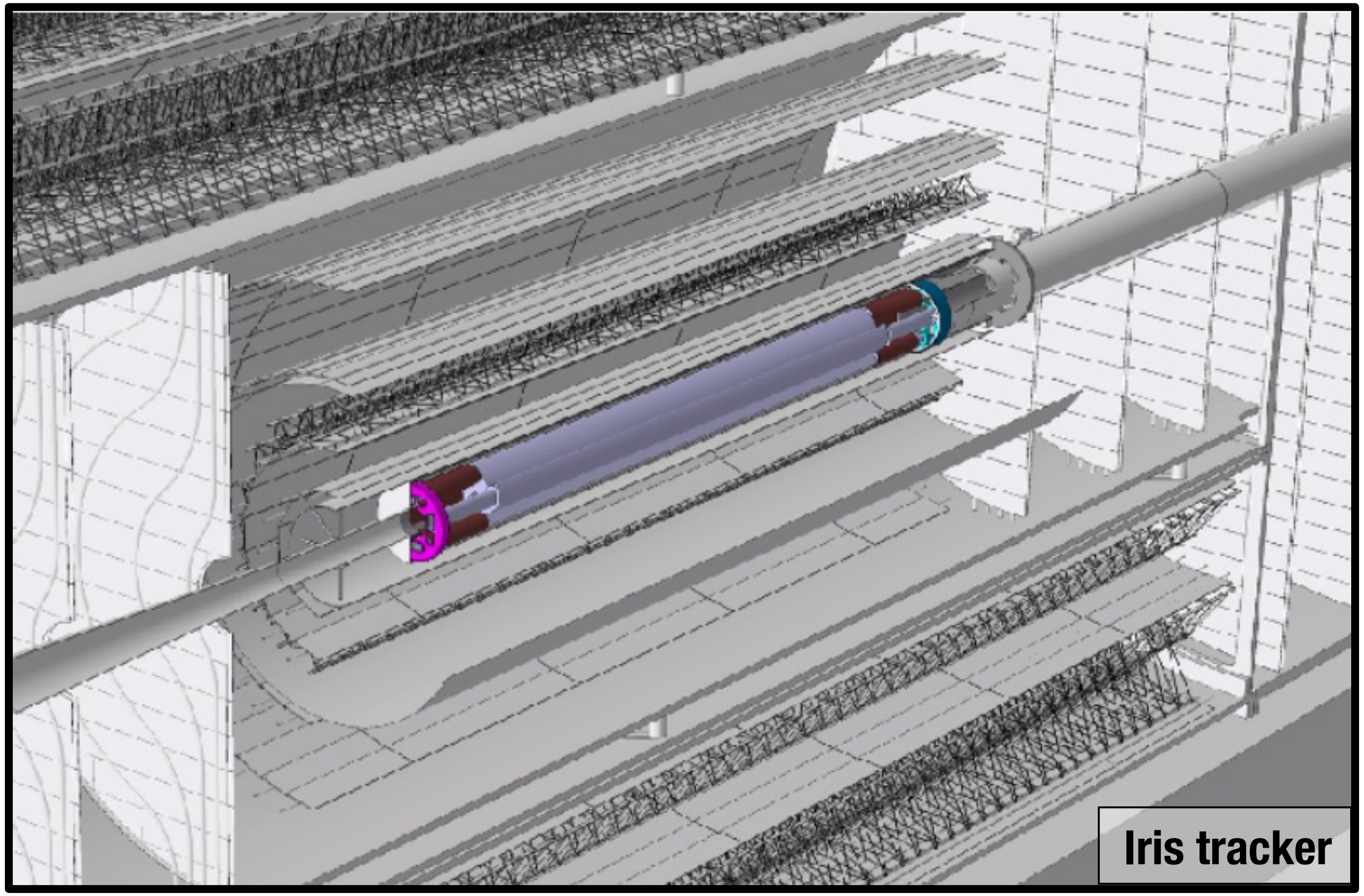
- clear **extension of ITS3 developments**
- pushes **improvements** on a number of fronts

Will be based on wafer-scale, ultra-thin, curved MAPS

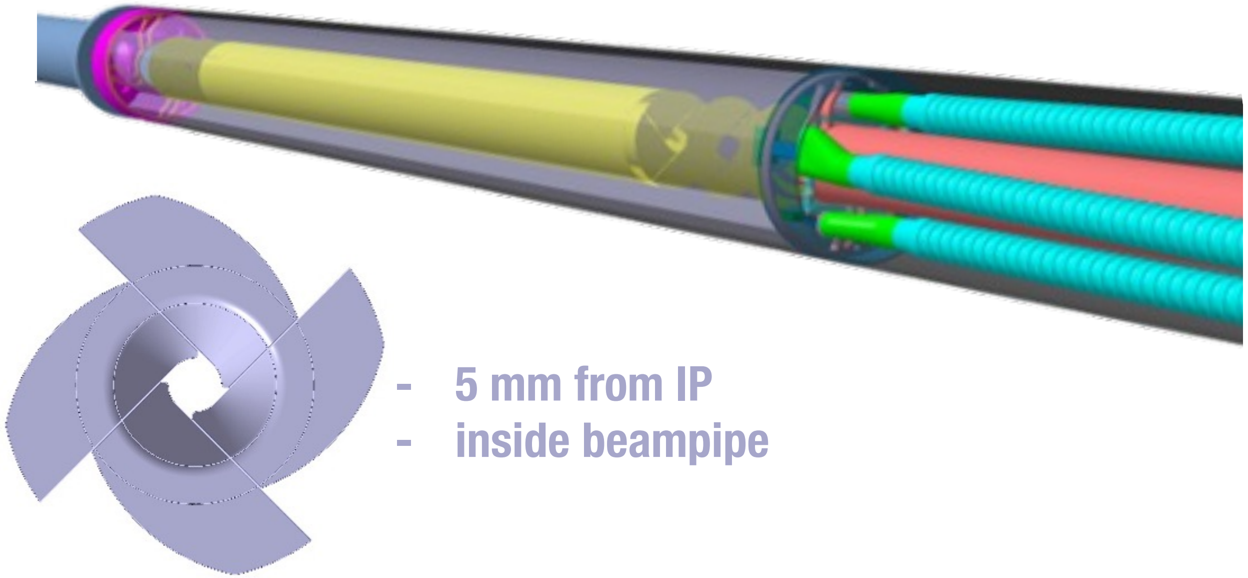
- distance from interaction point: **5 mm**
  → inside beampipe, retractable configuration

Requirements:

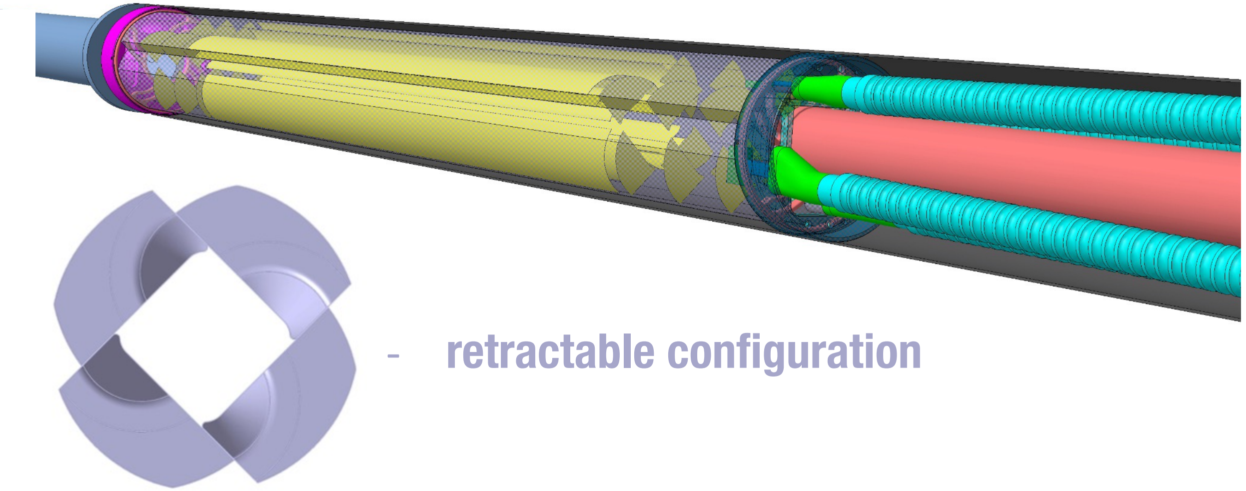
- spatial resolution: ≈ 2.5 µm
- material budget: ≈ 0.1%X_0/layer



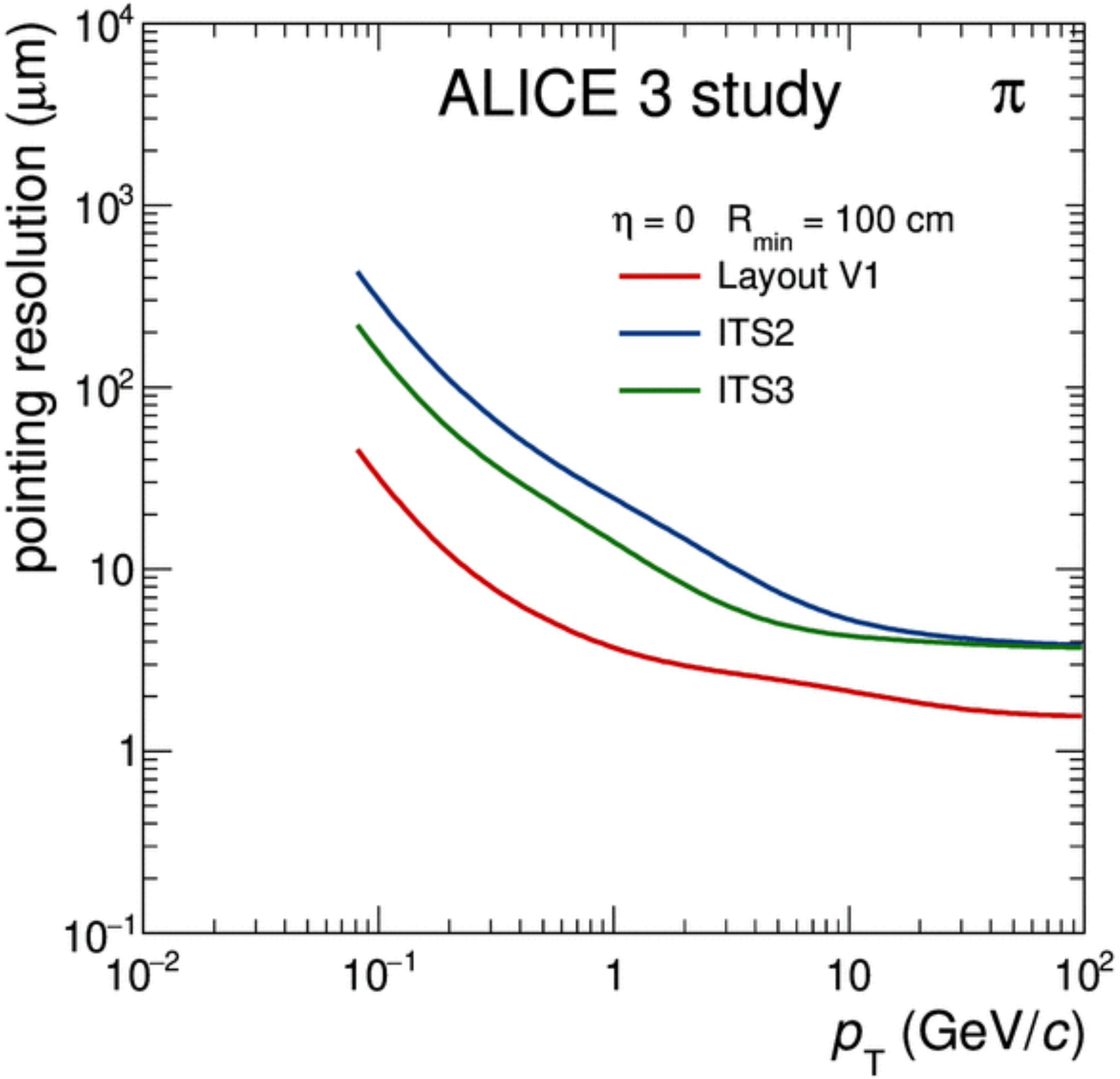
ALICE3 – vertex detector



- 5 mm from IP
- inside beampipe



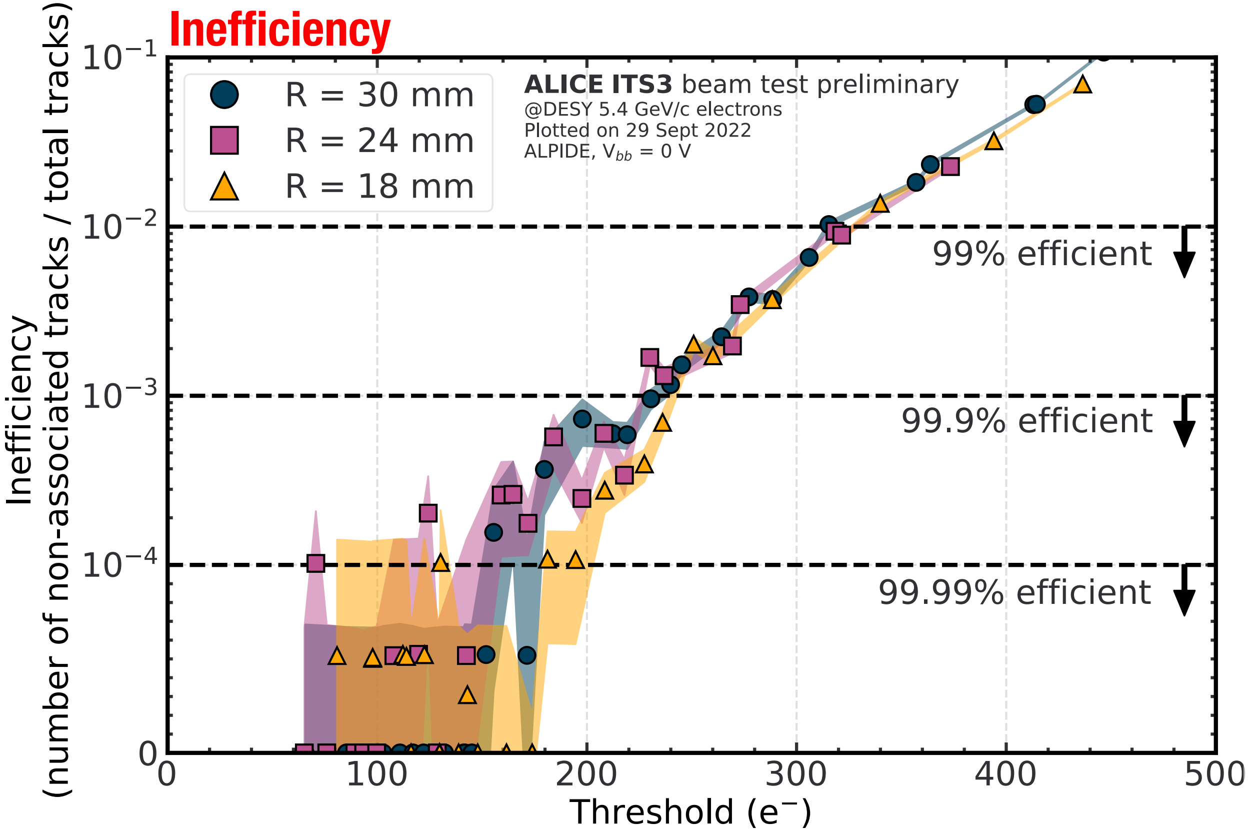
- retractable configuration

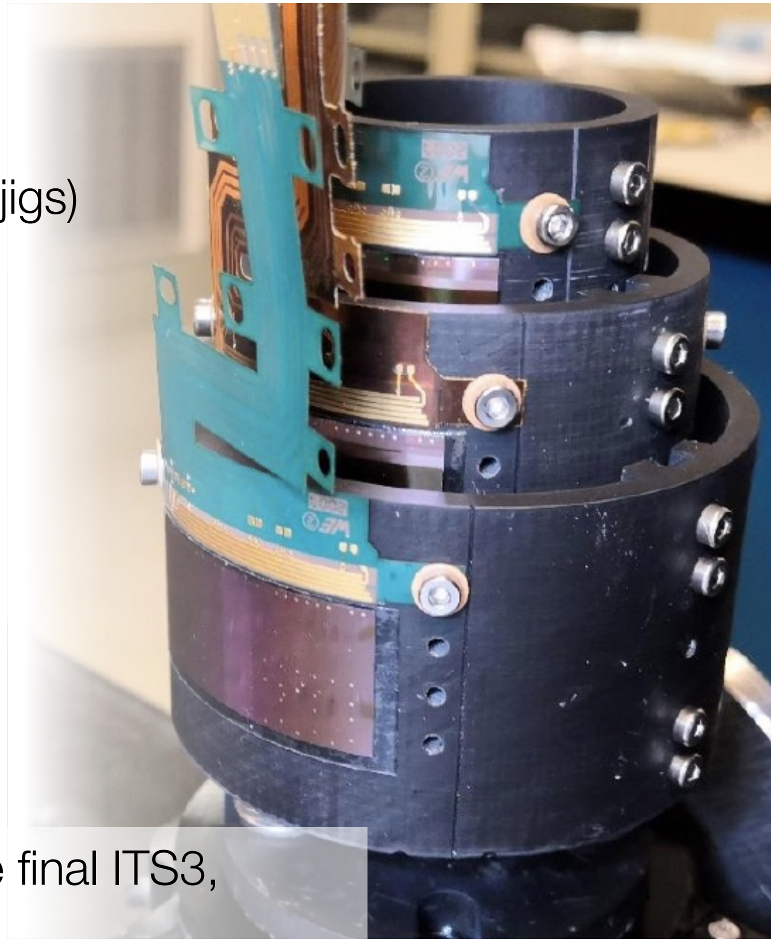


ALI-SIMUL-491785

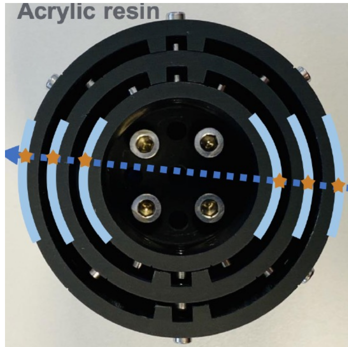
Other R&D ongoing – bending 180 nm

- Functional chips ALPIDEs have been bent bent routinely
- **Several ways** were explored (bending before bonding, or vice versa, different jigs)
- **The chips continue to work** (doi:10.1016/j.nima.2021.166280)



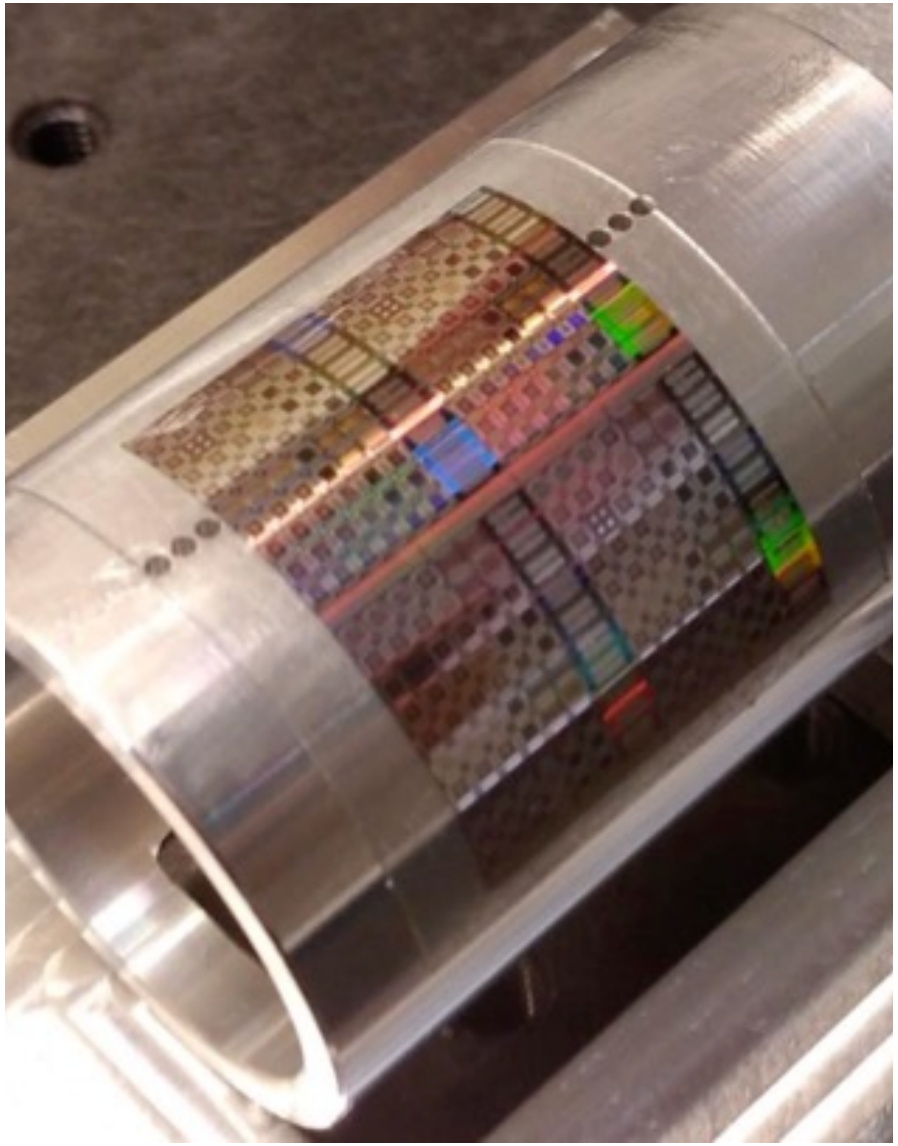


- Full mock-up of the final ITS3, called "**μITS3**" :
  - 6 ALPIDE chips, bent to the target radii of ITS3 tested
- **Beam test** on μITS3:
  - **uniform** among different radii

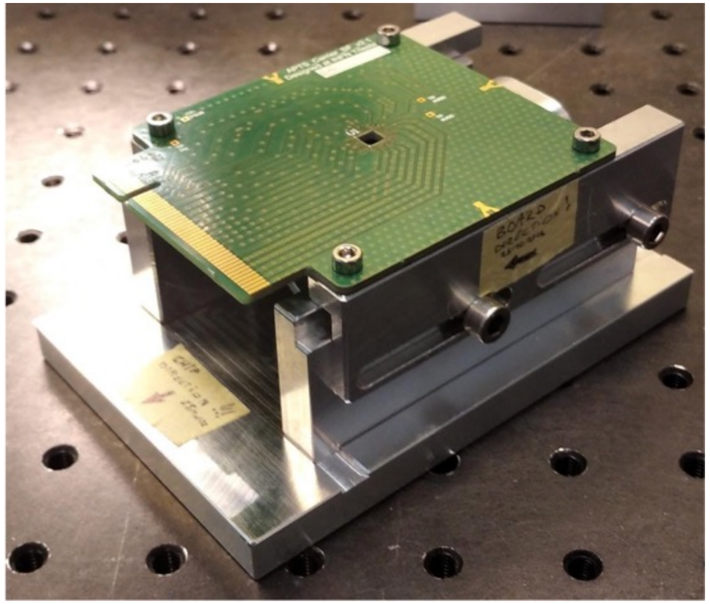


Other R&D ongoing – bending 65 nm

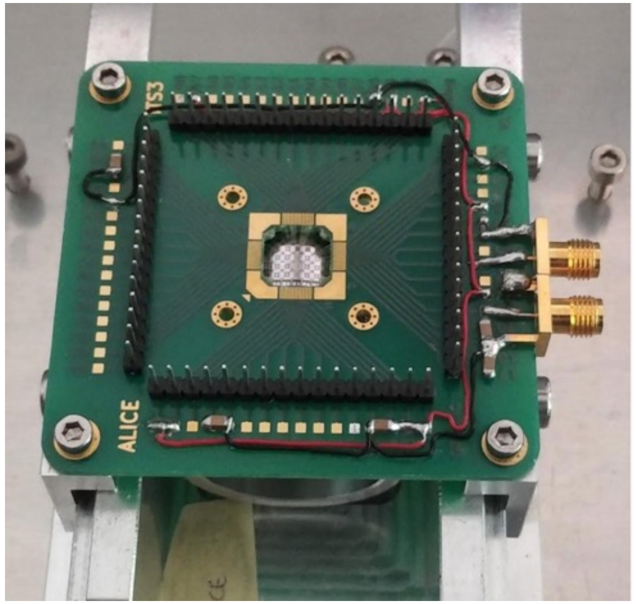
- **TPSCo 65nm chips bending**: both APTS and DPTS
- special boards developed to bond on the bent structure
- tests ongoing
  - so far all test structures are working
  - more measurements and sample preparation ongoing



APTS



DPTS



Other R&D ongoing – ACF

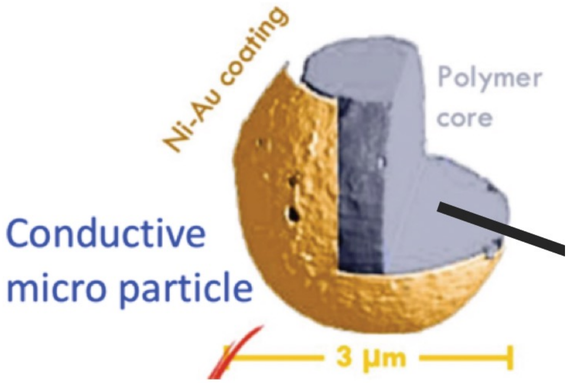
interconnections

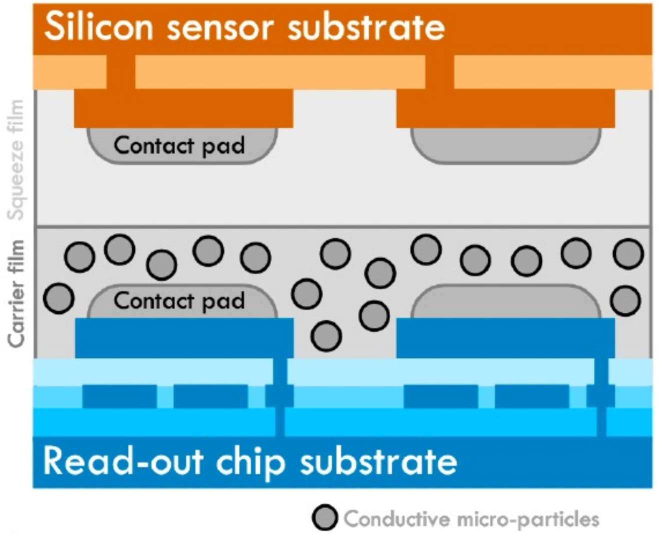
together with EP R&D WP1.3
(Dec 2020)

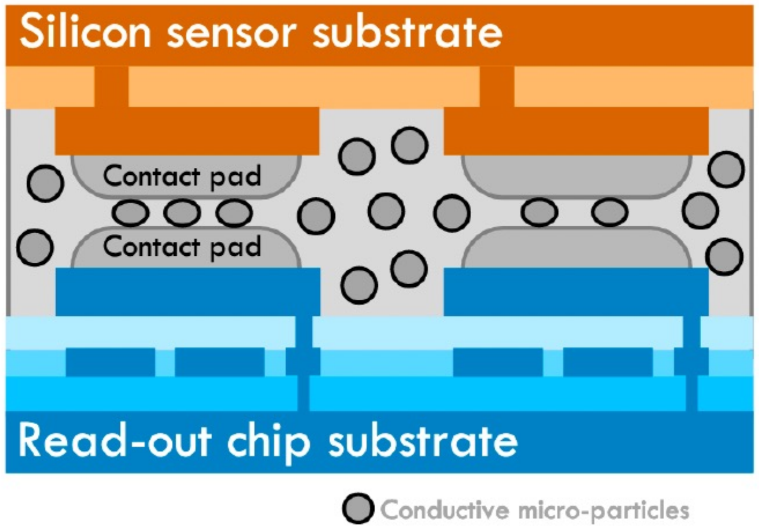
Anisotropic Conductive Films

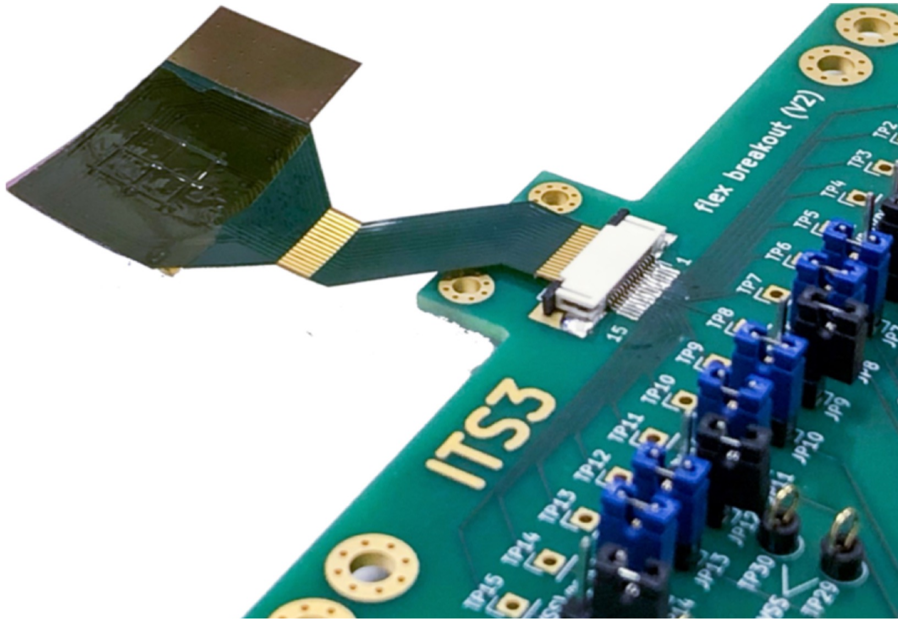
Different way to interconnect: glue and interconnection in one step

- Based on epoxy film for mechanical connections, embedded with conductive particles for electrical connections.
- Challenge is the optimization of the ACF film ad the flip chip parameters for small pads
- Conductive micro particle







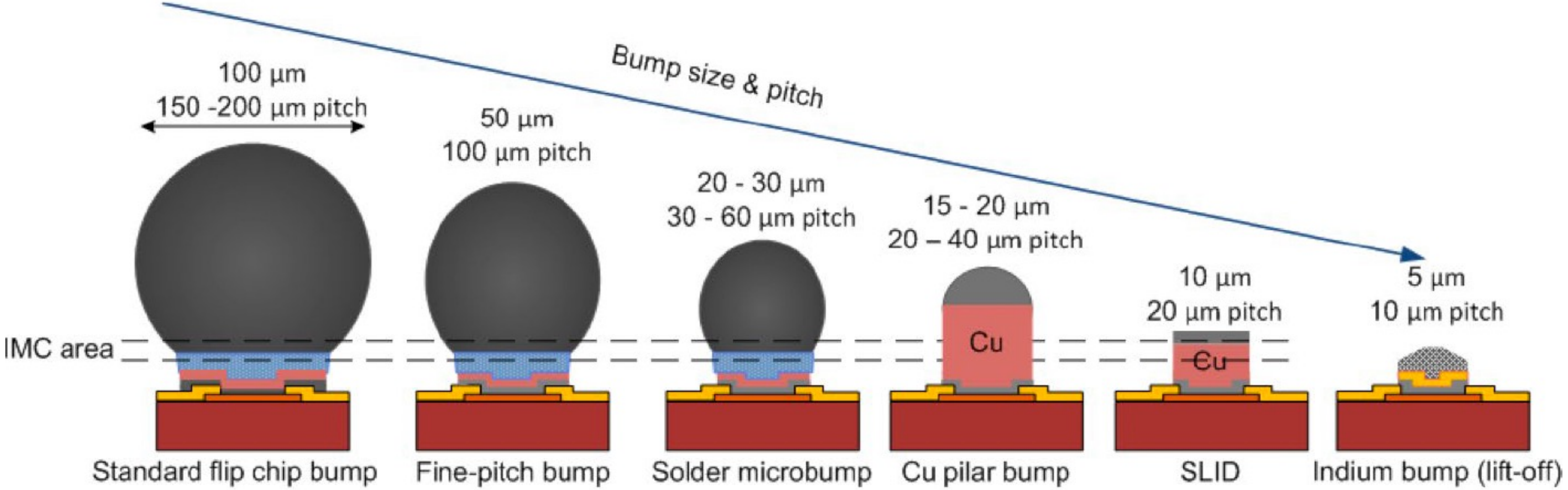


Other R&D ongoing – ACF interconnections

Anisotropic Conductive Films

In addition → also useful to deal with smaller and smaller pixels

- Pixel pitch and size can be limited by the interconnection size to the FE
- Standard soldering or copper pillar would limit the pitch to 10um



Other R&D ongoing – Embedding

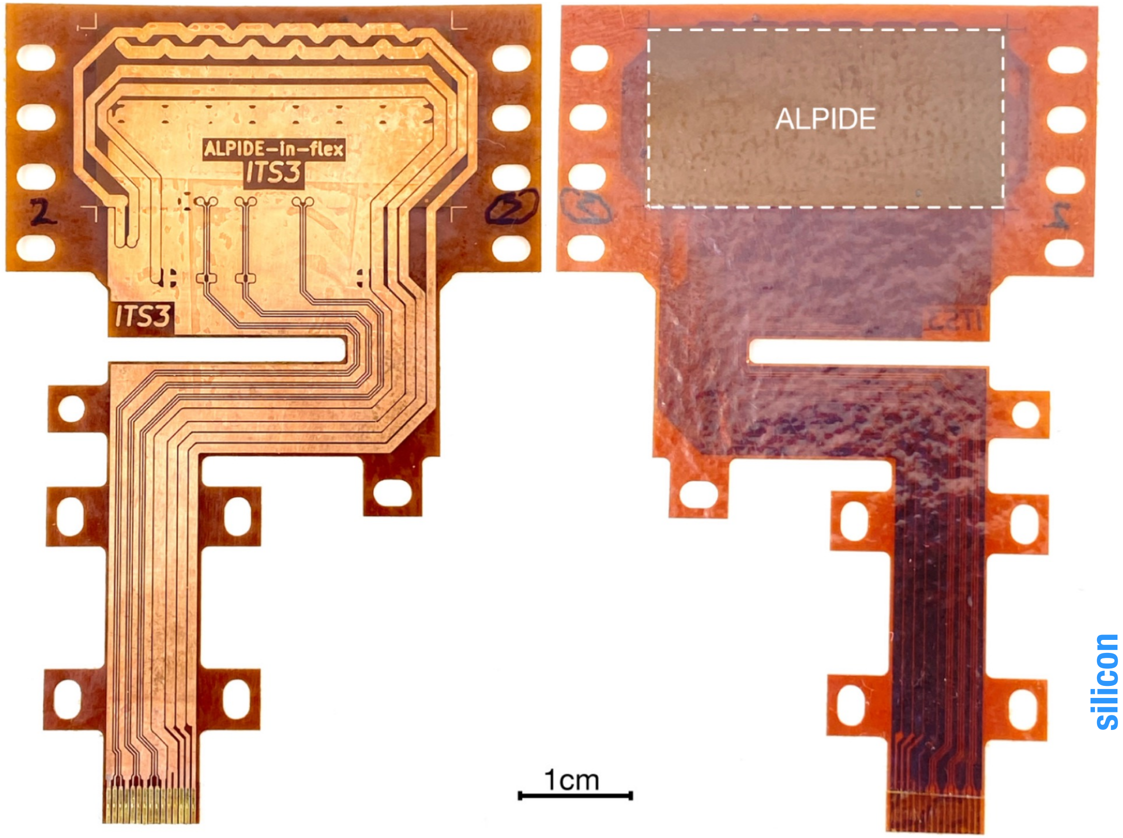
interconnections

MAPS foils

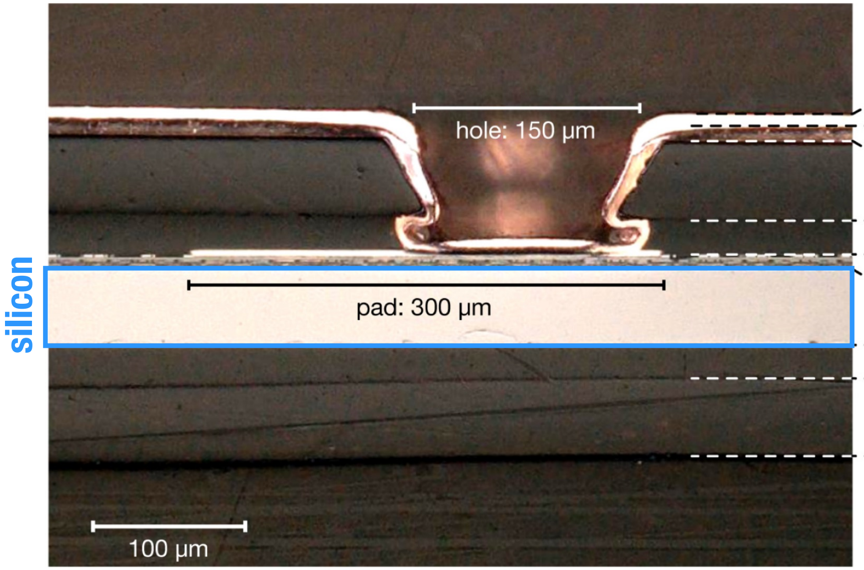
Idea back to 2014 (Dulinski et al.)
Embedding of chips into flexible printed circuit boards (Kapton foils)

- for **mechanical protection**
- as a possibility **to add a power distribution layer**

→ protect and interconnect sensors while adding only a small amount of material
→ Results in robust and flexible detector



https://doi.org/10.1016/j.nima.2022.167673



part	thickness	radiation length
Cu plating	13 µm	(0.09%)
Cu cladding	5 µm	(0.03%)
Polyimide	45 µm	0.02%
glue	25 µm	0.01%
metal stack	10 µm	0.01%
silicon	45 µm	0.05%
glue	25 µm	0.01%
Polyimide	45 µm	0.02%
total:	**213 µm**	**0.10%** (+ 0.13% Cu)

Summary

Large benefit from the commercial success (image sensors)
commercially available and easily obtainable in large quantities

CMOS MAPS are ideal devices for vertexing
low material budget (thin + low power), high resolution (small pixels), large surfaces (commercial process), non-planar geometries (thin silicon is flexible)

Large progress over the last decade
Several applications, e.g. STAR 2015 and ALICE ITS2 2021, and improvements on radiation hardness, low noise, and speed

Future/ongoing developments: bending, deeper sub micron tech. node (65 nm) and stitching (wafer scale)
Big push from ALICE ITS3 (LHC LS3, 2027/28): new inner-most 3 layers, wafer-scale, bent, stitched sensors and also paves the way for the future experiment like ALICE 3 (LHC LS4, 2033/34): 60 m^2 silicon-only vertexer and tracker

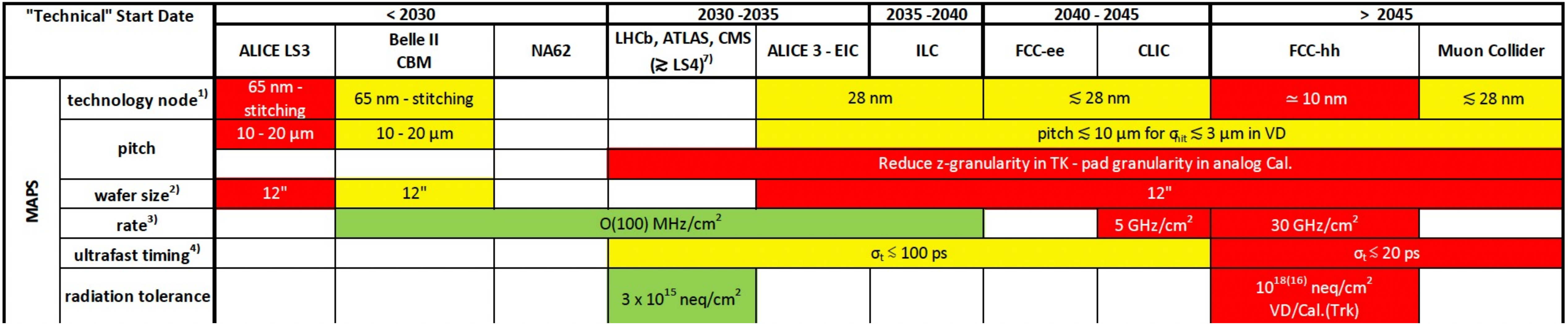
R&D far beyond the strict experiment needs:
More a common path, with small or large collection diode. Process modification to improve on radiation hardness but also timing performance. Other cutting edge R&D, like bending of several structures, ACF, MAPS foil

CMOS MAPS have great prospects in future vertexing (and tracking) applications
Already several experiments are indeed envisioning them

Backup

ECFA Roadmap

http://dx.doi.org/10.17181/CERN.XDPL.W2EX



"Technical" Start Date		< 2030			2030 -2035		2035 -2040	2040 - 2045		> 2045	
		ALICE LS3	Belle II CBM	NA62	LHCb, ATLAS, CMS ($\gtrsim$ LS4)$^{7)}$	ALICE 3 - EIC	ILC	FCC-ee	CLIC	FCC-hh	Muon Collider
MAPS	technology node$^{1)}$	65 nm - stitching	65 nm - stitching			28 nm		$\lesssim$ 28 nm		$\simeq$ 10 nm	$\lesssim$ 28 nm
	pitch	10 - 20 µm	10 - 20 µm			pitch $\lesssim$ 10 µm for $\sigma_{hit} \lesssim$ 3 µm in VD					
					Reduce z-granularity in TK - pad granularity in analog Cal.						
	wafer size$^{2)}$	12"	12"			12"					
	rate$^{3)}$		O(100) MHz/cm^2						5 GHz/cm^2	30 GHz/cm^2	
	ultrafast timing$^{4)}$				$\sigma_t \lesssim$ 100 ps					$\sigma_t \lesssim$ 20 ps	
	radiation tolerance				3 x 10^{15} neq/cm^2					$10^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	