UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386

ziti

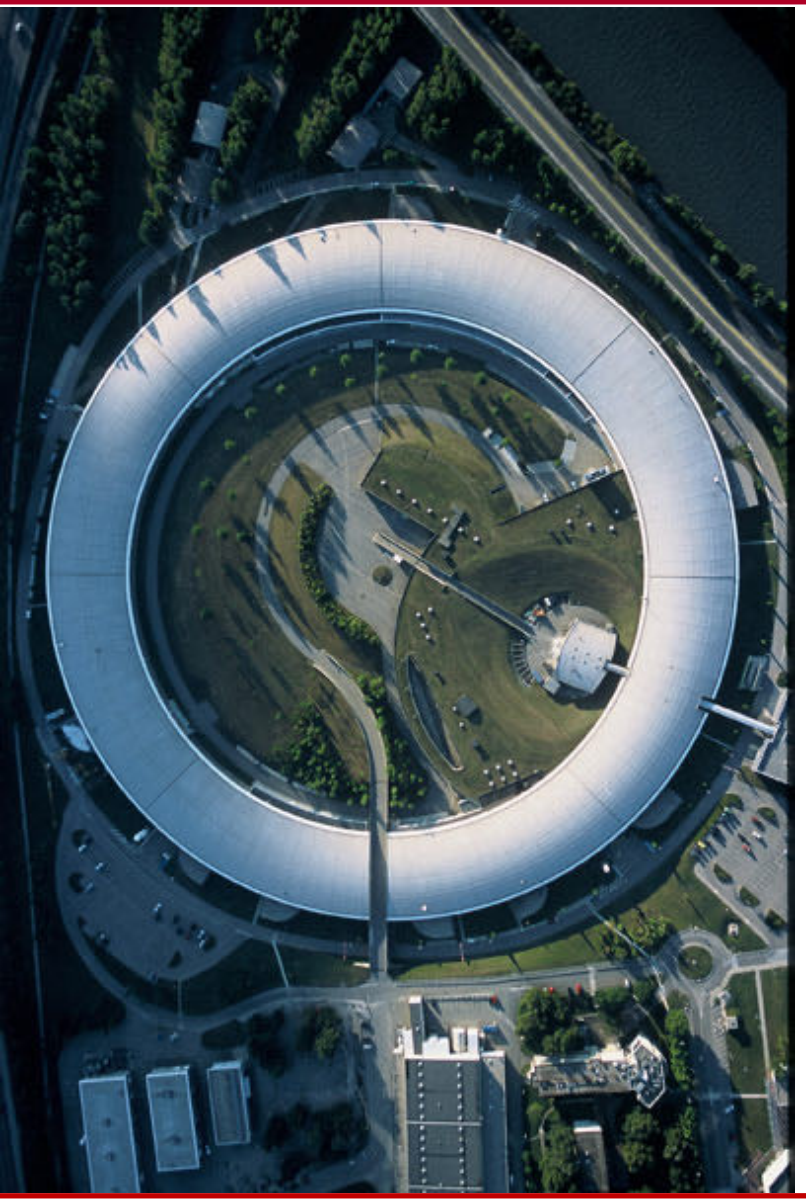
XIDer Status Update

Part I

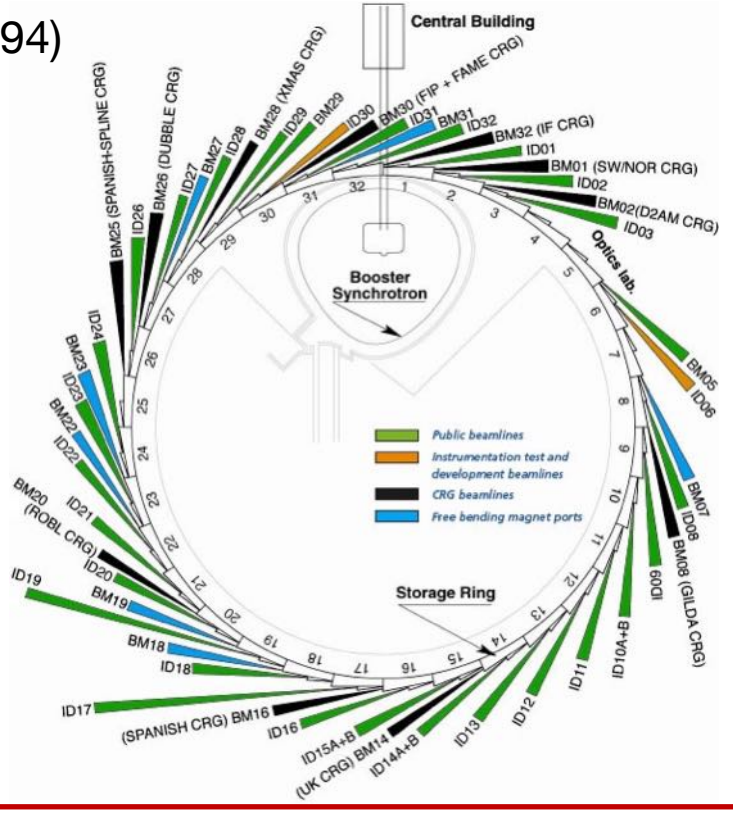
HighRR

Schaltungstechnik
und Simulation

European Synchrotron Radiation Facility (ESRF)



- Joint research facility in Grenoble, France (founded in 1988)
- Funded by 22 countries (France, Germany, Italy, ..)
- Electron synchrotron x-ray source (up to ~100keV)
- First 3rd generation synchrotron (opened in 1994)
- Circumference: 844m
- 2000 publications per year
- Advertises itself as „user facility“
- Available research methods
  - X-ray spectroscopy
  - X-ray tomography
  - X-ray diffraction



ESRF Upgrade Program (EBS)

EBS electromagnets

Extremely-Brilliant Source (ESRF-EBS):

- Storage ring & instrumentation upgrade program over the period 2015-2022
- New storage ring has been finished and opened in 2020 as planned
- Improved energy efficiency (30% cost reduction)
- Increased brilliance of x-ray beam
- Needs new detectors tailored to the upgraded source

  ⇒ Reach out to external laboratories

Project Outline

XIDer:

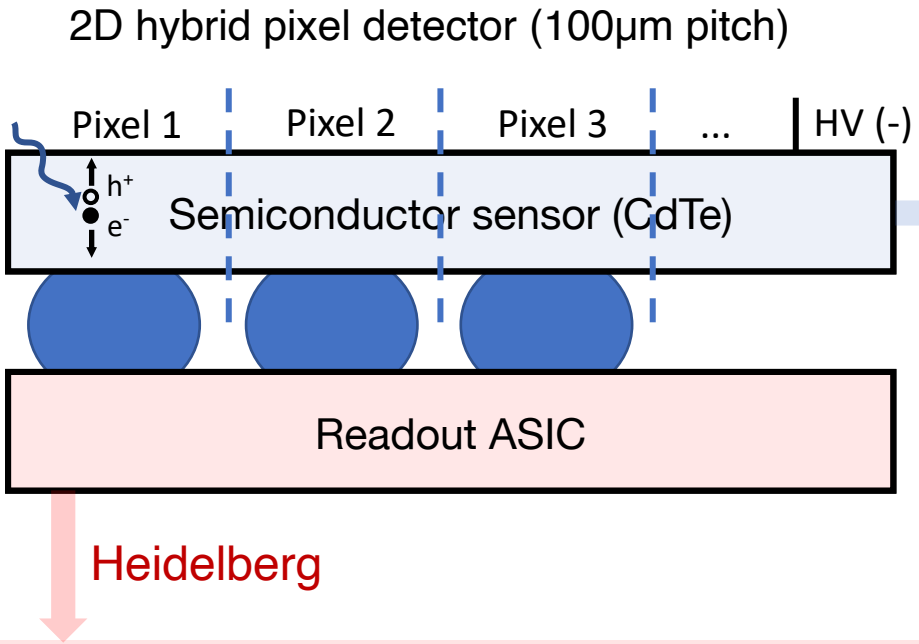
- R&D project until end of 2023
- 4-year funding: Shared 50/50 by ESRF and Heidelberg University
- HighRR members working on this project: Marin Collonge (ESRF), Christian Kreidl (HD), Michael Ritzert (HD), David Schimansky (HD)

Detector Requirements

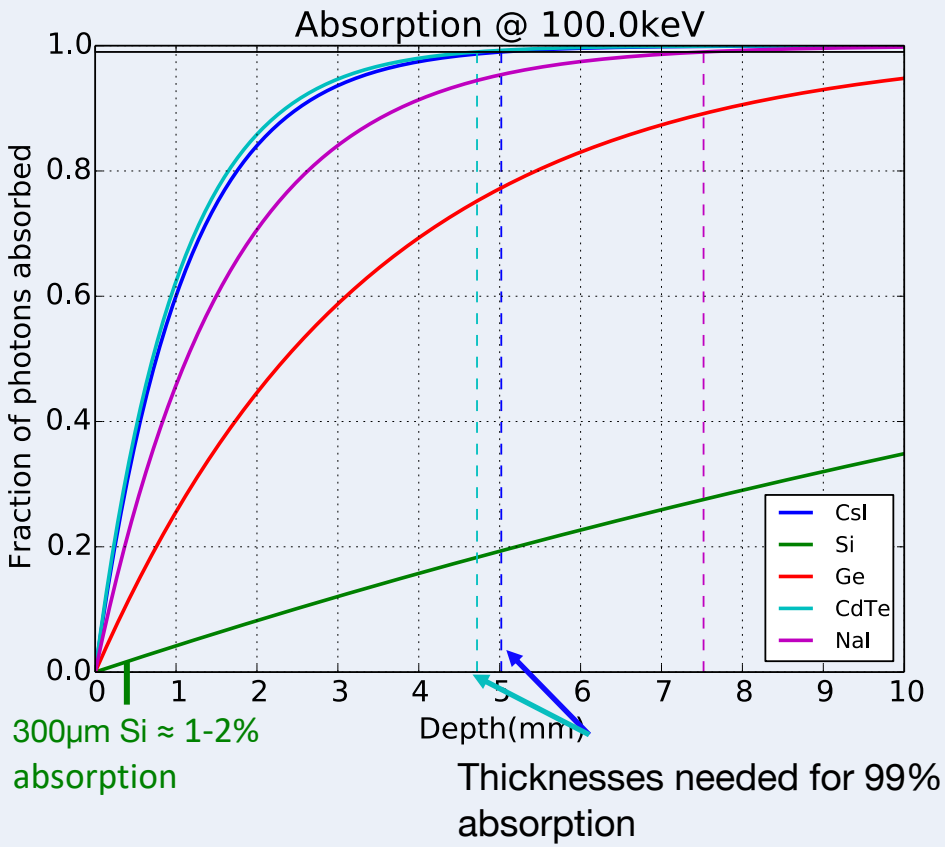
Build detector for any kind of (time-resolved) x-ray diffraction experiment at the ESRF:

Energy range	30-100keV
Dynamic range	Single photons up to $> 10^{11} \frac{ph}{mm^2 s}$
Different spatial resolutions	100µm vs. 200µm pixel pitch
Cope with different bunch filling modes of storage ring	7/8 + 1 mode, 4-bunch mode, 16-bunch mode, ..
Time-resolved	> 100k frames per second
Flexible readout schemes	Triggered readout, single frame, accumulated frames, burst mode, histogram mode, ..

Detector Concept



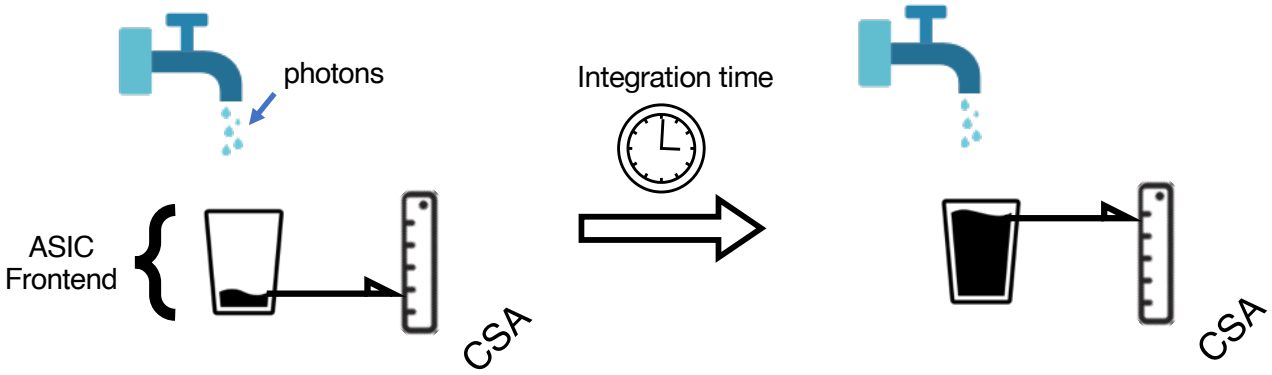
ESRF



- Every pixel is connected to its own frontend in the readout ASIC
- **Charge integrating** frontend with **continuous analog-to-digital conversion** for high dynamic range

- Use **high-Z material** to get high stopping power
- Tendency: Cadmium Telluride (CdTe)

Continuous Conversion Frontend with Single Stage



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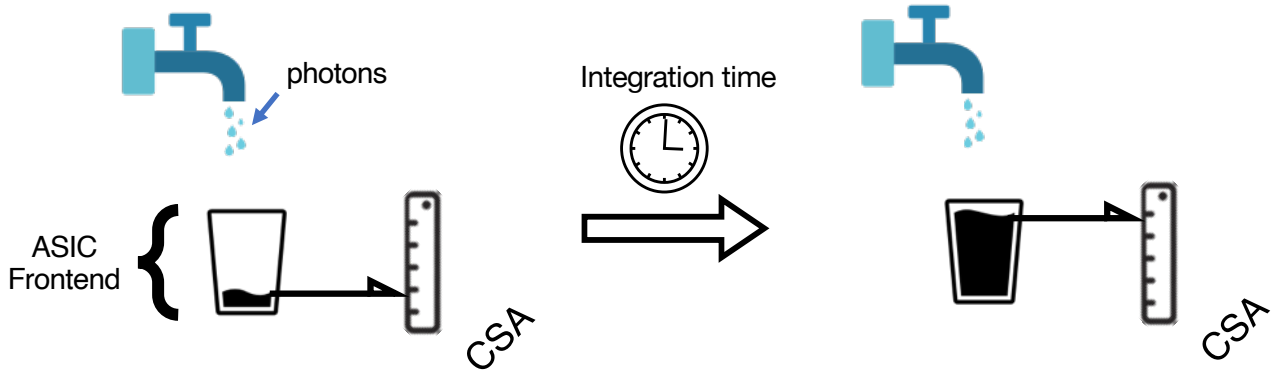
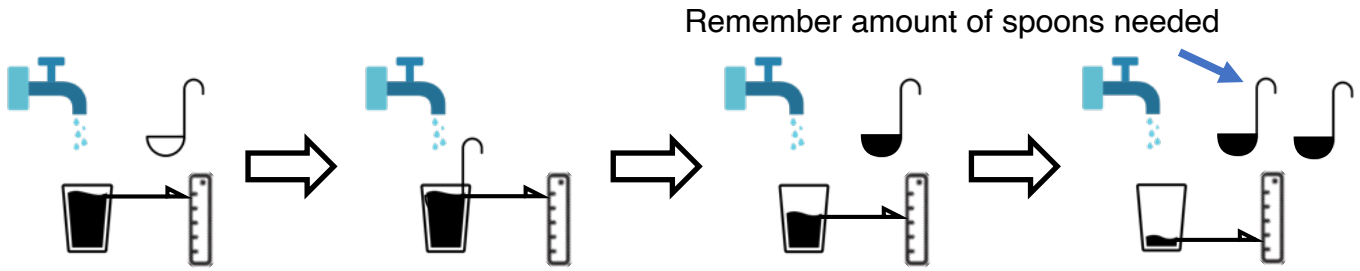


Prevent bucket from overflowing by emptying it with spoons



Single photon sensitivity & can handle high rates & dynamic range is not limited by bucket size

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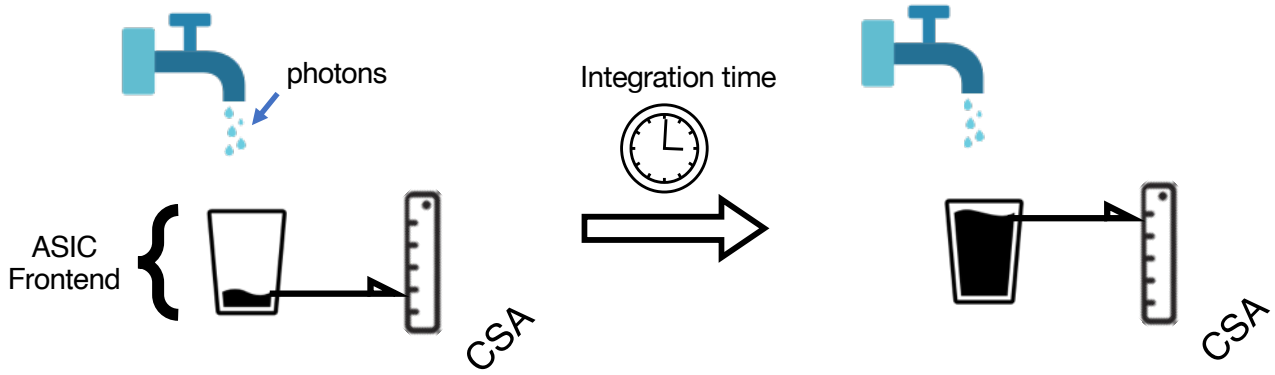

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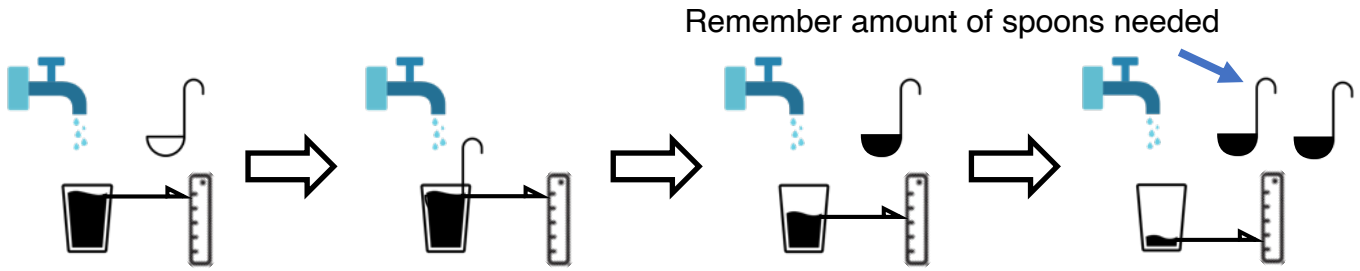

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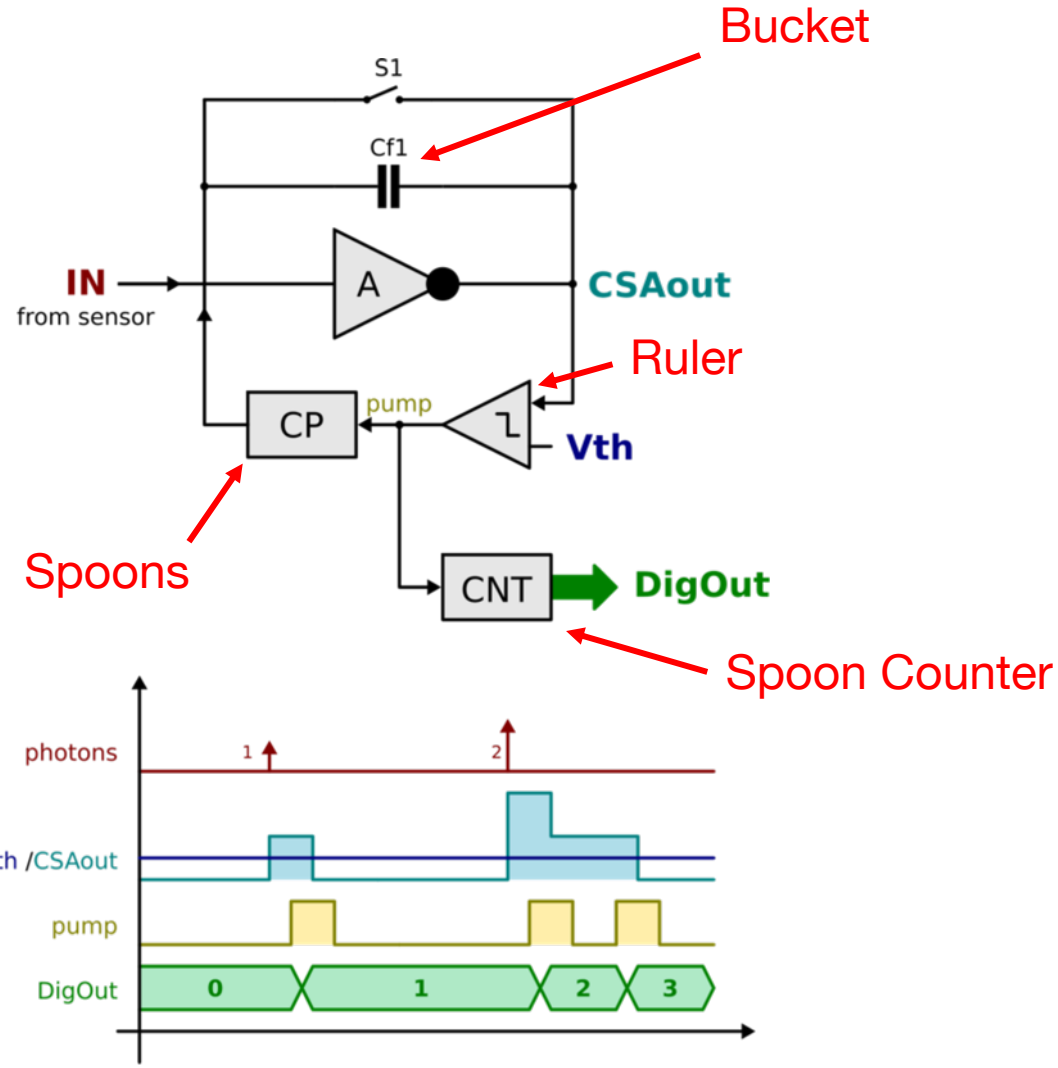
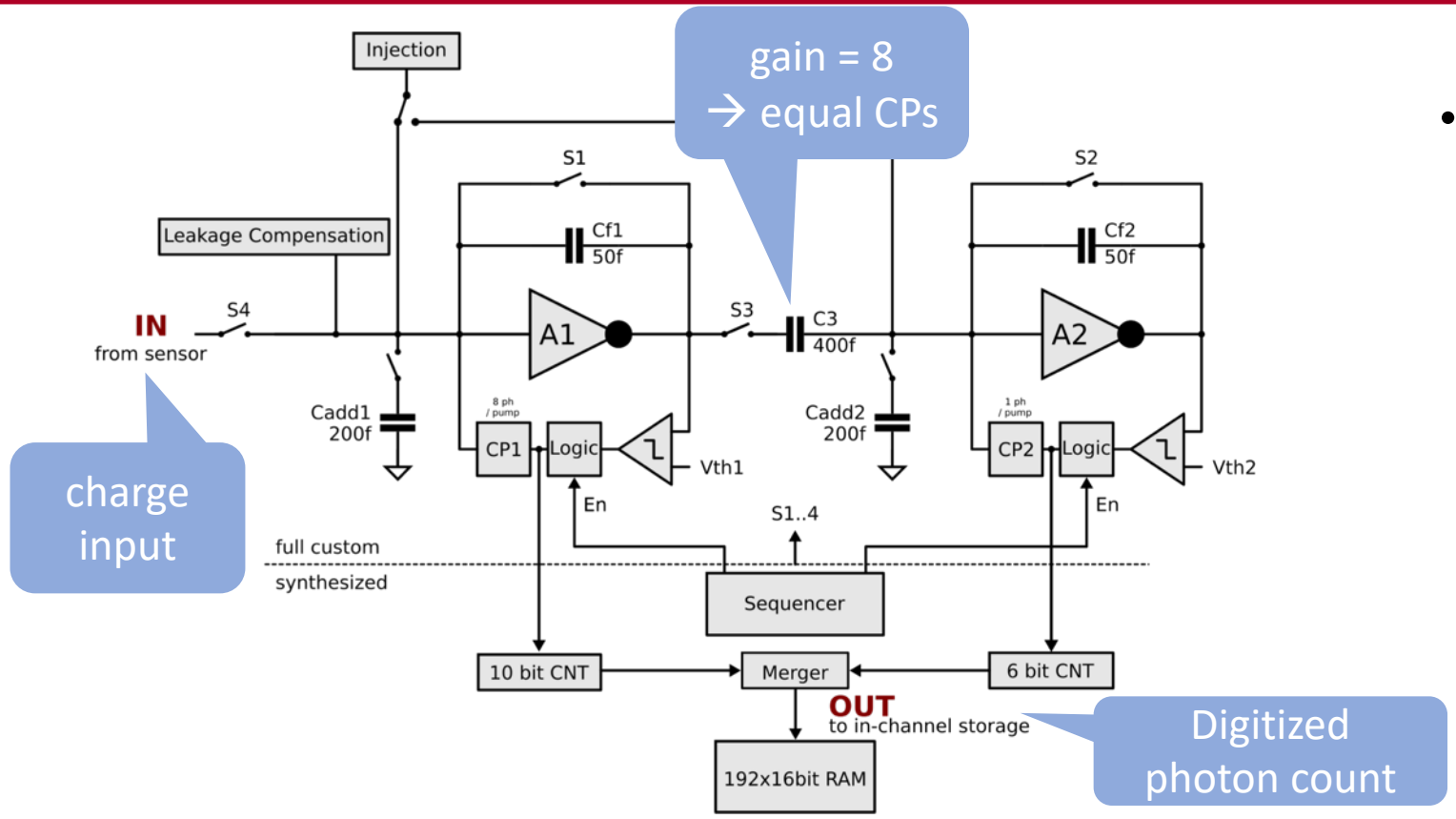


Continuous Conversion Frontend with Two Stages



- 1st stage pumps 8 ph per spoon
- 2nd stage pumps 1 ph per spoon
- f_{pump} ~ 200 MHz

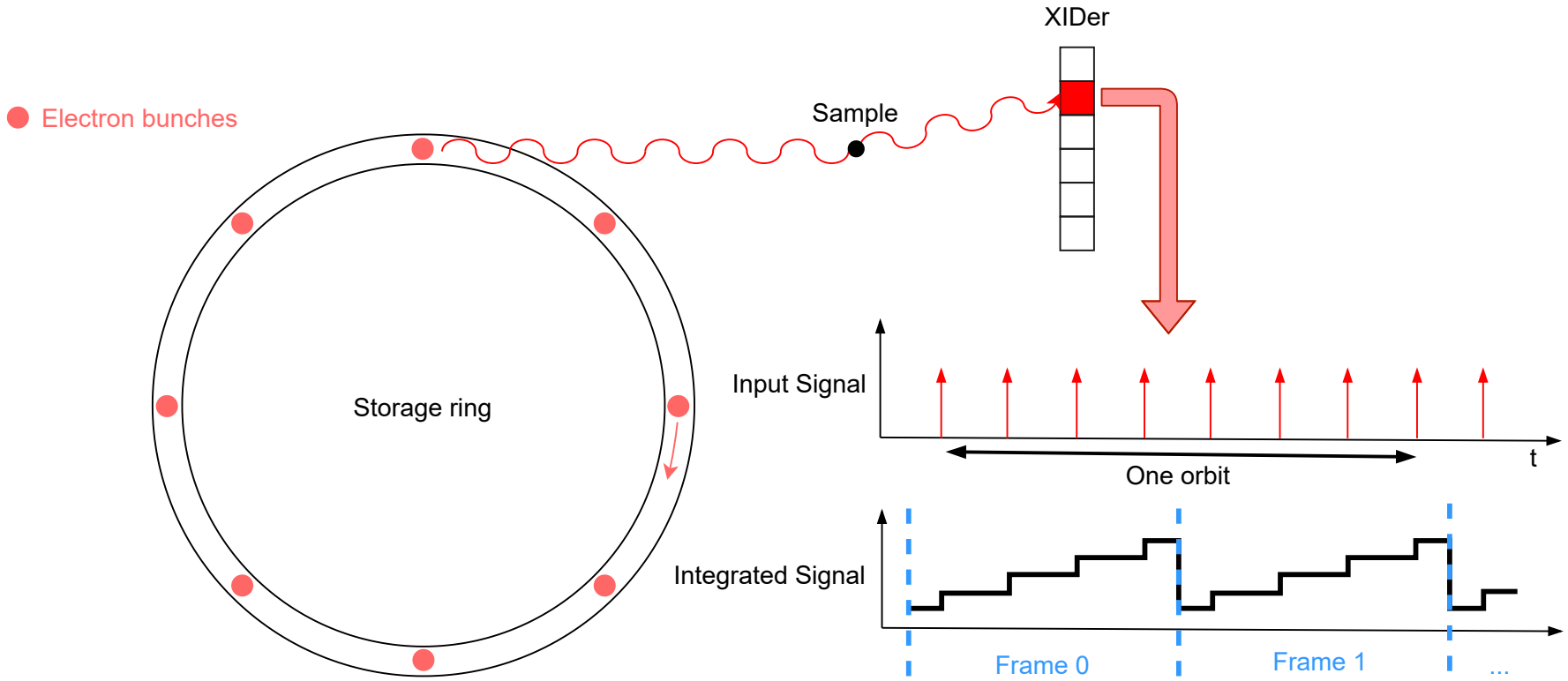
→ 1st stage: $1.6 \cdot 10^9 \frac{ph}{pixel \cdot s}$

- Design choices and challenges:
  - Spoon size
  - Spoon rate
  - Spoon ratio between stages
  - Bucket sizes
  - Charge pump (CP) topology
  - CP matching
  - Clean stage transition
  - Power limitation
  - Space limitation ($(100\mu m)^2$ pixels)

Detector Operation / Frame Acquisition Scheme

- Detector periodically repeats the same cycle to record frames
- Exposure time per frame freely adjustable via sequencer and telegram protocol
- XIDer is meant as a multi-purpose platfom

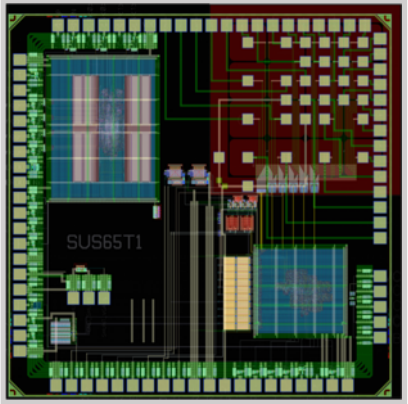
⇒ Need high flexibility to offer many different scenarios of data taking



Chip Iteration Overview

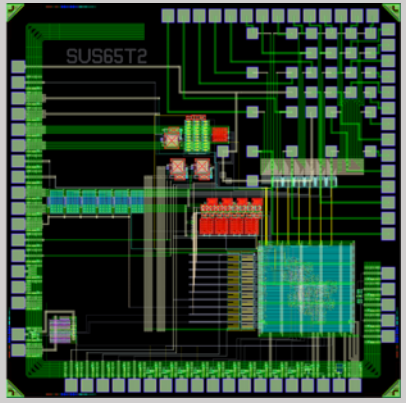
SUS65T1 (2018)

- First Prototype
- Mixed-Mode chip with full-custom frontend and semi-custom digital control block
- Basic frontend concept test



SUS65T2 (2019)

- SUS65T1 with major bug fixes
- Additional CdTe sensor characterisation circuits
- First sensor characterisation flagship



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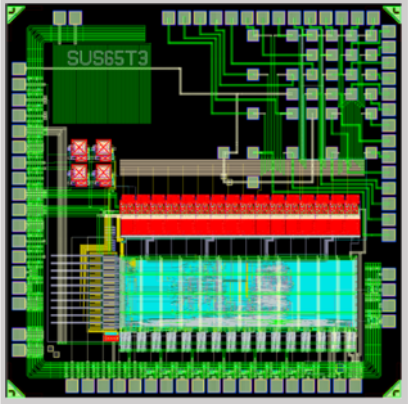
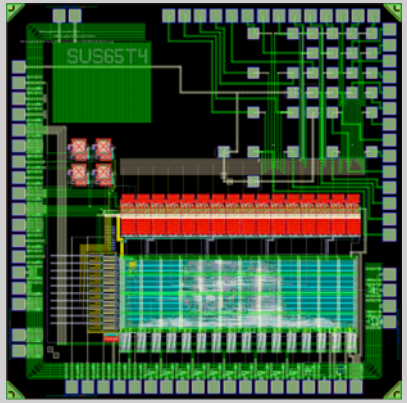
- First chip with 16 channels
- Introduces Telegram and sophisticated data output link
- “Problem child” of this project



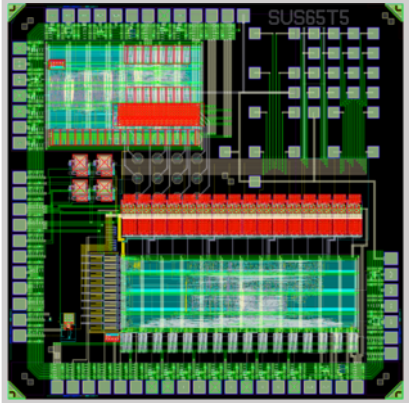
SUS65T4 (2021)

- SUS65T3 with major bug fixes
- Improved debugging capabilities
- Second sensor characterisation flagship



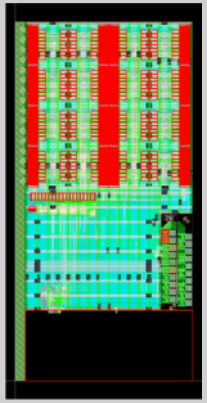
SUS65T5 (2021)

- Giant step towards large scale matrix
- Includes first scalable 4x4 pixel matrix design



SUS65T6 (2022)

- Upscaled SUS56T5 design to 16x16 pixels
- New sophisticated serializer IP by STFC (UK) to ramp up data output rates
- Chip has not yet arrived from foundry



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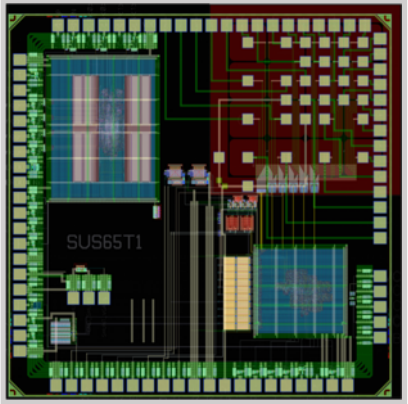

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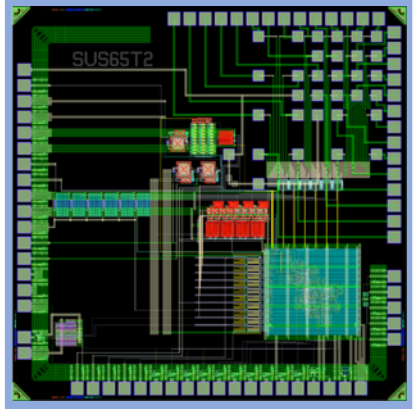

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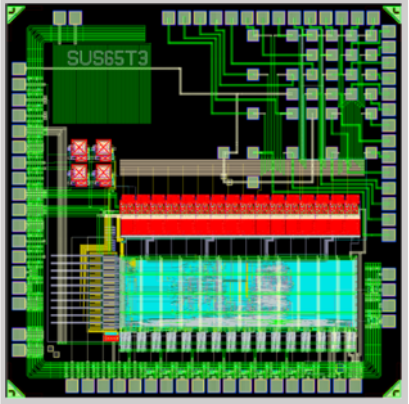

Measurements shown in 2021

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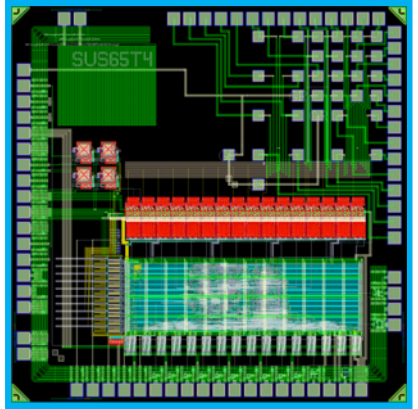

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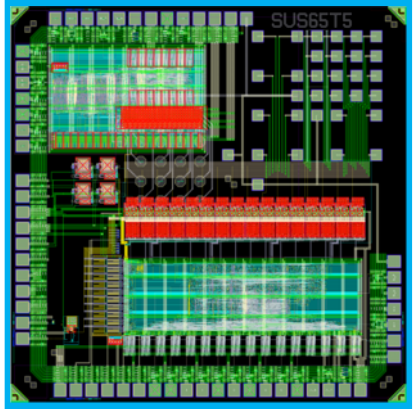

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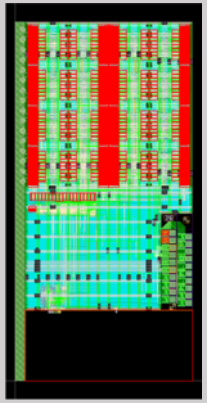
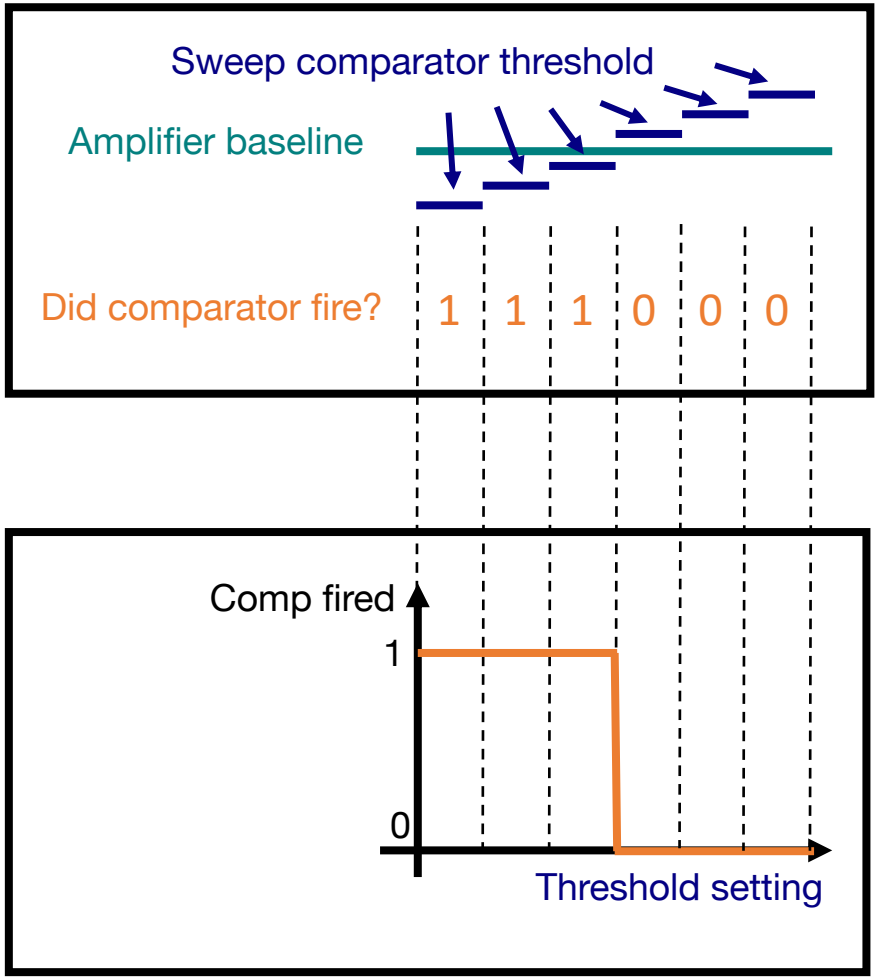


Circuit Optimisation

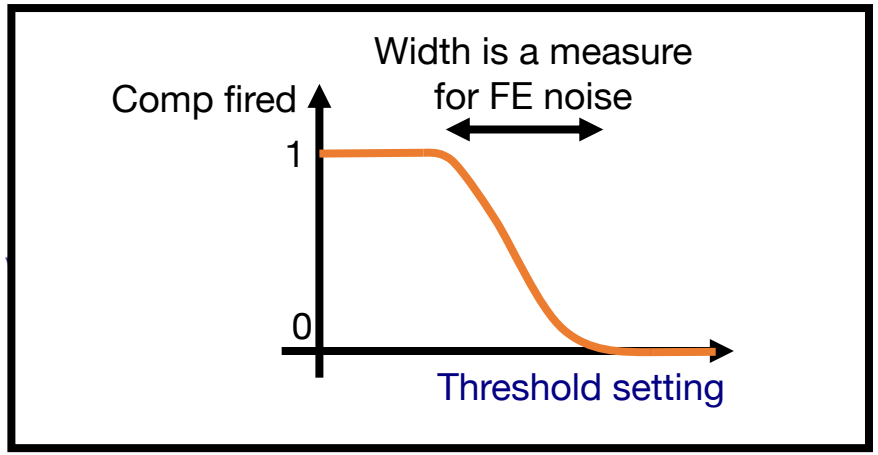
Since March 2021

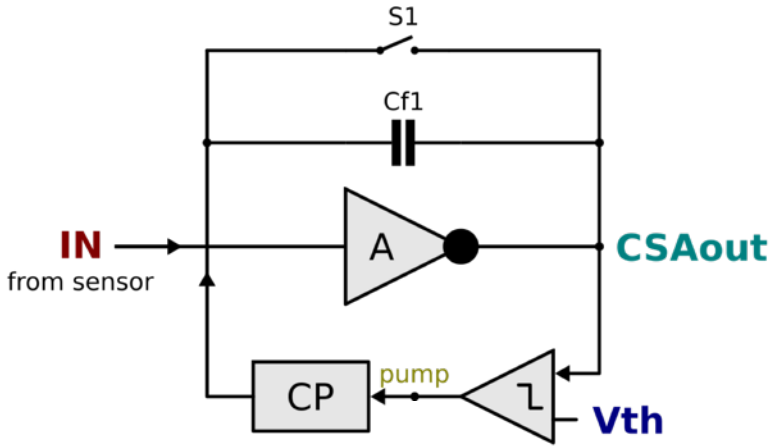
Frontend Noise Measurement



With noise

& statistics

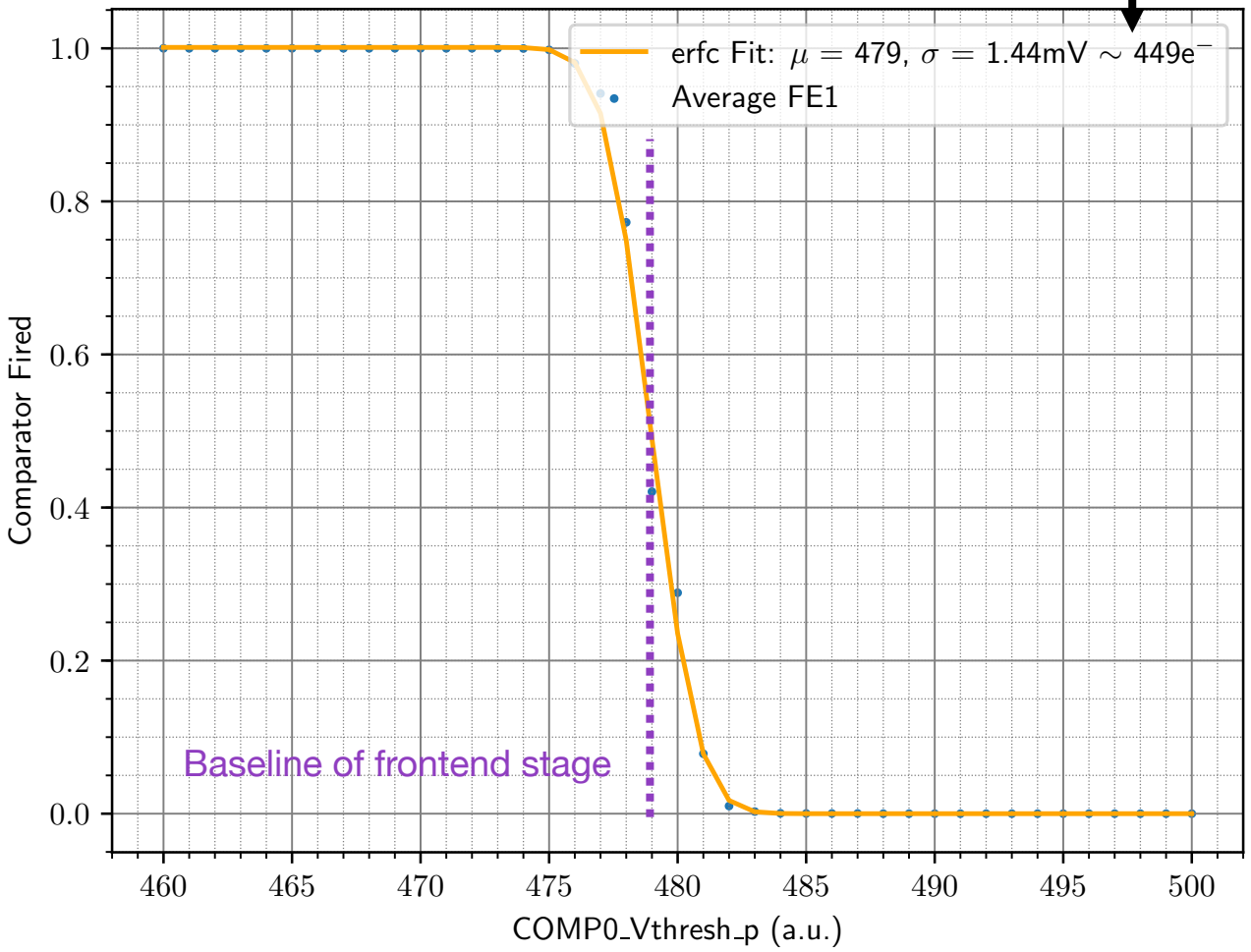




Frontend Noise Measurement of T2

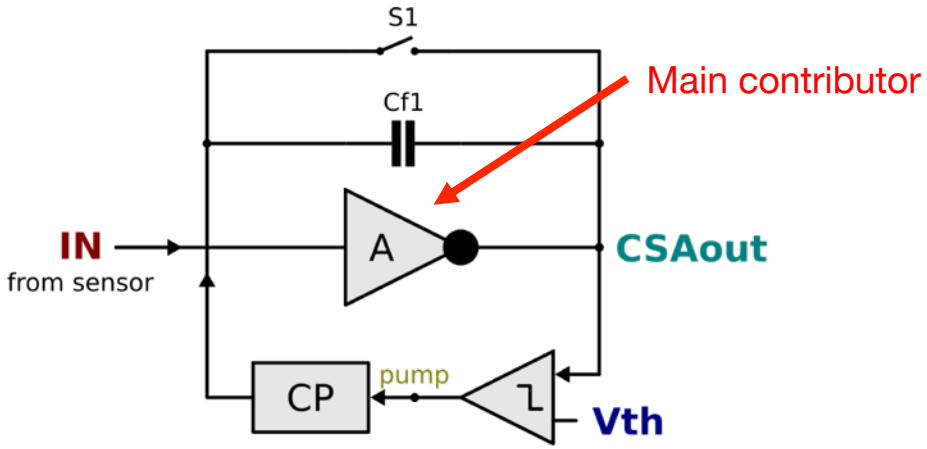
For this chip iteration, we want to be below 600e- (input referred noise)

T2 Measurement



- Smallest signal we want to see is a 30keV photon ~ 6000e-
- Noise level already below 1/10 of this value!
- BUT: ESRF detector simulations show, we should be below 300e- in the final design

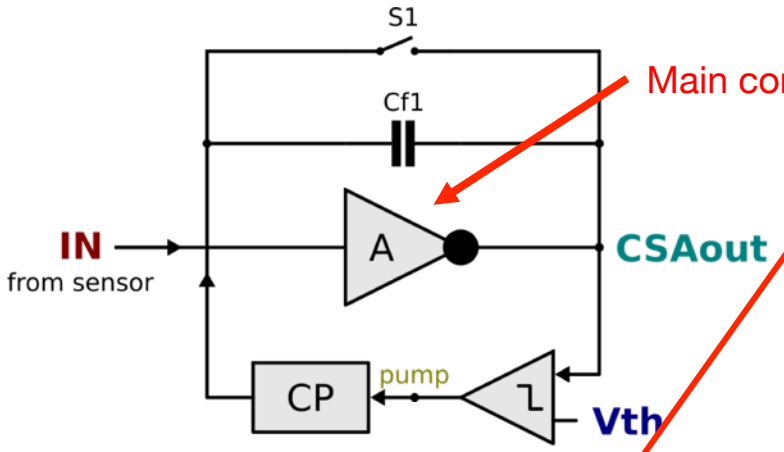
Reducing the Frontend Noise



Three ways to improve amp noise performance:

1. Supply amplifier with more current
2. Optimize amplifier design
3. Change amplifier architecture

Reducing the Frontend Noise



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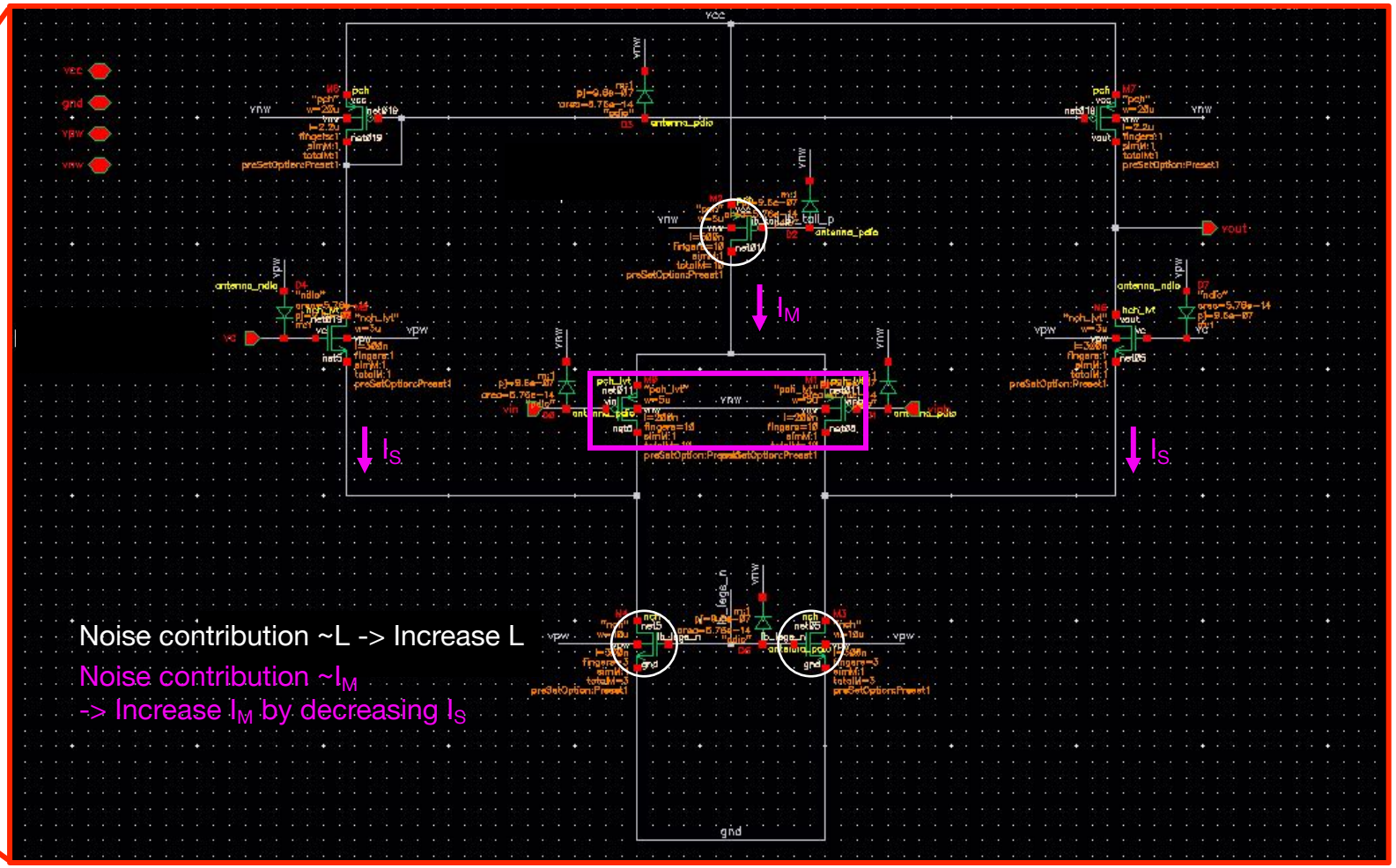
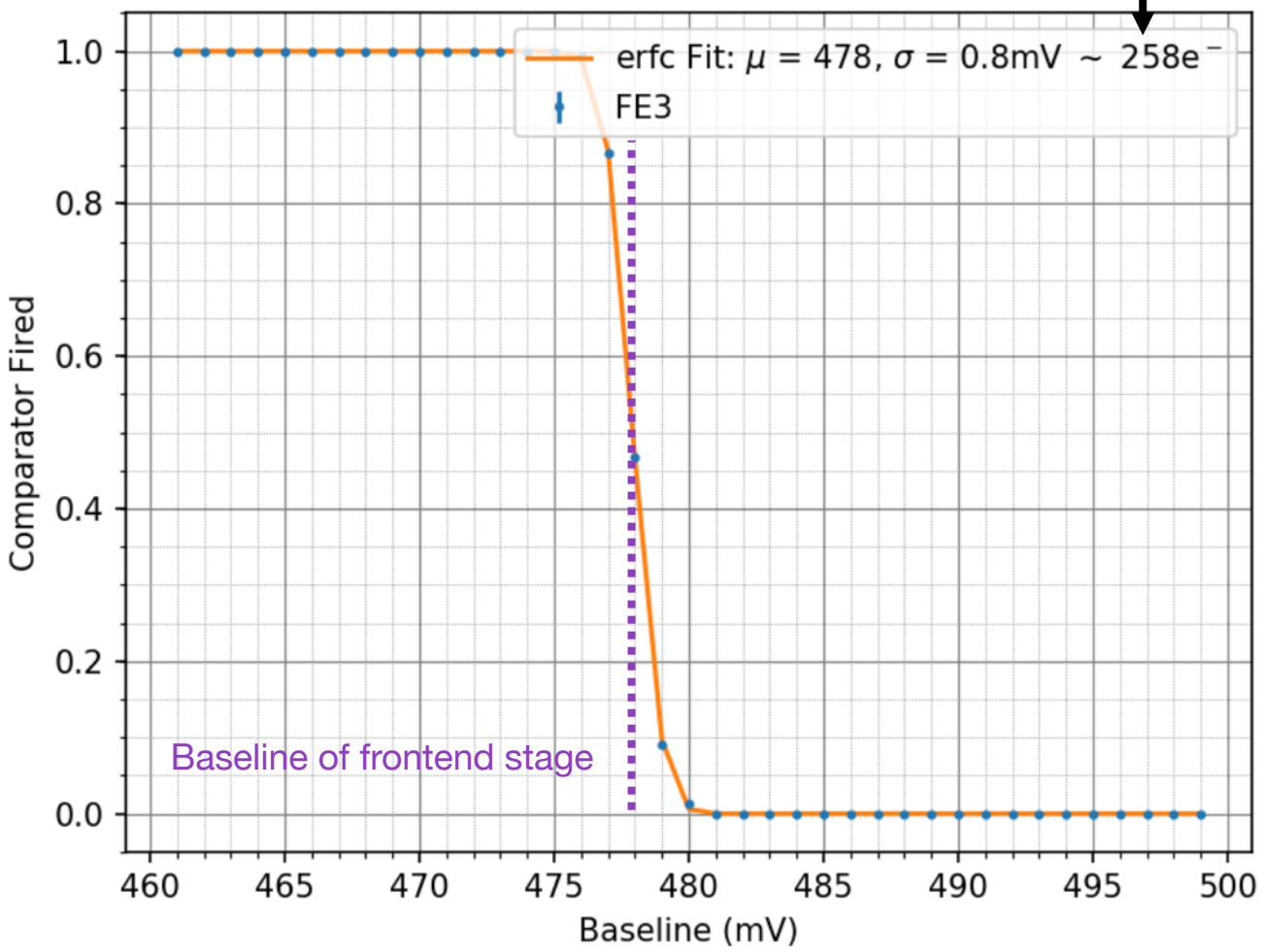


Frontend Noise Measurement of T5

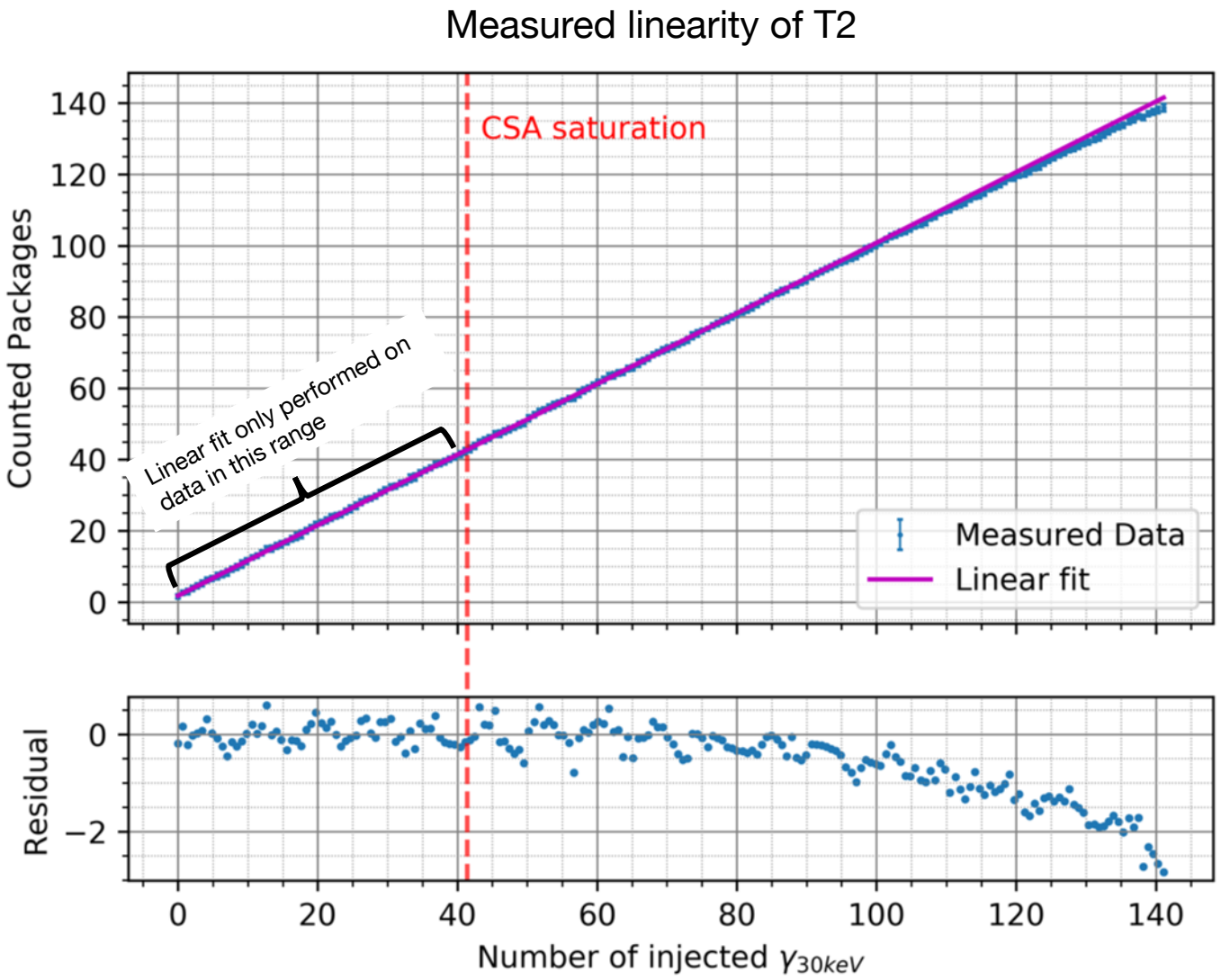
For this chip iteration, we want to be below 300e- (input referred noise)

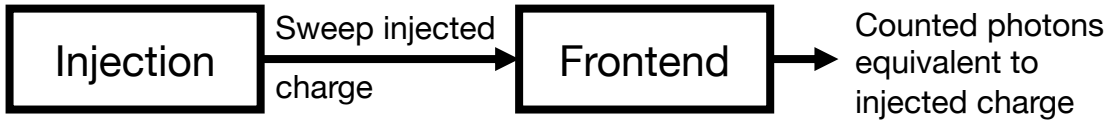
T5 Measurement



- Target reached!
- Noise decreased by factor of 1.8 from T2 to T5 while keeping the power consumption the same!
- In agreement with simulations

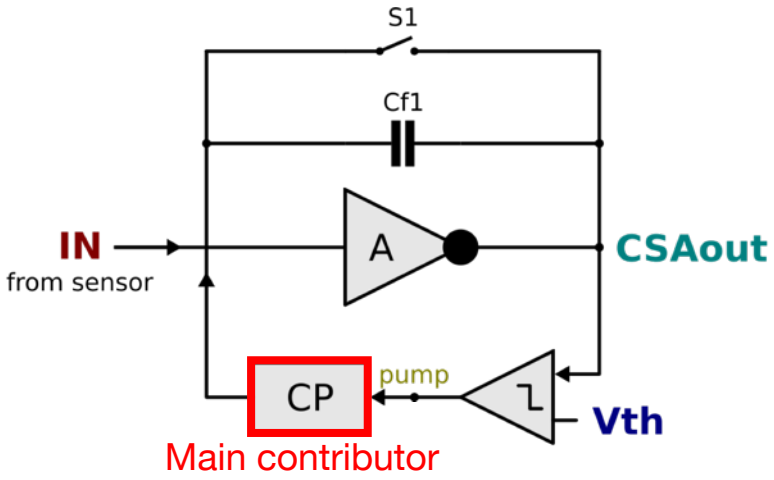
Frontend Counting Linearity Measurement





- Linear fit performed for injections $<42\gamma_{30keV}$
- Up to a point of 80 γ_{30keV}, FE shows linear behaviour, maximum deviation of less than 1 count
- Above 80 γ_{30keV} the curve bends
- At 140 γ_{30keV} the maximum deviation is roughly 3 ADUs

Non-Linearity Origin



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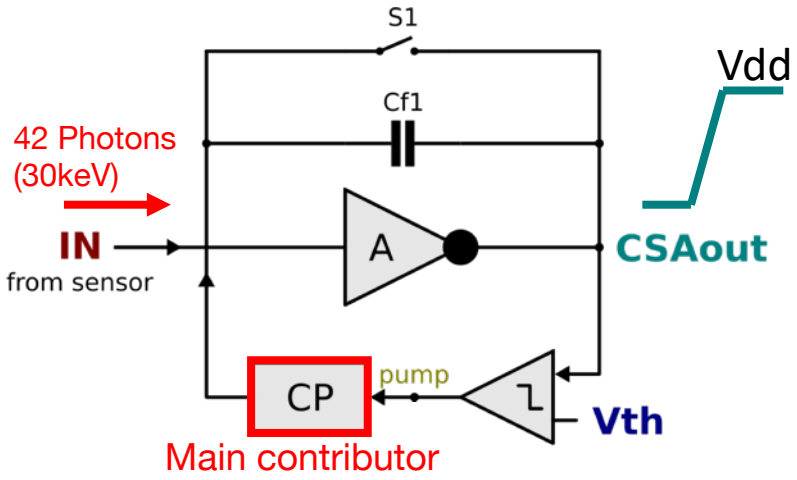
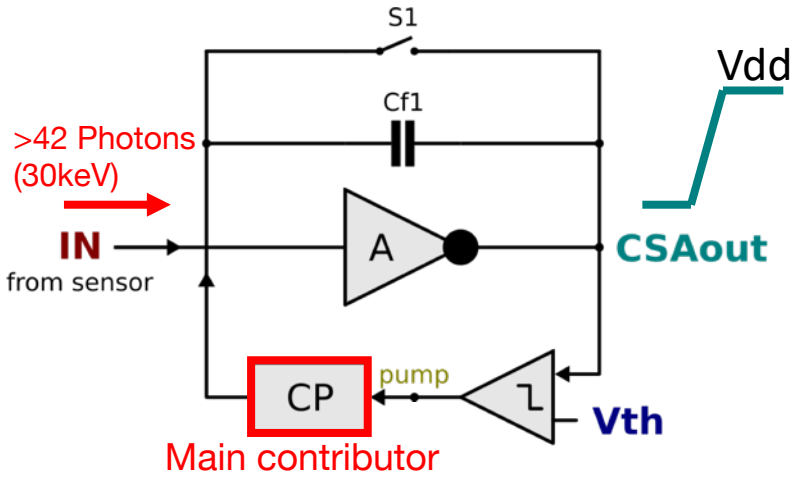


- Non-linearity of charge pump causes expected bend. How?
  - At 42 30-keV photons, the CSA saturates (no problem!)

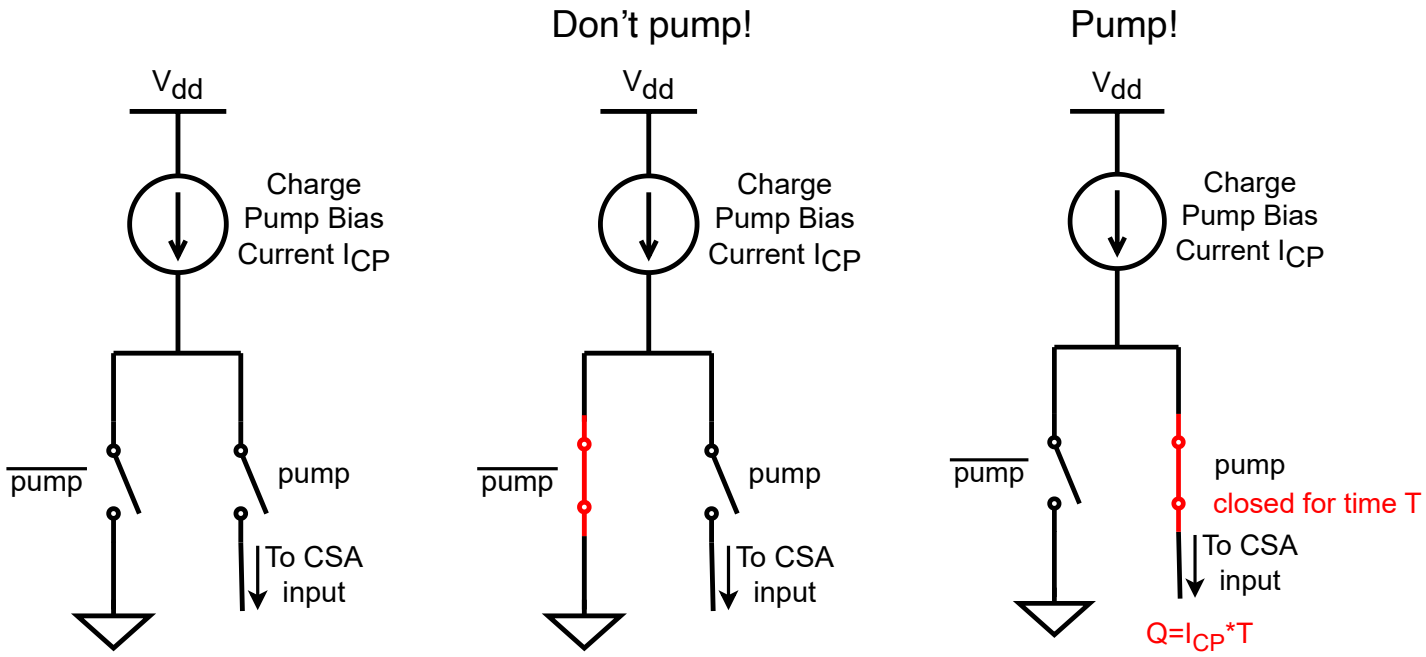
Non-Linearity Origin



- Non-linearity of charge pump causes expected bend. How?
  - At 42 30-keV photons, the CSA saturates (no problem!)
  - More input charge causes a decrease of the CSA input voltage (still no problem!)
- BUT:
  - The charge pump's output is connected to the CSA's input node
  - **A design flaw in the first charge pump version makes its spoon size dependent on the voltage at its output**

⇒ **Spoon size increases with input charge (not desired)**

Charge Pump Output Voltage Dependence



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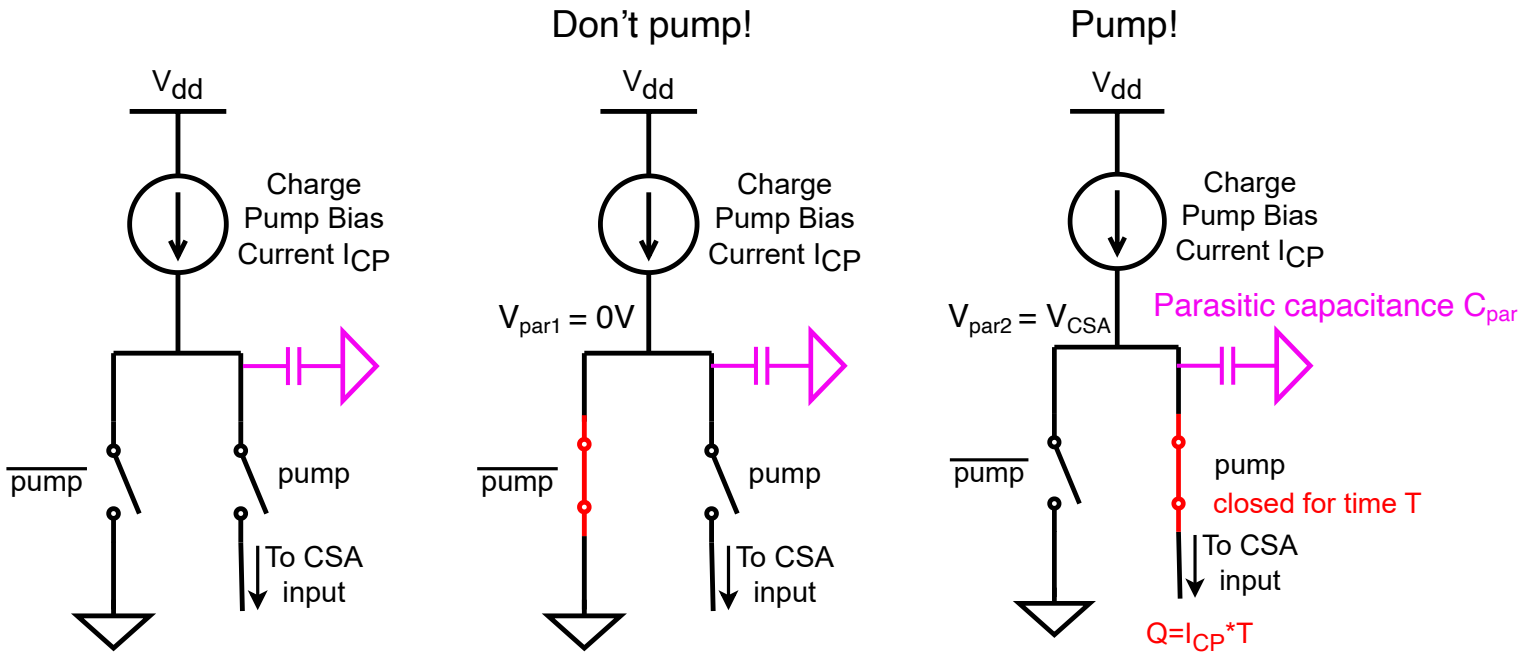

- Problem: Injected charge is actually

  $Q + Q_{par} = Q + C_{par} * (Vpar1 - Vpar2)$

  $= Q + C_{par} * V_{CSA}$

- Solution: Pin V_{par} to same value for *pump* and *don't pump* states

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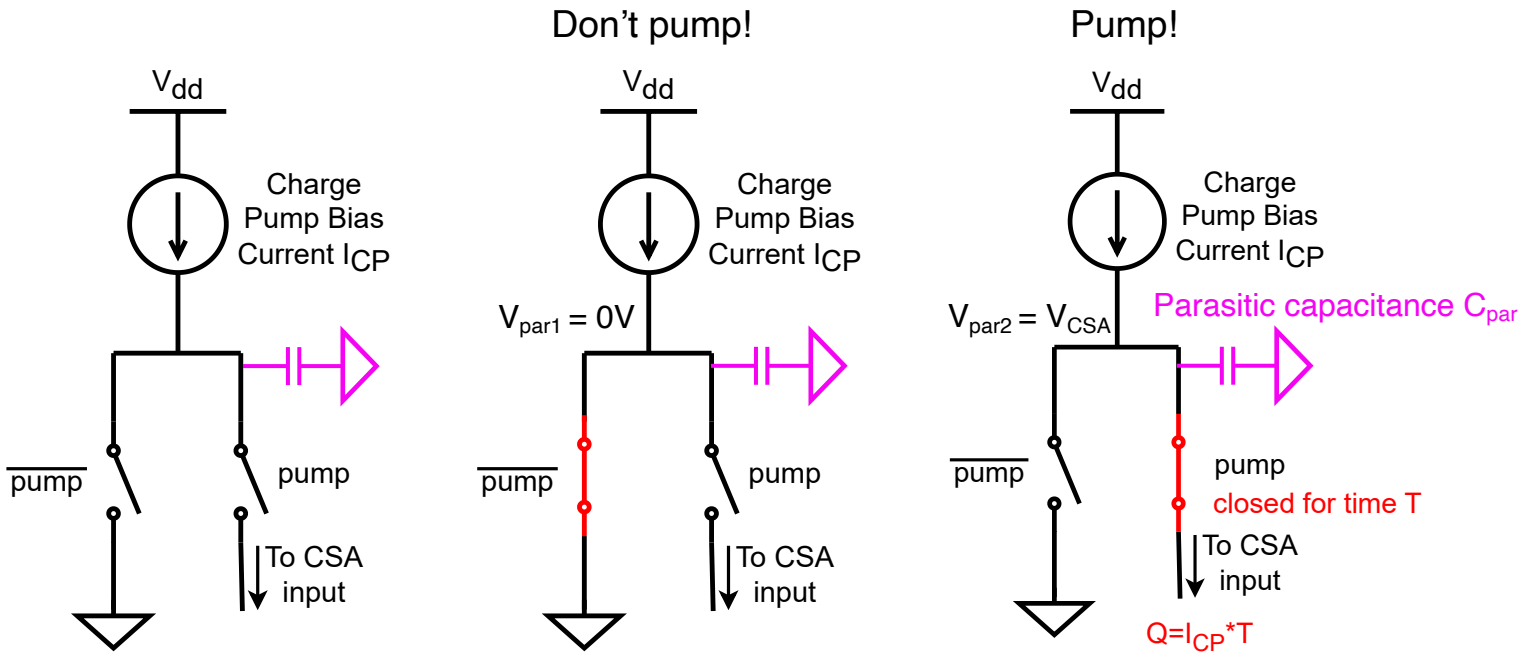

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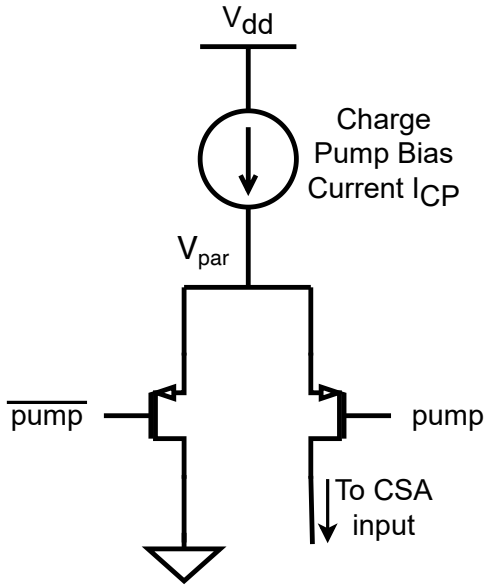
- Trick:

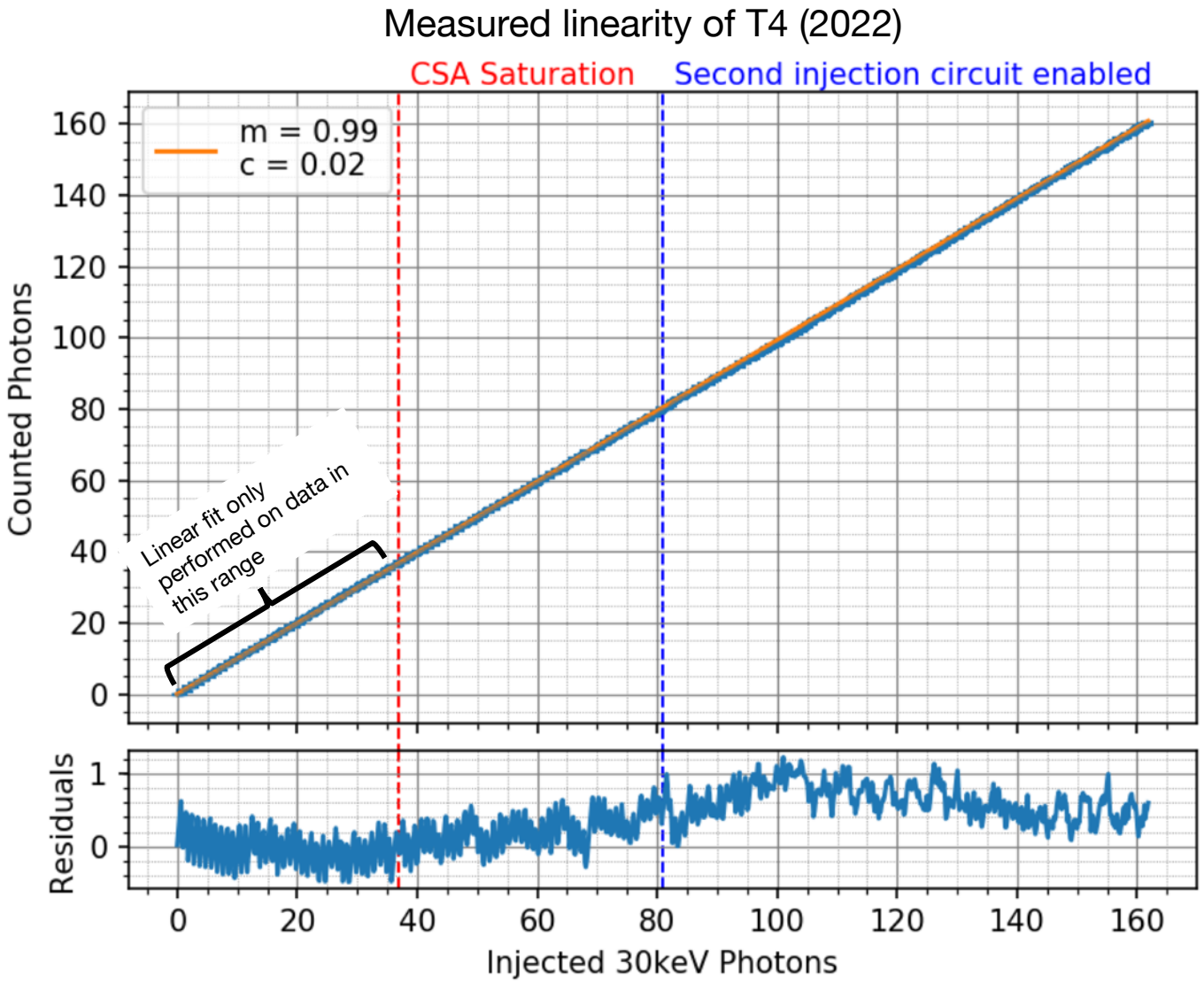


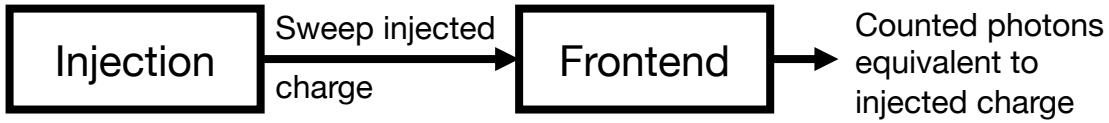
Use PMOSses as switches, make them act in saturation

⇒ Vpar is cascoded by switches

⇒ Vpar does not change between *pump* and *don't pump*

Frontend Counting Linearity Measurement





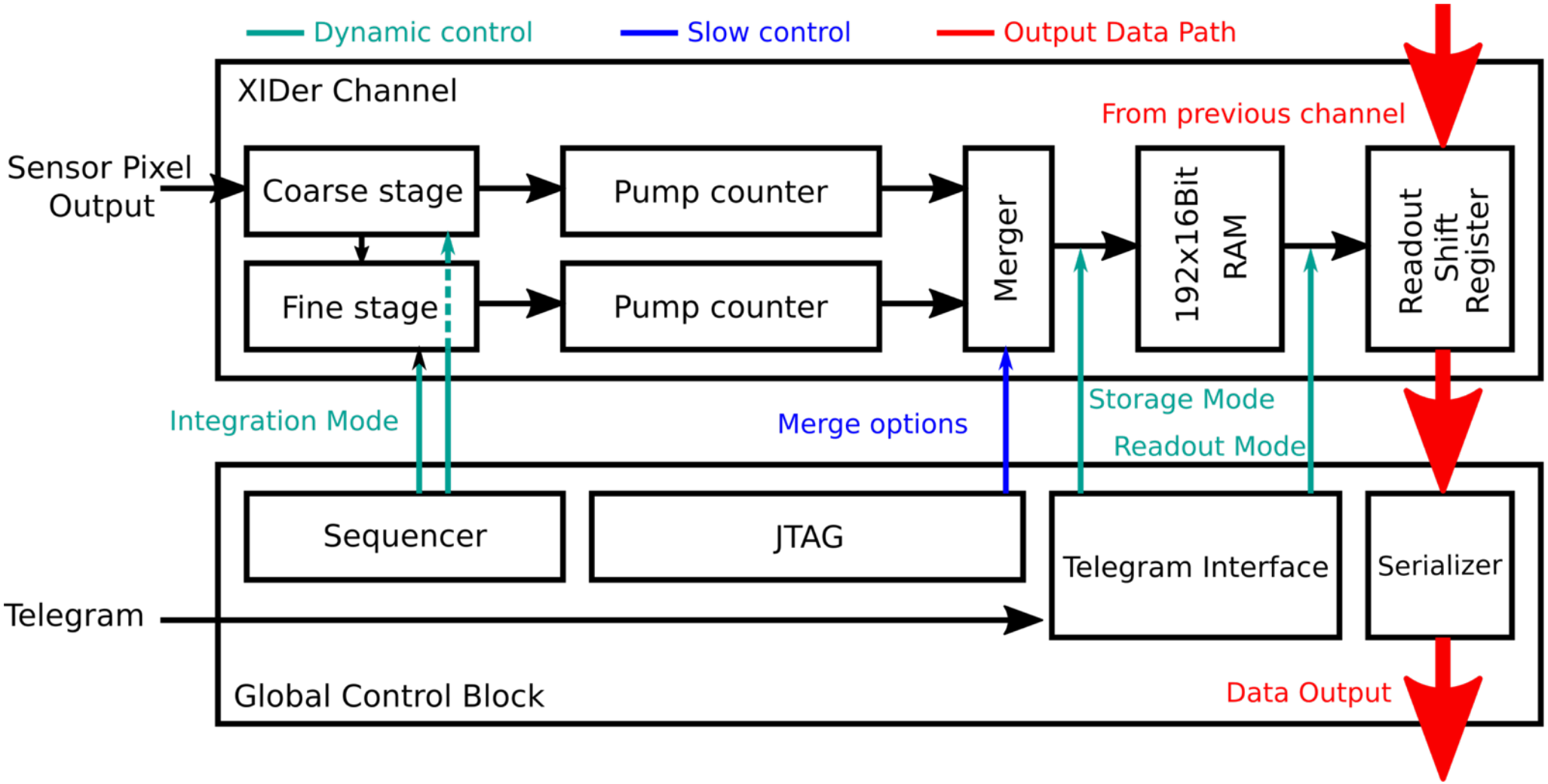
- Frontend linear throughout whole measurement range!
- Actual measurements will be far below 100 photons per shot
- **Only the charge pump linearity counts!**

  ⇒ **Very robust design**

Added Circuitry

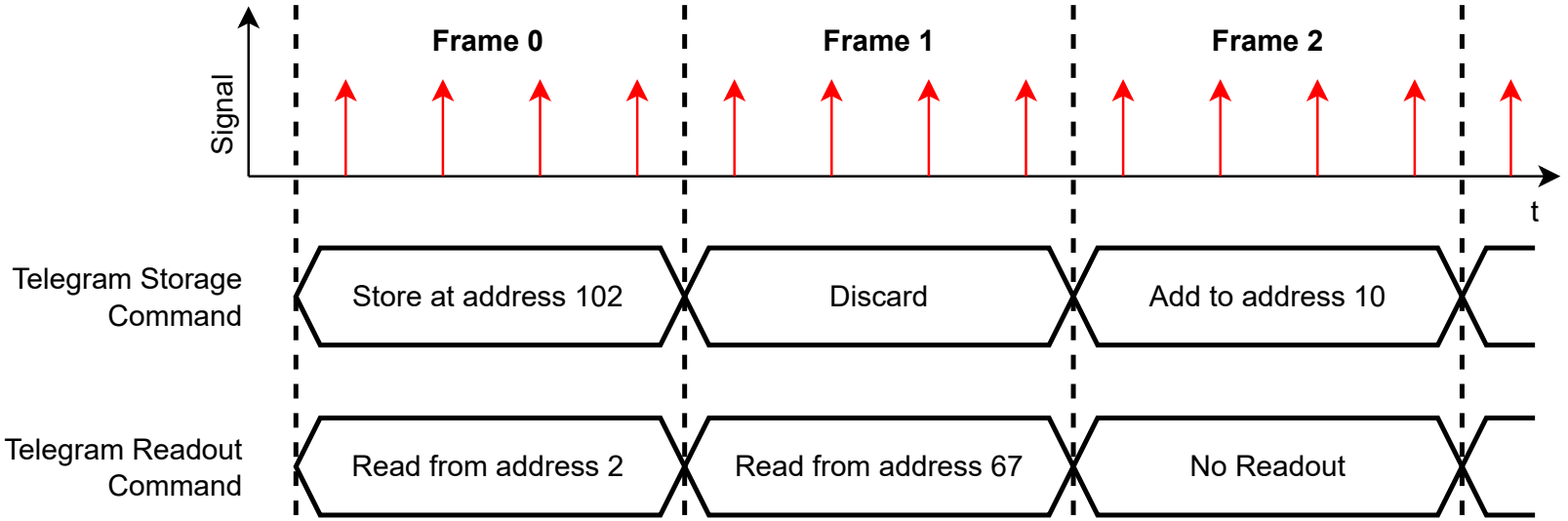
Since March 2021

On-Chip Data Handling



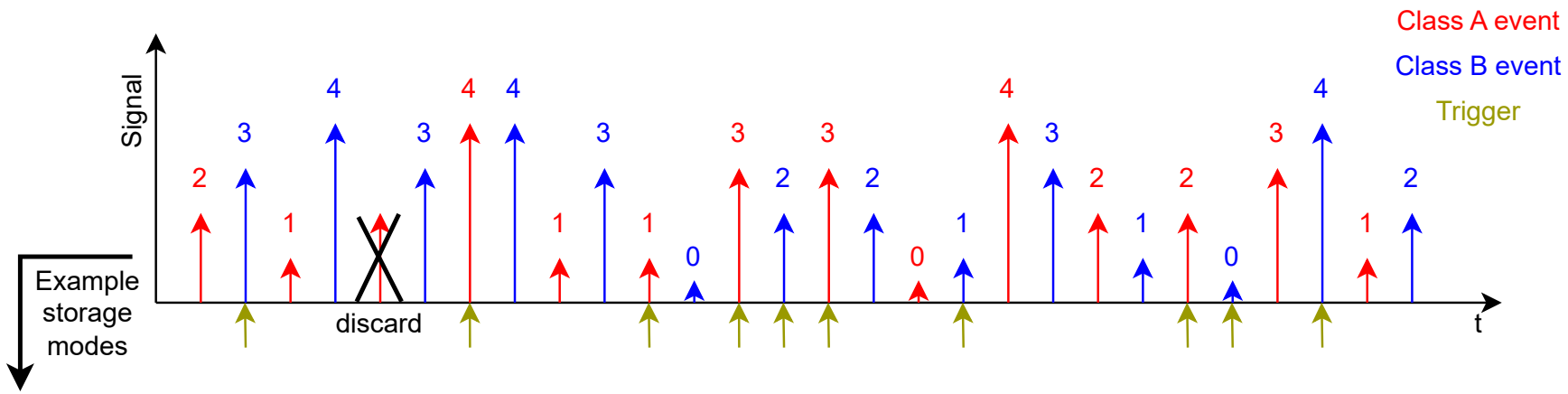
Design of digital blocks was carried out by Michael Ritzert

Telegram Protocol



- Telegram Protocol is meant to provide maximum flexibility in data taking
- Sends commands to the ASIC channels on frame-level for data storage and readout
- Example for currently available commands:
  - Store counted photons at given RAM address
  - Add/subtract counted photon value to/from value stored at given address
  - Increment value stored in given address
  - Read data from given address

Telegram Protocol Storage Mode Examples



RAM Address	Consecutive	Accumulated & consecutive	Histogram	Classified histogram	Triggered & consecutive
...	...	...	...	...	...
9	1	3+2=5	0	3	4
8	3	1+4=5	0	4	0
7	1	2+0=2	0	3	2
6	4	2+3=5	0	2	1
5	4	0+3=3	0	2	3
4	3	3+1=4	5	2	2
3	4	4+1=5	7	3	3
2	1	3+4=7	6	3	1
1	3	1+4=5	6	4	4
0	2	2+3=5	3	1	3

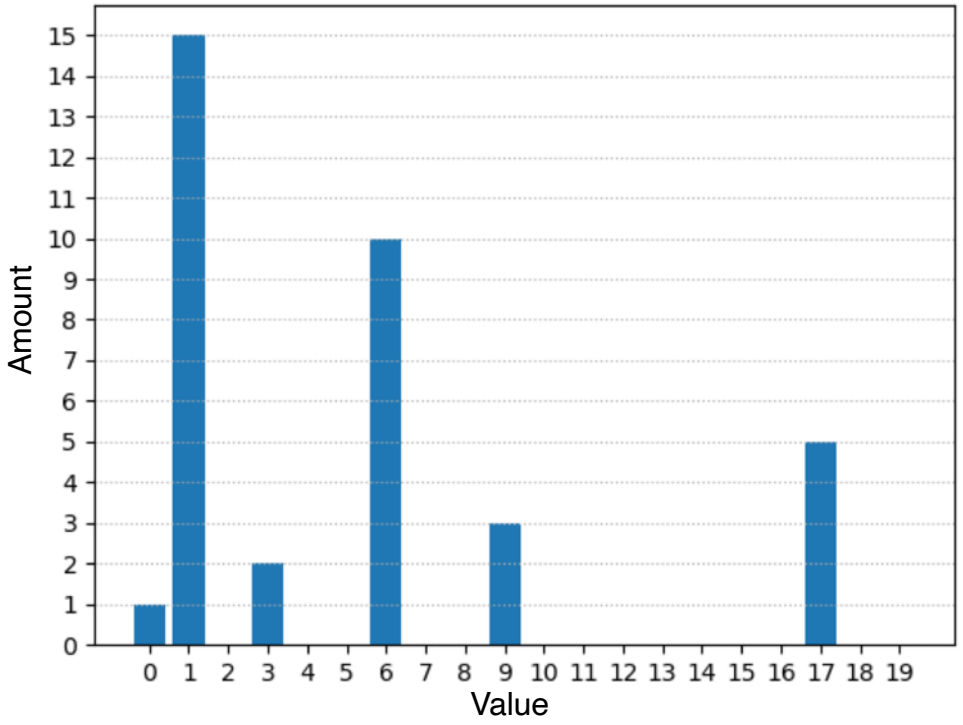
- There are many more modes
- Actual choice depends on the user's requirements

Lab Test of Histogram Mode

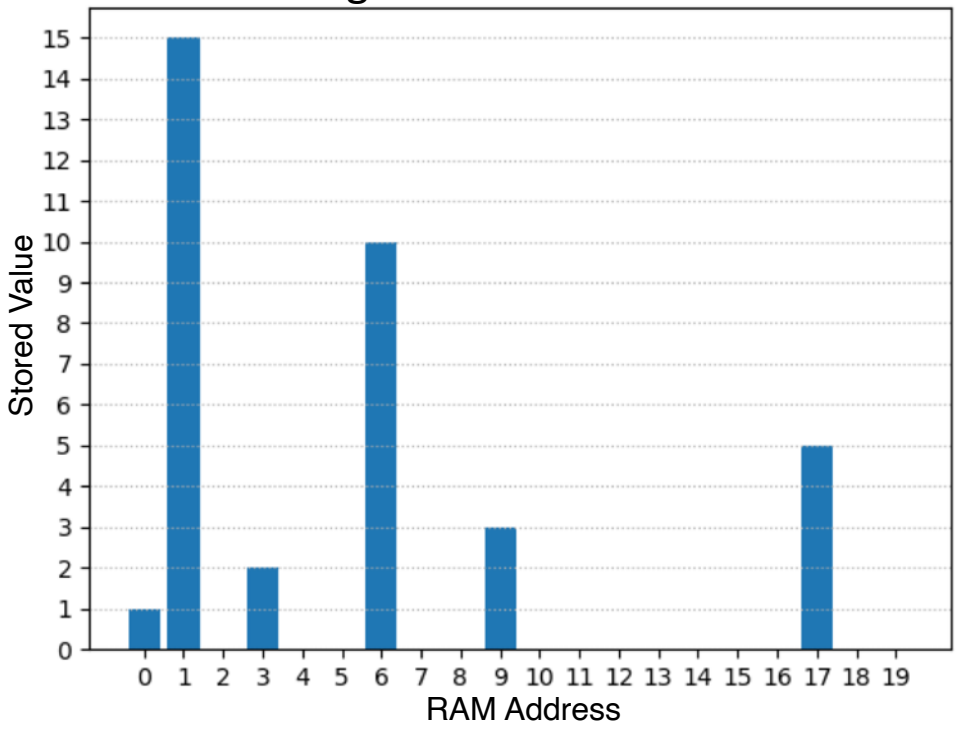
Simple lab test:

- Provide frontend with N values of known input distribution
- Readout on-chip RAM and compare stored histogram to input distribution

Input Distribution



Readout Histogram



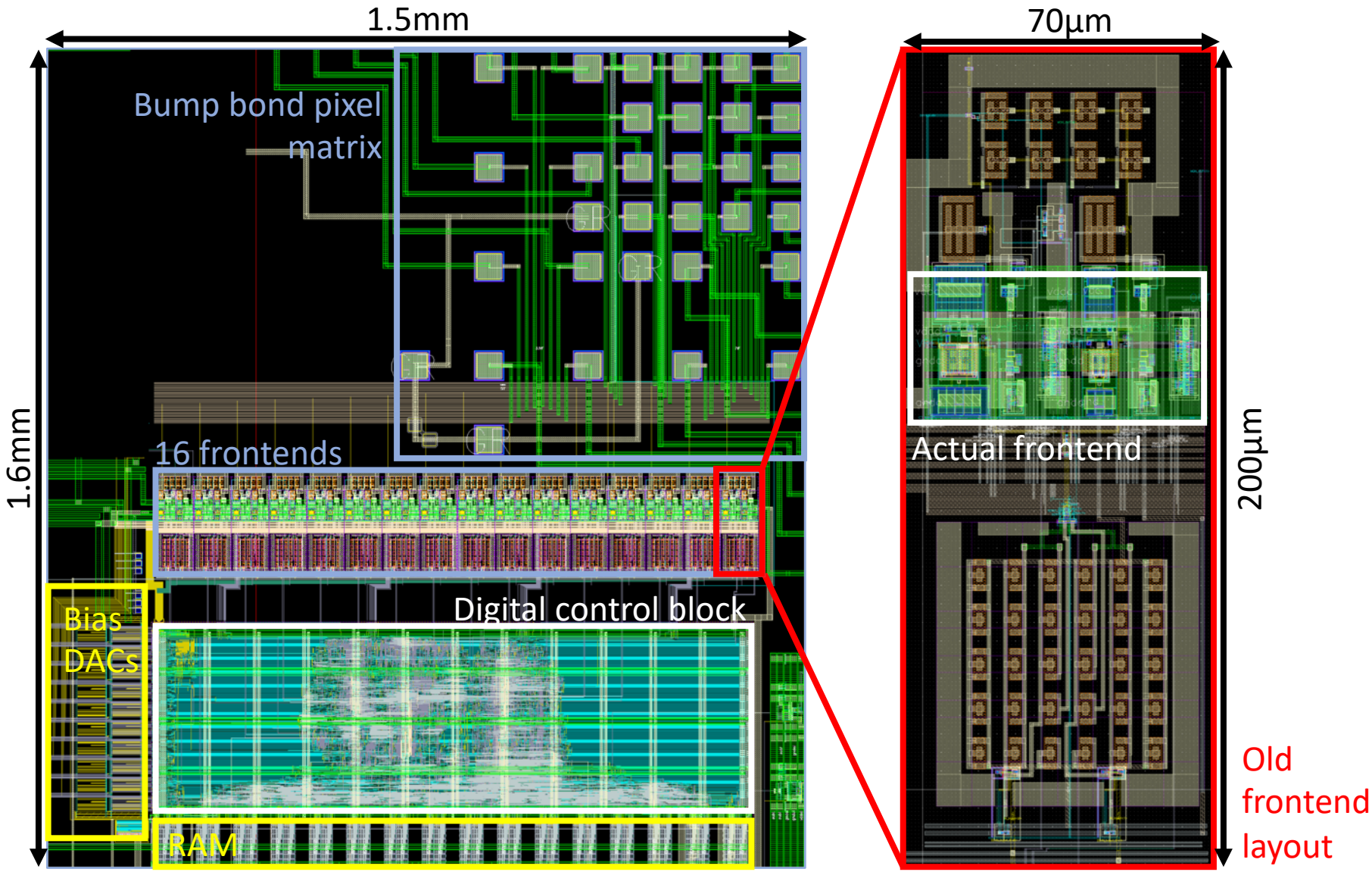
Road to Large Scales

Since March 2021

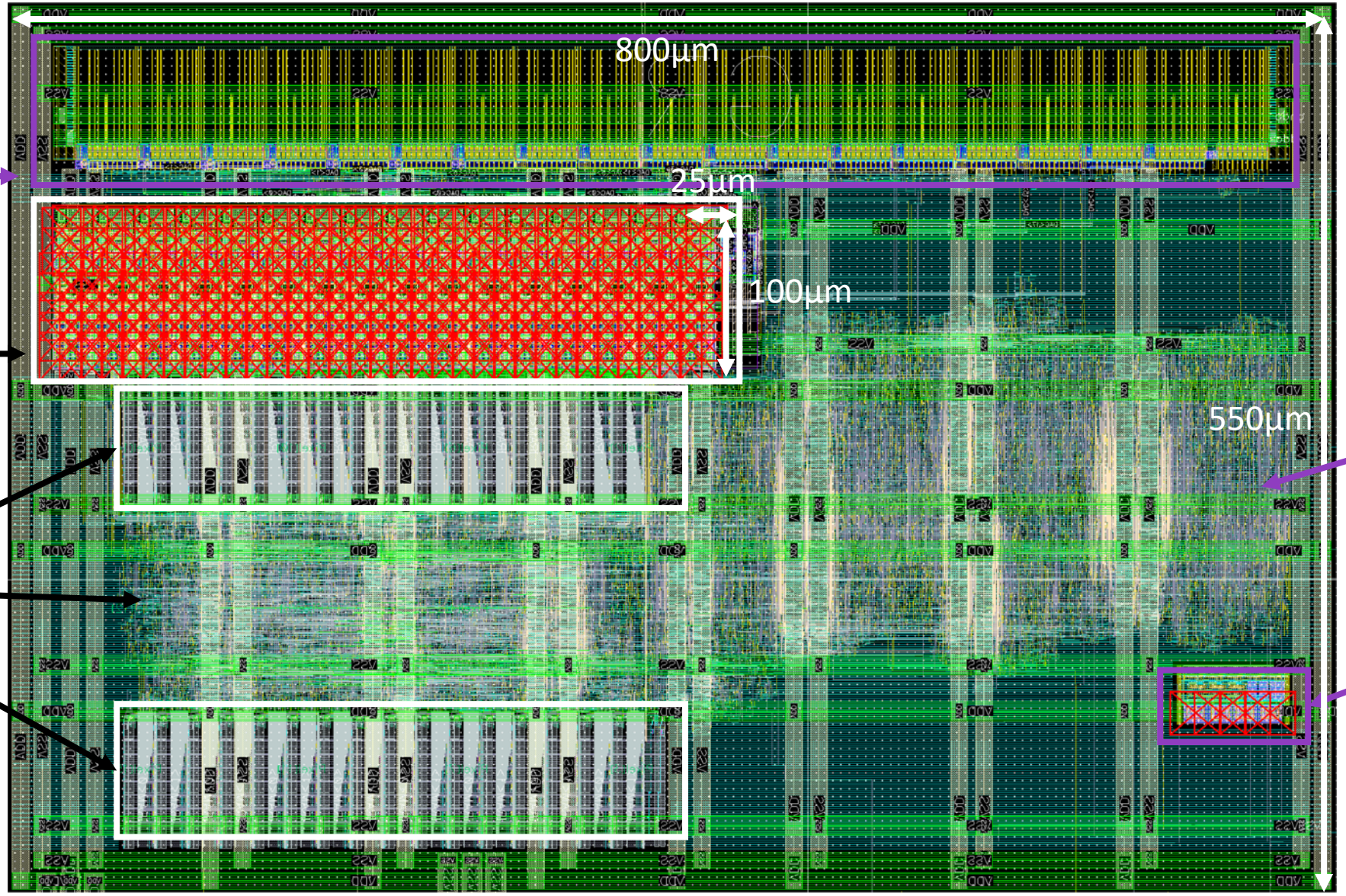
Old Chip Layout

T4 prototype matrix (until 2021):

- No electronics underneath pixel pads
- Long wires from pixel matrix to frontends
- Clear separation of single compartments
- Not scalable to larger pixel matrices
- Frontend design way too large for 100µm pixel pitch matrix



T5's New Scalable Pixelated Layout (2021)



Global (once per ASIC): DACs

16 FEs

RAM cells

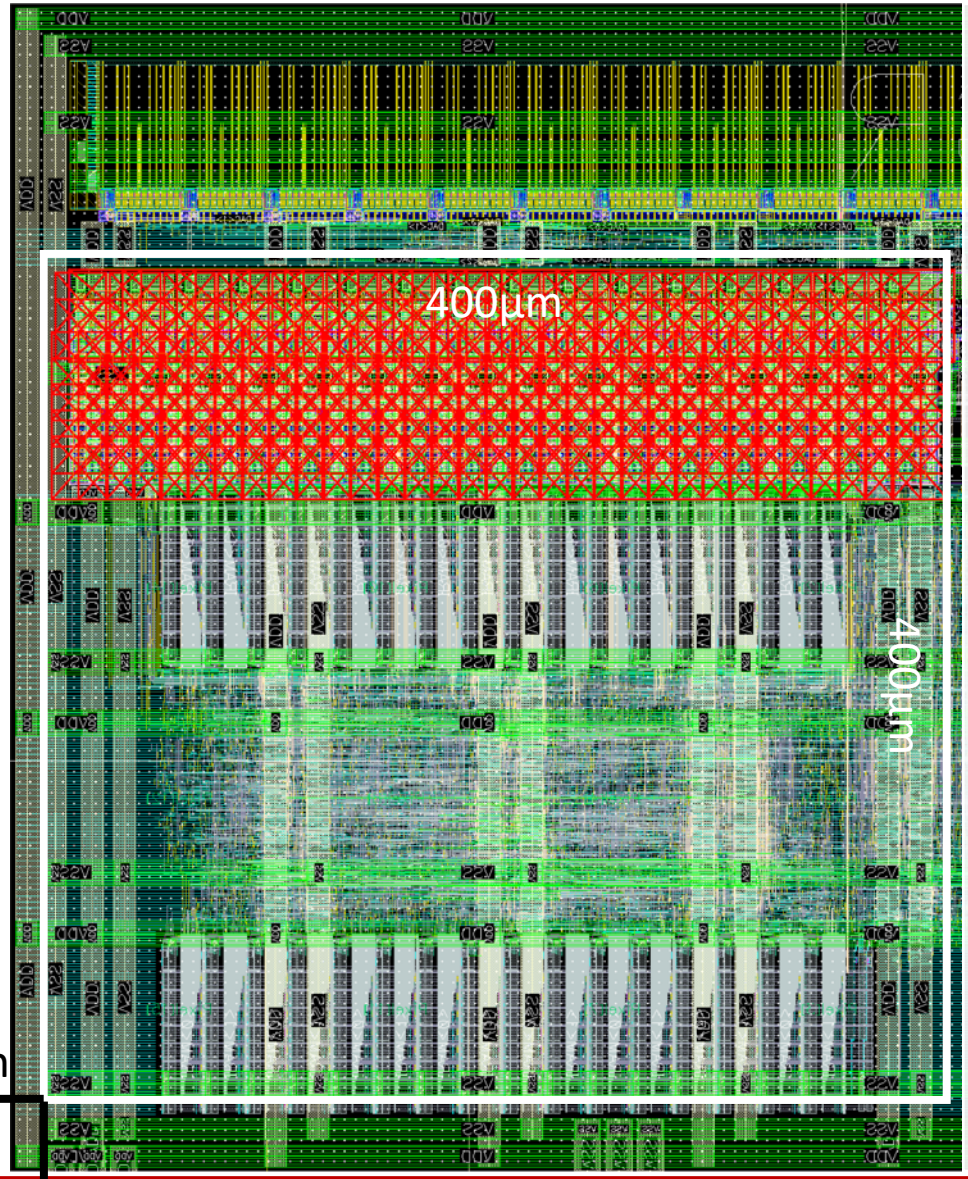
Pixel control

Global blocks: Sequencer, Telegram interface, output link serializer, JTAG interface

Global Power-on reset

Top-level integration and synthesis performed by Michael Ritzert

T5's New Scalable Pixelated Layout (2021)

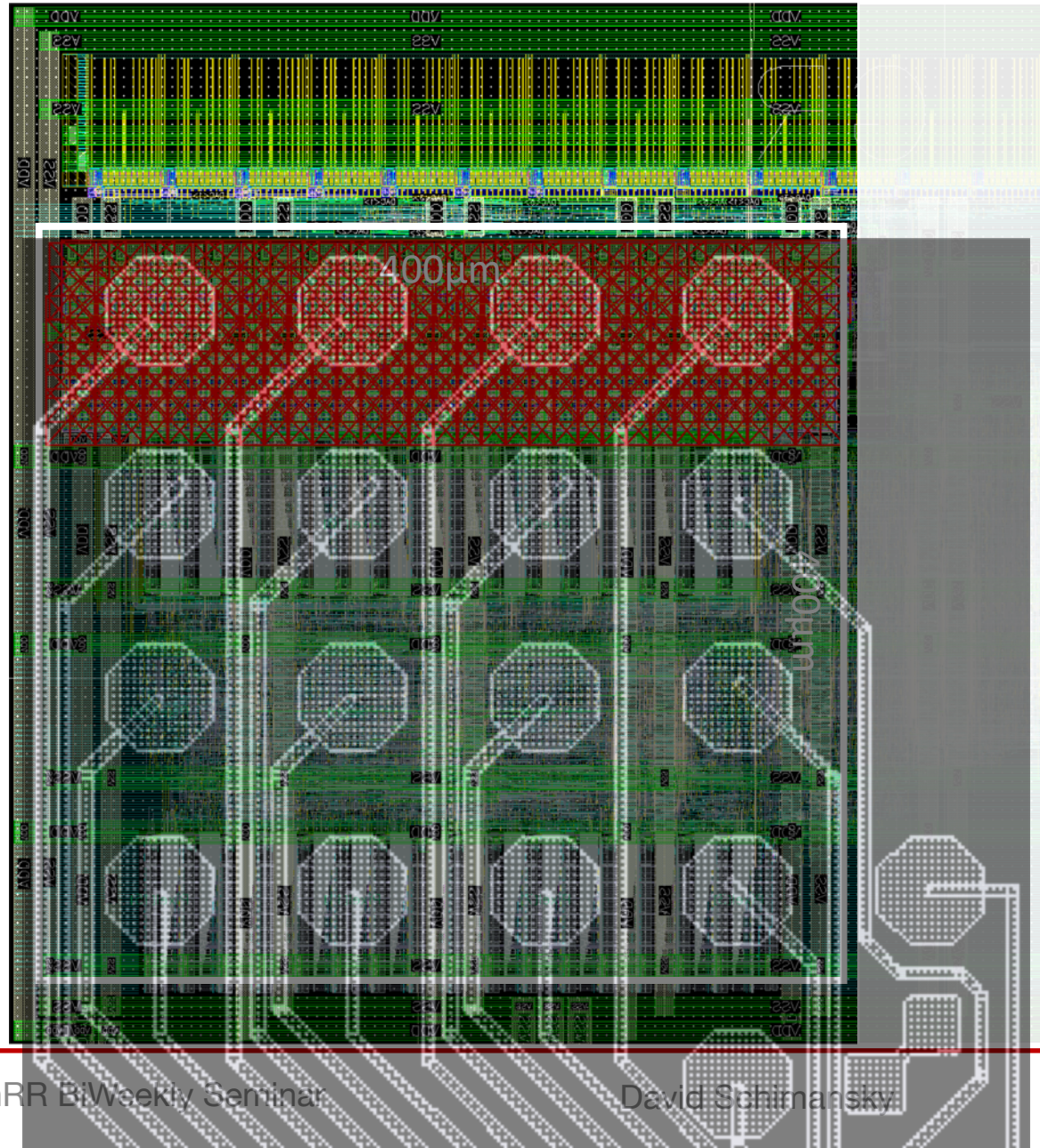


Can be stacked in this direction

Can be flipped in this direction

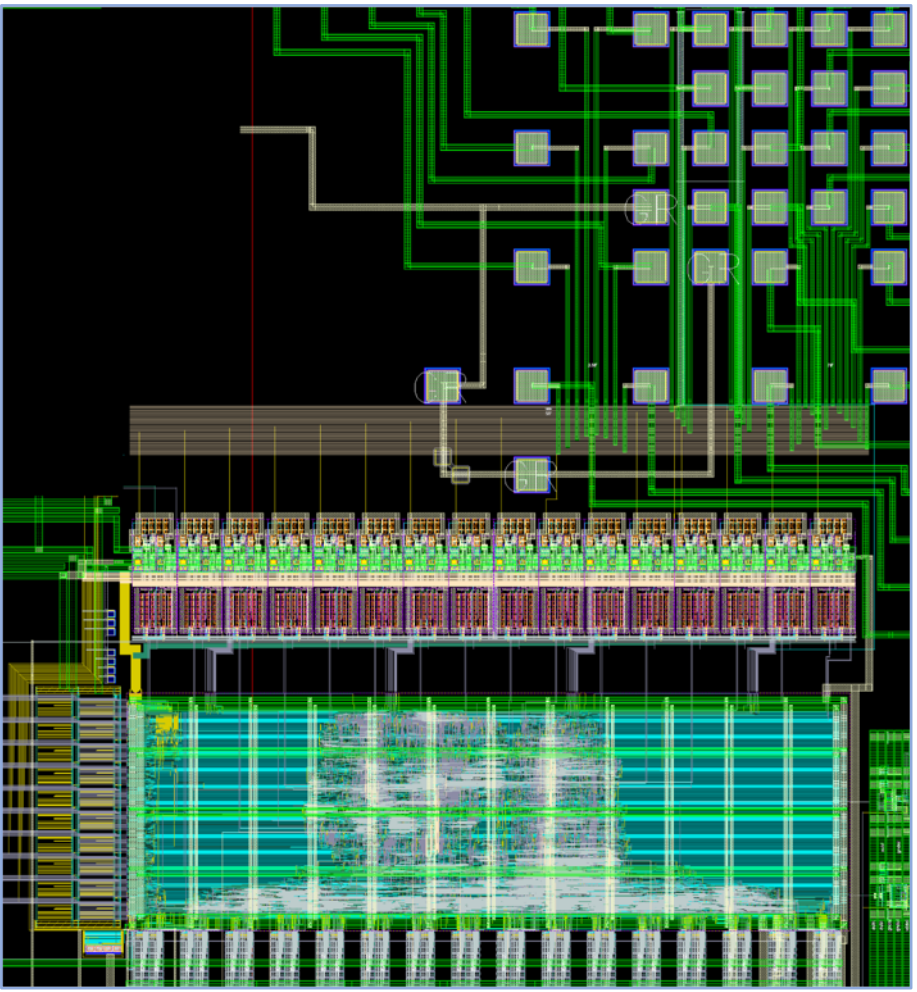
- 4x4-Pixel module with size: 400x400µm^2
- Can be stacked both in x and y direction to build large pixel arrays

T5's New Scalable Pixelated Layout (2021)

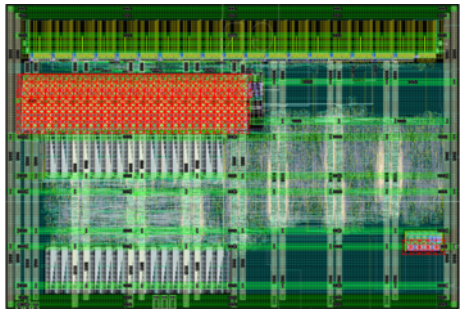


- 4x4-Pixel module with size: 400x400µm^2
- Can be stacked both in x and y direction to build large pixel arrays
- Pad-Matrix on top-most metal layer – above electronics

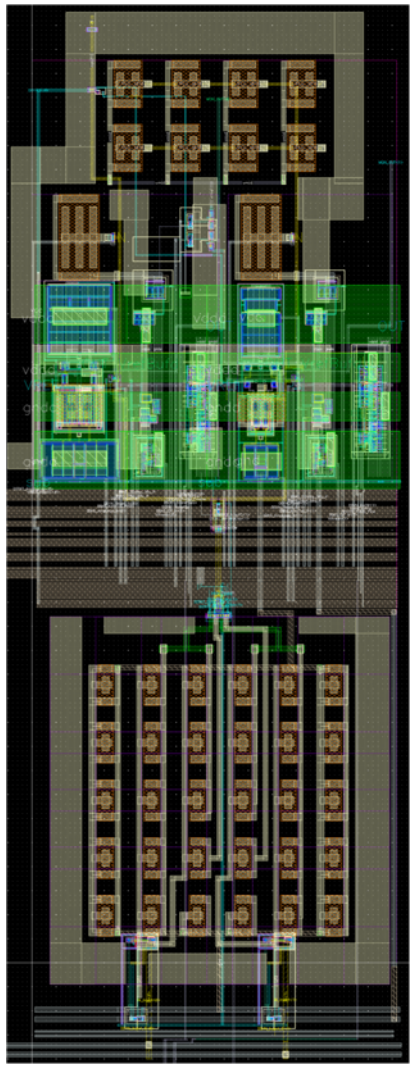
To-Scale Size Comparison of Old and New Layouts



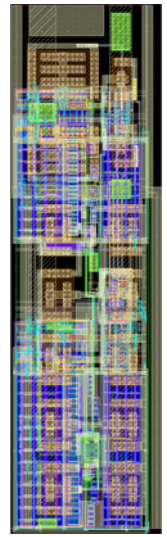
/6



Matrix | Frontend

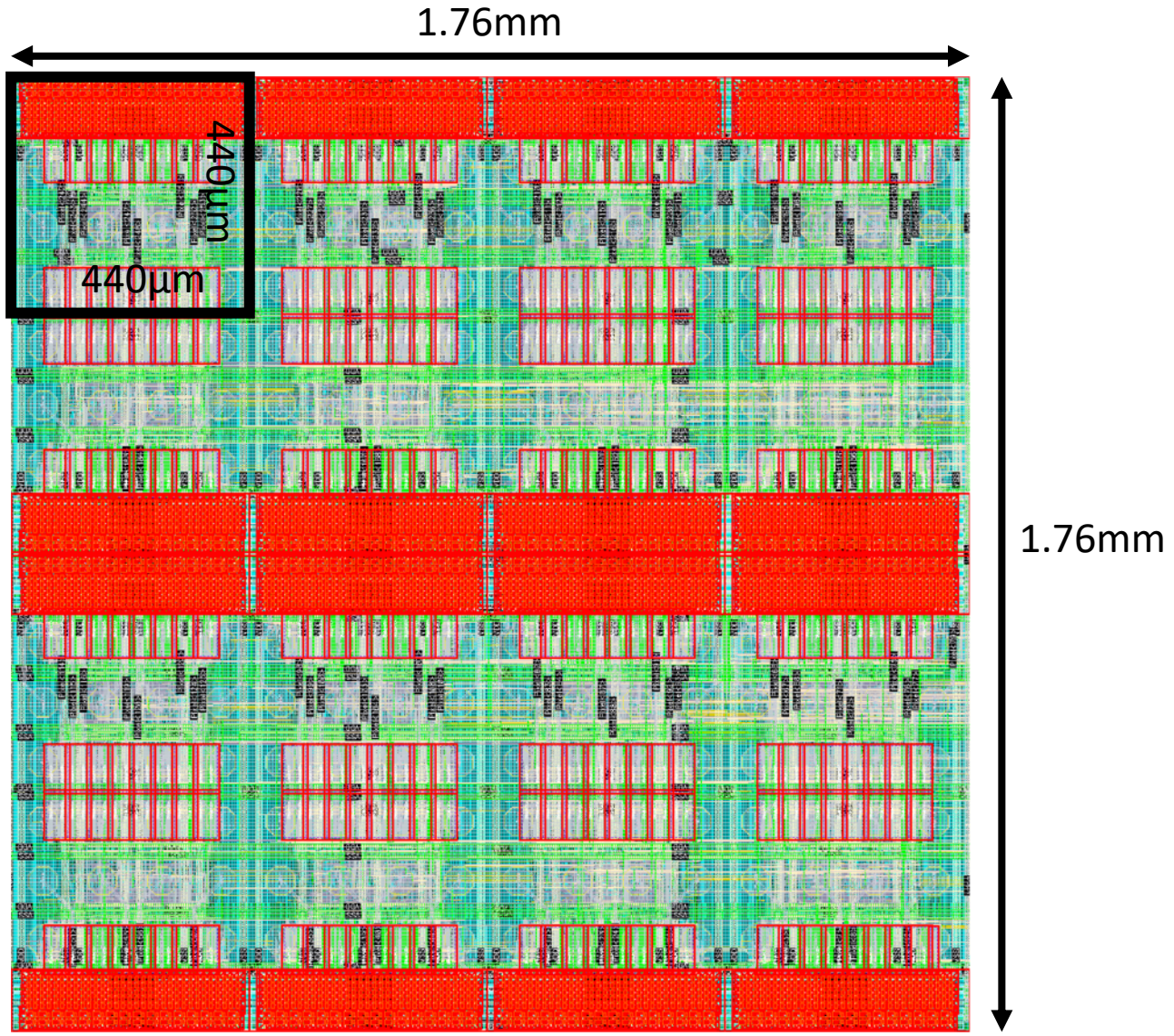


/6



T6: 16x16 Matrix Prototype

- Shared silicon die with STFC:
  - Cooperation for prototype testing and sharing IPs
  - STFC allocated free space on one of their runs for us (Thank you!)
- 110µm pitch
- 256 pixels
- Submitted in Oct. 2022
- Not yet received

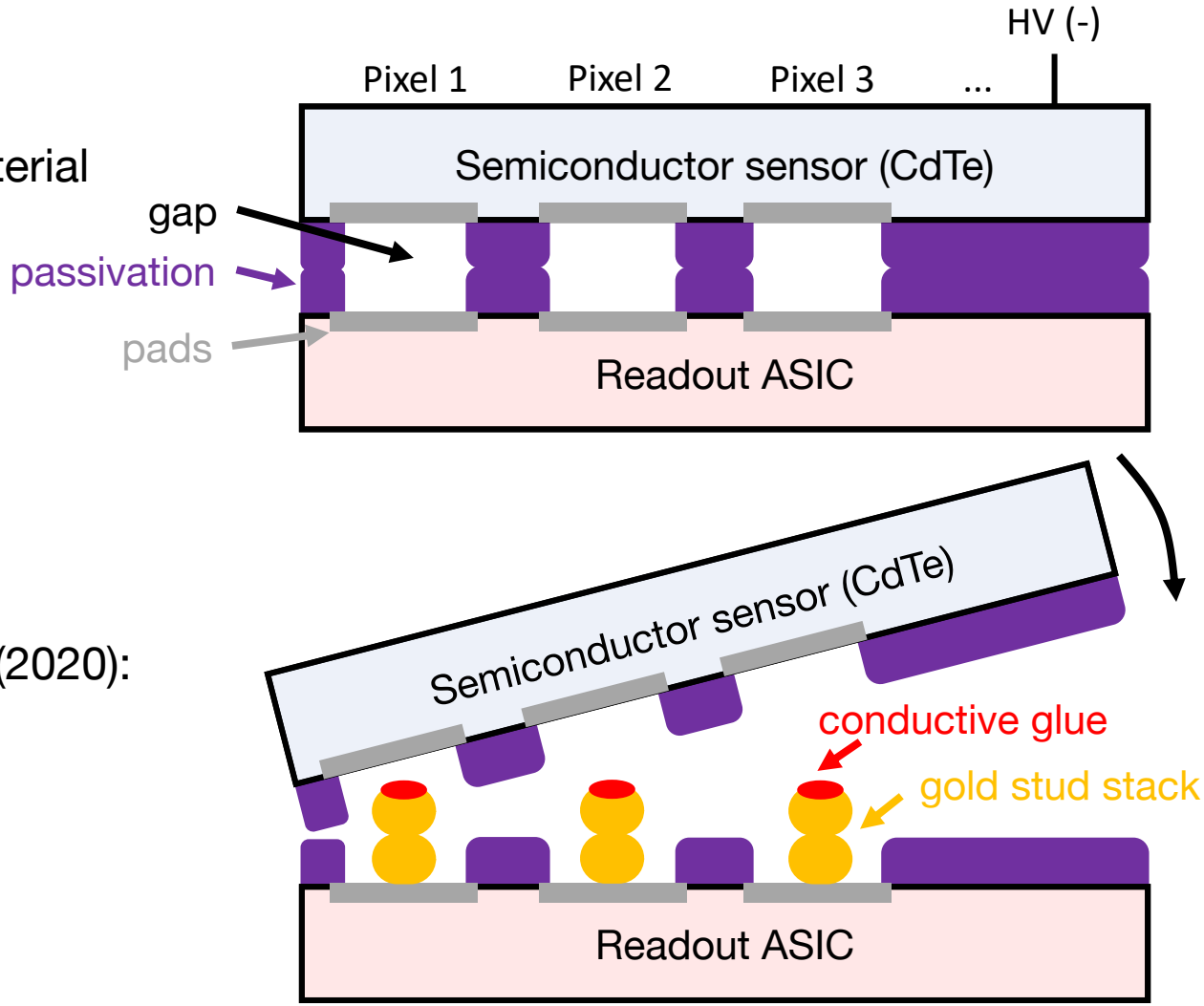


ASIC/Sensor Interconnection with T2 (2020)

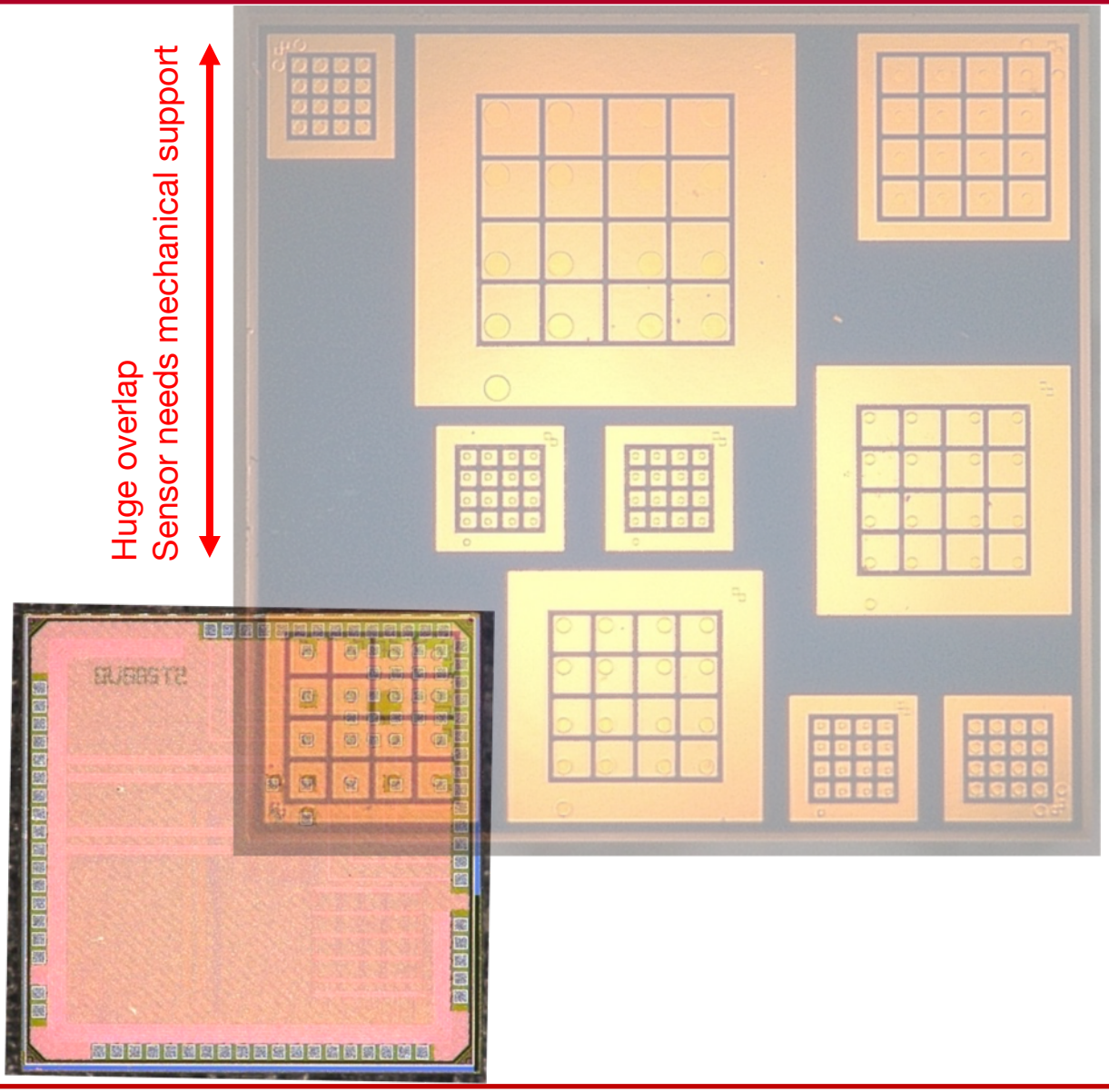
- Pixelwise flip-chip interconnection with 100µm pitch
- Need to fill gaps in between pads with conductive material
- Problems with CdTe:
  - No high temperatures (>80°C)
  - No mechanical pressure

⇒ Soldering is out of question

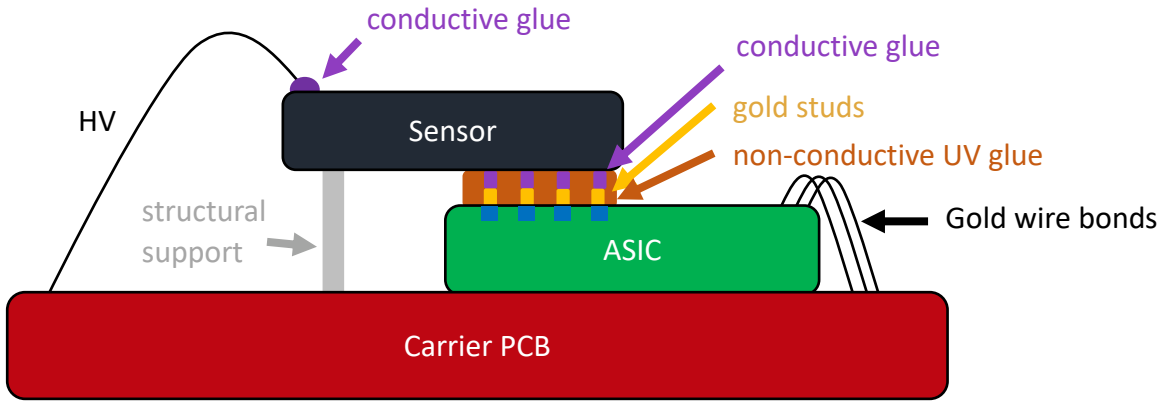
- Solution proposed and carried out by Christian Kreidl (2020):
  - Place stack of gold studs on ASIC to fill gaps
  - Dip gold stud tips in conductive glue that cures at room temperature
  - Flip sensor on top



ASIC/Sensor Interconnection with T2 (2020)

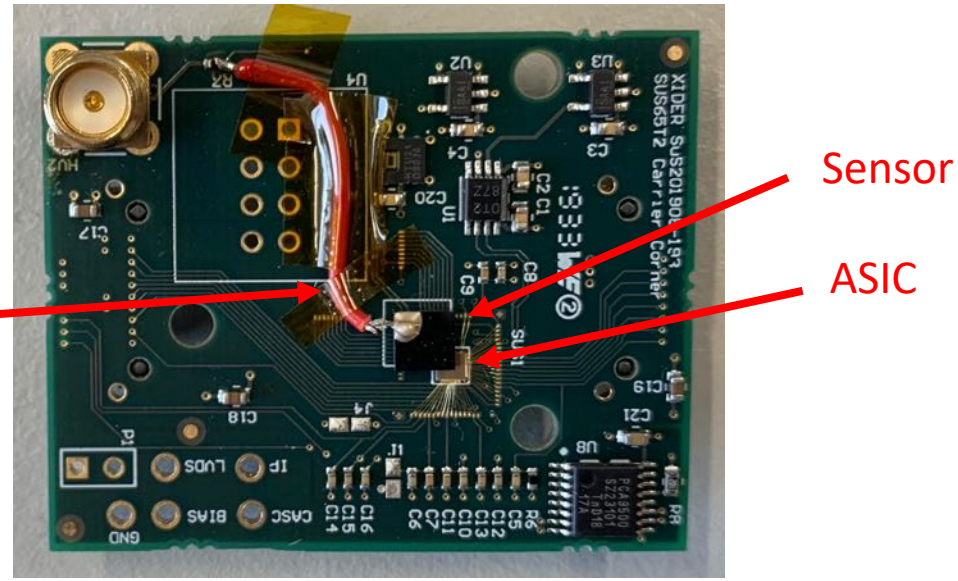


Schematic of ASIC/Sensor assembly on carrier PCB



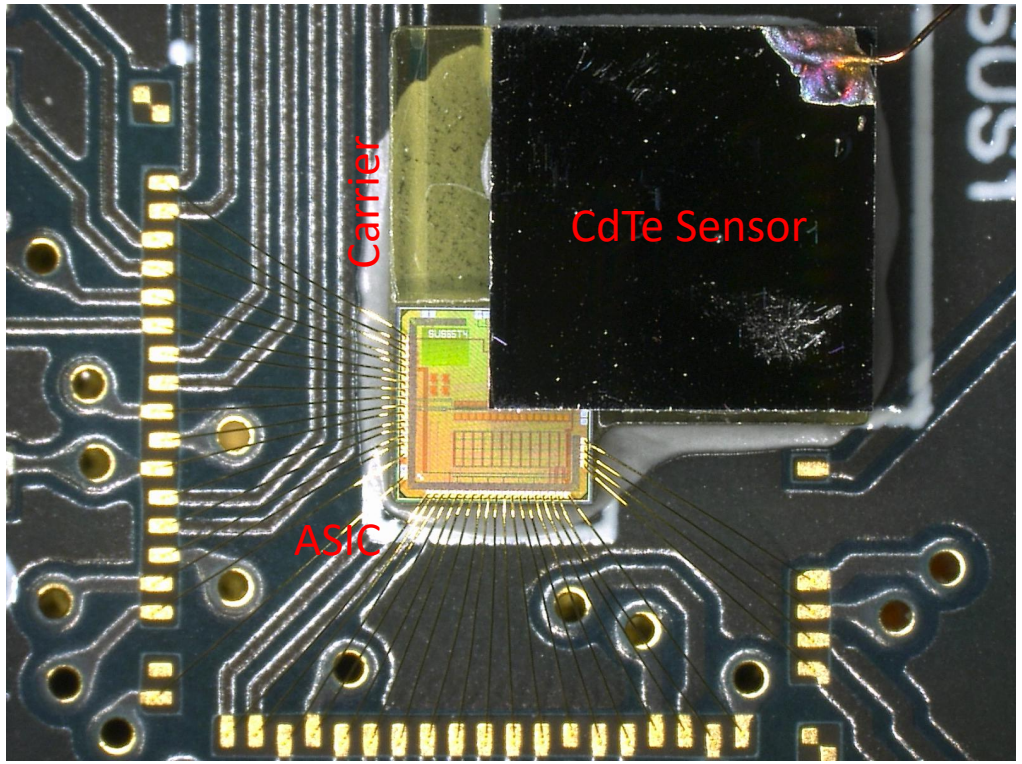
Carried out by Christian Kreidl

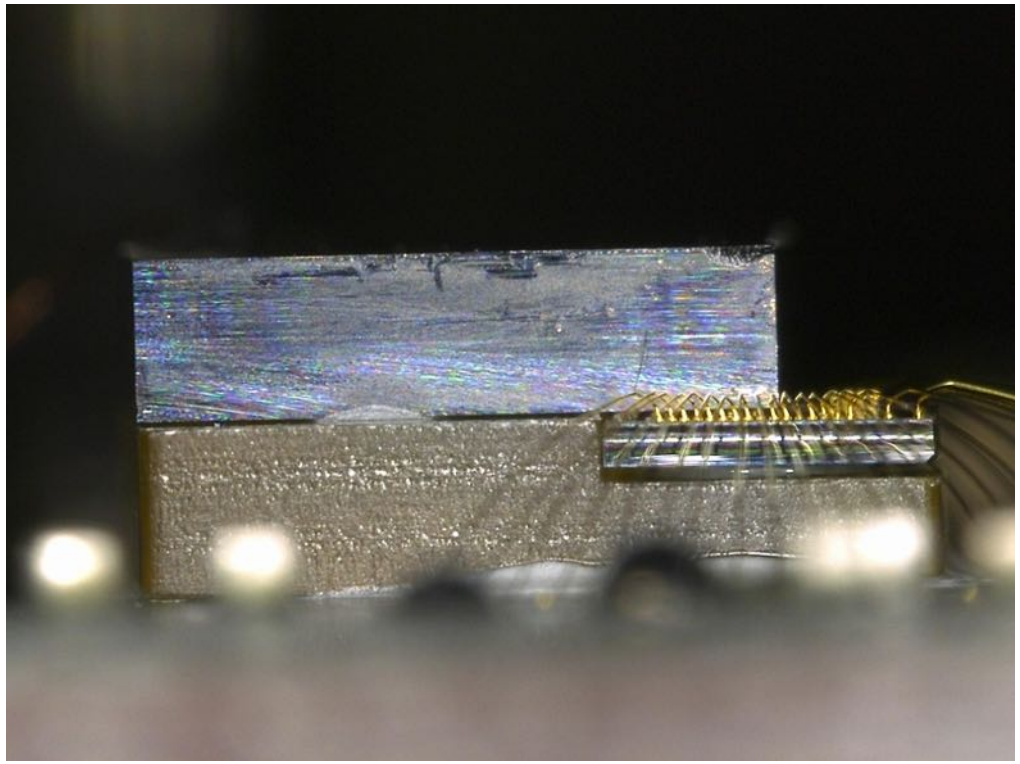
After almost one year of trying: Our first ASIC/Sensor assembly built in-house!



ASIC/Sencor Interconnection with T4

- Mid-end 2020, we established contact with a company (Polymer Assembly) for “mass” production
- Major difference to Christian’s procedure: Use ULTEM carrier to support overlapping sensor





- Beamtime characterization measurements will be presented by Marin Collonge

Summary

- XIDer is a multi-purpose platform for time-resolved x-ray diffraction experiments at synchrotron light sources
- High flexibility required with a broad range of requirements
- ASIC development:
  - Very promising R&D phase
  - Novel readout concepts with continuous conversion and telegram protocol
  - Small-scale readout ASIC prototypes meet the requirements
  - Cornerstone for large-scale designs has been laid
- Sensor research:
  - ASIC/Sensor bump-bond interconnection has been figured out
  - Readout ASIC used for CdTe and CZT sensors
  - Many beamtimes at the ESRF in the last two years for sensor and detector system characterisation
  - Details by Marin Collonge in two weeks