RD50-MPW4

- **To fix issues observed in RD50-MPW3**
  - Interface between matrix and periphery
    - We know the solution already (longer pull-down)
  - Easy generation of global time-stamp
    - We know the solution already (64-bit counter in the chip)
  - High noise in lower half of matrix
    - Currently studying this both in simulations and lab measurements

- **To further improve V_BD and therefore radiation tolerance too (V_BD > 400 V is possible)**
  - Improve rings around the chip as in test structures in RD50-MPW3
  - Improve HV distribution to the pixels (V_BD should not depend on the p/n pixel electrodes spacing any more)

- **To do backside biasing (thin beyond the 280 µm?)**
  - It is possible with MPW submissions (Liverpool experience with UKRI-MPW0 HV-CMOS chip)

Towards RD50-MPW4

- **Inquire RD50 management if they would support this new project**
  - Reply (18.11.2022): *“CERN-RD50 would be very supportive to this request”*

Towards RD50-MPW4

- **Inform LFoundry of our intentions, and inquire them especially about backside processing (p+ implantation, annealing and metallisation) (done on 07.12.2022)**
  - Is LFoundry interested in doing the backside processing?
    - If yes, that is excellent
    - If not, would they loan us the wafers to have the backside processing done at a third company (e.g. IBS)?
  - Currently waiting for a reply…

Towards RD50-MPW4

Technology	LF15A
Run ID	C15E23 (tape in 08.05.2023)
Project	RD50-MPW4
Quantity	3 high resistivity wafers (what high resistivities are available? in the past we have used 1.9 kohm*cm and 3 kohm*cm, and we are happy with them)
Requested area	Approx. 5 mm x 8 mm
Back grinding	Yes, 280 µm (thinner devices are also possible, but going <200 µm makes the chips incredibly fragile, not recommendable)
Back processing	Yes, backside p+ implantation, annealing and metallisation

Towards RD50-MPW4

- **Inquire Europractice about the Cadence Design Share Agreement? (done on 05.12.2022)**
  - Internal meeting at Europractice, with legal agreements expert, on 07.12.2022
  - Reply (08.12.2022): *New and simpler Multi-way Design Share Agreement* that minimises number of required agreements, and gives more flexibility for design collaborations
  - With N collaborators, we now need N agreements (rather than N*(N-1) agreements), but each agreement still needs to be signed by all the N collaborators
  - Not clear the new agreement can be used for more than one chip
  - We have received the reply today only, we need a bit more time to fully understand