PSD13

St. Catherine's College September 3-8, 2023

PSD TECHNOLOGIES FOR PARTICLE PHYSICS

PETRA MERKEL (FERMILAB)

b OUTLINE

- •Suite of recent detectors
- •Nearterm additions
- Future challenges

Apologies if I omitted your favorite detector!

Disclaimer:

Major tracking technologies for particle physics experiments include gaseous and fiber-based detectors. Here I focus on silicon-based systems only.

EVOLUTION OF SILICON TRACKERS FOR COLLIDERS \bigcirc

Dramatically increased challenges over the decades:

- Surface area
- Radiation exposure
- Readout channels

From P. Allport, Nature Reviews, Vol 1, (575), 2019

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SILICON TRACKERS AT THE LHC

ALICE ITS Pixels ATLAS Pixels with IBL ATLAS SCT Strips LHCb VELO Pixels

CMS Barrel Pixels

CMS Forward Pixels **CMS Strip Tracker**

ATLAS PIXELS

Insertable B-layer (IBL) upgrade in 2014

- closer to interaction point (3.35 cm)
- smaller pixels (50 x 250 μ m²)
- better sensors, better r/o chip (including 3D sensors at higher z)
- more rad hard
- significantly reduced X_0/L ayer

Improvement in impact parameter resolution

CMS PIXELS

Refurbishment during LS2

- new Barrel Layer1 with updated ASICs (lower thresholds)
- updated cooling and HV connections in the Endcap Disks
- new DC-DC converters with FEAST chip protected against failure in disabled output state
- upgraded HV power supplies up to 800 V $\overline{(\mathsf{I}_{\max} = 15 \text{ mA})}$

LHCB VELO UPGRADE

The VErtex LOcator was updated from silicon strips to pixels in 2022

- closest pixel at 5.1 mm to the LHC beam
- read out every event at 40 MHz (ultrahighspeed VeloPix ASIC)
- 41M pixels across 52 modules in secondary vacuum

RF Foil separating VELO vacuum from LHC vacuum

- 150 µm thick shield (Torlon with NEG coating)
- 3.5 mm from beam and 0.9 mm from sensors
- thermally stable, shields against RF pick-up

LHCB VELO UPGRADE

 $CO₂$ cooling through microchannels

- efficient, light and powerful cooling needed for operating in vacuum, very close to the beam
- building on success from original LHCb evaporative $CO₂$ cooling
- 500 µm Si wafer with 120 x 200 µm2 microchannels
- cooling power up to 40W at -30C

ALICE ITS UPGRADE

- New Inner Tracking System (ITS)
	- 10 m² of MAPS (Monolithic Active Pixel Sensor)
	- innermost layer: 2.2 cm from beam
- ALPIDE sensors
	- CMOS MAPS (180 nm TowerJazz technology) \rightarrow first CMOS MAPS-based tracker at the LHC!
	- 50 / 100 µm thick (inner / outer ITS)
	- 130,000 pixels/cm²
		- pixel size: 20 µm x 27 µm
		- sensor size: 15 mm x 30 mm
	- hit efficiency $> 99\%$
	- spatial resolution: 5 µm

FASER

- New small experiment installed in an old LEP injector tunnel during LS2
- Designed to detect particles in forward region, such as dark photons, Axion-like particles, etc.
- Tracker: 72 ATLAS SCT modules
	- single-sided p-in-n strip detectors, 80 µm pitch
	- \bullet 10⁵ channels in total in three stations

SILICON UPGRADES FOR HL-LHC

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HL-LHC UPGRADES: REQUIREMENTS

• New environment:

- Luminosity $@$ 5-7 x 10^{34} cm⁻²s⁻¹
- Integrated luminosity ≥ 3000 fb⁻¹ (x10 increase)
- Pile-up up to $<\mu$ = 200 (4x increase)
- Detector requirements:
	- High radiation tolerance
	- Improved track separation \rightarrow high granularity
	- Low occupancy, high bandwidth
	- Low mass

ATLAS ITK PIXELS

- Solutions for increased challenges:
	- All-silicon tracker with higher granularity $(5x10^9$ pixels)
	- Increased transparency: x2 lower (2.4 $X_0/Layer$)
	- Increased acceptance ($|\eta|$ <4): 5 barrel layers, up to 28 disks per endcap
	- 13m² active area
- Planar and 3D sensors
	- 3D (L0): 25x100µm2 (Barrel), 50x50µm2 (Endcap); more rad tolerant
	- Planar (L1-L4): $50x50\mu m^2$
- ITkPix chip developed out of RD53 (ATLAS-CMS common ASIC, 65nm TSMC)
- **Challenges**: large ASIC (20x20mm2); high density, low-pitch bump bonding; large V_{bias} across thin air gap (10µm) \rightarrow Parylene coating; large T_{ops} range; serial powering; low-mass services

CMS PIXEL UPGRADE

- $4.9m^2$, $2x10^9$ pixels, $100x25\mu m^2$ cell size
- Tracking coverage extended to $|\eta| \leq 4$
- 3D sensors in L1, planar n-in-p sensors everywhere else
- CROC chip based on common RD53 ASIC
- Parylene coating for spark protection
- Serial powering (insensitive to voltage drops, low mass cables)

light-weight mechanics: inner tracker can be removed for maintenance in an extended technical stop

ATLAS ITK STRIPS

- 180m² silicon, 60M channels
- 4 barrel cylinders, 6 disks per endcap
	- Barrel is made up of 1.4m long staves
	- Disks are made up of petals (60cm in r x 30cm in ϕ)
	- CF-based sandwich with embedded cooling
- n-in-p type FZ sensors from HPK
- ABCStar/HCCStar/AMC chip family (130nm) CMOS, GF), binary readout

CMS OUTER TRACKER

provides track information @ L1 trigger for 1st time at a hadron collider

- OT designed to provide L1 trigger stubs: p_T module concept
	- two closely spaced sensors read out by common set of ASICs
	- correlated stubs sent to backend at 40MHz
- Two types of module:
	- 2S (strip-strip) at outer radii
	- PS (pixel-strip) in inner layers
- 190m² silicon, 213M channels

CMS HGCAL

- Composed of cassettes, multiple modules mounted on cooling plates with electronics and absorbers
	- Hexagonal modules based on silicon sensors in high-radiation regions (EM+HAD)
	- Scintillating tiles with SiPM readout in lowradiation areas (HAD)
- $1.5 < |\eta| < 3.0$, \sim 215 tonnes per endcap
- ~600m² of silicon, 8" wafers, 6M channels $(0.5 \text{ or } 1 \text{ cm}^2 \text{ cell size})$
- $~\sim$ 500 m^2 of scintillators
- ~110kW(!) per endcap at end-of-life

ALICE ITS3

- 300mm wafer-scale MAPS (65nm TPSCo), fabricated using stitching
	- thinned down to ≤50µm making them flexible; bent to target radii
	- mechanically held in place by carbon foam ribs
- Extremely low material budget: $<$ 0.05% X_0 , homogeneous material distribution
- Planning to use air cooling

LHCB VELO UPGRADE II

- Planned for Run5 (2035+)
- Increased pileup $x10 \rightarrow$ add timing (50ps/hit)
- R&D on candidate sensors:
	- 3D pixels, LGADs, SiEM (Silicon electron multiplier sensor)
- Radiation tolerance up to $6x10^{16}$ 1 MeV n_{eq}/cm^2 (or regular module replacement)
	- extreme rates: 350kHz/pixel, 250Gb/s per ASIC
- Need to reduce mass by 80% X0 before 2nd hit \rightarrow operation in LHC vacuum

R&D needed for RF shielding: e.g. NEG coating \rightarrow amorphous carbon coating

R&D needed for active cooling: e.g. considering bi-phase Krypton cooling for operation $<$ -40C

SILICON BEYOND THE LHC

BELLE II PIXELS AND STRIPS

- SVD: double-sided strip sensors
	- AC-coupled strips on N-type substrate
	- \bullet 1.2m² sensor area, 224k strips
	- Wrapped flex circuit to read both side
- PXD: DEPFET pixel sensors
	- Ultra-thin sensor (75μ m), pixel size ($50x55-85\mu$ m²)
	- Low power consumption
	- High signal-to-noise
	- Switcher: rolling-shutter readout, 20µs integration time
	- Experienced some damage from beam loss events

MU3E

- Search for lepton flavor violating decay at PSI, under construction
- High-rate capability ($>10⁹$ muons/s)
- Excellent momentum resolution (<0.5 MeV/c)
- \rightarrow Extremely low material budget
	- Ultra-thin (50 µm) HV-CMOS MAPS sensor modules $(X/X_0 = 1.1 \text{ %}o)$
	- Gaseous Helium cooling

ELECTRON ION COLLIDER

Advanced silicon technologies under study:

- LGAD and AC-LGAD (Low Gain Avalanche Detectors)
	- Pixel size: $0.5 1.3$ mm
	- Resolution: spatial \sim 30 μ m, temporal \leq 30ps
- DMAPS (Depleted MAPS), e.g. MALTA
	- Pixel size: 36.4 µm
	- Resolution: spatial \sim 7 μ m, temporal \sim 2ns
- Lots of synergies with HEP developments \rightarrow early deployment of new ideas

LGAD irradiation tests at LANSCE

FUTURE COLLIDER DETECTORS

Focusing on e⁺e⁻ Higgs factories

Physics goals set stringent requirements for vertexing and tracking at Lepton Colliders:

misid. probability

jet

 10^{-}

 10^{-} Ω

- fast readout, low power (<20mW/cm²)
- low material (\sim 0.15 χ ₀)
- spatial resolution (\sim 3 μ m)
- "perfect" hit finding efficiency (~100%)
- extremely low fake rate

For future hadron or muon colliders, need R&D into radiation hardness and ultrafast timing

FUTURE COLLIDER DETECTORS

e.g. R&D on fine-pitch hybridization

- 25µm pitch bump bonding, sensor thickness down to 50µm
	- excellent interconnect yield >99.7% at IZM
- Hybridization with Anisotropic Conductive Films

e.g. R&D on Silicon-on-Insulator / 3D Integration

- SOI r/o electronics on thin low-resistivity wafer separated from highresistivity sensor wafer by buried insulation oxide layer
- thin and fast "monolithic" sensors
- challenge: specialized and complex fabrication

SMART PIXELS

• Idea: read out incident particle's properties (e.g. angle, or p_T) instead of raw data

- reduces data rates to manageable levels
- use AI to perform physics-motivated data reduction on-ASIC
- Use CMS Run2 data and simulation of charge evolution with time
	- train classifier to select clusters with p_T >200 MeV
	- Implement classifier on-ASIC: 1,163 parameters, <300µW, $\overline{\alpha}$ rea \leq 0.2mm²

SUMMARY

- Silicon-based detectors are vital to the physics program of many different kinds of experiments
- In future collider experiments they will be even more ubiquitous
- However, in some cases we might be nearing the end of the possible (radiation hardness, feature size, low mass, timing, etc.)
- \rightarrow Need for a strong and diverse R&D program to explore novel concepts, including new materials

THANK YOU!

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