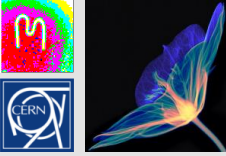


PROGRESS TOWARDS SEAMLESS LARGE AREA X-RAY AND GAMMA-RAY DETECTORS

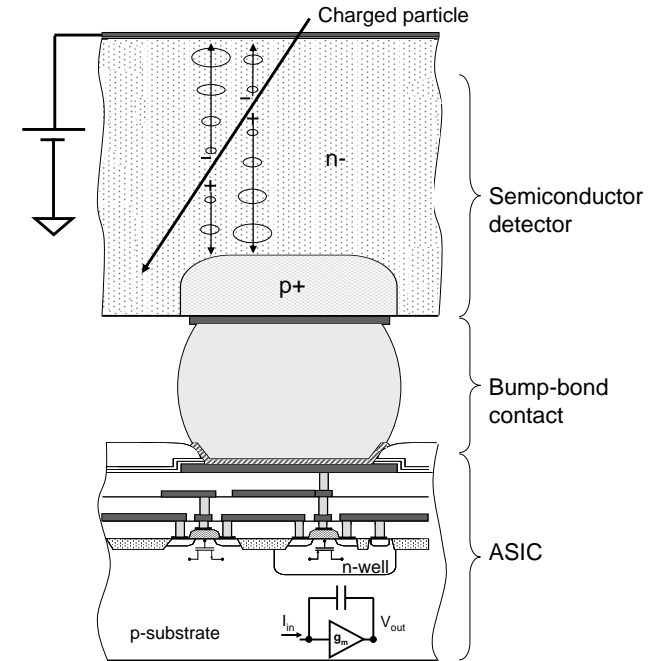
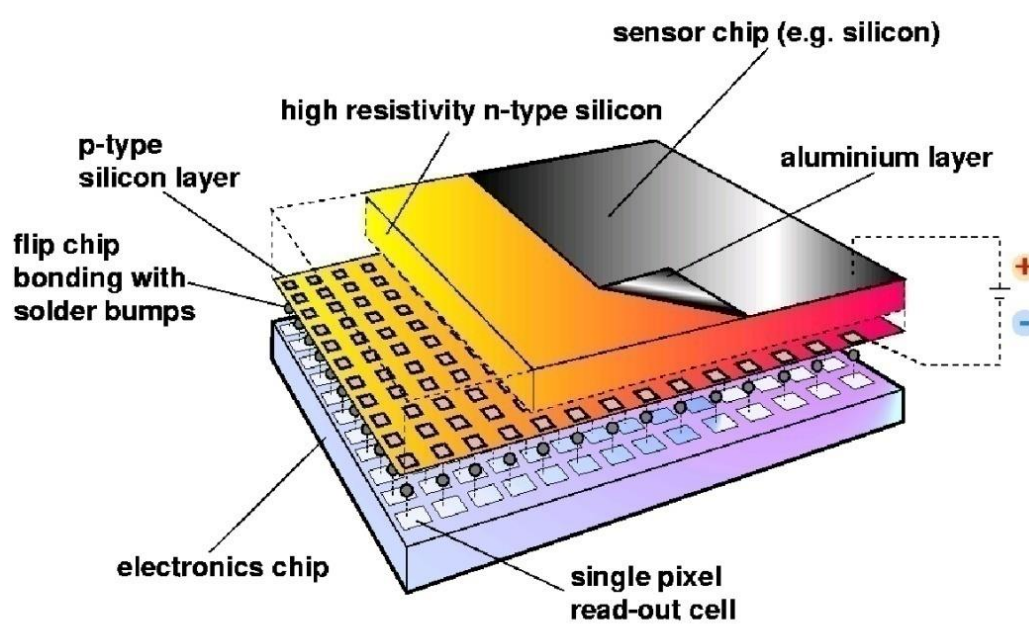
**M. Campbell¹, J. Alozy, R. Ballabriga, P. Christodoulou, X. Llopart,
F. Piernas Dias, V. Sriskaran, and L. Tlustos**

**CERN,
EP Department
1211 Geneva 23
Switzerland**

¹ Honorary Professor at Glasgow University

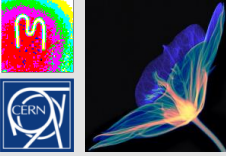


Hybrid Silicon Pixel Detectors

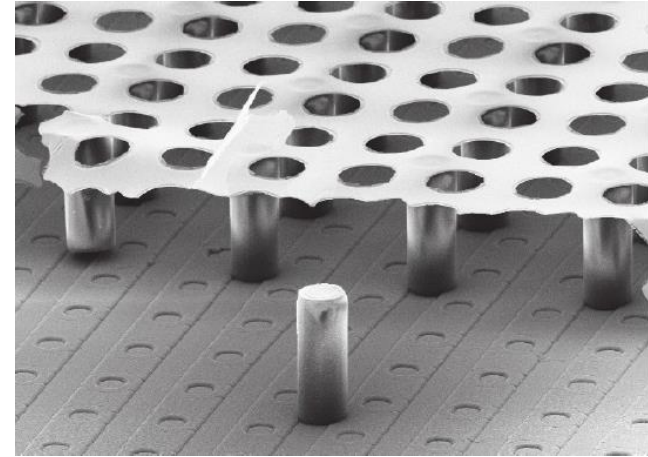
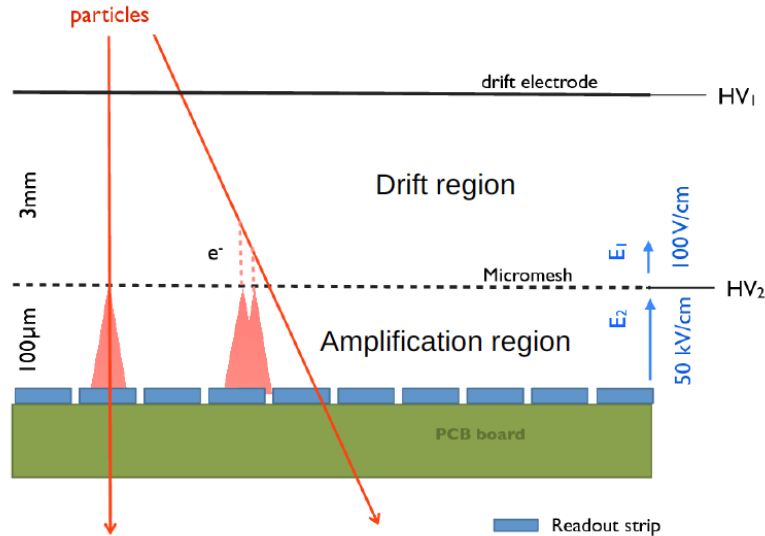


Standard CMOS can be used allowing on-pixel signal processing

Sensor material can be changed (Si, GaAs, CdTe..)

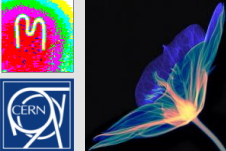


Gas detector readout - InGrid

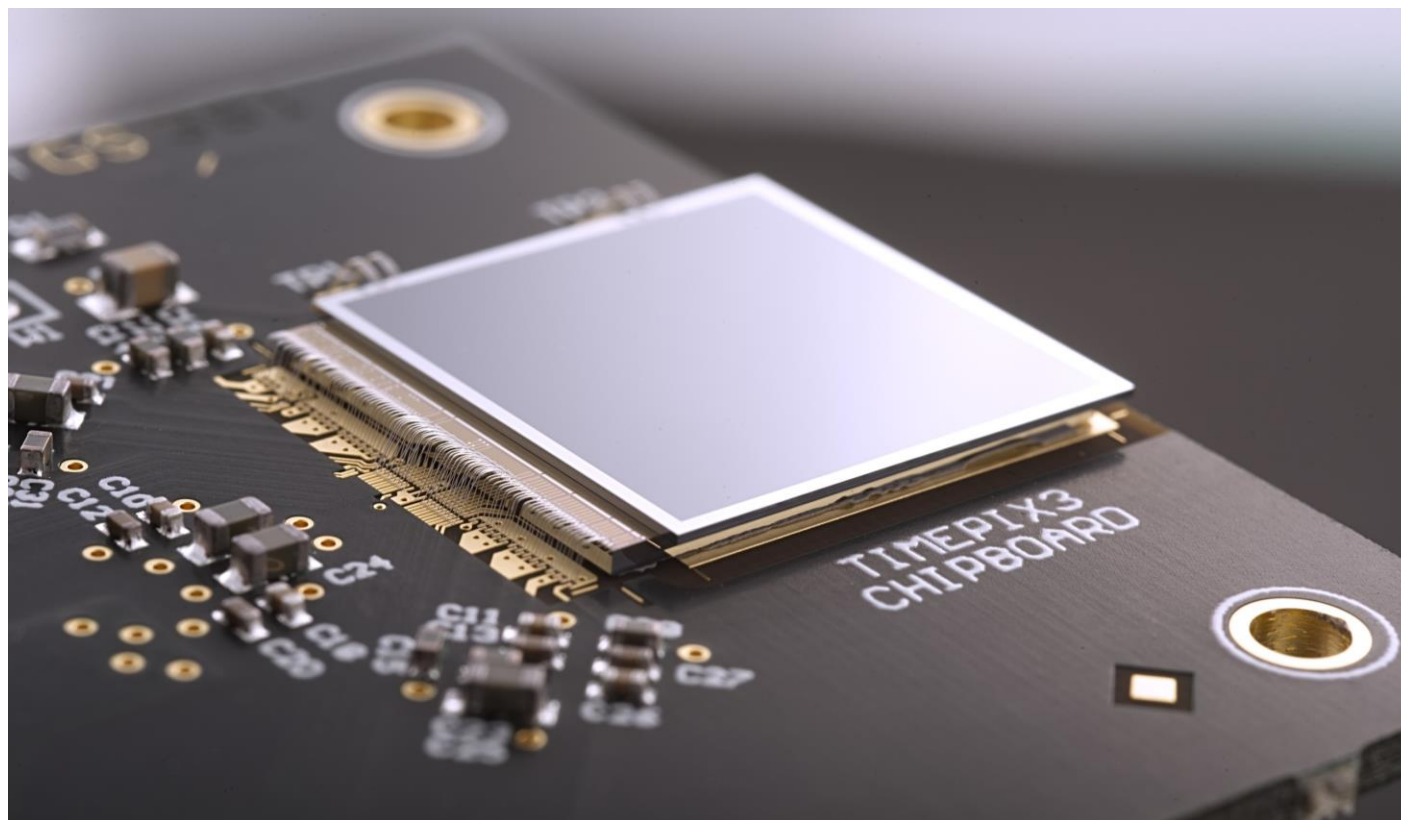


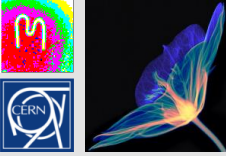
Semiconductor detector is replaced with charge amplification grid
Permits lower energy events to be detected
NB: GEM foils may be used in place of the InGrid foils

If placed in a photo tube together with a MCP visible photons may be detected
(see: M. Fiorini et al 2018 J.Instrum 13 C12005)

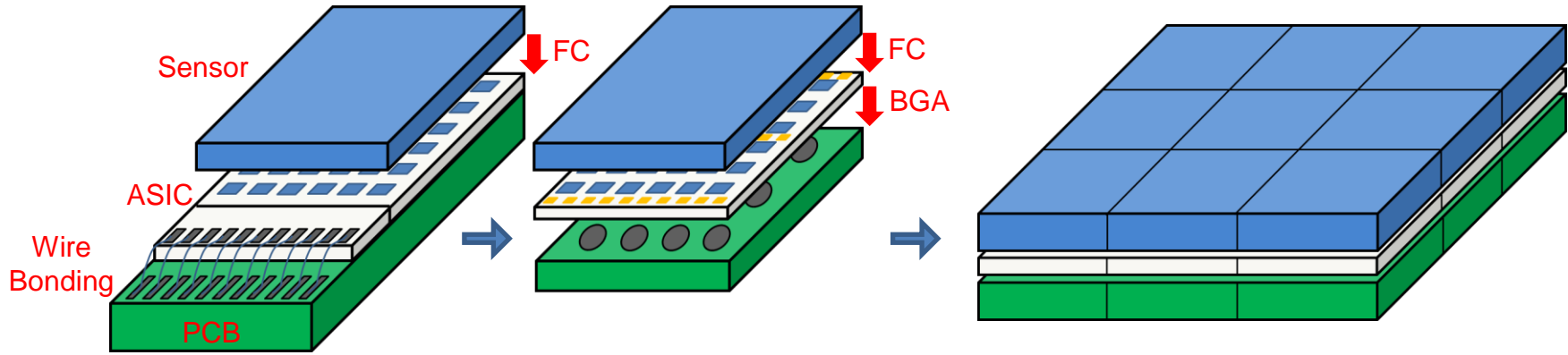


Timepix3 Photo





Tiling larger areas



- Target to build large area detectors by combining single chip modules.
- Through-silicon vias (TSVs) are the key technology enabler.
- Medipix4 and Timepix4 use on-chip interposer for bump to pixel redistribution layer (RDL).
- The detector is fully sensitive: even above the peripheral circuit and I/O pads.



Medipix2 (1999 ->)

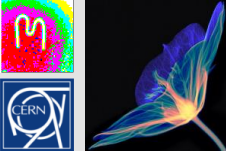
Albert-Ludwig Universität Freiburg, Germany
 CEA, Paris, France
 CERN, Geneva, Switzerland
 Czech Academy of Sciences, Prague, Czechia
 ESRF, Grenoble, France
 IEAP, Czech Technical University, Prague, Czech Republic
 IFAE, Barcelona, Spain
 Mid Sweden University, Sundsvall, Sweden
 MRC-LMB Cambridge, England, UK
 NIKHEF, Amsterdam, The Netherlands
 University of California, Berkeley, USA
 Universität Erlangen-Nurnberg, Erlangen, German
 University of Glasgow, Scotland, UK
 University of Houston, USA
 University and INFN Section of Cagliari, Italy
 University and INFN Section of Pisa, Italy
 University and INFN Section of Napoli, Italy

Medipix3 (2005 ->)

Albert-Ludwig Universität Freiburg, Germany
 AMOLF, Amsterdam, The Netherlands
 Brazilian Light Source, Campinas, Brazil
 CEA, Paris, France
 CERN, Geneva, Switzerland
 DESY-Hamburg, Germany
 Diamond Light Source, England, UK
 ESRF, Grenoble, France
 IEAP, Czech Technical University, Prague, Czech Republic
 KIT/ANKA, Forschungszentrum Karlsruhe, Germany
 Mid Sweden University, Sundsvall, Sweden
 NIKHEF, Amsterdam, The Netherlands
 Univesridad de los Andes, Bogota, Columbia
 University of Bonn, Germany
 University of California, Berkeley, USA
 University of Canterbury, Christchurch, New Zealand
 Universität Erlangen-Nurnberg, Erlangen, German
 University of Glasgow, Scotland, UK
 University of Houston, USA
 University of Leiden, The Netherlands
 Technical University of Munich, Germany
 VTT Information Technology, Espoo, Finland

Medipix4 (2016 ->)

CEA, Paris, France
 CERN, Geneva, Switzerland
 DESY-Hamburg, Germany
 Diamond Light Source, England, UK
 IEAP, Czech Technical University, Prague, Czechia
 IFAE, Barcelona, Spain
 JINR, Dubna, Russian Federation
 NIKHEF, Amsterdam, The Netherlands
 University of California, Berkeley, USA
 University of Canterbury, Christchurch, New Zealand
 University of Geneva, Switzerland
 University of Glasgow, Scotland, UK
 University of Houston, USA
 University of Maastricht, The Netherlands
 University of Oxford, England, UK
 INFN, Italy
 Chinese Spallation Neutron Source, Dongguan City, China
 Brazilian Light Source, Campinas, Brazil
 Philippine Nuclear Research Institute, Manila, Philippines

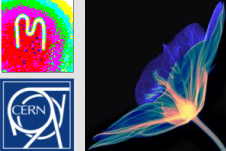


Acknowledgements – Commercial Partners

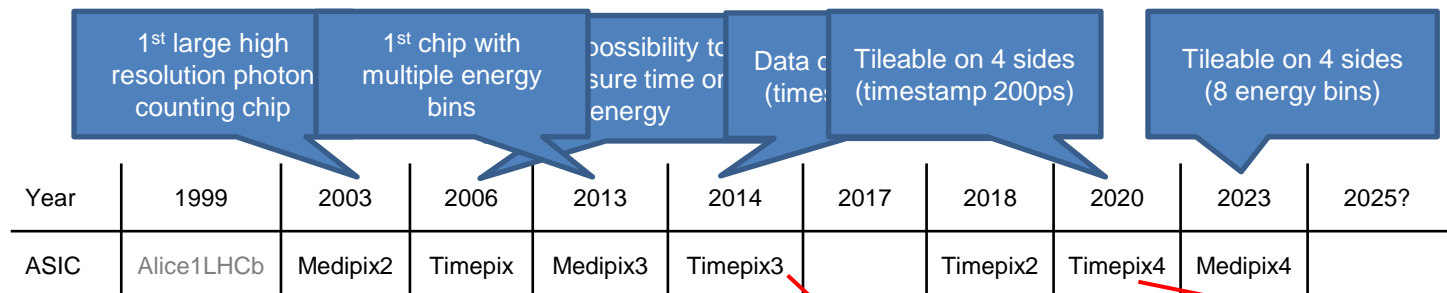
COLLABORATION NAME	Medipix2			Medipix3		Medipix4	
ASICS	Medipix2	Timepix	Timepix2	Medipix3	Timepix3	Medipix4	Timepix4
ADVACAM s.r.o., Czech Republic	X	X	X	X	X		X
Amsterdam Scientific Instruments, The Netherlands	X	X	X	X	X		X
Kromek, UK	X	X	X		X		
Malvern-Panalytical, The Netherlands	X	X	X	X			
MARS Bio Imaging, New Zealand				X			
PITEC, Brazil				X			X
Quantum Detectors, UK				X	X		X
Sydor Technologies, USA							X
X-ray Imaging Europe, Germany	X	X	X				
X-spectrum, Germany				X			X

X = commercial licensee

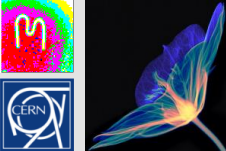
X = R and D licensee



The Medipix and Timepix ASICs - Timeline



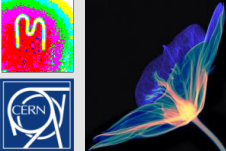
- Medipix chips aim at energy sensitive photon counting and typically use frame-based readout
- Timepix chips are more oriented towards single particle detection
- This talk will focus on Timepix4 and our efforts towards large area tiling



Timepix3 Specs

CMOS node	130nm
Pixel Array	256 x 256
Pixel pitch	55 μ m
Charge collection	e ⁻ , h ⁺
Pixel functionality	TOT (Energy) and TOA (Arrival time)
Preamp Gain	~47mV/ke ⁻
ENC	~60e ⁻
FE Linearity	Up to 12ke ⁻
TOT linearity (resolution)	Up to 200ke ⁻ (<5%)
TOA resolution*	Up to 1.6ns
Time-walk	<20ns
Minimum detectable charge	~500e ⁻ → 2 KeV (Si Sensor)
Max Analog power (1.5V)	500 mA/chip
Digital Power (1.5V)	~400mA data driven
Maximum hit rate	80Mhits/sec (in data driven)
Readout	Data driven (44-bits/hit @ 5Gbps)

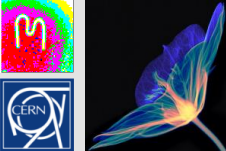
* Thanks to V. Gromov, et al. Nikhef, C. Brezina et al., Bonn



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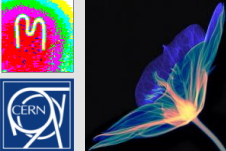
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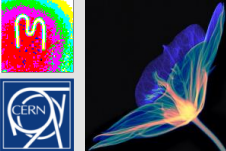
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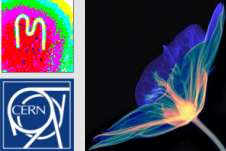
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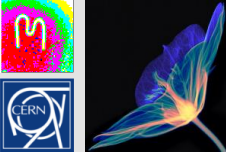
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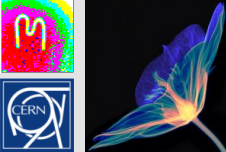
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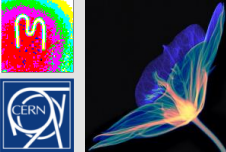
Timepix3 miniaturised readout



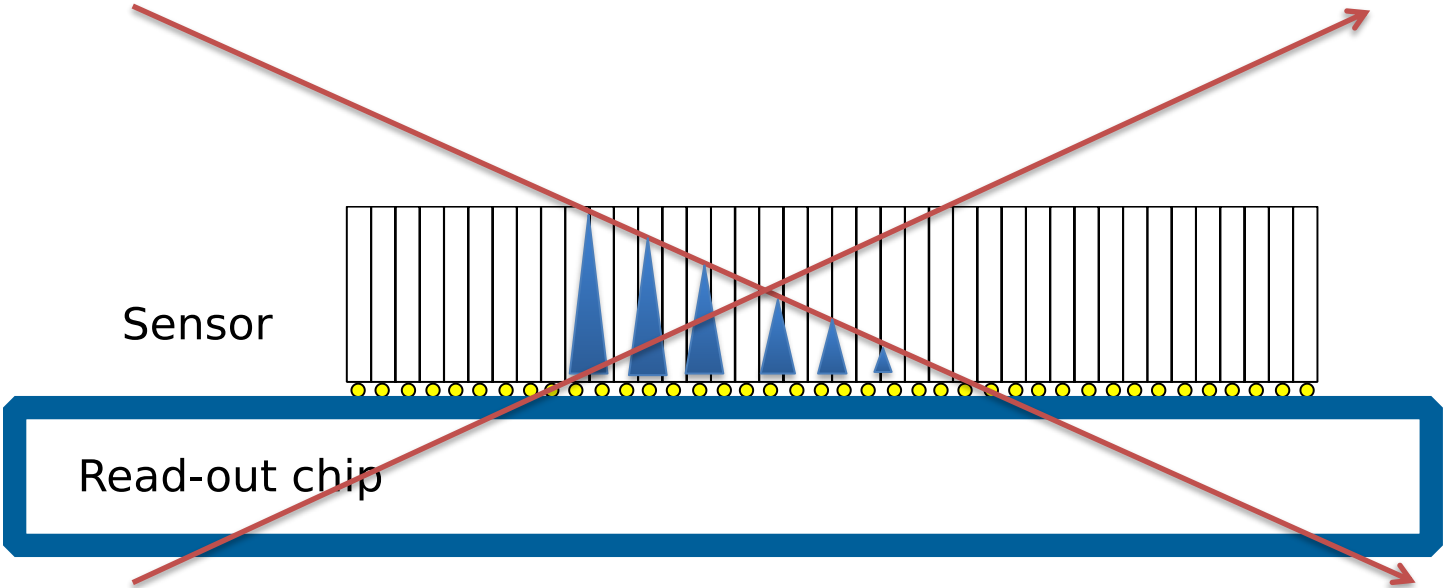
Advacam s.r.o., Prague

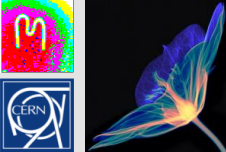


Timepix3 Demo

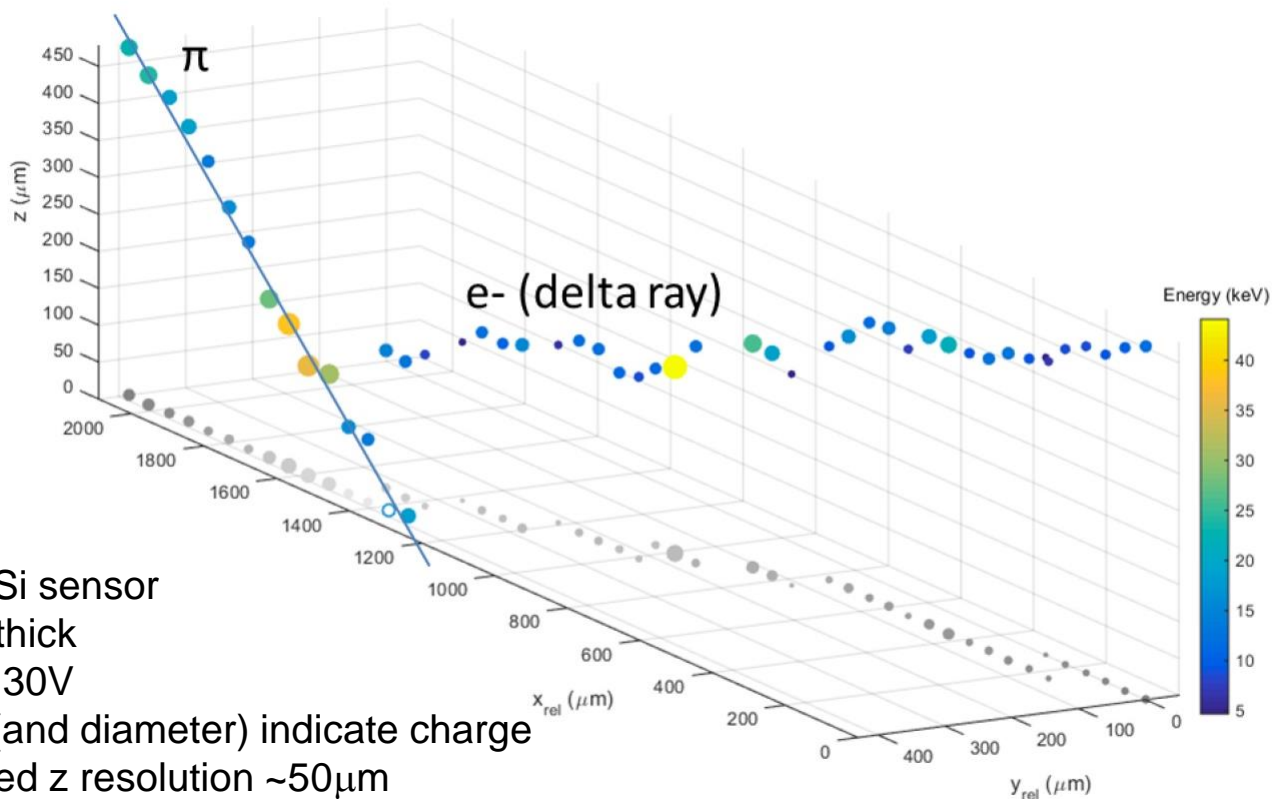


Tracking in a single Si layer



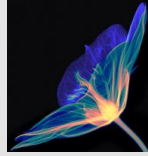
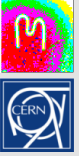


Test with 120GeV/c Pion Track



60 deg
p+ in n Si sensor
500 μm thick
 $V_{\text{bias}} = 130\text{V}$
Colour (and diameter) indicate charge
Measured z resolution $\sim 50\mu\text{m}$

Slide courtesy of B. Bergmann, S. Pospisil, IEAP, CTU, Prague



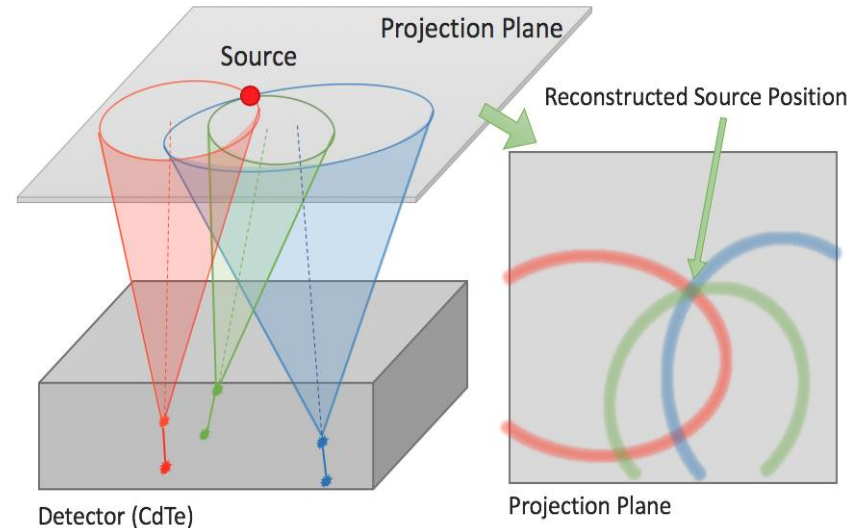
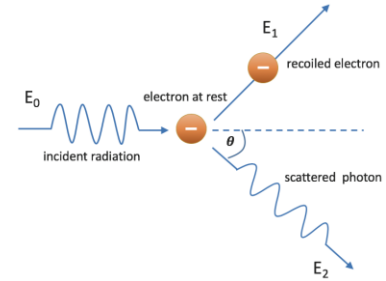
Single Layer Compton Camera with MiniPIX TPX3

Compton camera principle

- Typical two detectors
- primary gamma is scattered in first detector (position and energy recorded), scattered gamma continues to second detector (absorbed, position and energy recorded)
- from energies - > scattering angle calculated
- from position and energies -> possible position of the source on the surface of a cone
- Multiple cones intersection - > source position
- Single Timepix3 layer camera
 - Instead of 2 detectors, only single TPX3
 - Using time of charge collection to determine relative depth

$$\cos \theta = 1 - m_e c^2 \frac{E_1}{E_0(E_0 - E_1)}$$

$$E_0 = E_1 + E_2$$



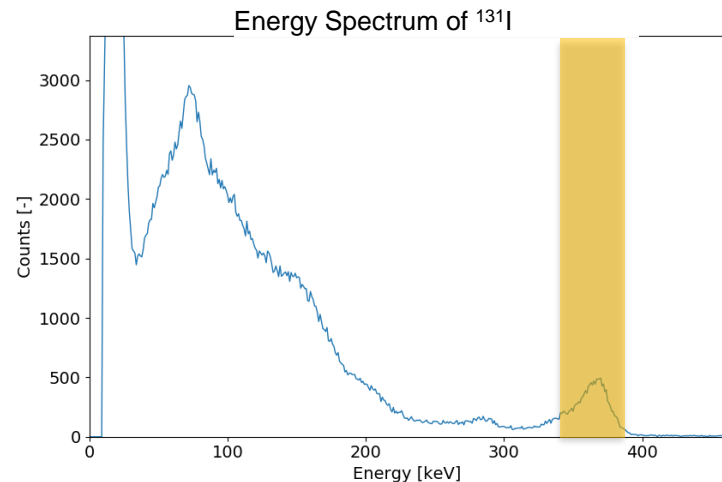
Courtesy of D. Turecek, Advacam s.r.o



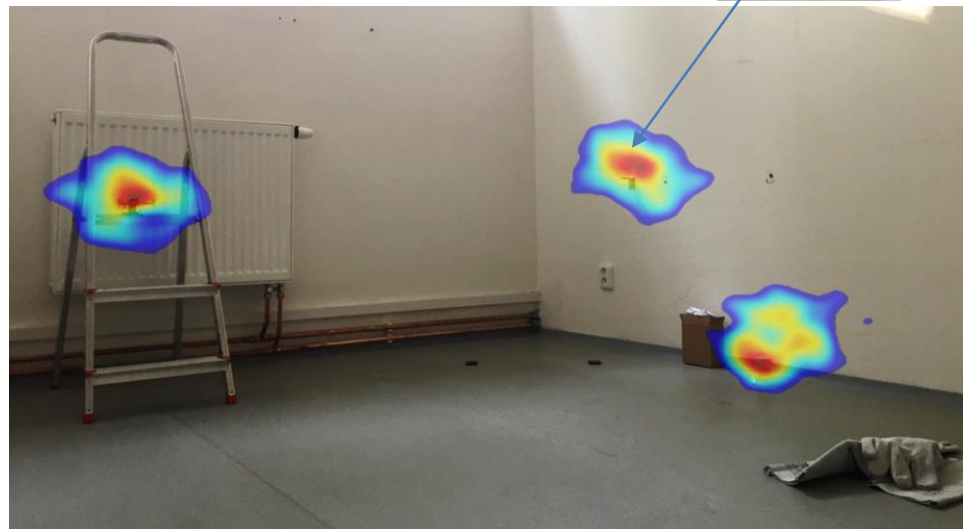
Single Layer Compton Camera with MiniPIX TPX3

^{131}I Iodine gamma source

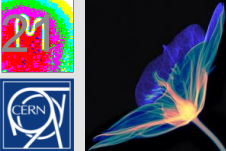
- 3 different Iodine solution in small bottles positioned in a room at different positions
- Distance from detector 3.5 m (activity 10's of MBq)
- Mapped on photograph of the room
- Sources located correctly within minutes
- Image took hours to collect



Courtesy of D. Turecek, Advacam s.r.o



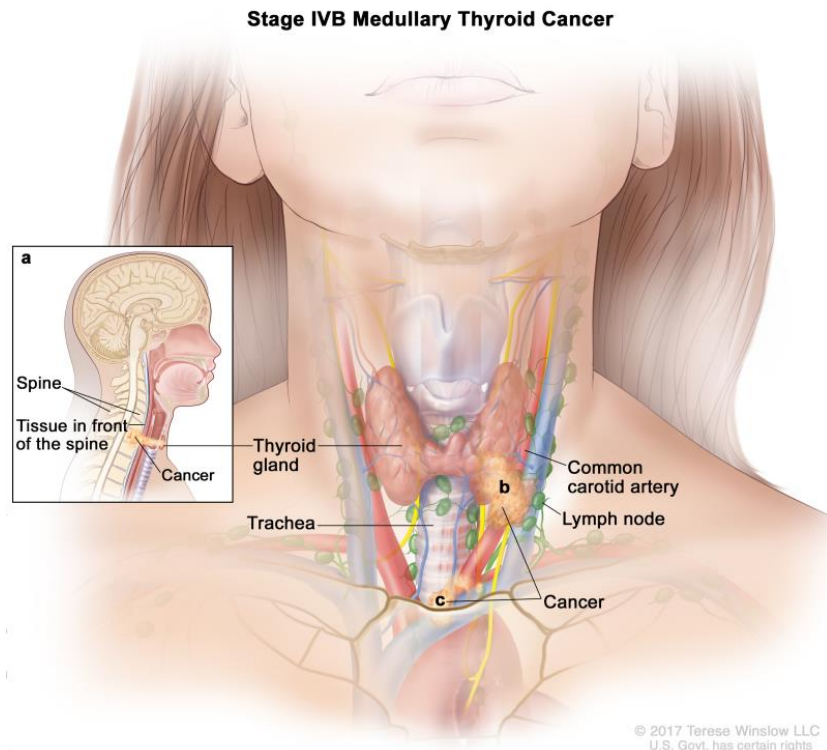
Reconstruction of position of three ^{131}I gamma sources (364 keV)



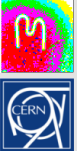
Gamma camera application: Thyroid diagnostics

Thyroid cancer diagnostics and treatment monitoring:

- The second most frequent cancer for women (after breast cancer)
- Current imaging methods offer resolution of about 12 mm in 2D
- Our technology allows
 - 5 times better resolution and 3D (2.5 mm)
 - 4 times lower dose

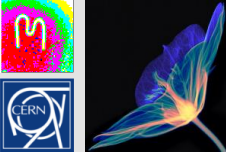


Courtesy of D. Turecek, Advacam s.r.o

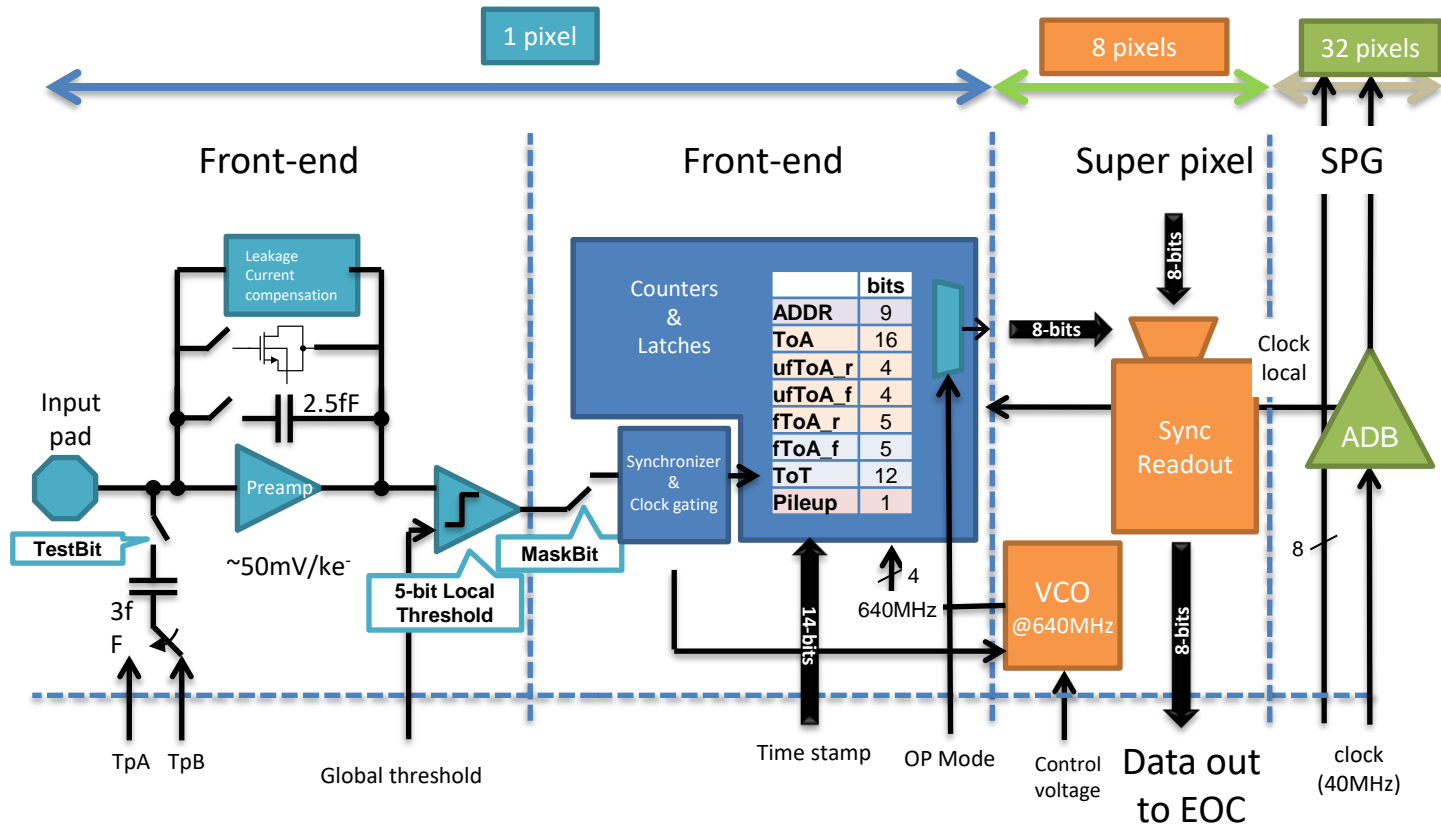


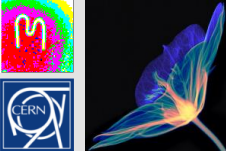
Timepix3 → Timepix4

		Timepix3 (2013)	Timepix4 (2018/19)	
Technology		130nm – 8 metal	65nm – 10 metal	
Pixel Size		55 x 55 μm	55 x 55 μm	
Pixel arrangement		3-side buttable 256 x 256	4-side buttable 512 x 448	
Sensitive area		1.98 cm ²	6.94 cm ²	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	<80 Mhits/s	<365 MHz/cm ² /s
		Max pix rate	1.3kHz/pixel	10.6kHz/pixel
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr) CRW (8-bit / 16-bit) Up to 44 KHz frame @8b
		Max count rate	82 Ghits/cm ² /s	~800 Ghits/cm ² /s
TOT energy resolution		< 2KeV	< 1Kev	
Time resolution (bin size)		1.56ns	~200ps	
Readout bandwidth		≤5.12Gb (8 x SLVS@640 Mbps)	≤163 Gbps (16 x 10.24 Gbps)	
Target global minimum threshold		<500 e ⁻	<500 e ⁻	

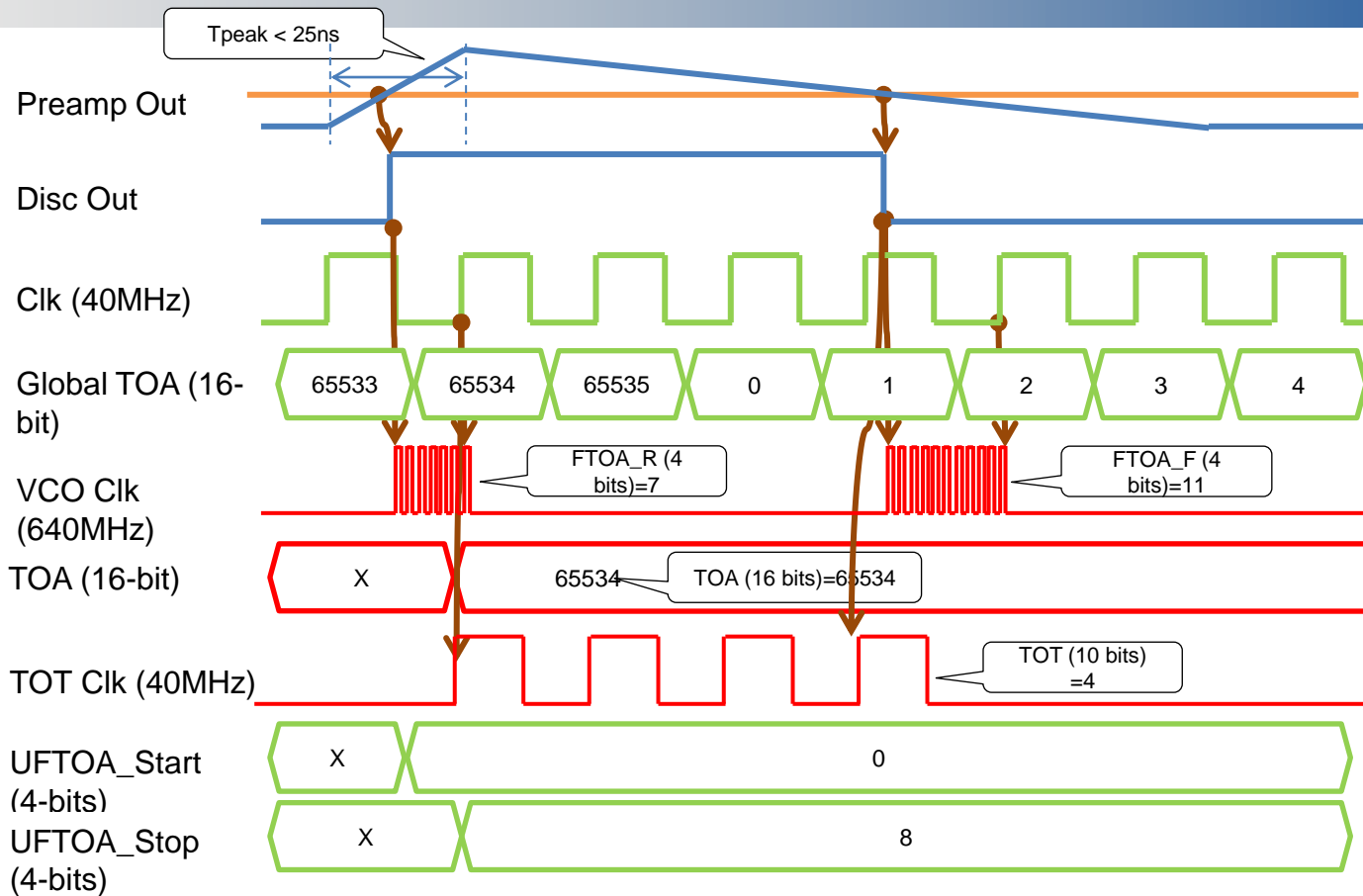


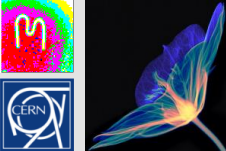
Timepix4 Pixel Schematic





Pixel Operation in TOA & TOT [DD]



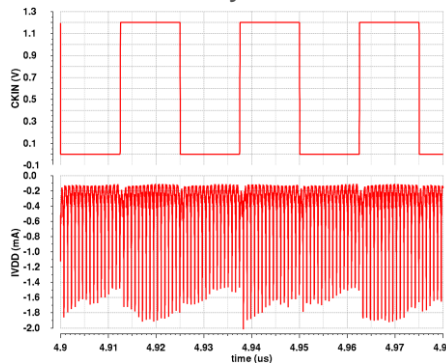
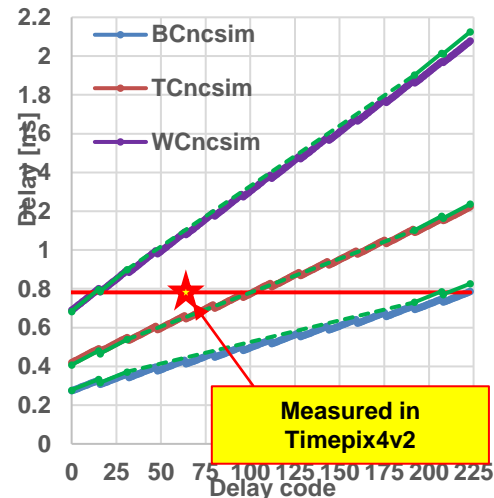
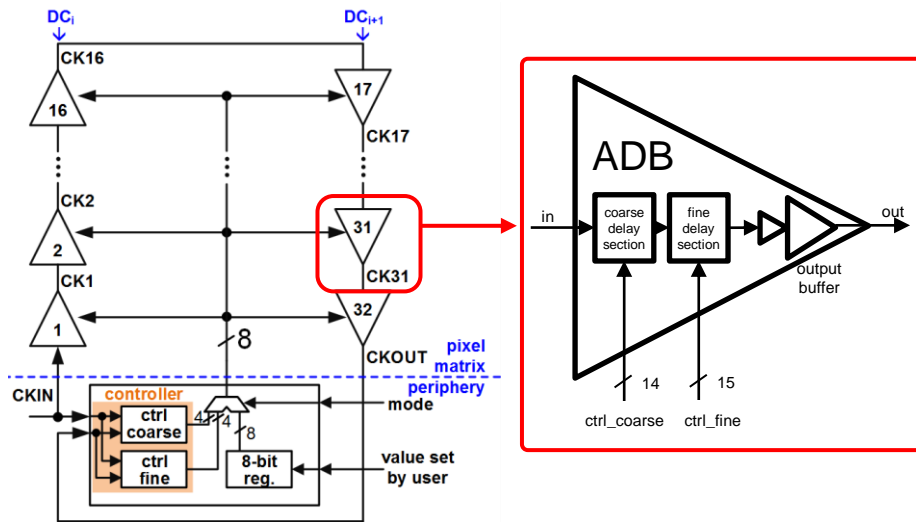


Full digital double column DLL

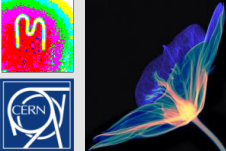
[448 dDLL: 224 Top Matrix and 224 Bottom Matrix]

iWoRID 2018

X. Llopert et al 2019 JINST 14 C01024

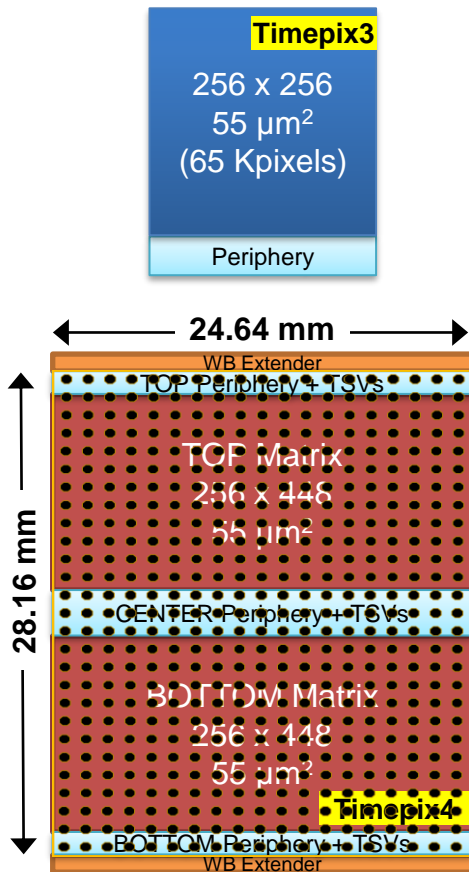


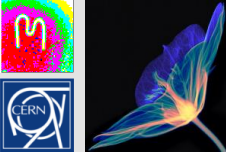
- Timepix4 $\sim 23 \text{ mW/cm}^2$ @40MHz clock with a $100 \text{ ps}_{\text{rms}}$
- Timepix3 $\sim 100 \text{ mW/cm}^2$ @40MHz clock with $\sim 1.2 \text{ ns}$ skew
- Dynamic digital power consumption is distributed across the clock period



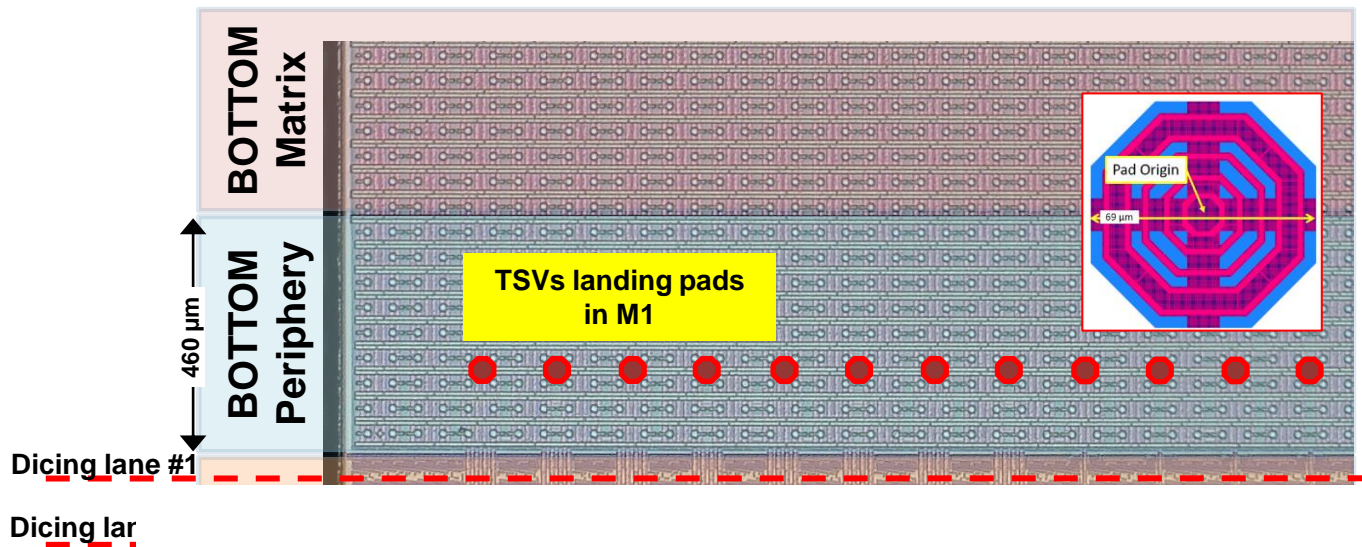
Timepix4 floorplan

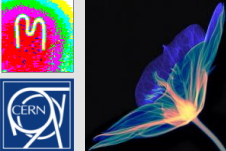
- 512 x 448 of 55 x 55 μm pixels
 - 2 Matrices (TOP and BOTTOM)
- 3 'peripheries' with TSV (Through-Silicon-Vias):
 - TOP, BOTTOM (TSV, WB): Data Readout (16x 10.24 Gbps Serializers)
 - CENTER (TSV): Analog Blocks (DACs, ADC, Band-Gap...)
- On-chip bump to pixel redistribution layer (RDL):
 - Pixel matrix pixels are shorter (51.4 μm) than sensor pixels (55 μm)
 - Equalized C_{in} for all pixels \rightarrow ~46 fF increase for a 460 μm periphery
- Edge peripheries include 1mm Wire Bond Extender
- Dicing options:
 - With WB (Wire-Bonds Extenders): 29.96 mm x 24.7 mm
 - >93.7% active area (28.16mm x 24.64mm)
 - Without WB (TSV Only) : 28.22 mm x 24.7 mm
 - >99.5% active area (28.16mm x 24.64mm)
 - Through Silicon Vias (TSV) requires post processing at wafer level to create TSV and on the ASIC back sides RDL + BGA pads





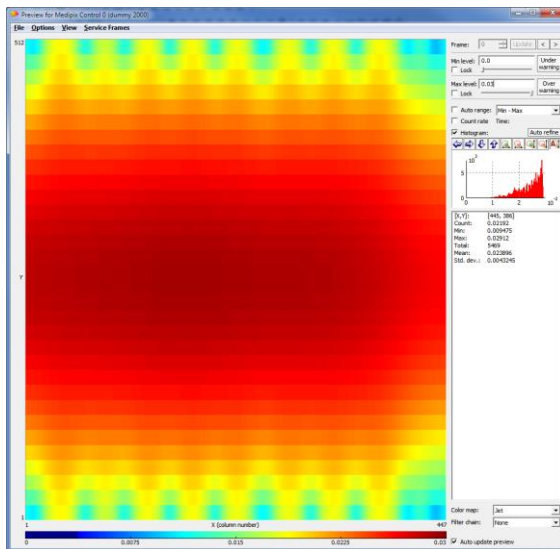
Timepix4 Bottom left detail



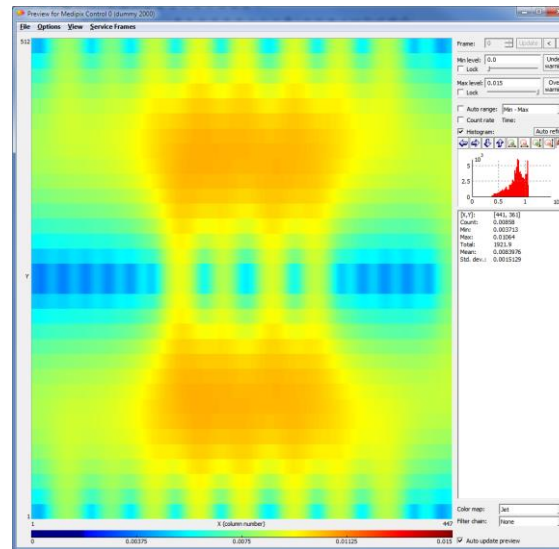


Analog (static) power supply distribution

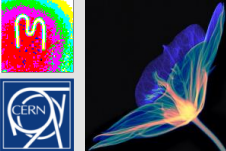
	Total I (chip)		2 WB	3 TSV
Nominal Analog Power [10 μ A/pixel]	~2300 mA	V_{drop} [VDDA-GNDA]	19.6 mV	6.9 mV
		I _{max} pad	60 mA	57 mA
Low Analog Power [1 μ A/pixel]	~230 mA	V_{drop} [VDDA-GNDA]	1.96mV	0.69mV
		I _{max} pad	6 mA	5.7 mA



2 wire bonds



3 TSV



Timepix4 submissions

Q4 2019

Timepix4v0

Full mask engineering run

6 wafers received

Chip is operational

- 1) Excess noise coupling from peripheries to FE
- 2) 640 MHz clock in edge peripheries
- 3) VCO not oscillating at nominal frequency

Q3 2020

Timepix4v1

4 BEOL masks changed

Small test VCO chip

6 wafers received

- 1) Improved RDL shielding in peripheries
- 2) 640MHz in peripheries recovered

- 1) VCO not oscillating at nominal frequency

Q2 2021

Timepix4v2

4 FEOL + 4 BEOL masks changed

19 wafers received

- 1) TDC and High speed links working as expected
- 2) Further improvement in RDL shielding in peripheries

Chip at its final version

Q3 2022

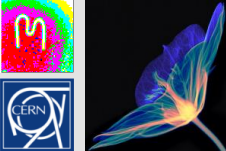
Timepix4v3

2 BEOL masks changed

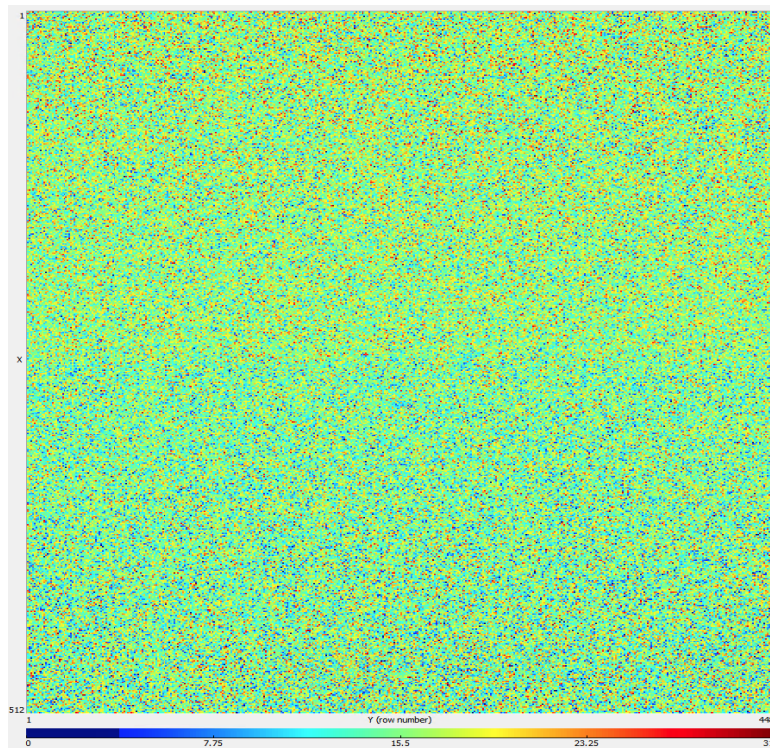
25 wafers received

- 1) Larger IO Pads

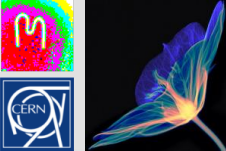
Chip at its final version



Uniformity of response Timepix4 (all versions)



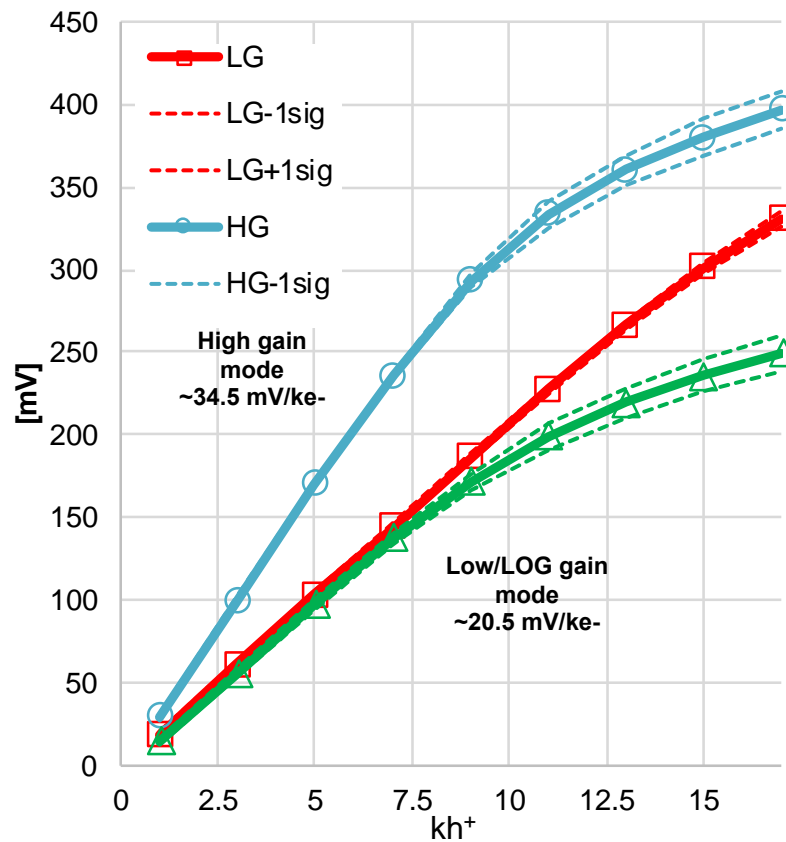
Threshold adjustment bits



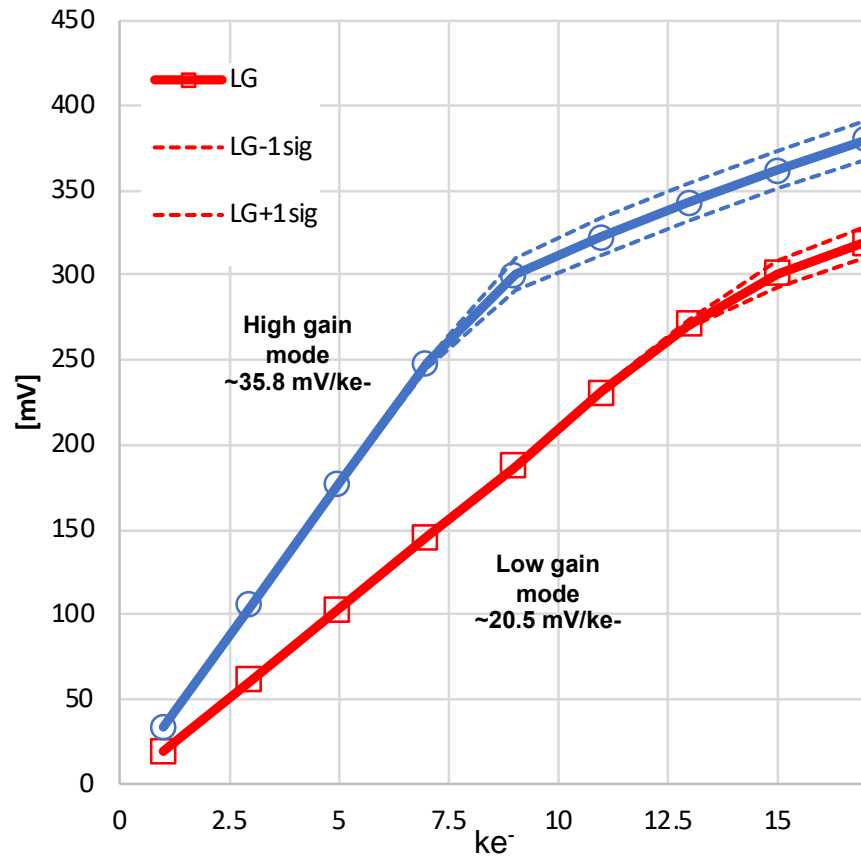
Gain slopes for different FE Gain

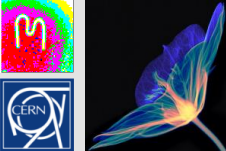
[TOA-TOT, few pixels]

Hole collection

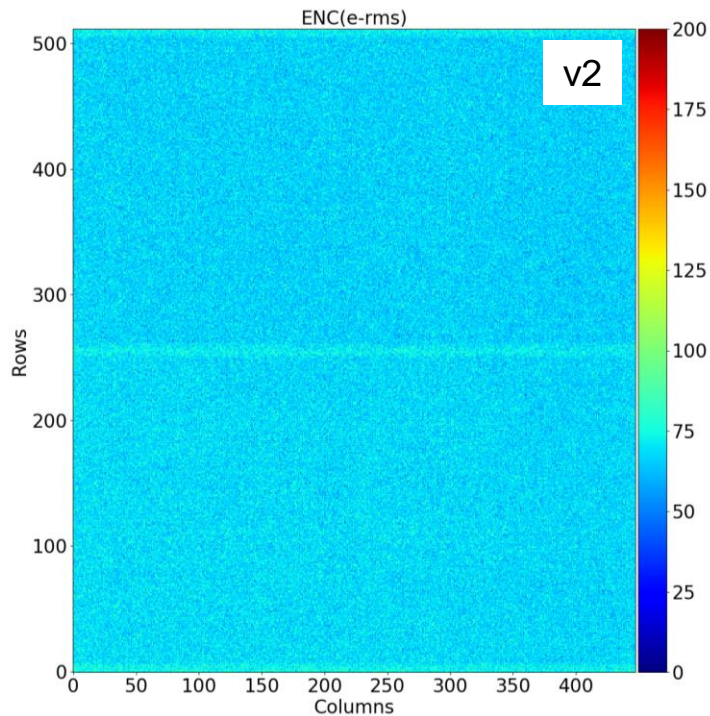
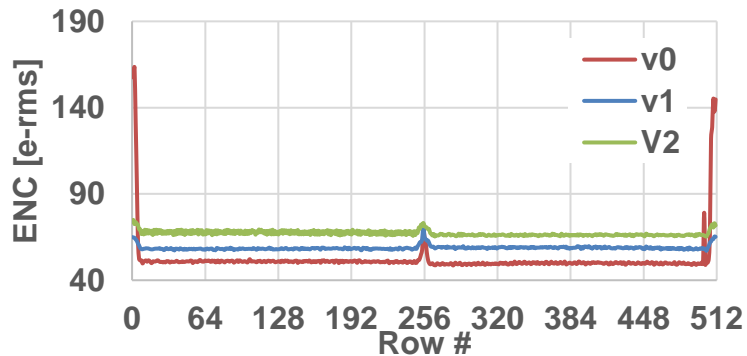
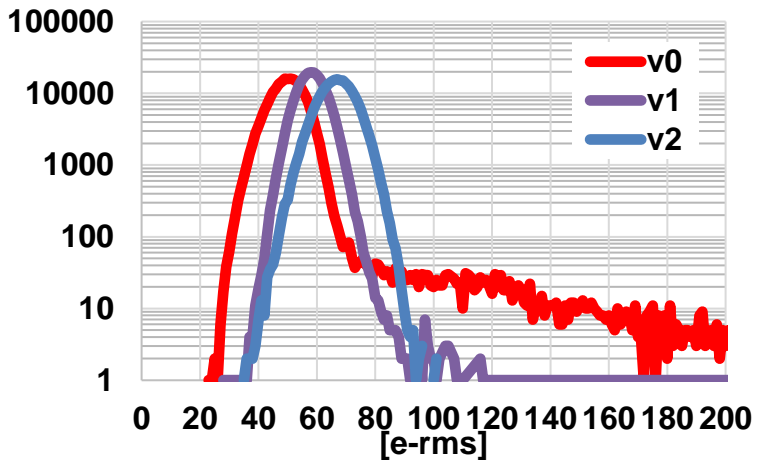


Electron collection

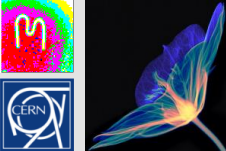




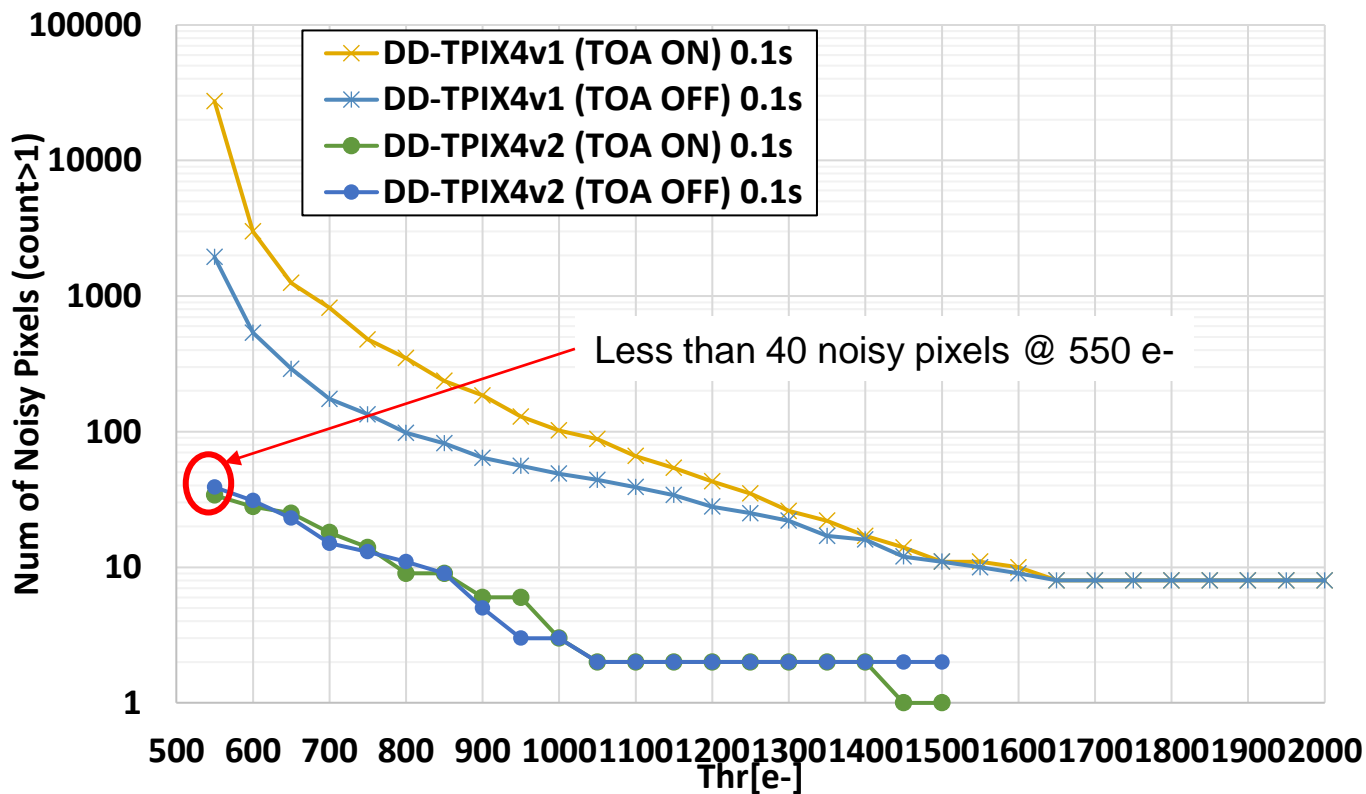
Noise uniformity - Timepix4v0, v1 and v2

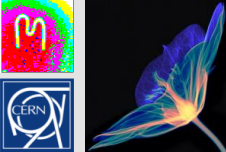


When a Si sensor is attached the noise slightly increase $\sim 3e^-$ / pixel



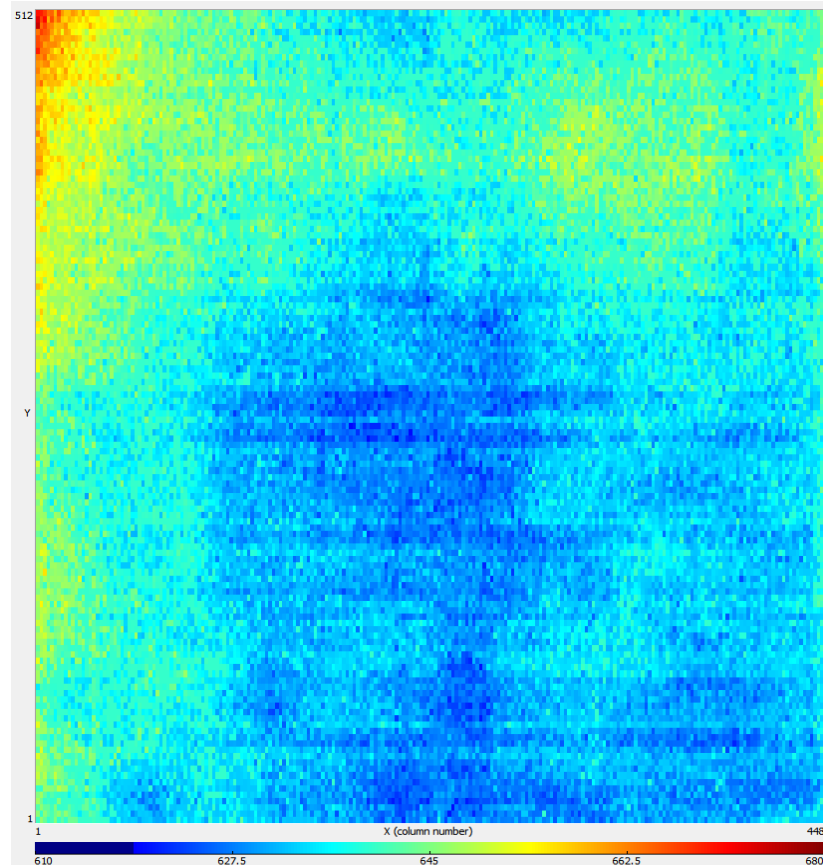
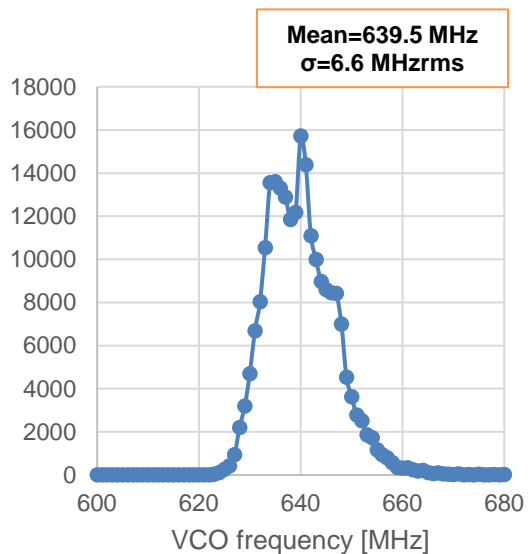
Timepix4v1 and v2: Number of Noisy pixels (>1 count) Data-Driven mode [DD]

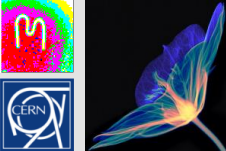




Timepix4v2 2D VCO frequency distribution

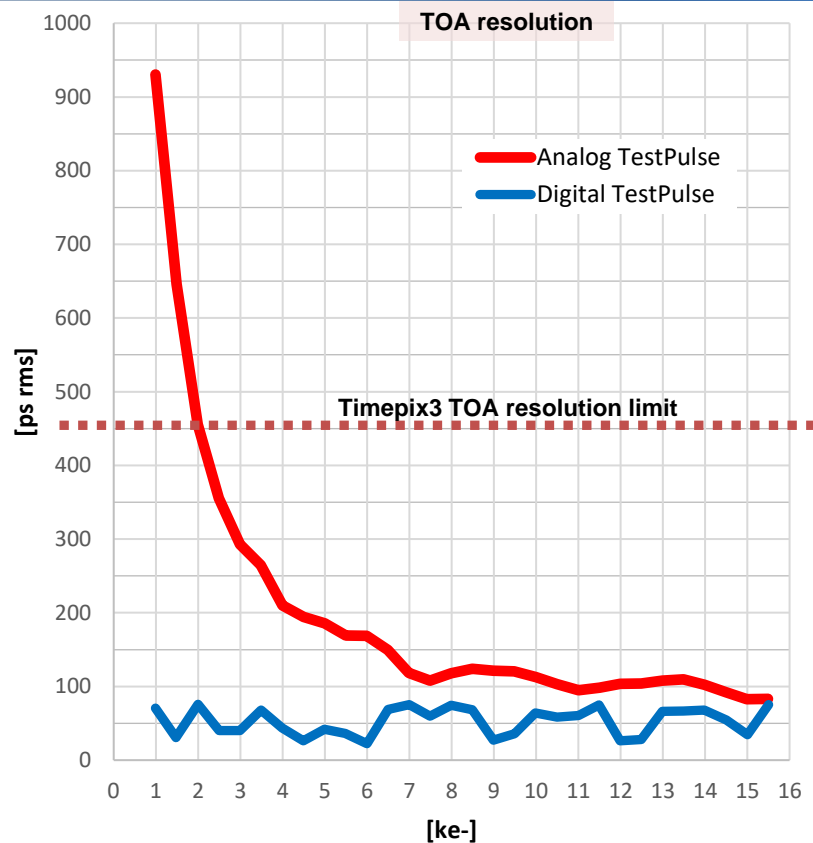
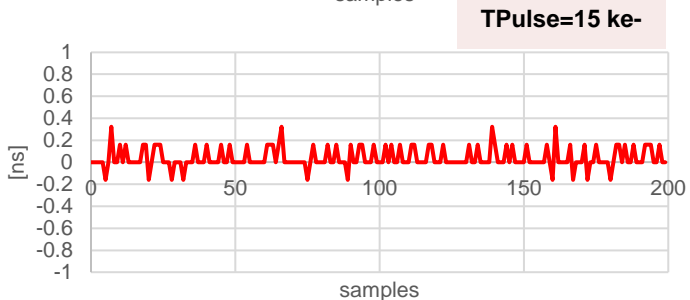
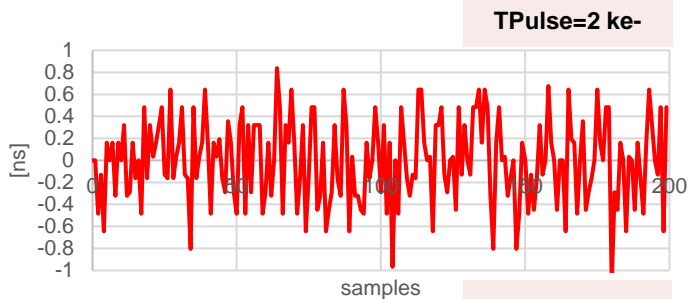
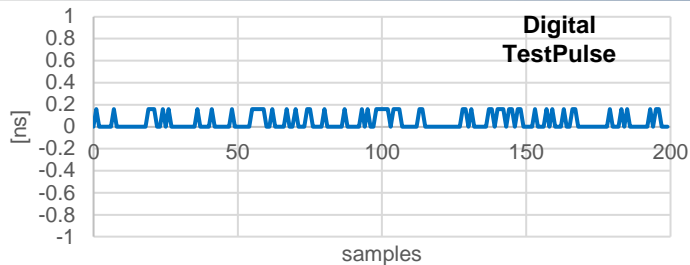
- Measured VCO oscillation frequency in Timepix4
- Calibration is required in order to get to the designed time resolution (~ 60 psrms)
- How could this be improved/simplified?

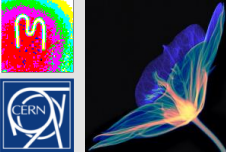




TOA Resolution

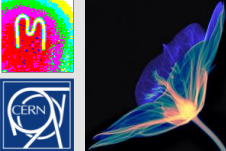
[TOA-TOT, 1 pixel, 10000 samples, HG e-]



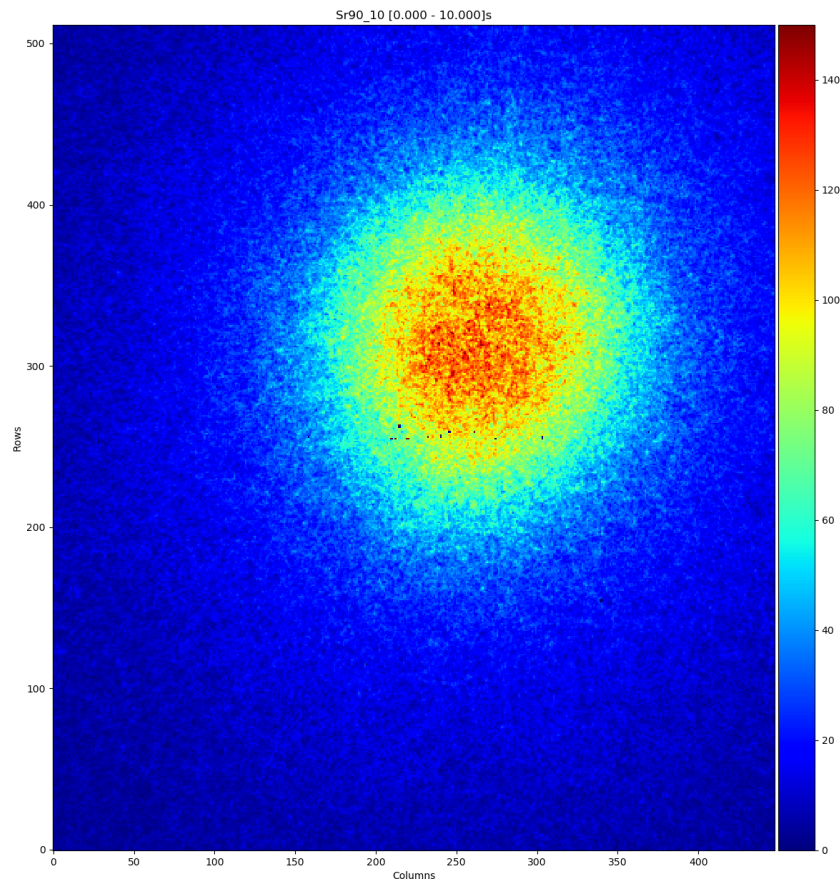


Timepix4 assembly (300 μ m Si sensor)



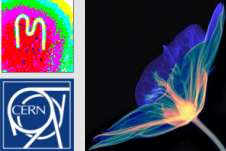


Data driven mode

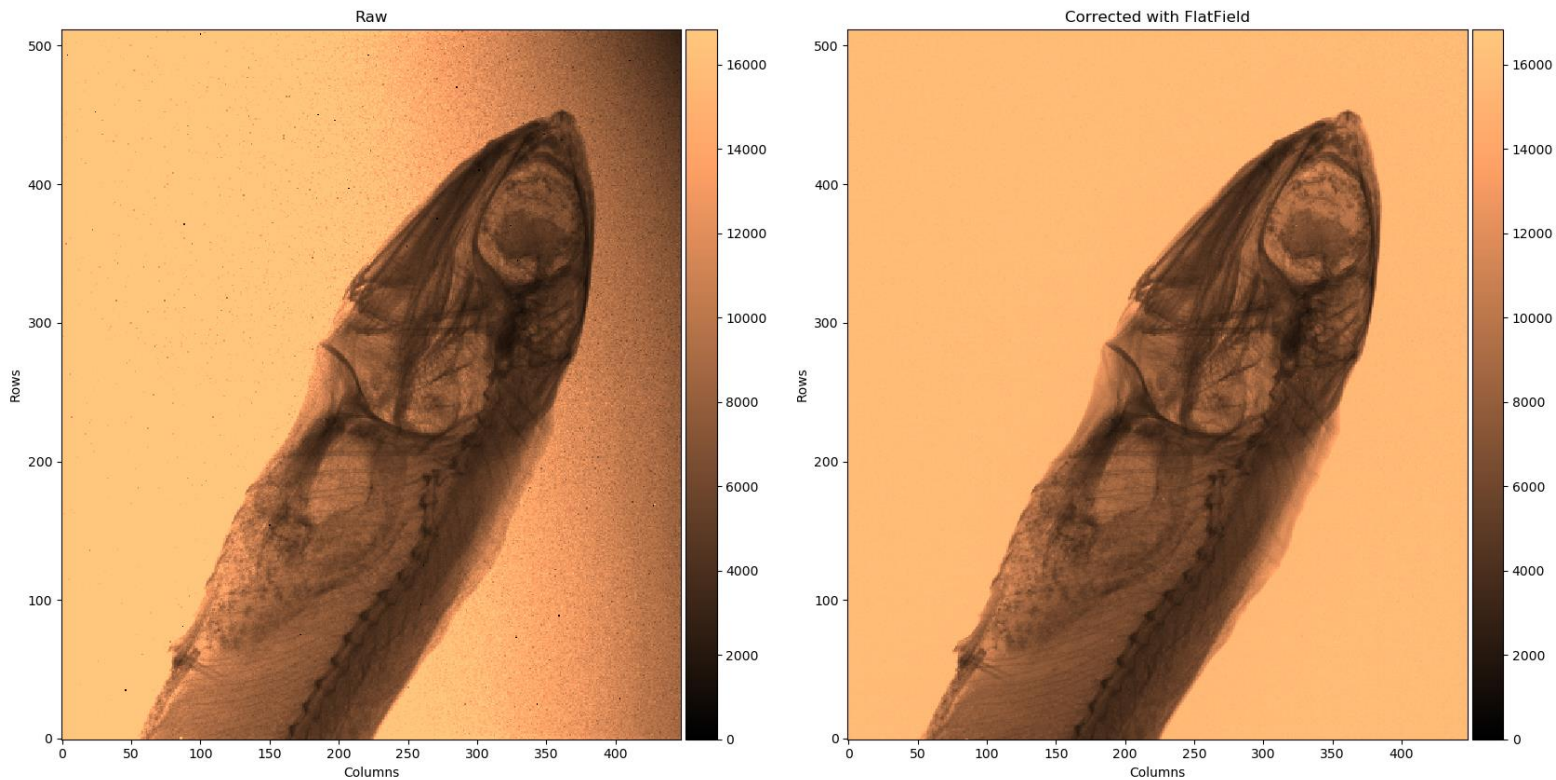


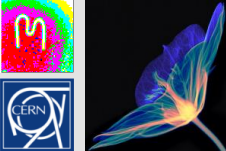
10s exp. ^{90}Sr

Threshold $\sim 800e^-$
6.1 M packets @ 5 Gbps



Photon counting image Timepix4

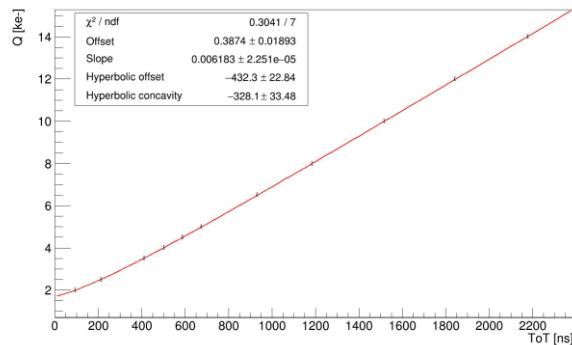




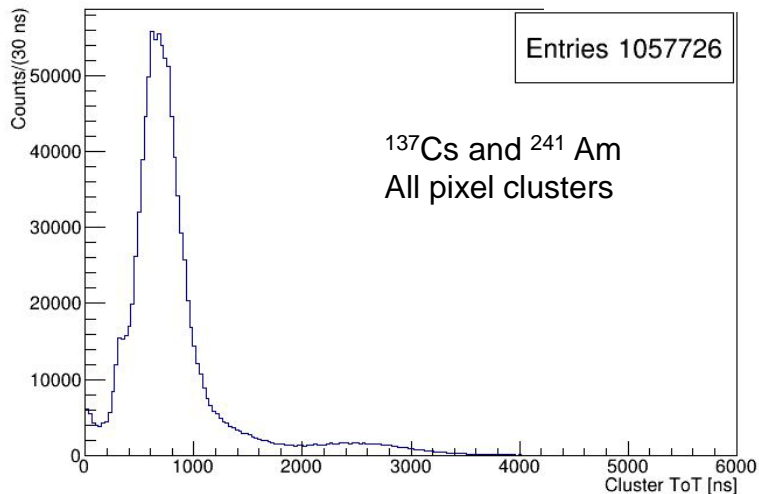
Energy calibration using test pulses

R. Bolzonella et al., TIPP
Cape Town, 4-8 Sept
Under submission to JINST

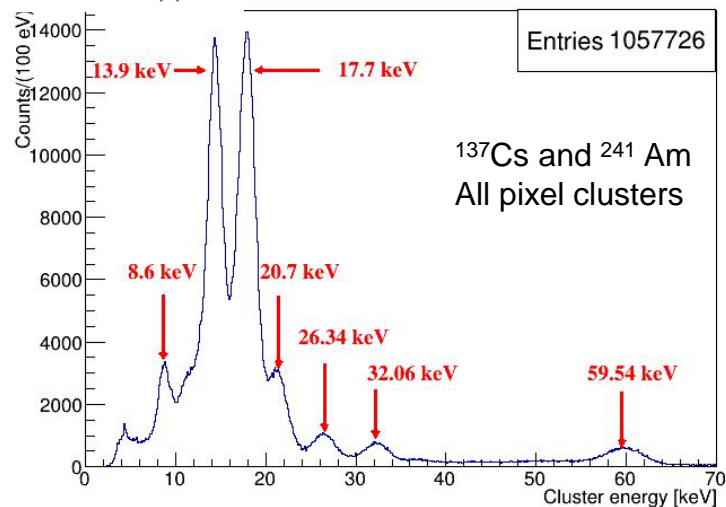
Calibration of pixel [305,144]

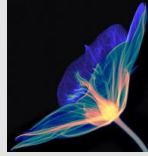
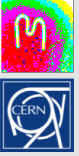


Per-pixel energy vs
ToT calibration using
test pulses



After test pulse
calibration

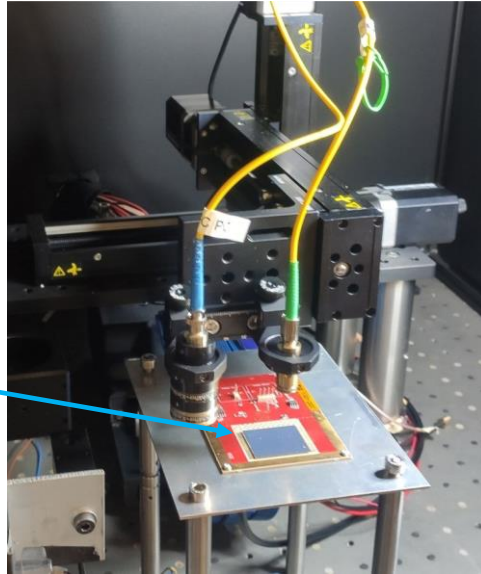




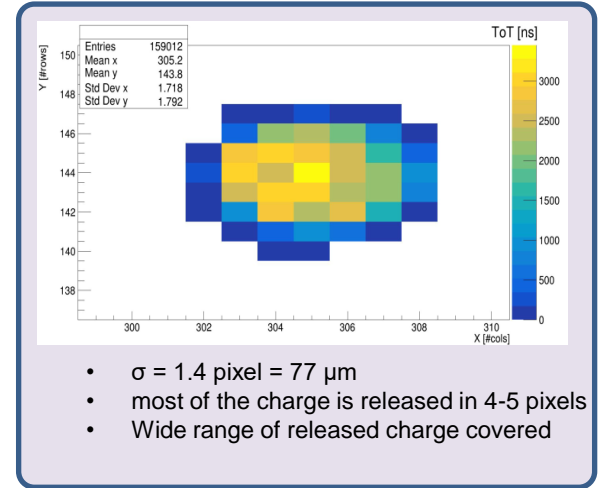
Timing test setup with laser



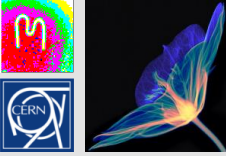
- Rear side metallization with holes
- Timepix4V2 bonded to a 100 μ m thick n-on-p Si detector:
- Biased at -150 V



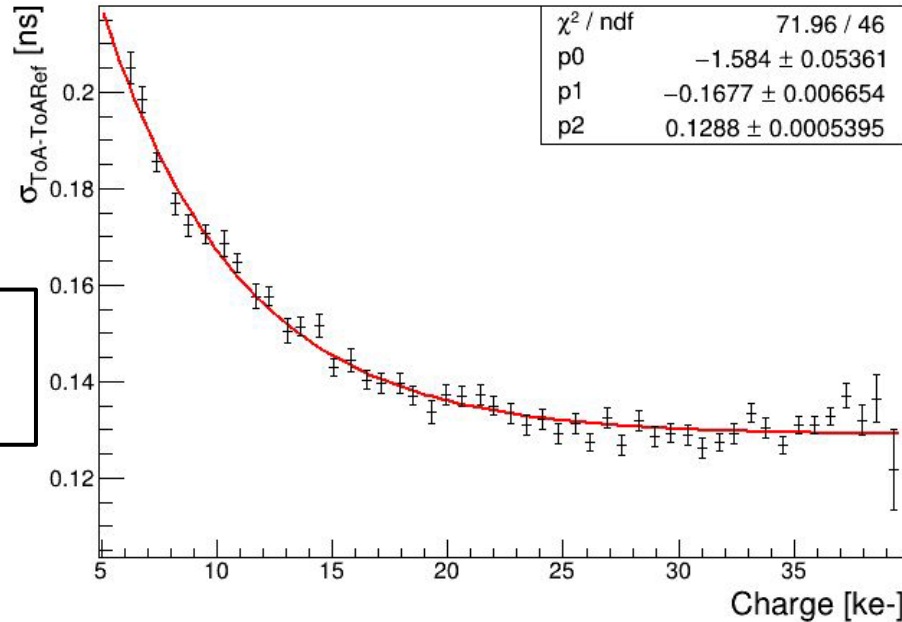
- 1020nm laser pulsed with 6ps jitter generator
- Generator connected to electrical test pixels



R. Bolzonella et al., TIPP Cape Town, 4-8 Sept
Under submission to JINST

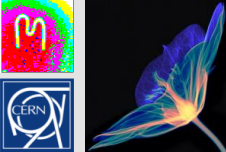


Single pixel pulse resolution

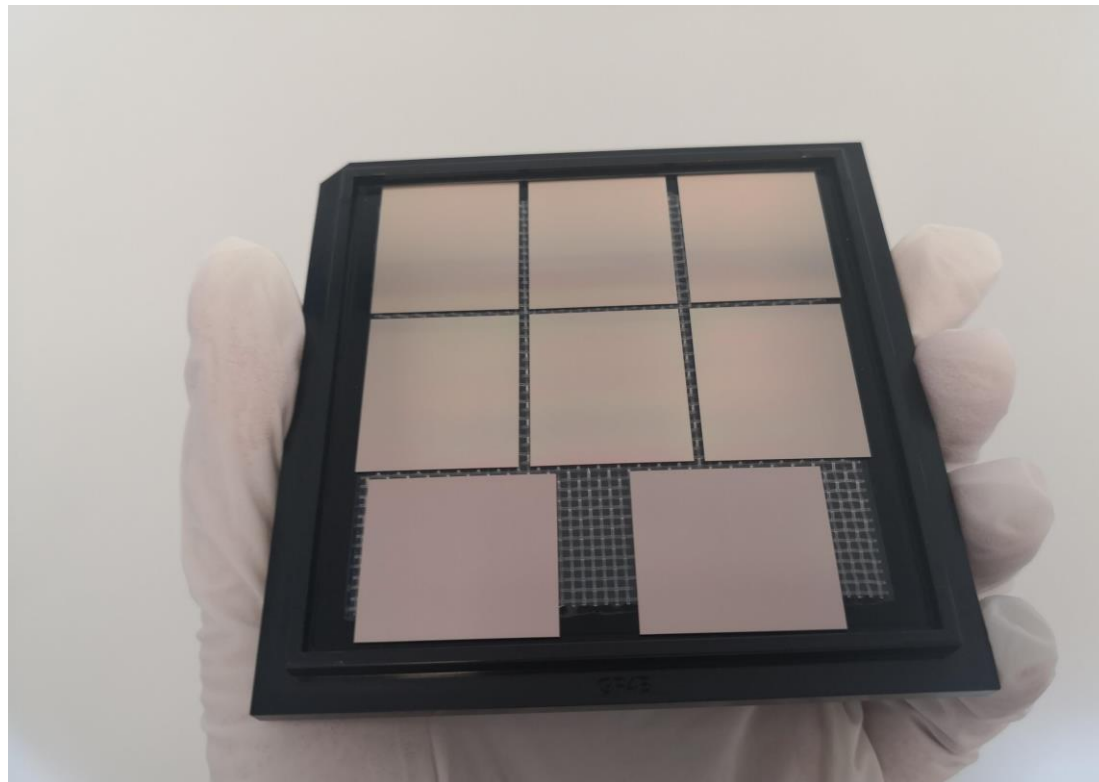


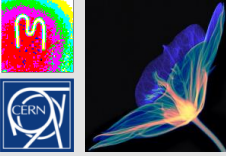
R. Bolzonella et al., TIPP
Cape Town, 4-8 Sept
Under submission to JINST

- For the pixel [305,144], where the laser is focused, the standard deviation saturates at 129 ± 1 ps rms
- Subtracting the contribution of the reference TDC (60 ps), a resolution of 111 ± 1 ps rms is obtained
- Timing resolution dependency on cluster charge best result: $\sigma_{\text{ToADiffAvg}} = 79 \pm 1$ ps rms
- Timing resolution subtracting reference TDC contribution: $\sigma_{\text{ToAAvg}} = 49 \pm 1$ ps rms

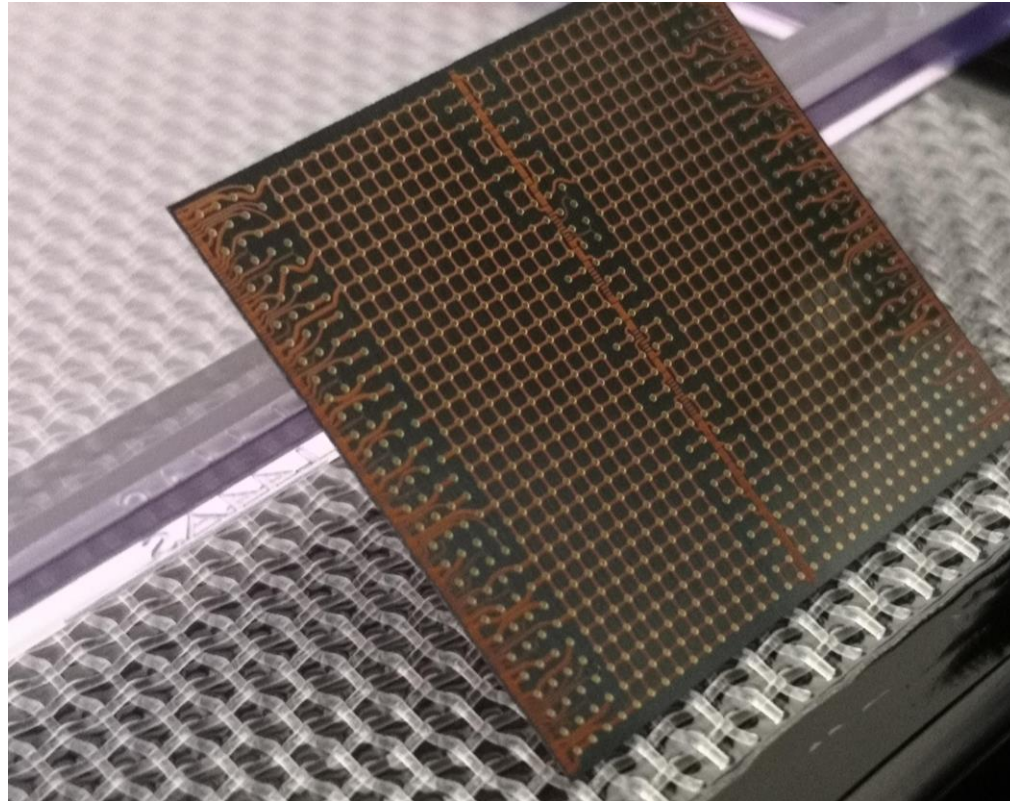


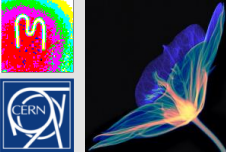
June 2023 – TSV processes TPIX4v0 delivered



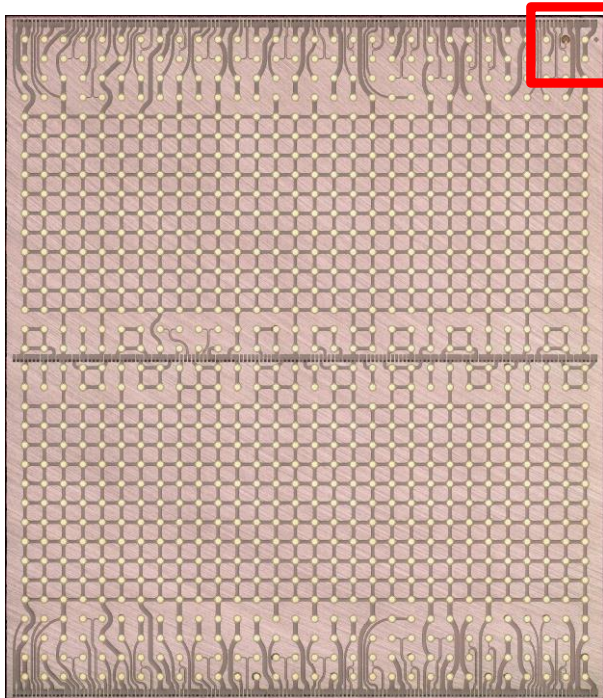


Rear side Re-Distribution Layer (RDL)

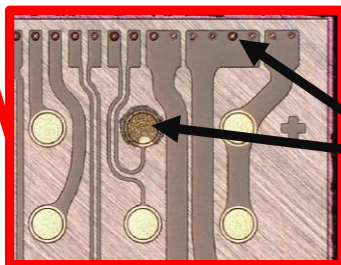




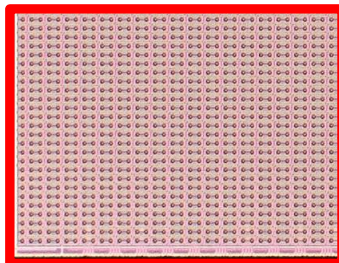
Visual Inspection – front and rear side



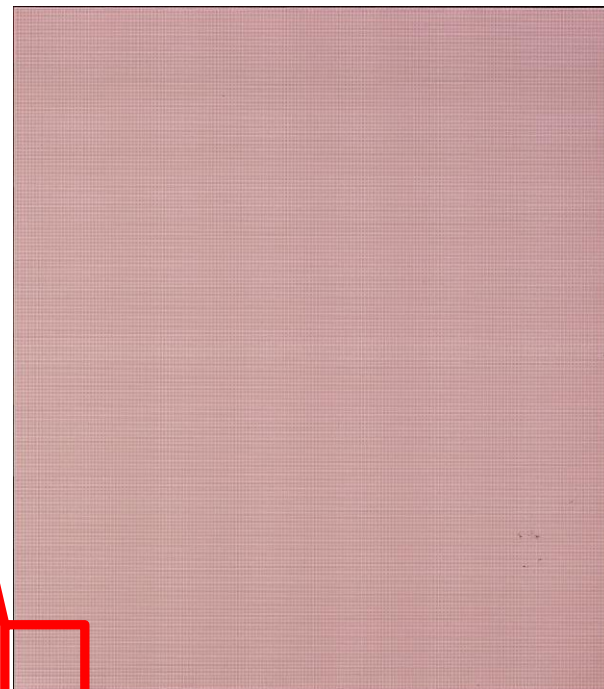
Back Side



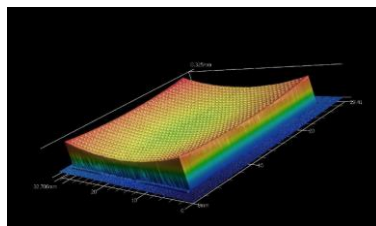
- Redistribution Layer
- 1020 BGA pads
- TSV
- Residues of dicing tape



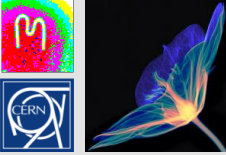
Pixel size



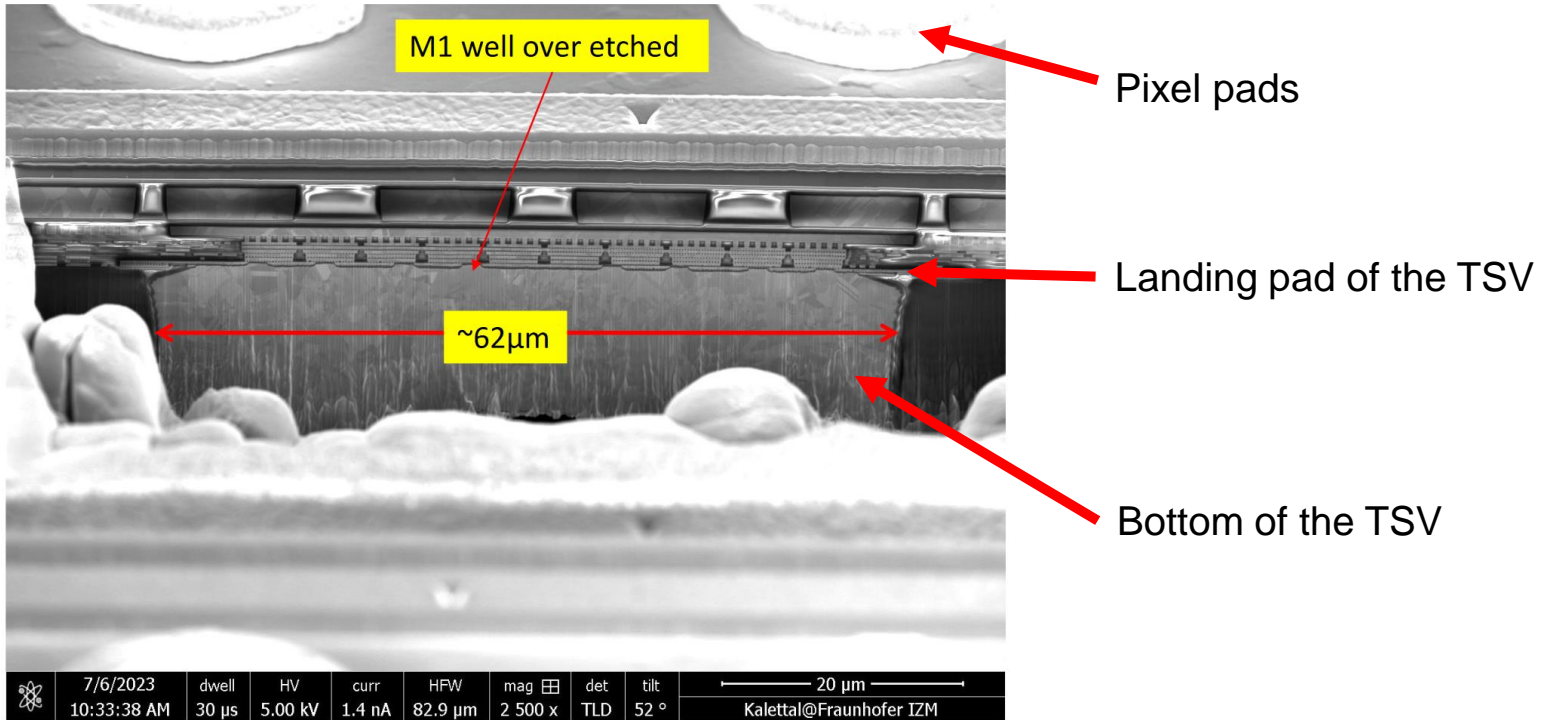
Front Side



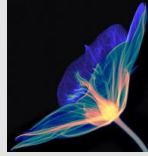
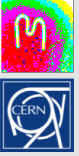
Chip bow ~ 100 μ m (over 3cm)
Magnified bowing (the chip is thin: ~120 μ m)



Inspection with Electron Microscope of one TSV

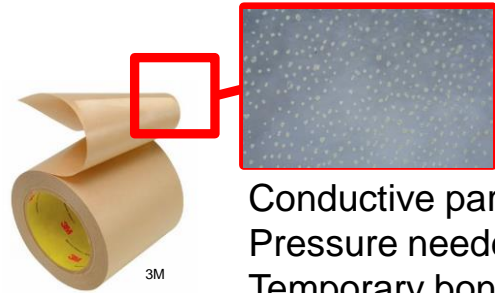


Courtesy of IZM

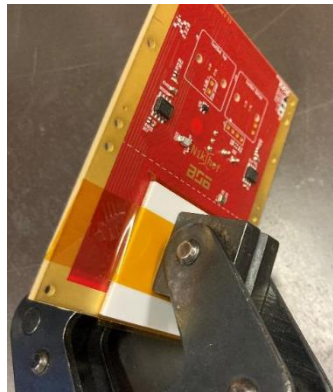


Mounting of TSV processed chips on Nikhef carrier board

ACF: Anisotropic Conducting Film

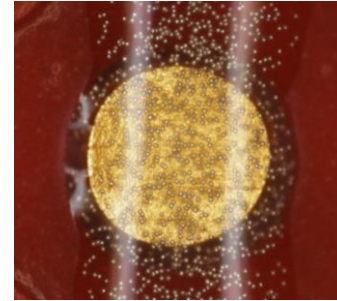


Conductive particles
Pressure needed
Temporary bonding

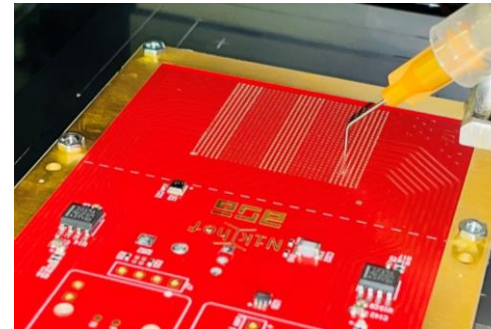


- We could communicate with the chip, test the DAC...
- After releasing the clamp and putting it again, chip not responding, maybe due to reusing the tape.
- Work in progress

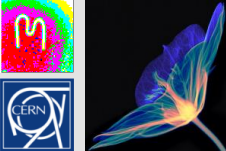
ACP: Anisotropic Conducting Paste



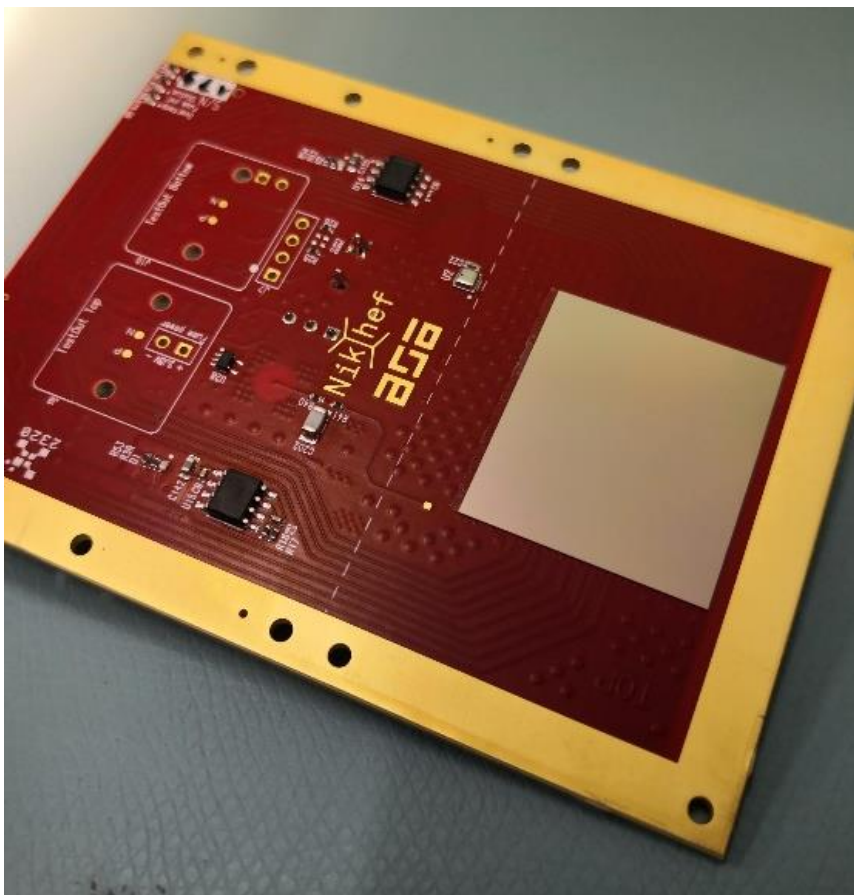
- Araldite with conducting particles
- Done at UniGe (Mateus Vicente Barreto Pinto m.vicente@cern.ch)
- Flip chip bond machine



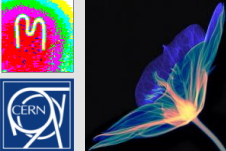
- Results Timepix4V0:
- Good communication with the chip
- Promising low cost approach



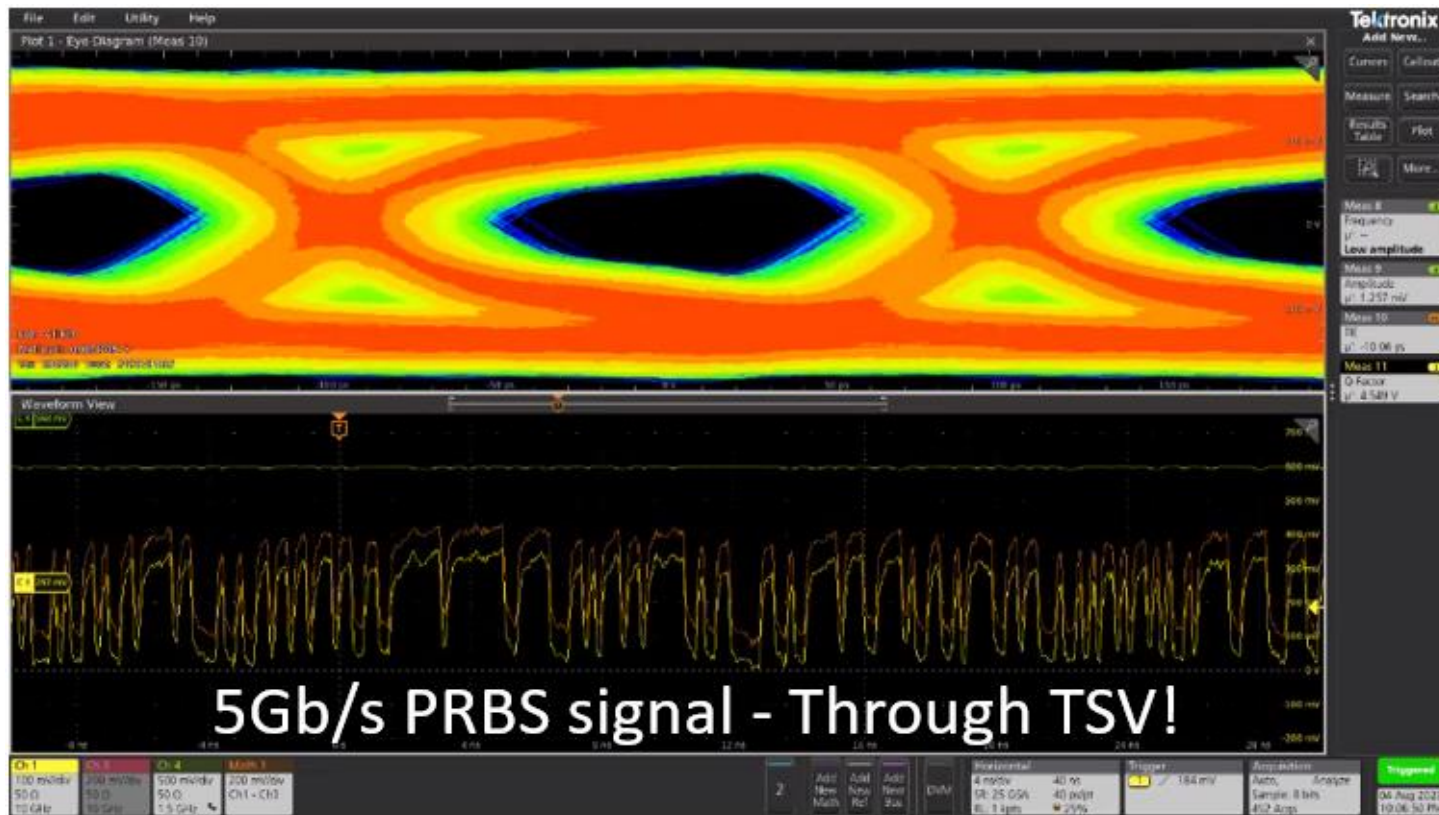
TSV-processed successfully mounted

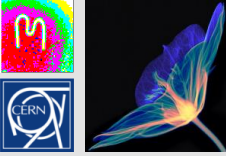


Chip behaves identically to a wire bonded version



Output from TSV processed Timepix4v0

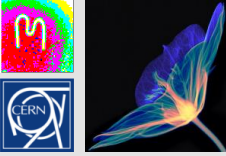




Medipix3 → Medipix4

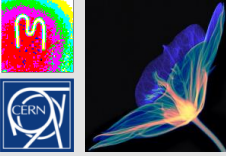
	Medipix3RX (2013)	Medipix4 (2022)
Technology	CMOS 130nm	CMOS 130nm
Pixel Size	55/110 μm	75/150 μm
Matrix Size	256 x 256 / 128 x 128	320 x 320 / 160 x 160
Tile-ability	3-side	4-side buttable
Thresholds	1/4 Continuous RW	2/8 Continuous RW
Readout scheme	Sequential RW & Continuous RW	
Count Rate (10% deadtime loss)	4.3×10^6 ph/mm ² /s (CSM 110)	19×10^6 ph/mm ² /s (CSM 140)
Dynamic Range	25 Ke-	32 Ke-
CSM energy resolution (FWHM)	~ 4.4 KeV (CSM 110)	~ 2.5KeV (CSM 150)
Readout bandwidth	<1.6 Gbps (8x LVDS)	1,2 Serializers @5.12 or 2.56 Gbps
Power	<1W @1.5V	<1W/cm ² @1.2V

Status: Medipix4 chip first version under test – bugs being addressed



Conclusions

- Hybrid pixel detectors offer unique solutions for X-ray and gamma-ray imaging and have found widespread applications
- The Timepix4 (and Medipix4) chips are designed explicitly for tiling in 2 dimensions using Through Silicon Vias for IO
- Measurements with Timepix4 in data driven mode are consistent with the design values
- Single pixel time resolution is ~ 111 ps rms
- TSVs have been successfully implemented on Timepix4v0 and the chip behaves as normal
- Future work includes demonstrating a large area implementation with minimal dead area



Thank you for your attention!

