The MONOLITH project: towards **picosecond timing** with monolithic silicon

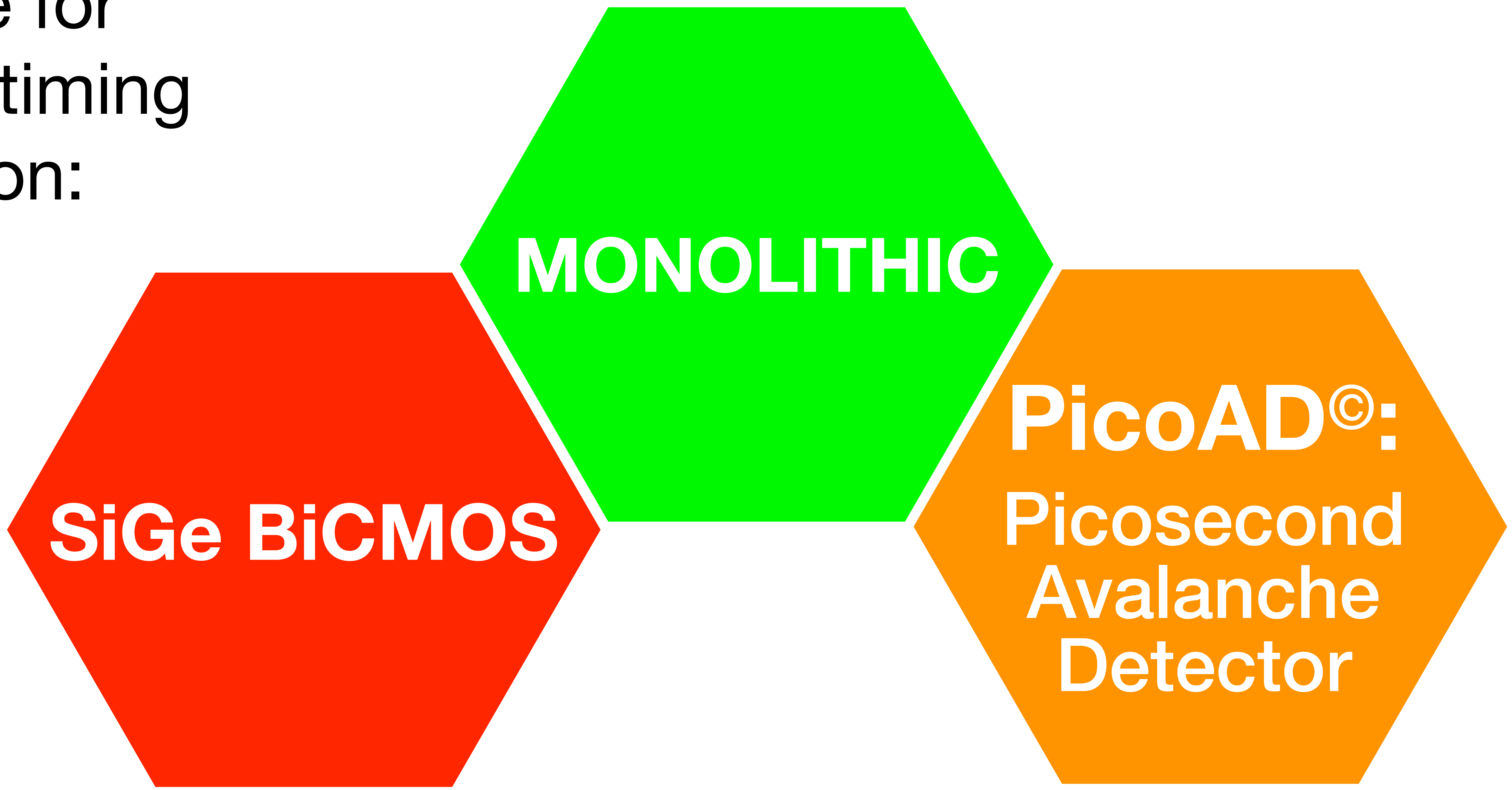
Giuseppe Iacobucci — Université de Genève

UNIVERSITÉ DE GENÈVE
Swiss National Science Foundation
European Research Council
Established by the European Commission

The MONOLITH Project

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

Our recipe for picosecond timing with silicon:



The UniGe Silicon Team

Giuseppe Iacobucci
- project P.I.
- System design

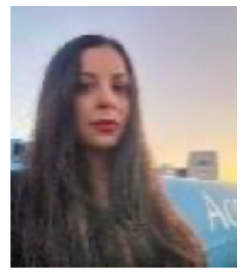
Thanushan Kugathasan
- Lead chip design
- Digital electronics

Stefano Zambito
- Laboratory tests
- Data analysis

Jordi Sabater Iglesias
- Detector simulation
- Laboratory tests

Matteo Milanesio
- Laboratory tests
- Data analysis

Antonio Picardi
- Chip design
- Firmware



Rafaella Kotitsa
- Sensor simulation
- Data analysis

Carlo Alberto Fenoglio
- Chip design
- Firmware

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Roberto Cardella
- Sensor design
- Laboratory tests

Mateus Vicente
- System integration
- Laboratory tests

Chiara Magliocca
- Laboratory tests
- Data analysis

Théo Moretti
- Laboratory tests
- Data analysis

Jihad Saidi
- Laboratory tests
- Data analysis

Luca Iodice
- Chip design
- Firmware

Andrea Pizarro Medina
- Data analysis
- Laboratory tests

Didier Ferrere
- System integration
- Laboratory tests

Sergio Gonzalez-Sevilla
- System integration
- Laboratory tests

Yannick Favre
- Board design
- RO system

Stéphane Débieux
- Board design
- RO system

Main research partners:

Roberto Cardarelli
INFN Rome2 & UNIGE

Holger Rücker
IHP Mikroelektronik

Marzio Nessi
CERN & UNIGE

Matteo Elviretti
IHP Mikroelektronik

Funded by:

Swiss National Science Foundation

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Sinergia

ATTRACT

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MONOLITH

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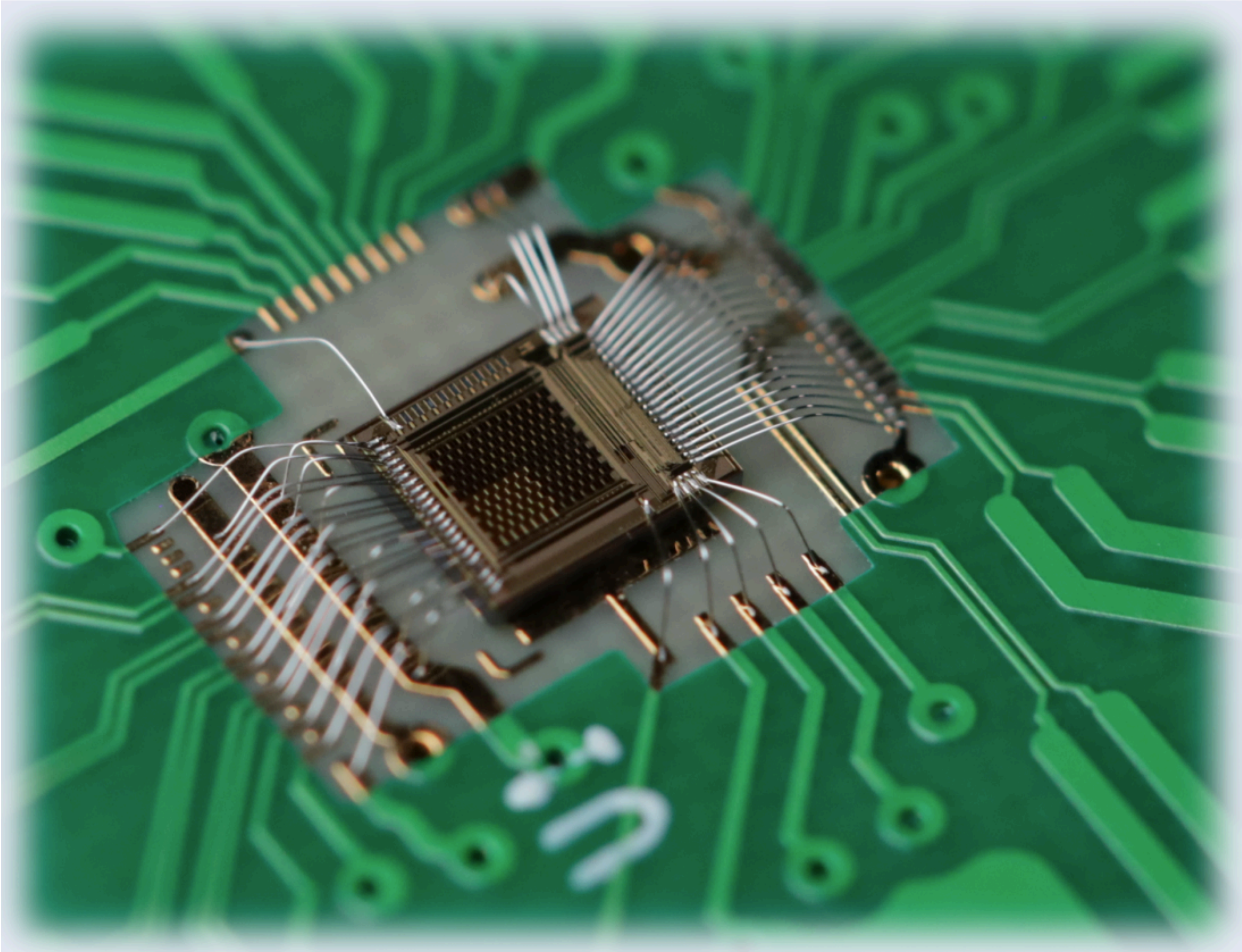
Today I will show the results obtained with:

1. the **2022 prototype WITHOUT GAIN LAYER** with improved SiGe electronics, and the effects of proton irradiation up to **1×10^{16} 1MeV n_{eq}/cm^2**
   ➡ PicoAD version back from foundry in October
2. the **PicoAD proof-of-concept**, produced on SiGe electronics of 2020 prototype

All ASICs were produced in the 130nm SiGe BiCMOS SG13G2 process by

ihp
innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik



MONOLITH

European Research Council
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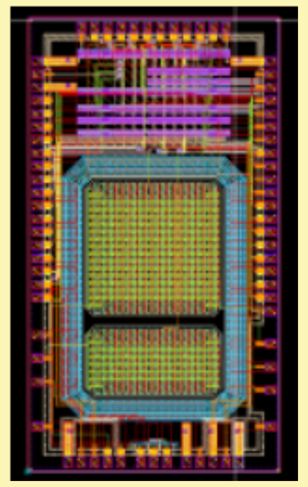
2022 prototype
no gain layer

MONOLITH Project prototypes

Monolithic prototypes in SiGe BiCMOS (without internal gain layer)

2016



200ps

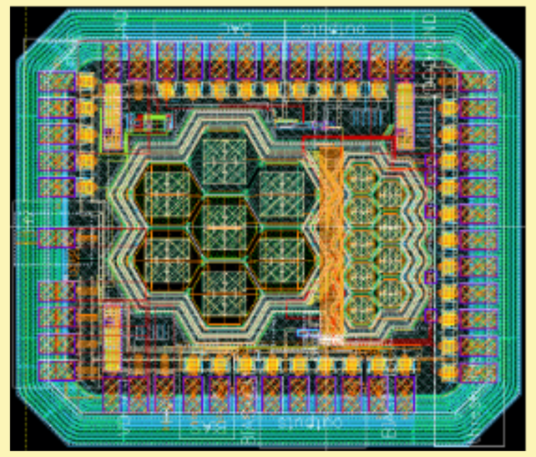
- 1 mm^2 pixel
- Discriminator

2017

110ps

- 30 pixels 500x500µm^2
- 100ps TDC +I/O logic

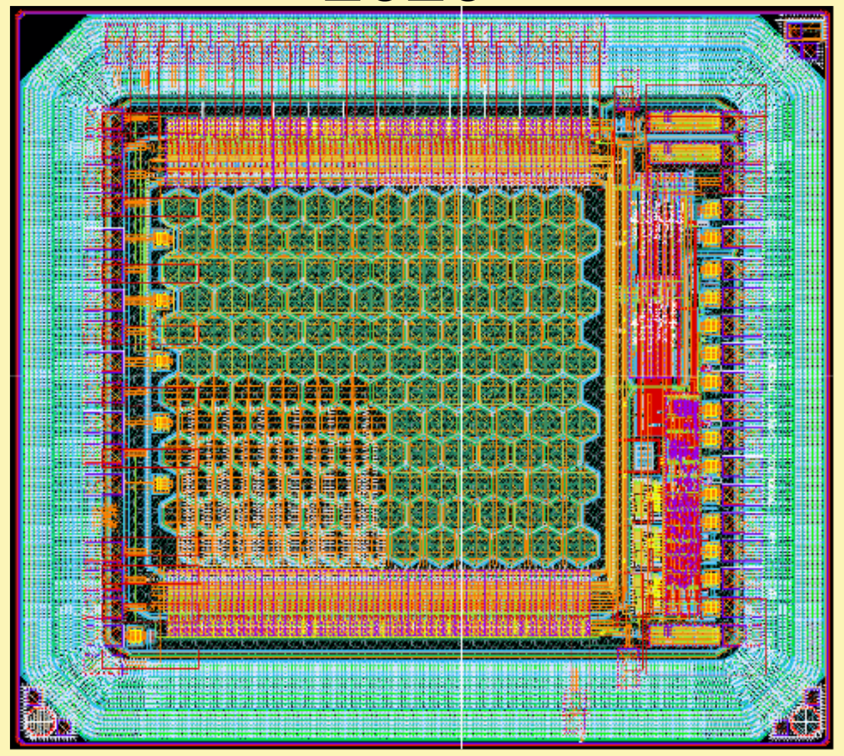
2018



50ps

- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

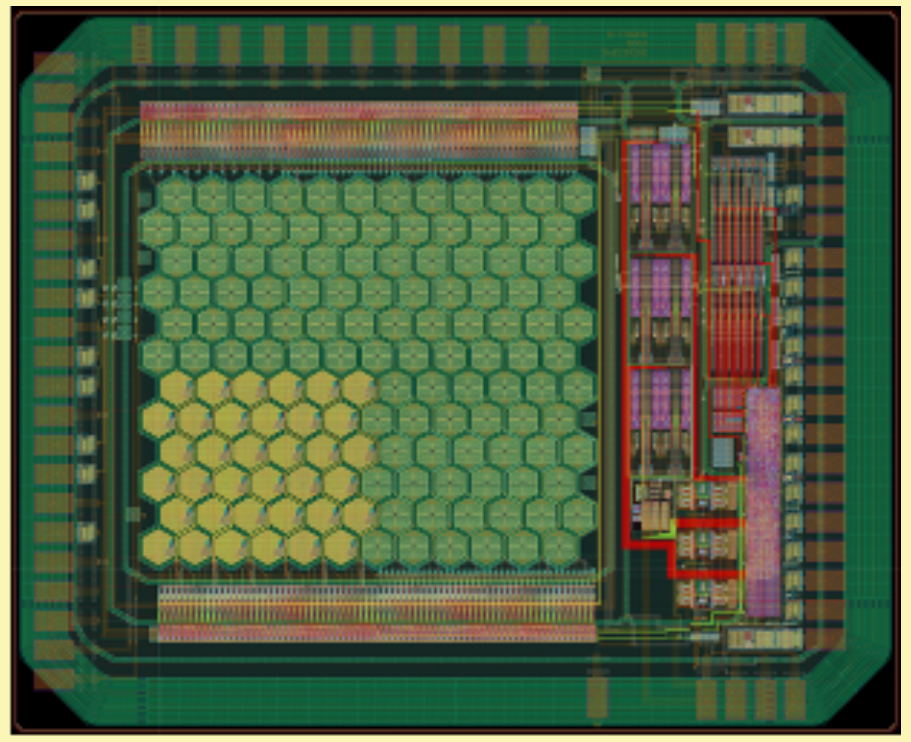
MONOLITH prototype 1
2020



36 ps

- Hexagonal pixels 100µm pitch
- 30ps TDC + I/O logic
- 4 analog channels

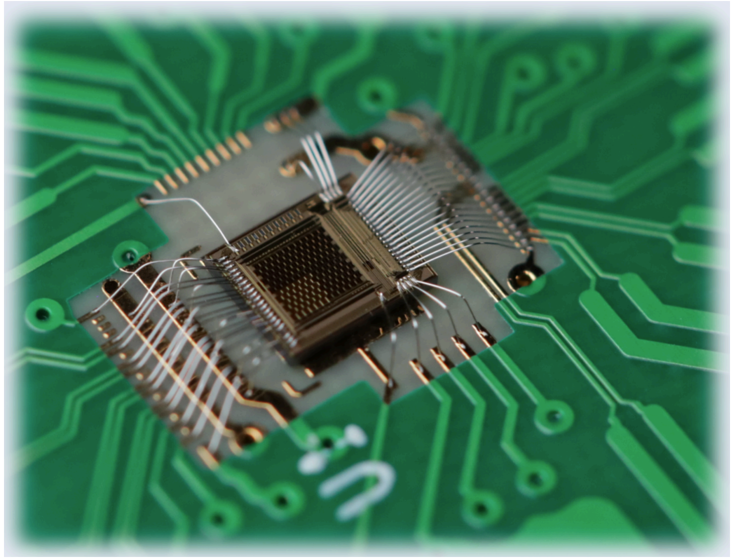
MONOLITH prototype 2
2022



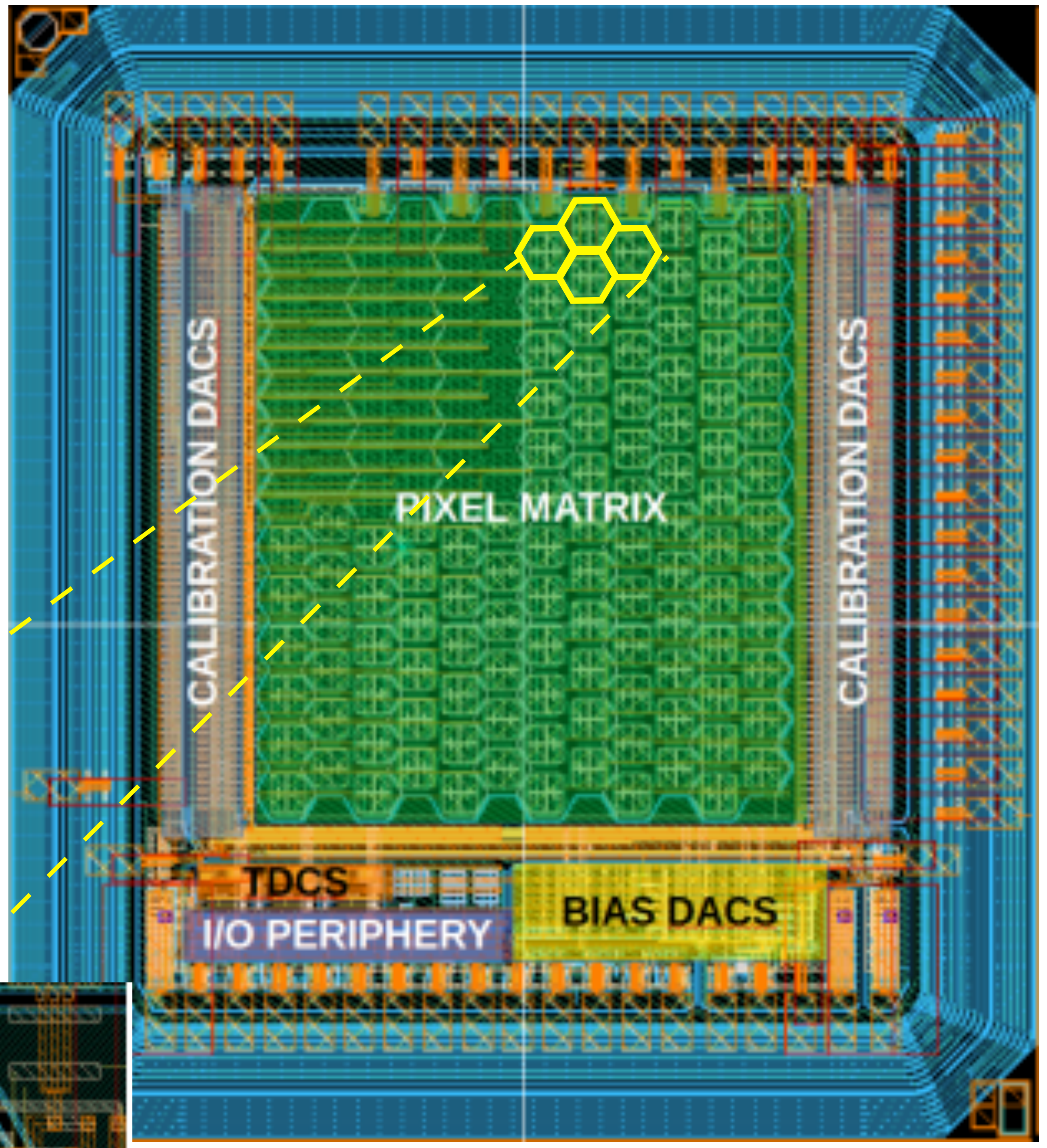
- Matrix of 12x12 hexagonal pixels
- 100µm pitch
- improved electronics
- 50µm epitaxial layer (350Ωcm)

evolution of 2020 prototype

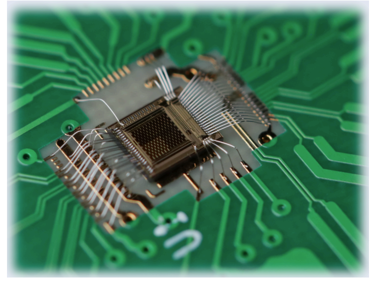
prototype2 (2022) — no gain layer



- Same matrix configuration as prototype1, but
  - **Substrate**: 50Ωcm → 350Ωcm epilayer, 50μm thick on low-res (1Ωcm)
    - ➡ smaller pixel capacitance
    - ➡ depletion 23μm → 50μm
    - ➡ larger voltage plateau
    - ➡ can operate sensor with v_{drift} saturated everywhere
  - **Preamp and driver** voltage decoupled
    - ➡ was limiting optimal amplifier operation
    - ➡ was creating cross-talk, removed
  - **Optimised FE layout**, **differential output**, high-frequency cables
    - ➡ better rise time (600ps → 300ps)

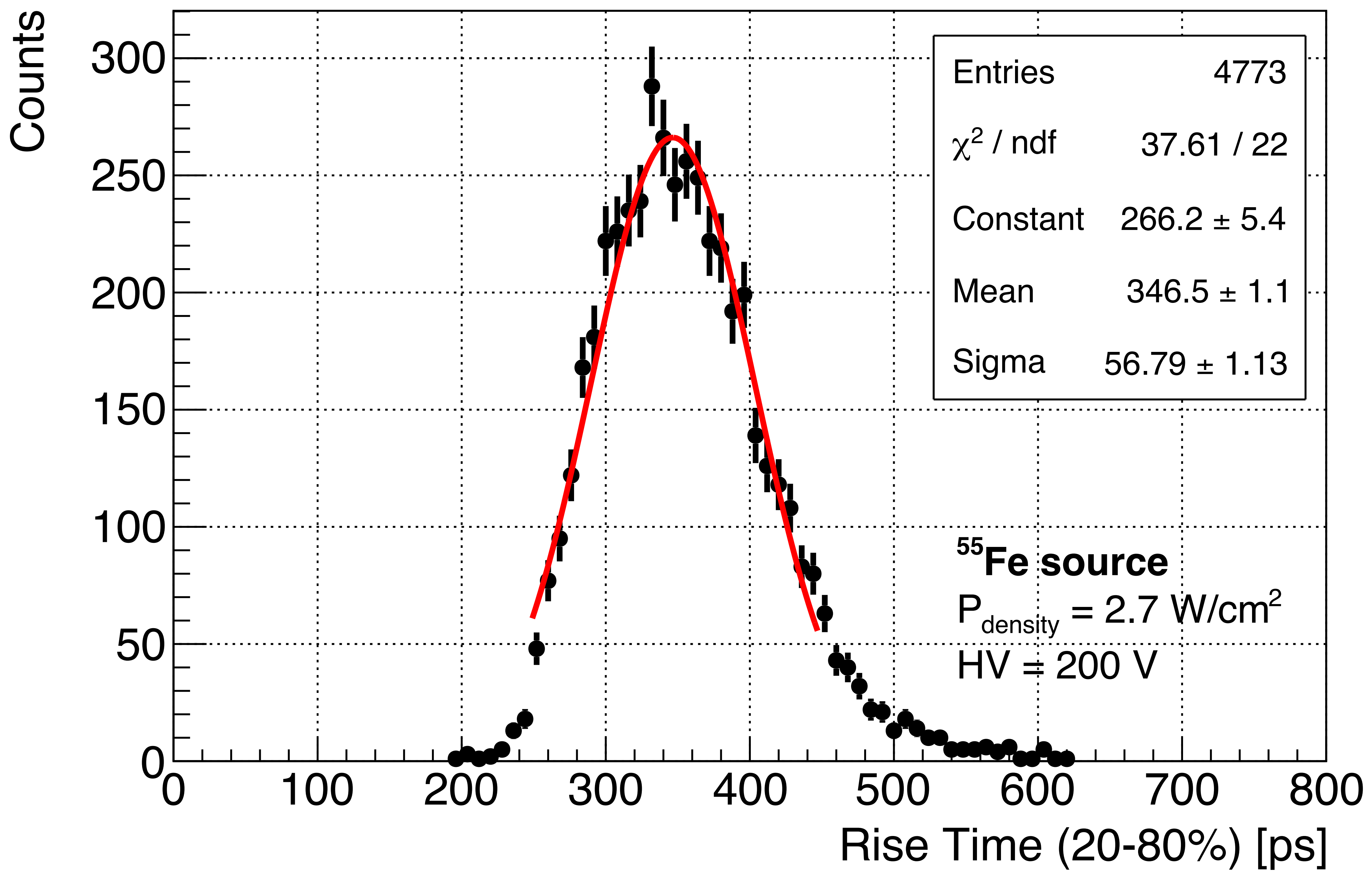


prototype2 (2022) — no gain layer

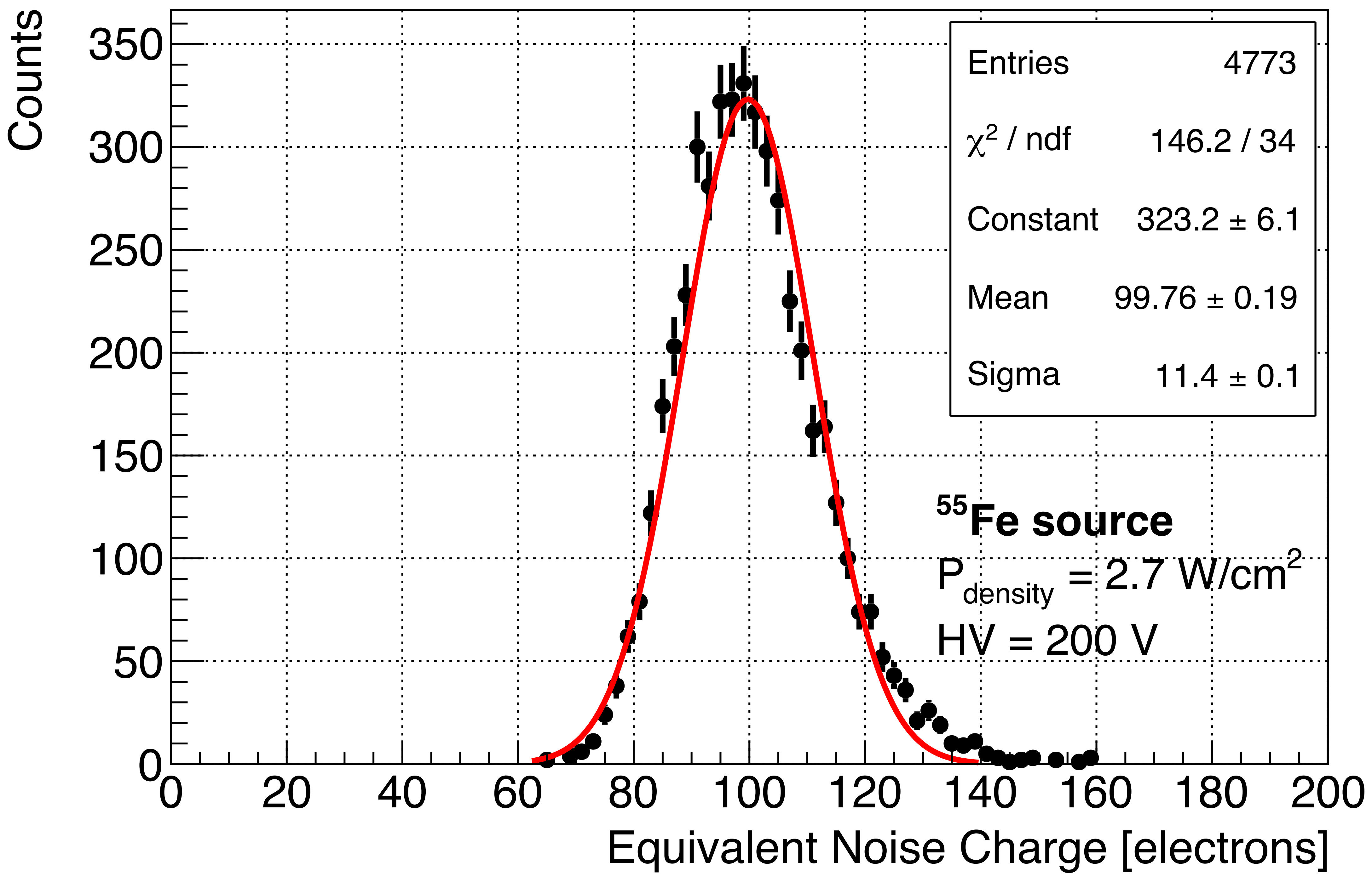


^{55}Fe measurements in cleanroom:

Risetime (20%–80%) ≈ 350 ps

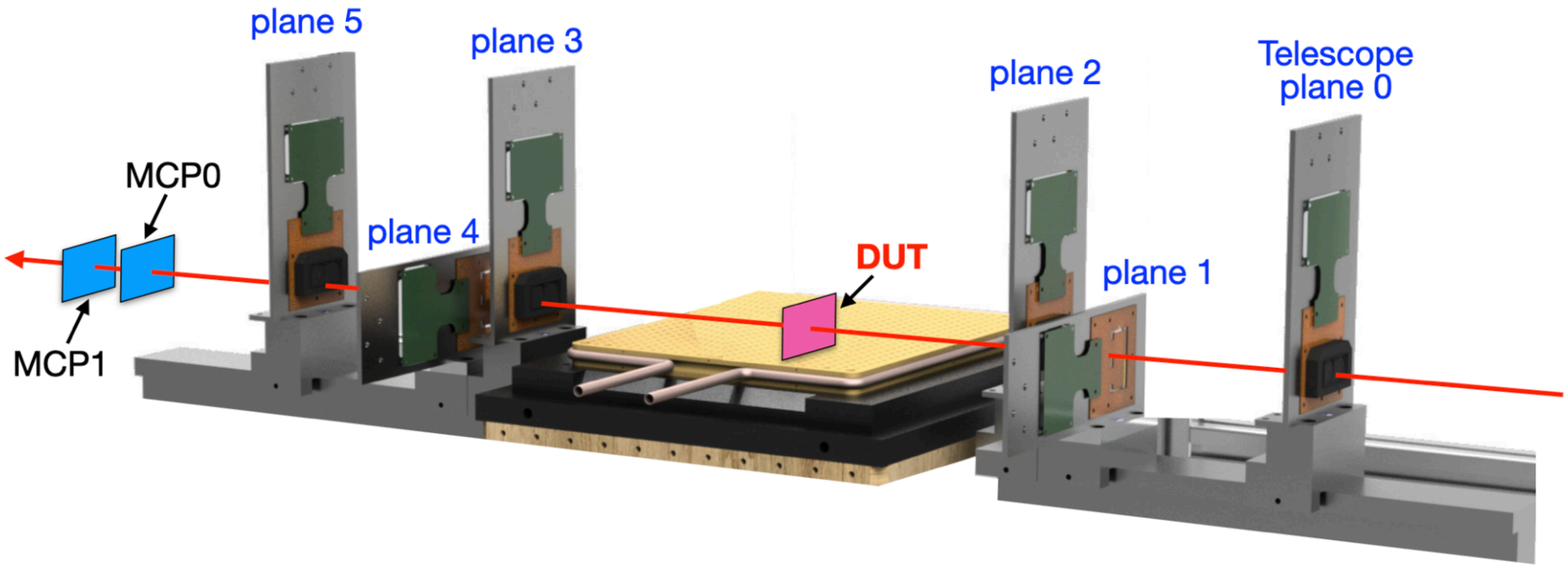


ENC ≈ 100 e⁻



Test Beam: Experimental Setup

Mid October SPS testbeam with 120 GeV/c π to measure **efficiency** and **time resolution**

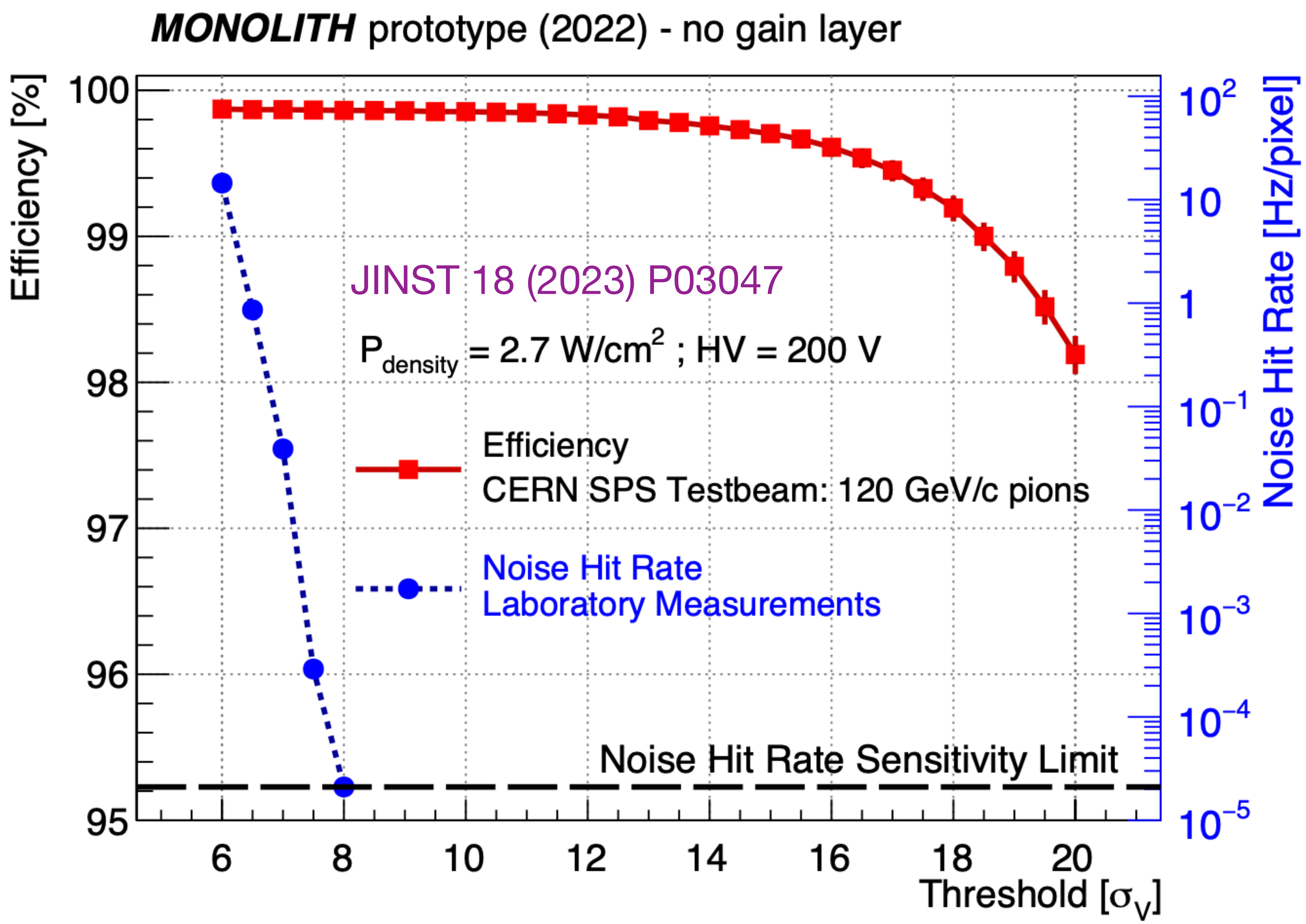


UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx 10\ \mu m$)

Two MCPs ($\sigma_t \approx 5$ ps) to provide the timing reference

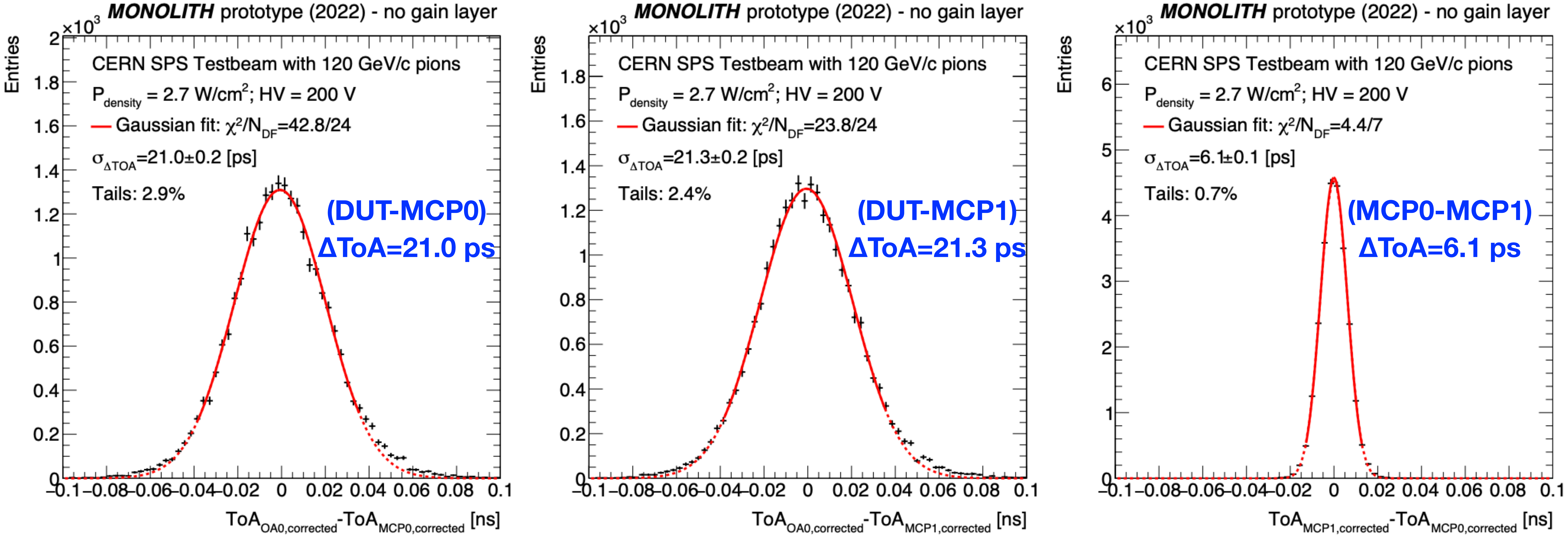
Lots of data taken: results in **JINST 18 (2023) P03047**

prototype2 (2022) — no gain layer



Large efficiency plateau at ≈ **99.8%**,
that allows operation at very low noise-hit rate

prototype2 (2022) — no gain layer



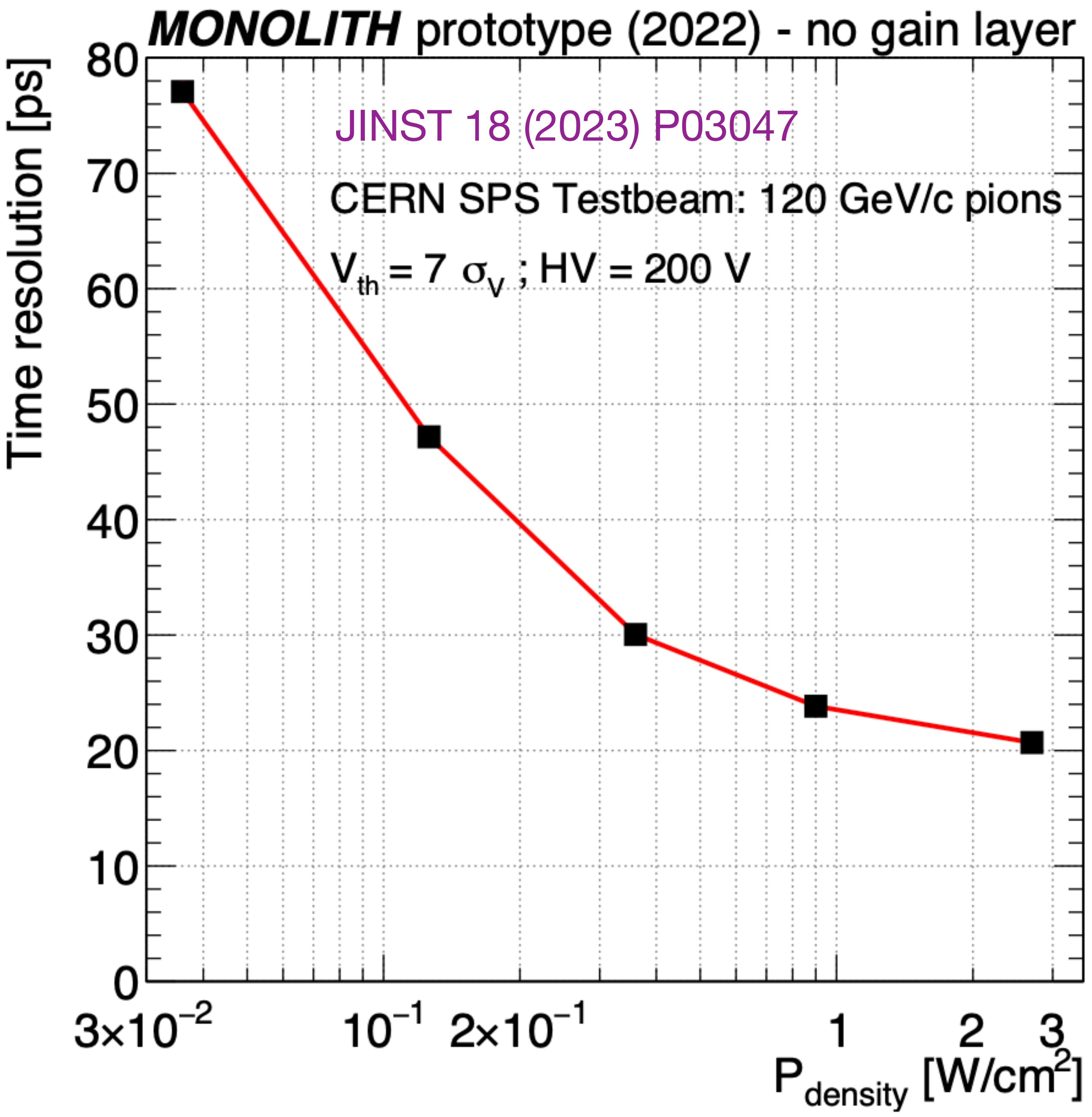
- Simultaneous fit to extract time resolutions of the DUT, MCP0, MCP1:

Fit results: MCP0 σ_T = (3.6 ± 1.5) ps
MCP1 σ_T = (5.0 ± 1.1) ps

σ_T = (20.7 ± 0.3) ps

non-Gaussian tails ≈ **3%**

prototype2 (2022) — no gain layer

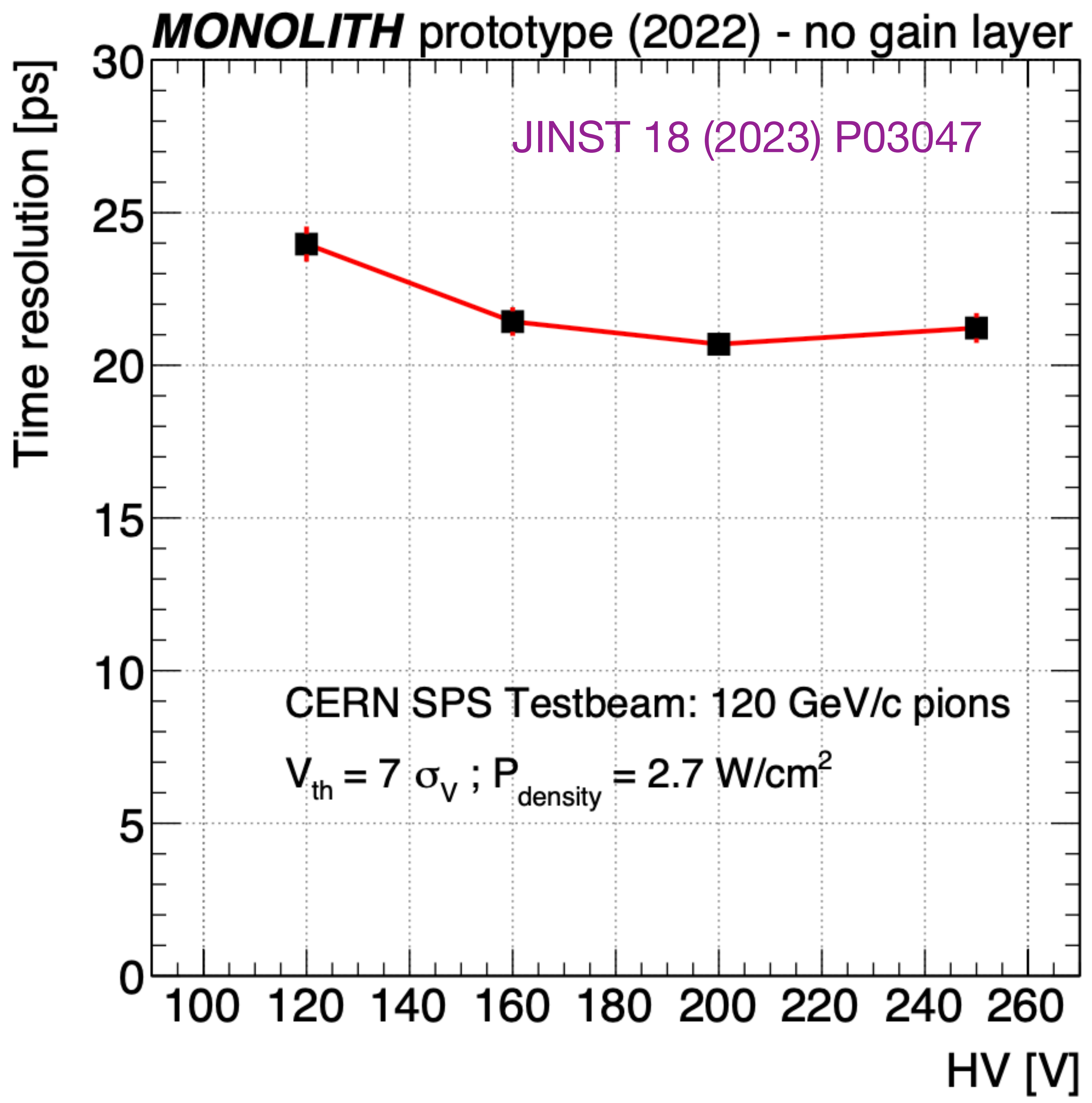


DUT operated at HV = 200 V and $V_{th} = 7\sigma_V$		
$P_{density}$ [W/cm^2]	Amplitude MPV [mV]	Time Resolution [ps]
2.7	48.6 ± 0.5	20.7 ± 0.3
0.9	35.8 ± 0.5	23.8 ± 0.3
0.36	22.6 ± 0.4	30.1 ± 0.4
0.13	14.2 ± 0.3	47.2 ± 0.7
0.04	16.2 ± 0.3	77.1 ± 0.9

20 ps at 2.7 W/cm^2
50 ps at 0.1 W/cm^2

Without gain layer.

prototype2 (2022) — no gain layer



Plateau of 100V with time resolution of
≈ 20 ps

Without gain layer

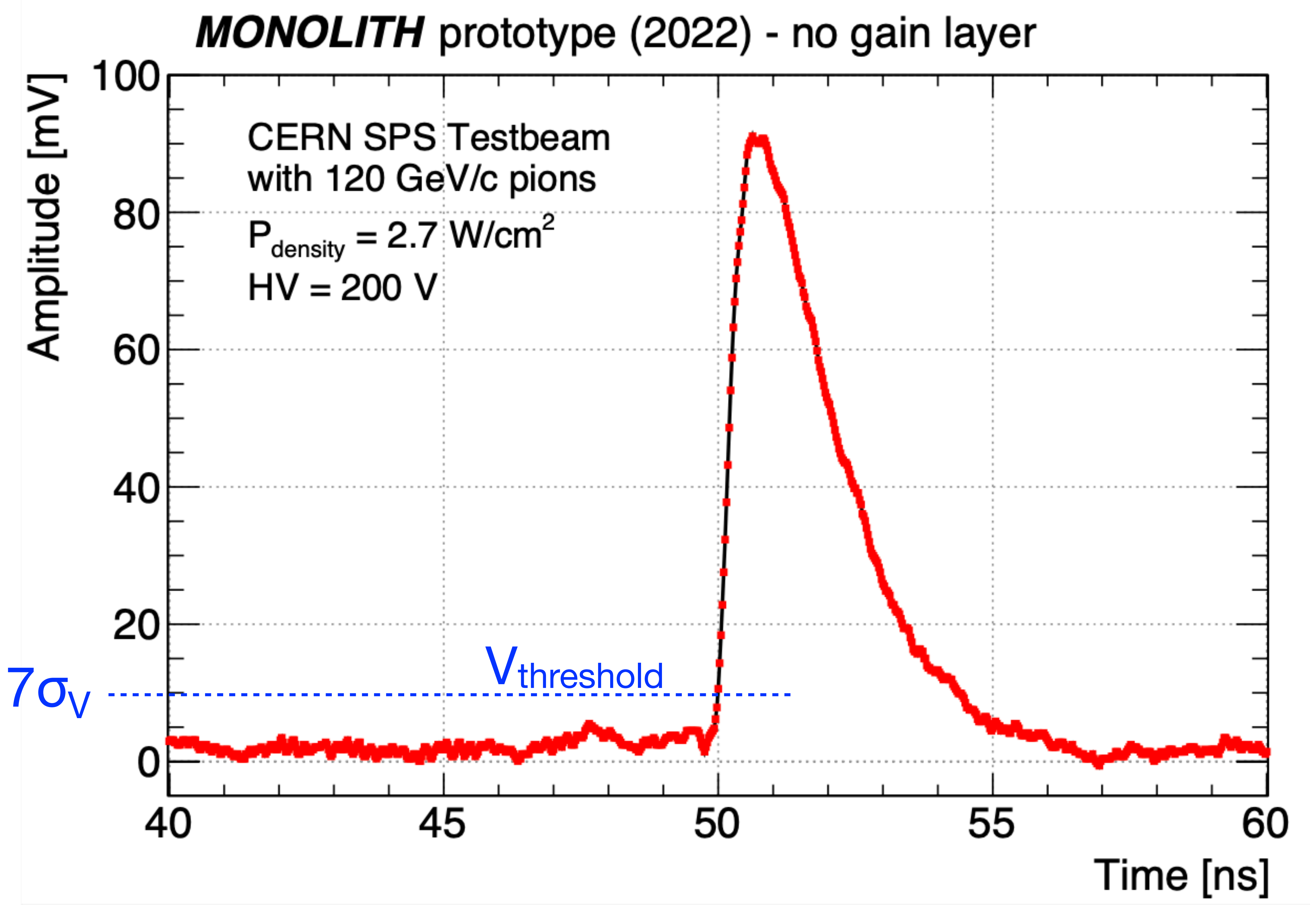
Results obtained with simple analysis and simple signal processing

Time resolution measurements

Remark :

20.7 ps obtained with very simple analysis:

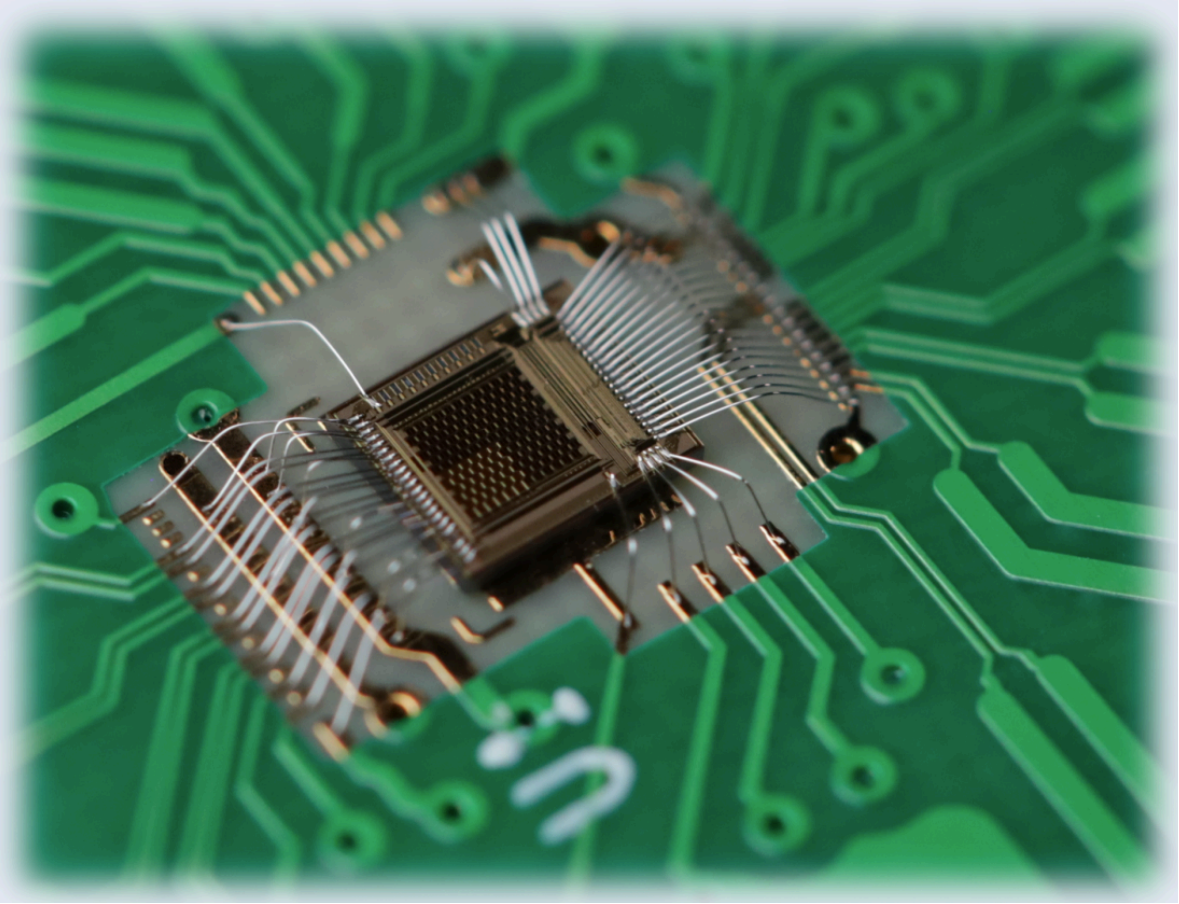
- **Linear interpolation** of oscilloscope samplings (25ps)
- Time Of Arrival (ToA): time at **$V_{threshold} = 7\sigma_V$**
- Δ_{ToA} distributions are **time-walk corrected**



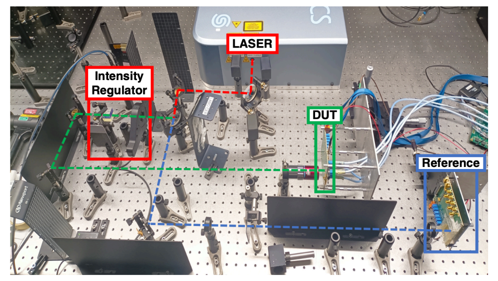
More complex analysis (spline interpolation, filtering, …) reaches **17.7 ps**

Laser measurements

with the 2022 prototype2 without gain

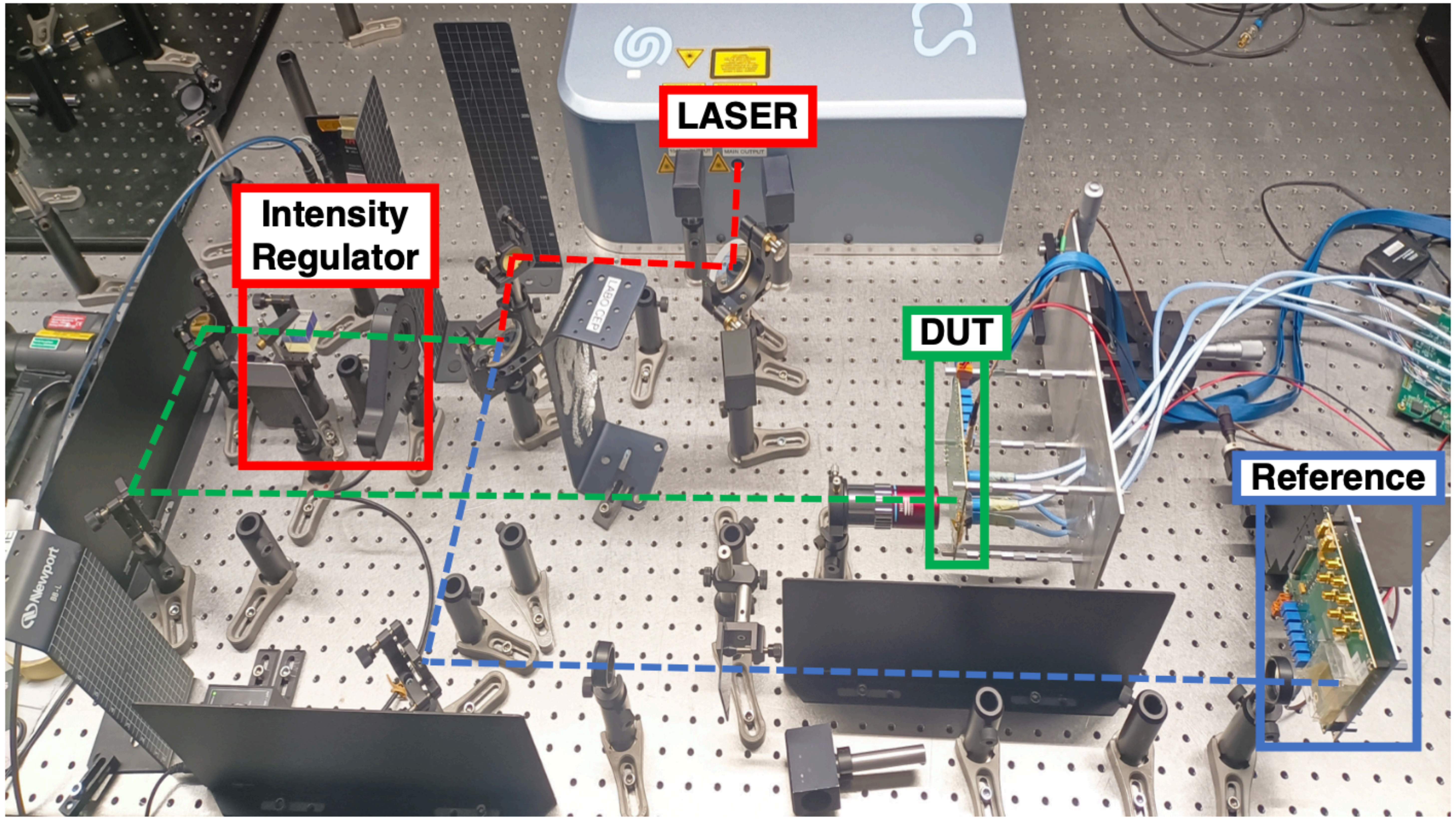


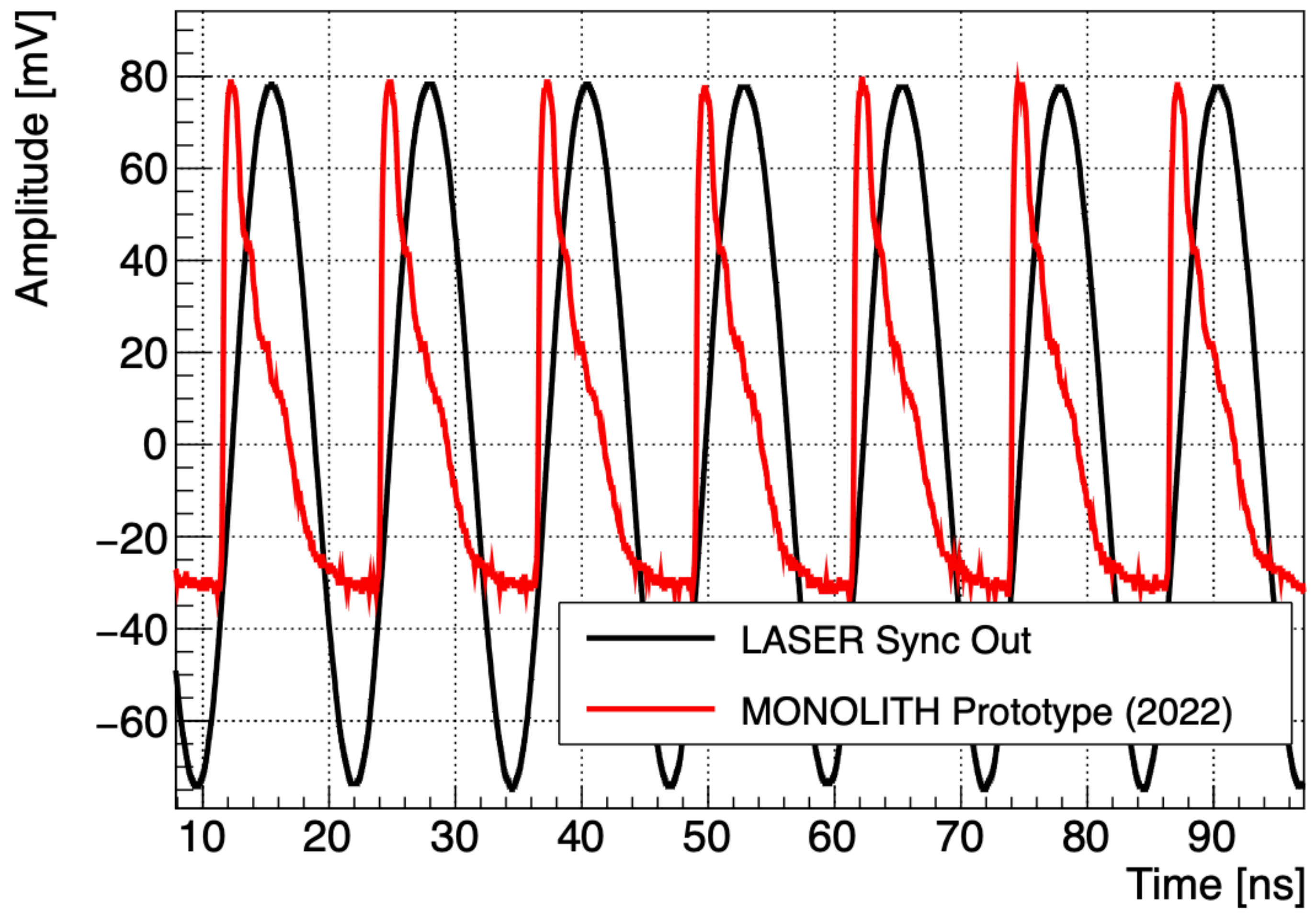
prototype2 (2022) — no gain layer



Measurement with a **laser** with a jitter of **100 fs**
(repetition frequency = **80 MHz**)

Many thanks to
L. Bonacina's lab of GAP UNIGE





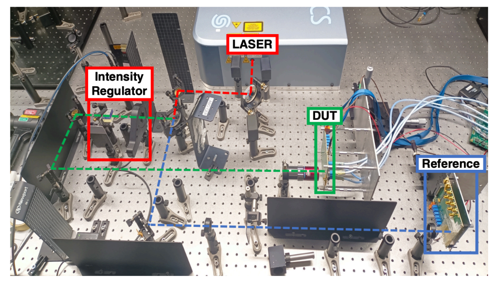
Time coincidence between two of our samples:

➡ "**Reference**" receiving always large laser pulse producing 17k electrons (σ_t = 2.5 ps)

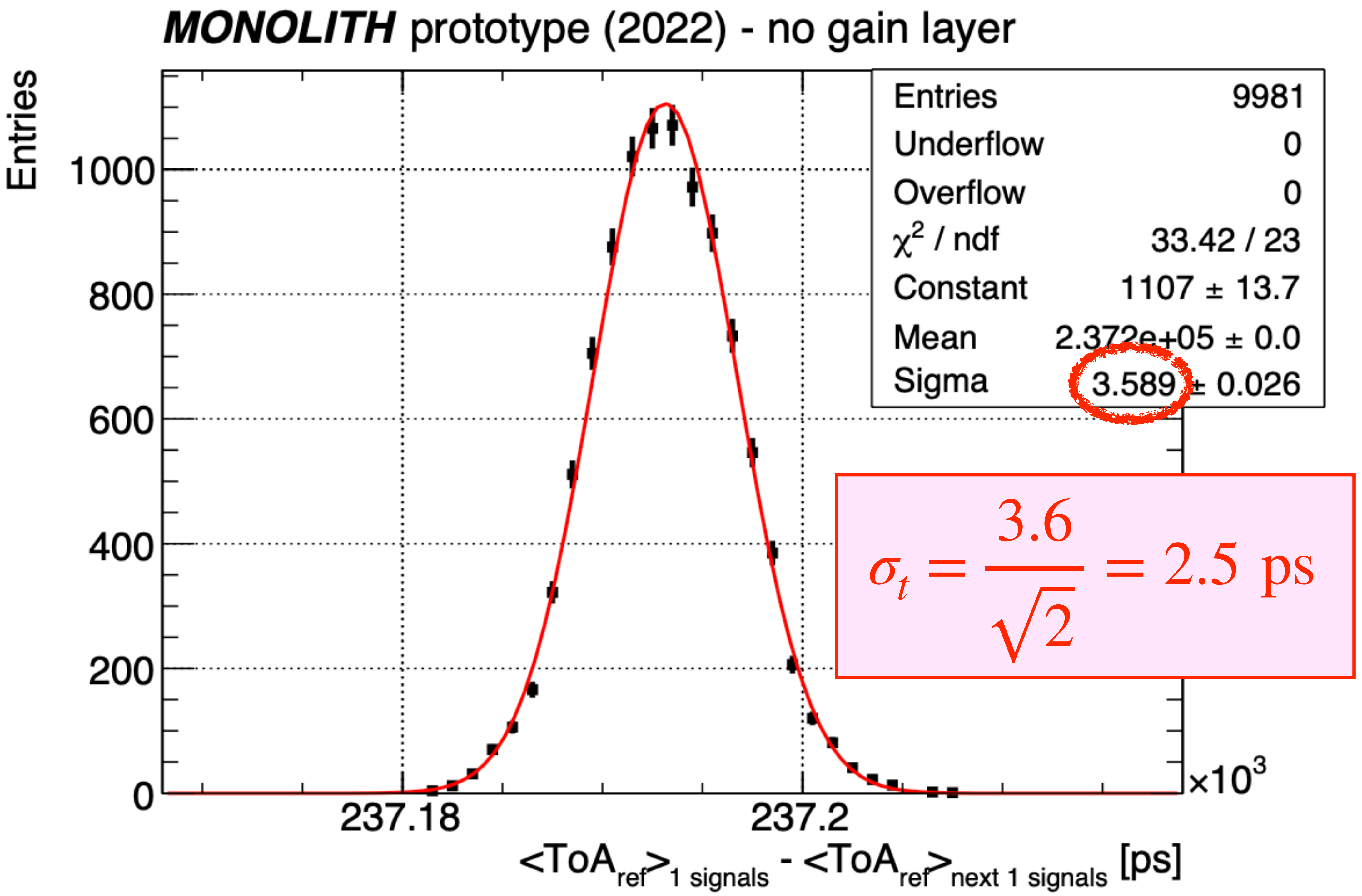
➡ "**DUT**" receiving variable laser power, to study the performance vs. amplitude

prototype2 (2022) — no gain layer

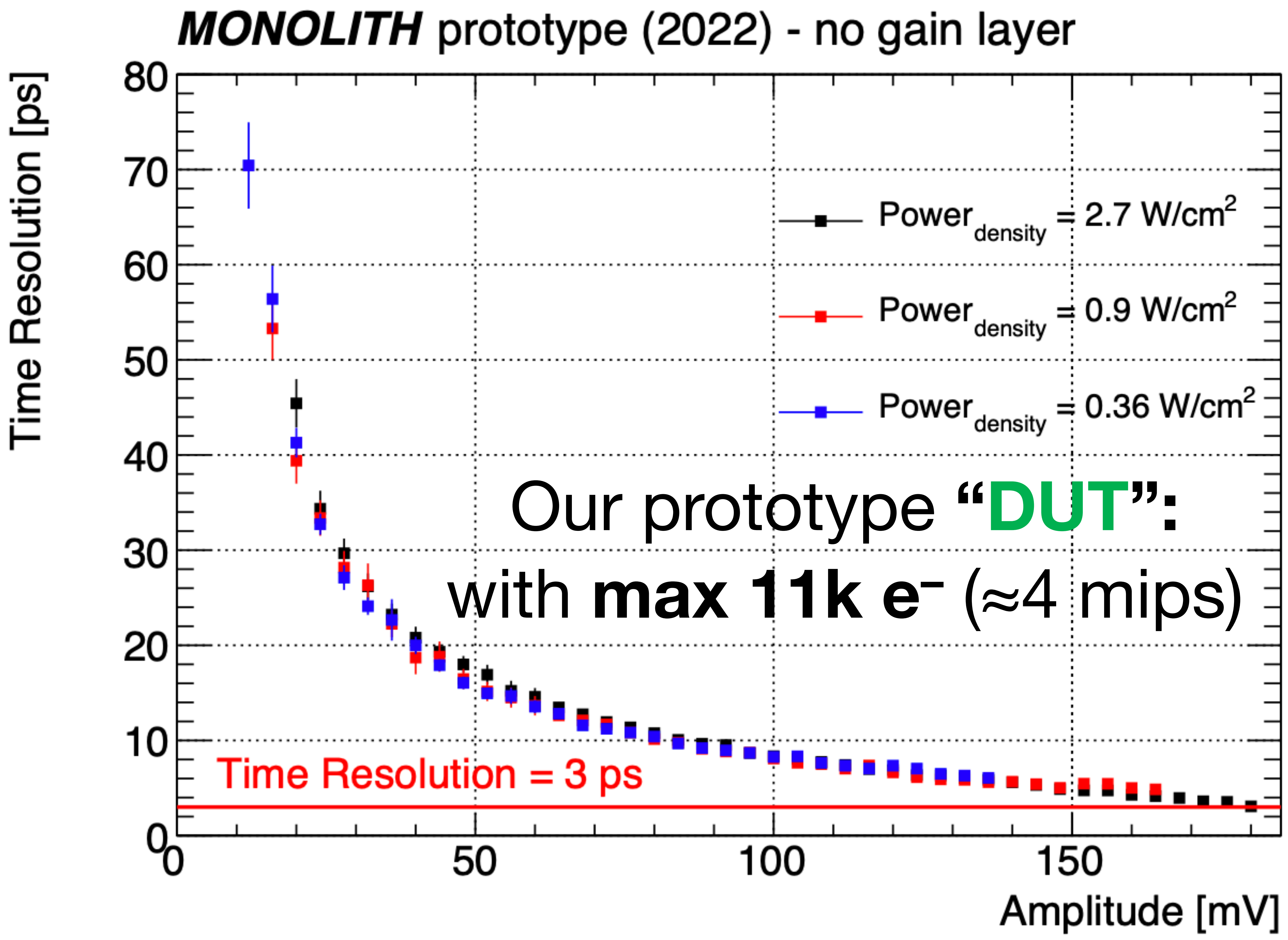
Laser Measurement (preliminary)



Laser Measurement



$$\sigma_t = \frac{3.6}{\sqrt{2}} = 2.5 \text{ ps}$$

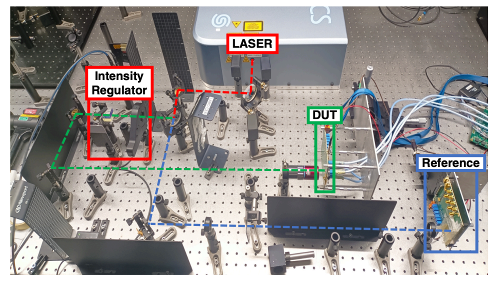


Our prototype "**Reference**":

Time resolution = 2.5 ps

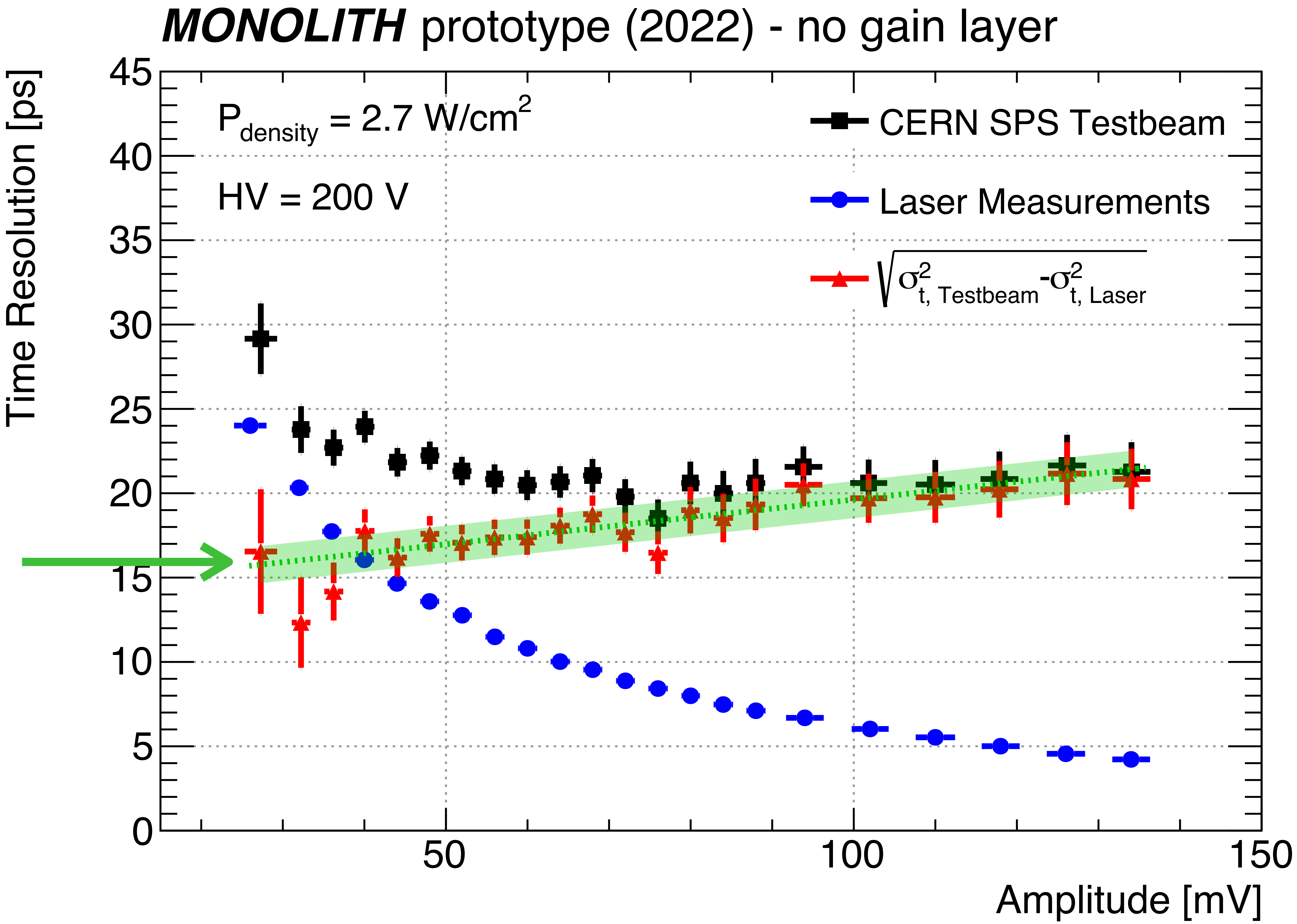
with **17k e⁻** (5—6 mips)

prototype2 (2022) — no gain layer



Laser Measurement (preliminary)

Estimate of the charge-collection ("Landau") noise



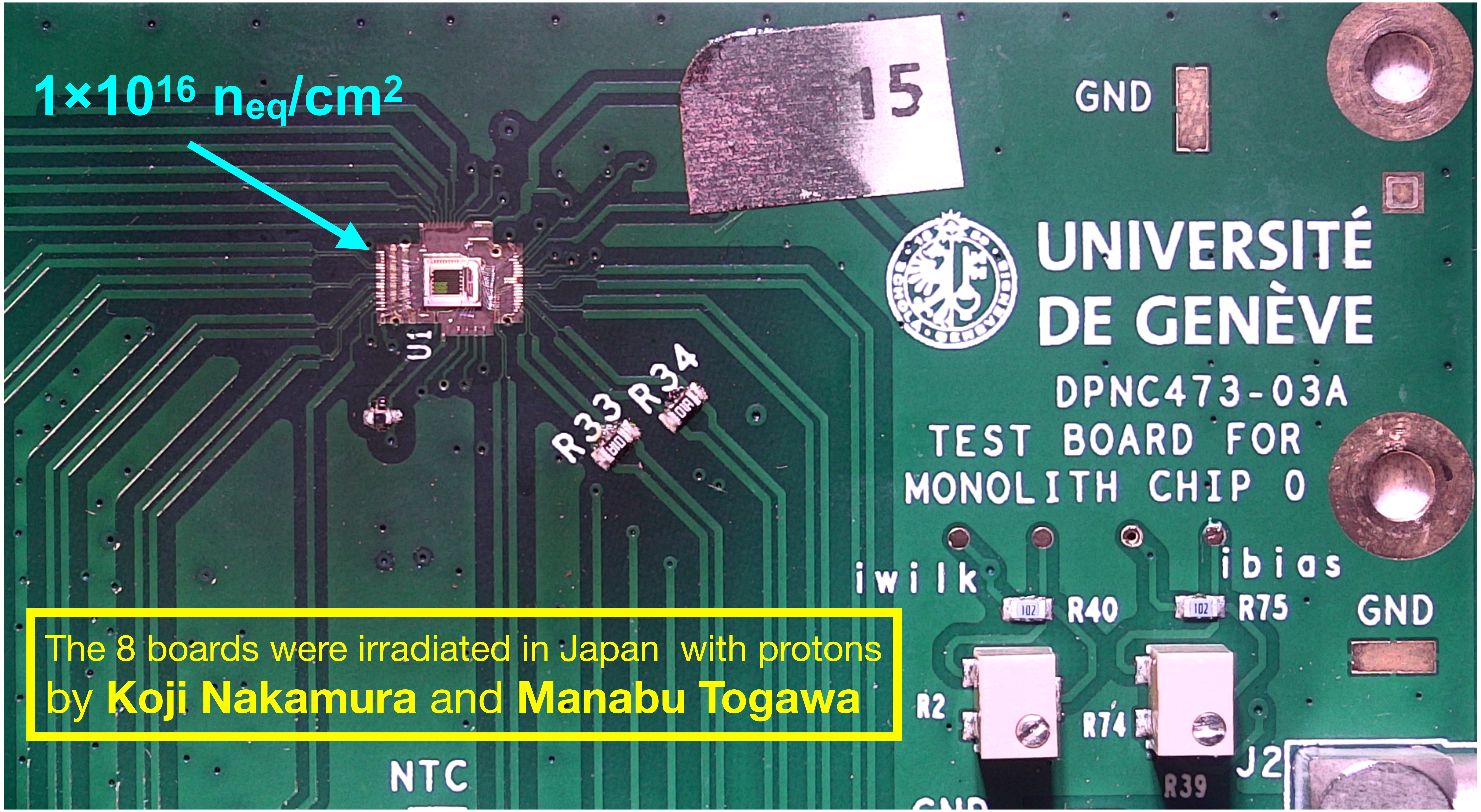
Radiation hardness studies

with the 2022 prototype2 <u>without gain</u>

Total of 40 analog pixels studied

Radiation hardness of SiGe HBTs

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.
8 samples of prototype2 ASIC were irradiated in Japan up to $1{\times}10^{16}\ n_{eq}/cm^2$.



Radiation hardness of SiGe HBTs

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.
8 samples of prototype2 ASIC were irradiated in Japan up to $1{\times}10^{16}$ n_{eq}/cm^2.

7 out of the 8 irradiated boards had **damaged voltage regulators**: **bypassed** with wire bonds

One board **not configurable** : short on the digital logic. Not used

Three unirradiated boards. (one is the same of the CERN testbeam, results published in JINST 18 (2023) P03047)

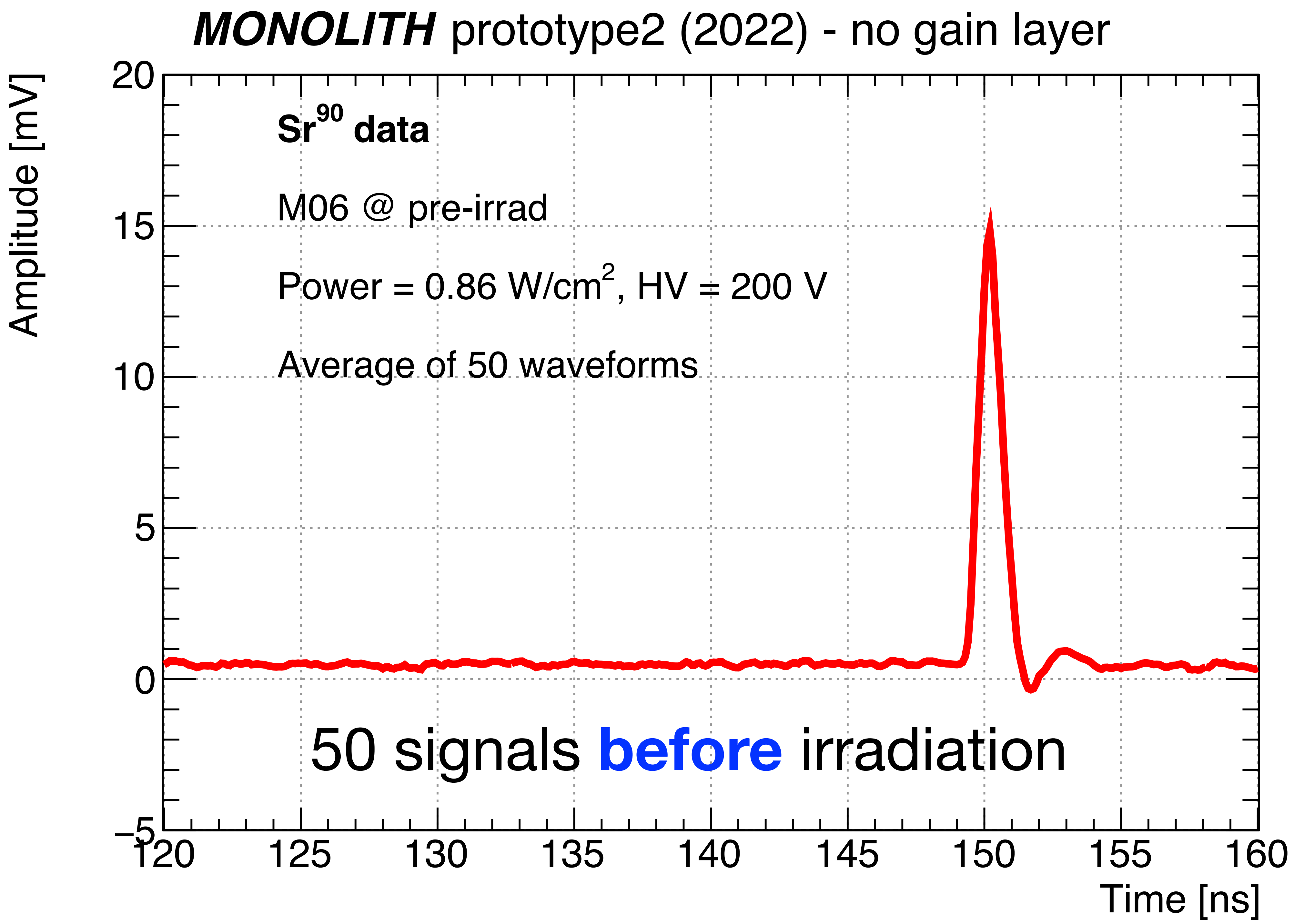
Board Name	Fluence [1 MeV n_{eq}/cm^2]
M23	$2 \cdot 10^{13}$
M22	$9 \cdot 10^{13}$
M21	$6 \cdot 10^{14}$
M19	$6 \cdot 10^{14}$
M18	$3 \cdot 10^{15}$
M17	$3 \cdot 10^{15}$
M16	$1 \cdot 10^{16}$
M15	$1 \cdot 10^{16}$
M06	not irradiated – for comparison
M05	not irradiated – for comparison
M07	not irradiated – for comparison

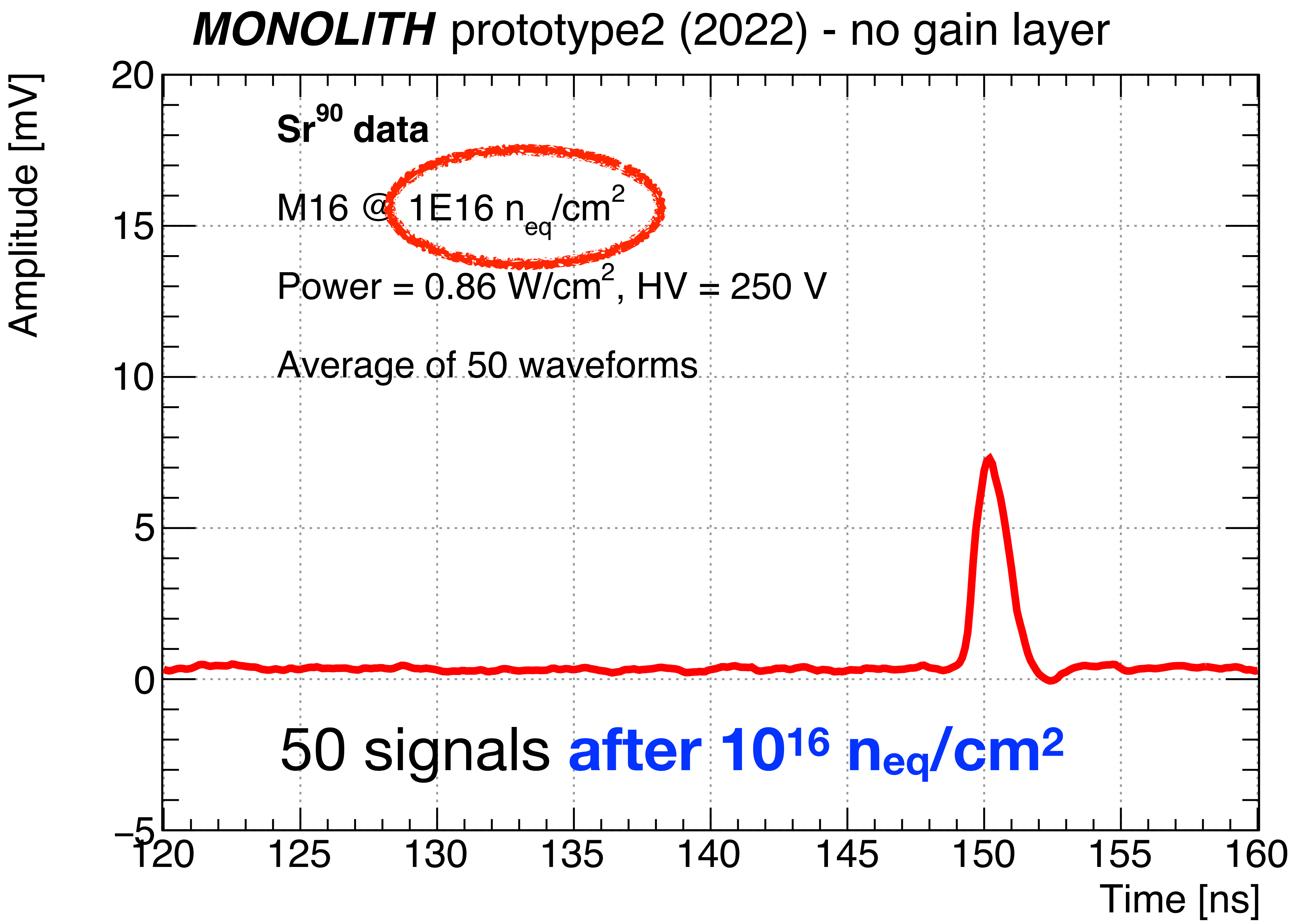
Radiation hardness of SiGe HBTs

Very good news:

even after $1{\times}10^{16}$ n_{eq}/cm^2 the ASICs work !!!

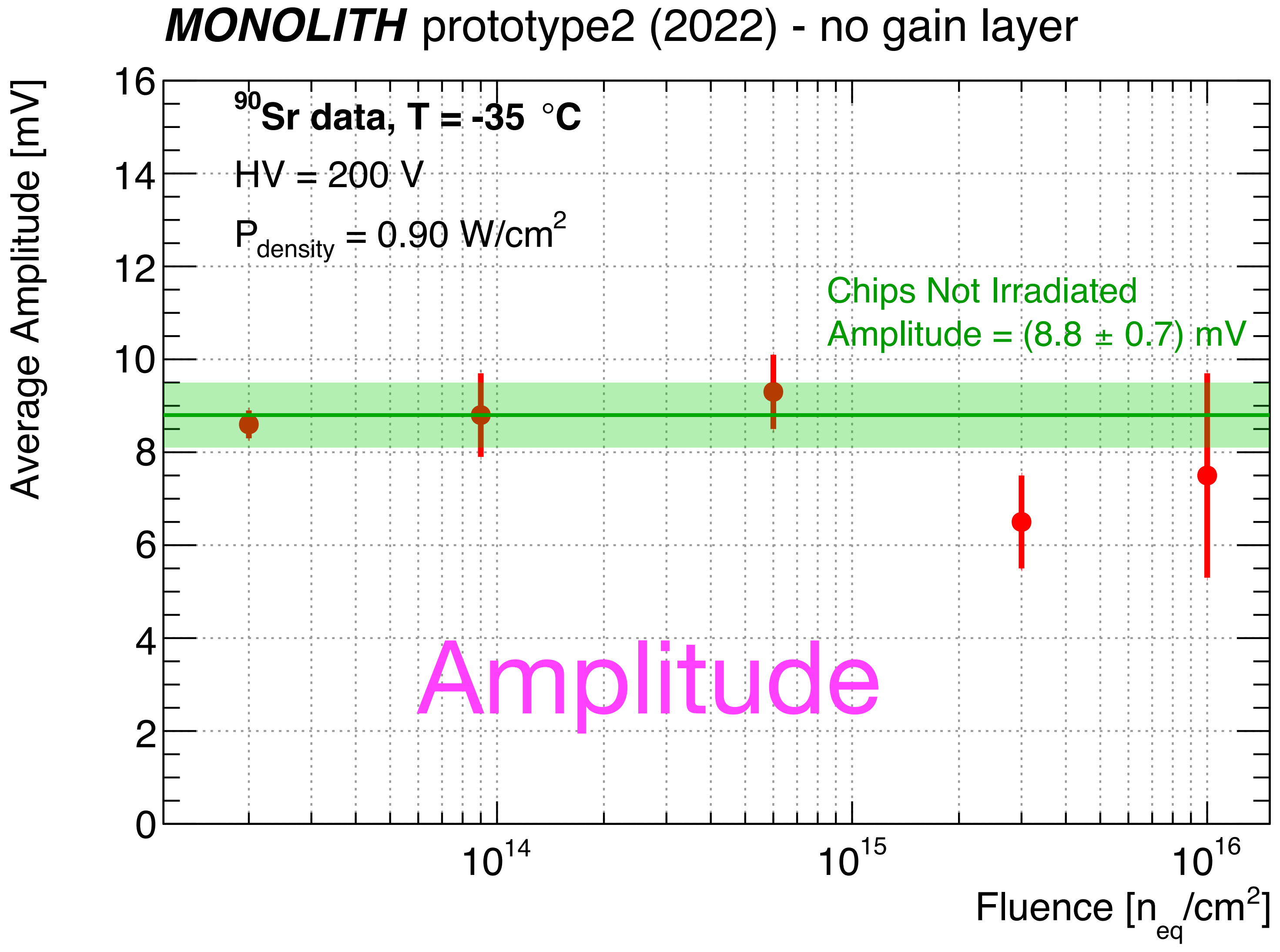
although signals are clearly degraded

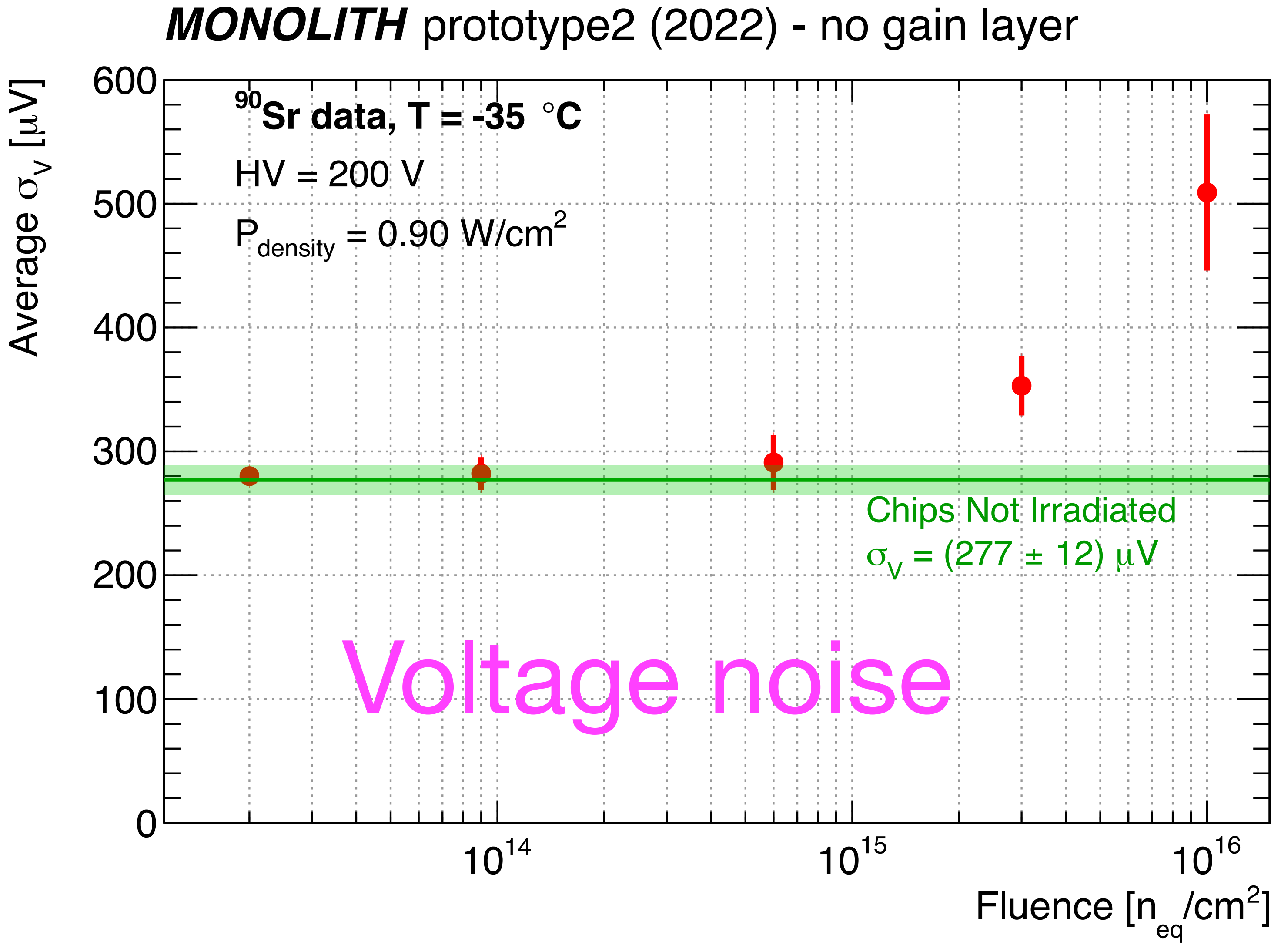


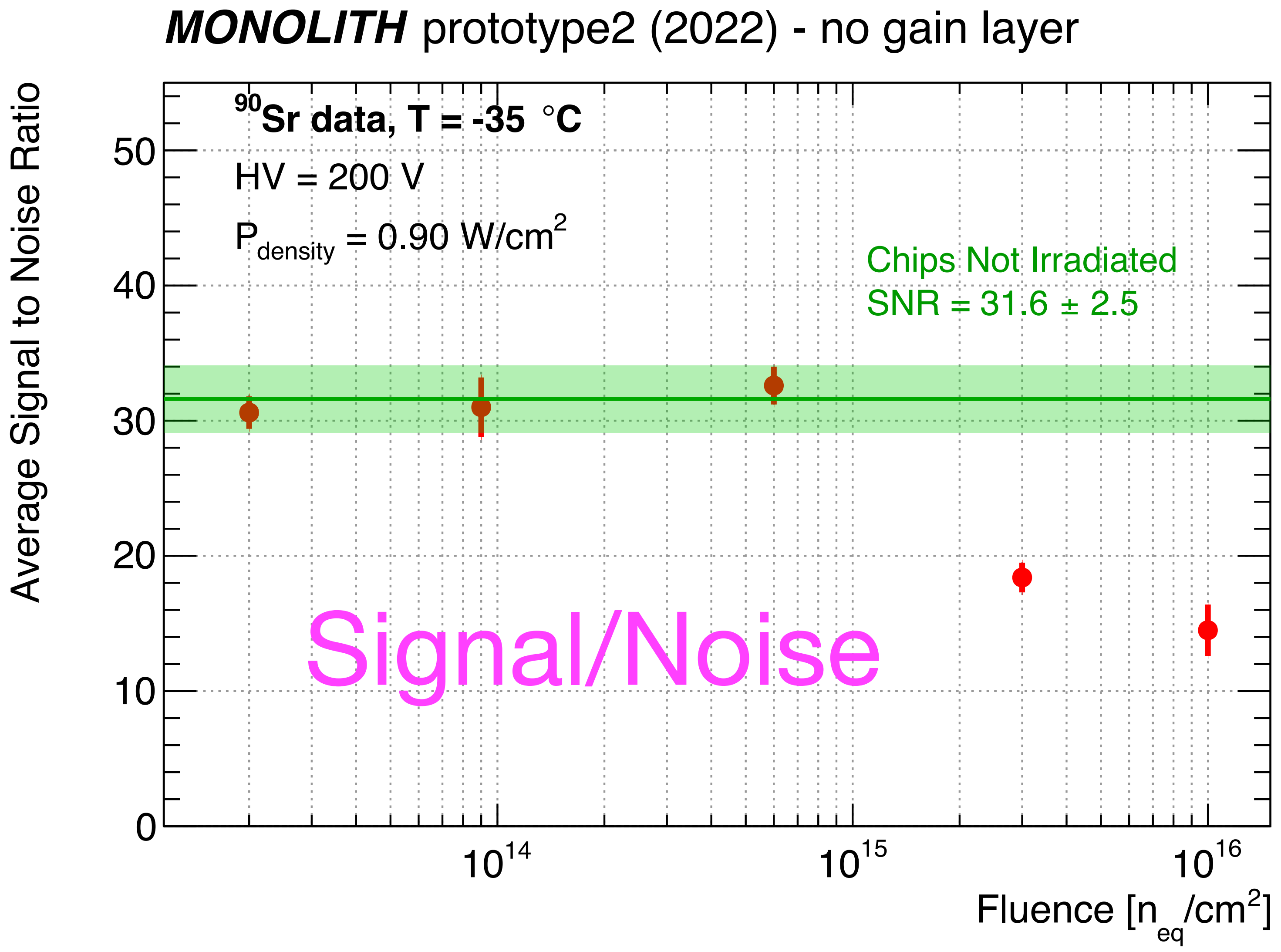


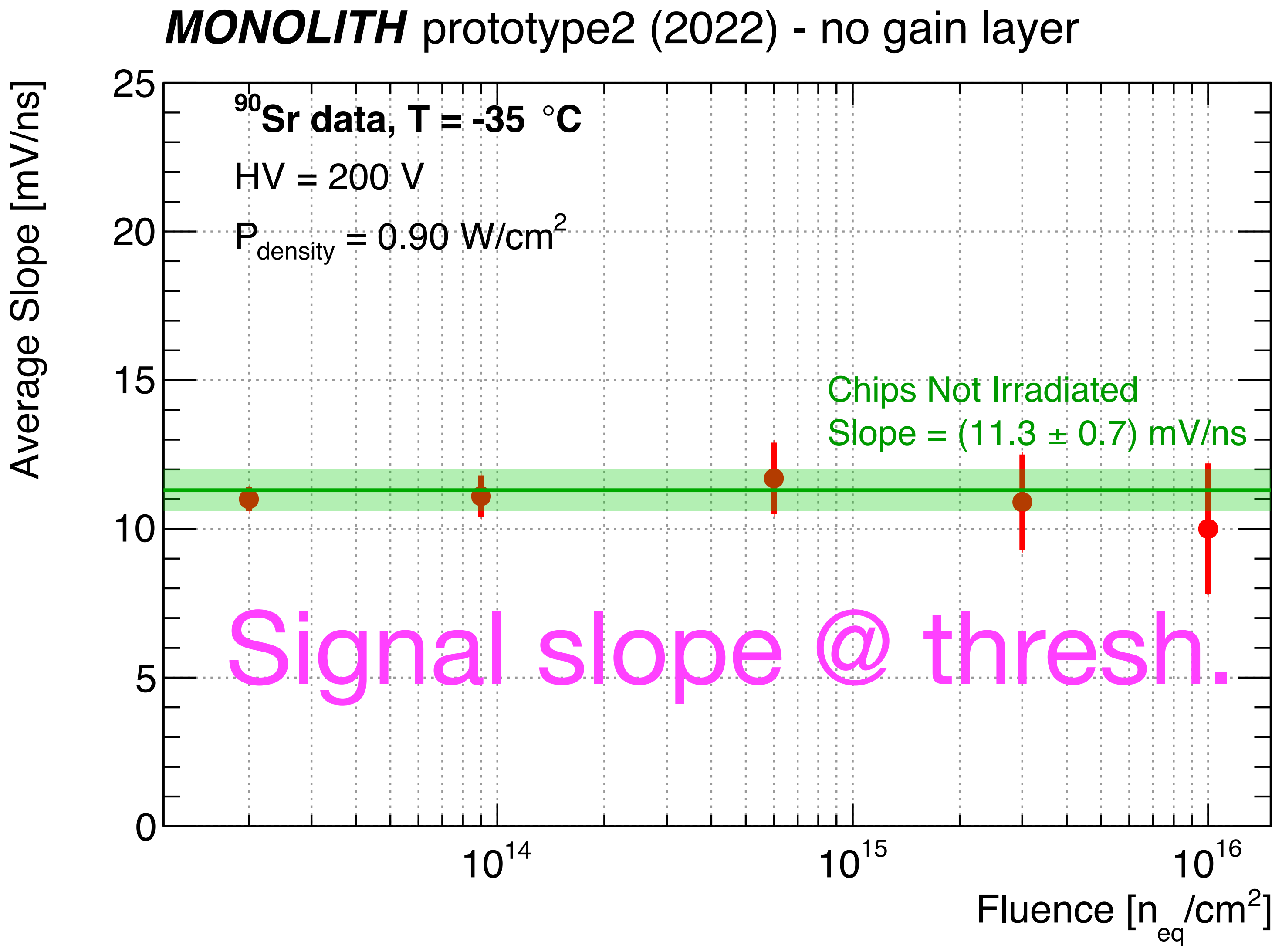
Radiation hardness of SiGe HBTs

Preliminary





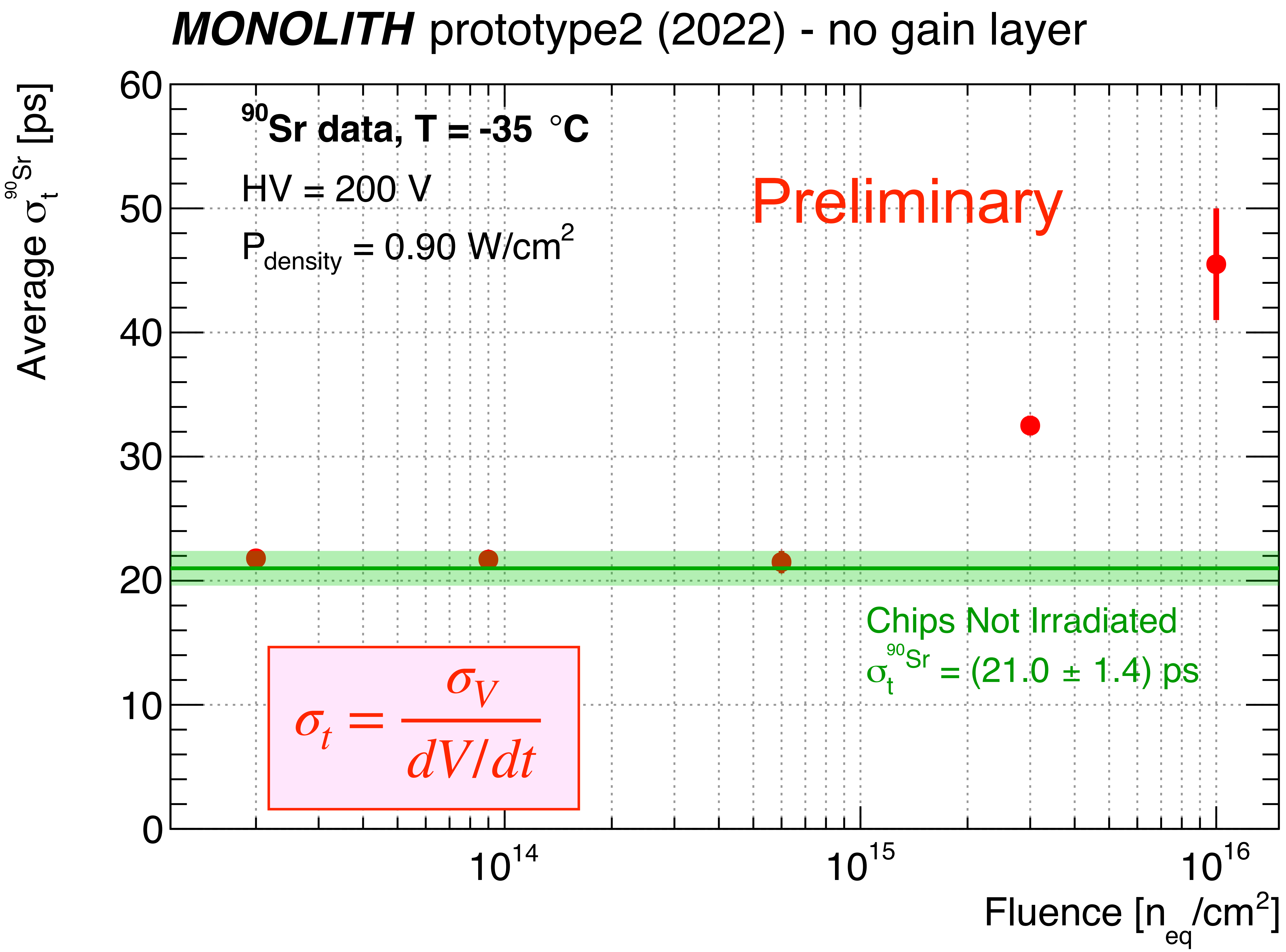




Characterisation with ^{90}**Sr** source of boards irradiated up to **10^{16} n_{eq}/cm^2**

Averages of the 4 analog pixels (HV = 200 V, T=-35°, 0.9 W/cm^2)

Radiation hardness of SiGe HBTs



Excellent news from radiation tolerance studies:

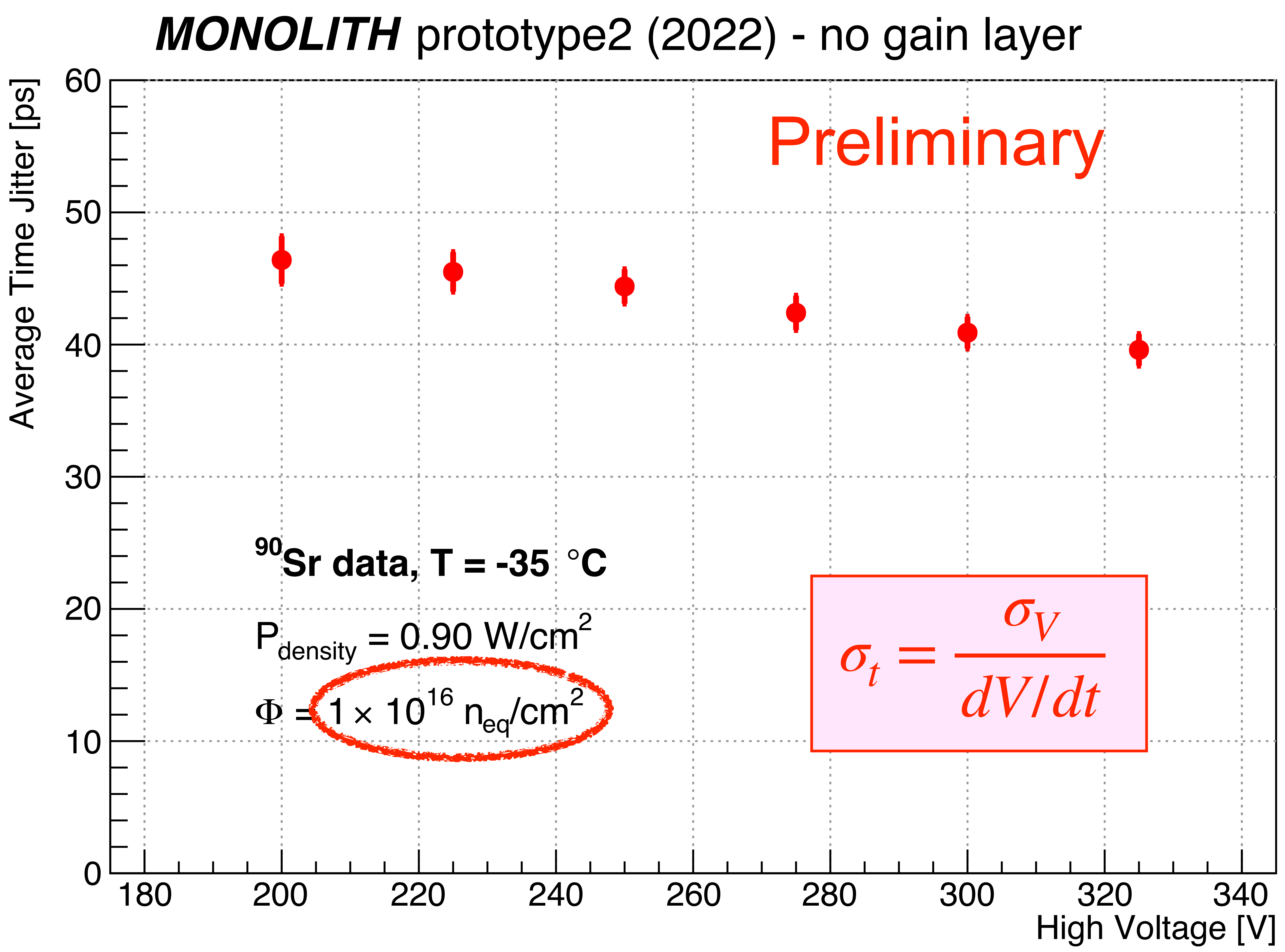
The time jitter with ^{90}**Sr** increases **from 21ps** (unirradiated) **to 46ps** (at 10^{16} n_{eq}/cm^2) at **HV = 200V** and **0.9 W/cm²**

Radiation hardness of SiGe HBTs

Total of **40 pixels studied** with **^{90}Sr**, at different proton fluence.
At a given proton fluence, pixel-to-pixel **time jitter variations within 20%**.
(quoted uncertainties on the averages are the standard deviations)

Fluence [n_{eq}/cm^2]	$\sigma_t^{^{90}Sr}$ [ps] pixel 1	pixel 2	pixel 3	pixel 4	Average $\sigma_t^{^{90}Sr}$ [ps]
0	22.1	20.5	18.8	19.9	21.0 ± 1.4
	22.1	22.7	19.5	19.6	
	22.9	22.2	21.1	20.7	
2×10^{13}	21.4	22.2	21.2	22.4	21.8 ± 0.6
9×10^{13}	21.4	22.5	21.0	21.8	21.7 ± 0.6
6×10^{14}	21.5	22.4	20.2	20.9	21.5 ± 0.8
	20.7	22.3	22.6	21.3	
3×10^{15}	32.7	33.2	31.4	32.8	32.5 ± 0.8
1×10^{16}	43.3	50.9	44.0	47.5	45.5 ± 4.5
	49.7	53.0	36.2	40.0	

Radiation hardness of SiGe HBTs



Rate measurements with **^{109}Cd** source show that after 1×10^{16} n_{eq}/cm^2 the sensor is not fully depleted at HV = 200 V

At 0.9 W/cm² the time jitter with **^{90}Sr** at Φ = 1×10^{16} n_{eq}/cm^2 decreases

from 46ps at HV = 200 V

to 40ps at HV = 325 V

Radiation hardness of SiGe HBTs

Very preliminary

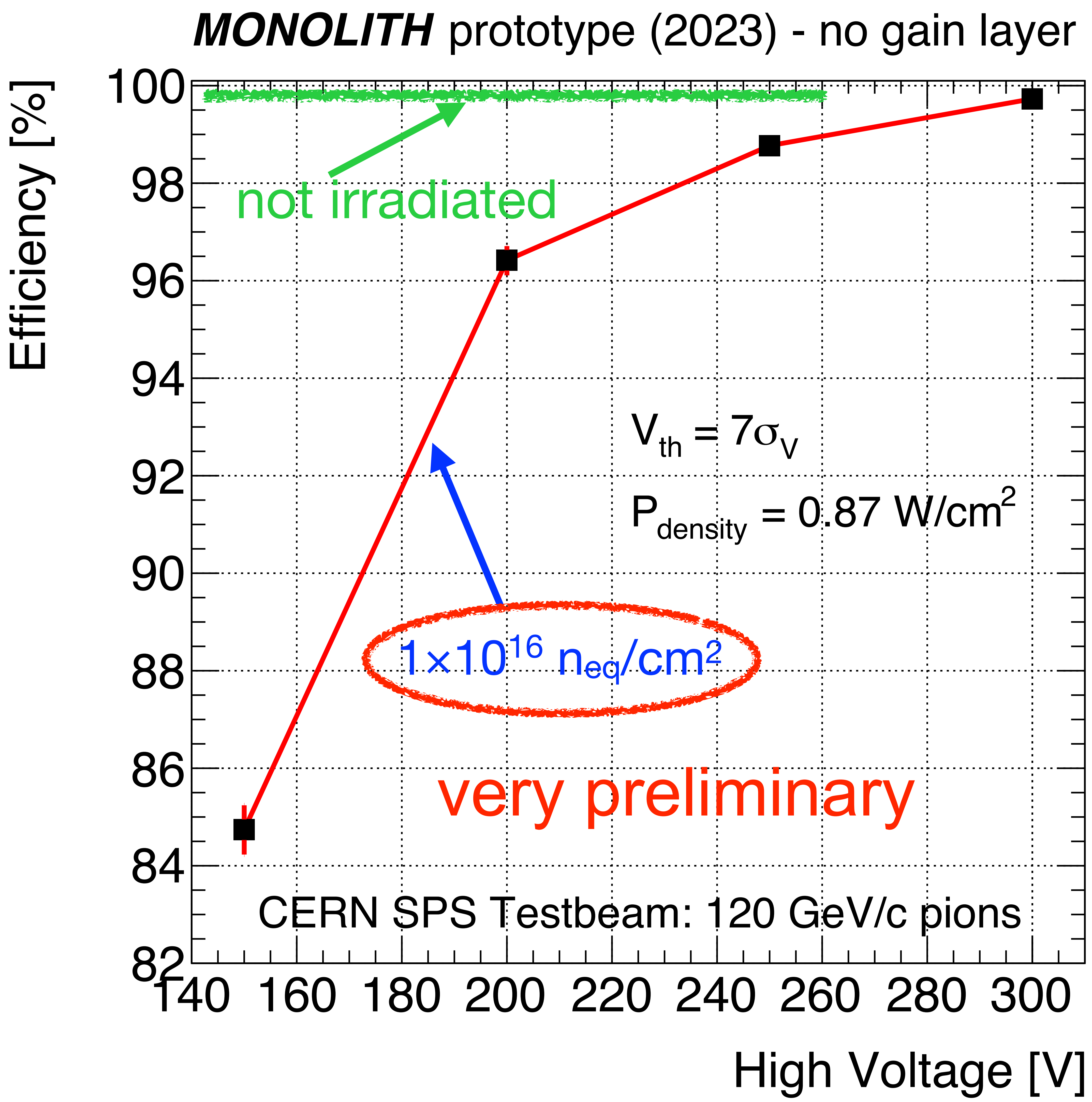
August 2023 testbeam at CERN SPS

Board irradiated $1\times10^{16}\ n_{eq}/cm^2$:

efficiency still ≳ 99%

for HV ≳ 250 V

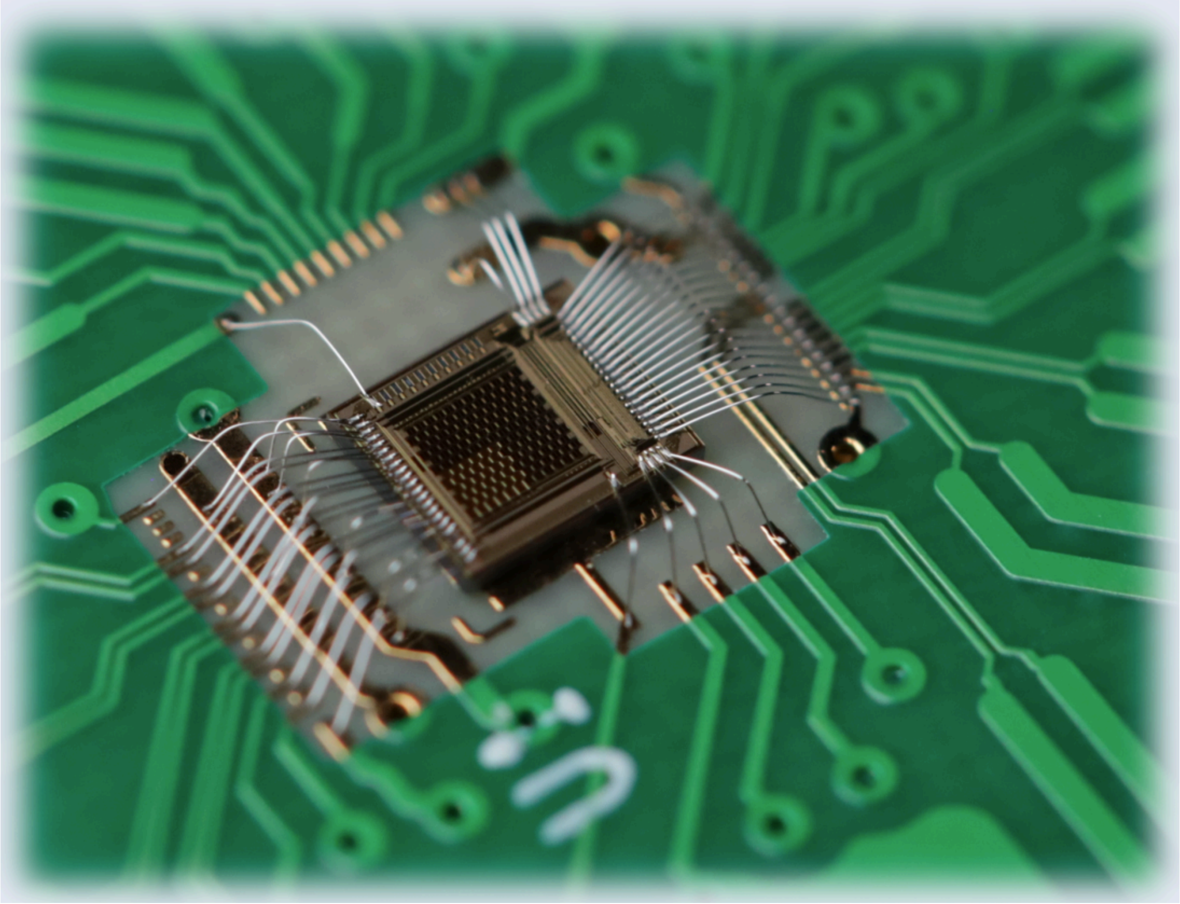
at 0.9 W/cm²



Summary

A monolithic prototype ASIC without gain produced in SiGe BiCMOS provided:

- **Efficiency of 99.8%** and **time resolution of 21 ps**
- **Laser** measurement: down to 2.5 ps.



After proton fluence of **10^{16} 1MeV n_{eq}/cm^2** :

- Increasing HV from 200 V to 325 V gives
  Efficiency up to 99.7 % and **time resolution of 40 ps**

This performance was obtained **without gain layer**

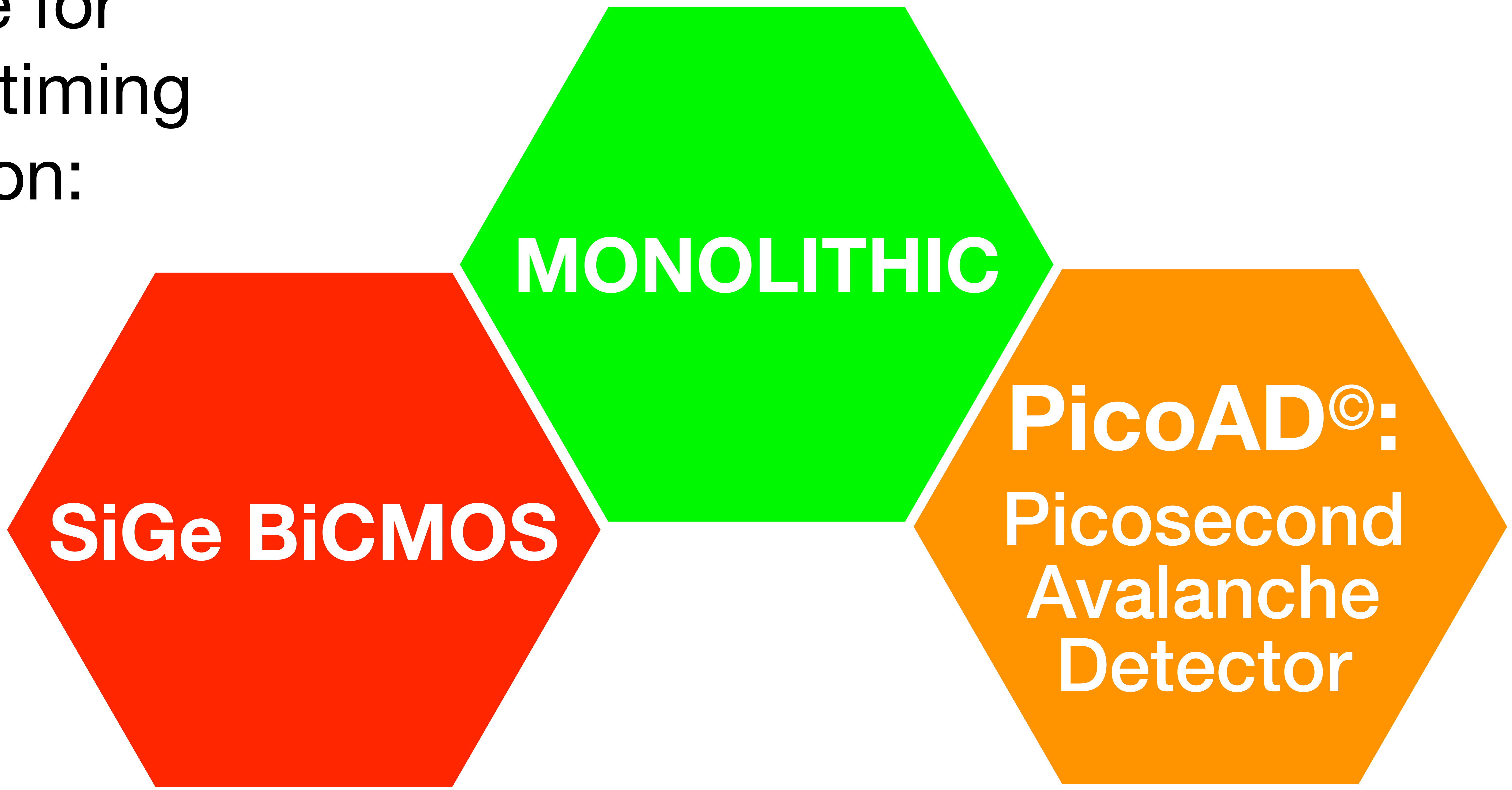
SiGe BiCMOS seems to be a serious candidate for future 4D trackers (and much more)

The MONOLITH Project

European Research Council
Established by the European Commission

Funded by the H2020 ERC Advanced grant 884447,
July 2020 - June 2025

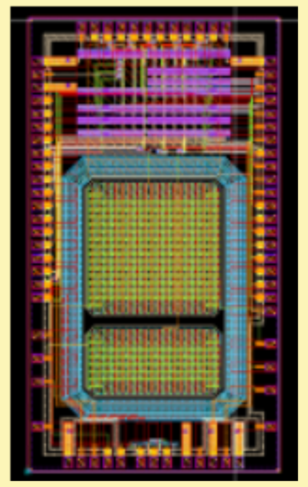
Our recipe for picosecond timing with silicon:



Monolithic SiGe BiCMOS for timing

Monolithic prototypes with SiGe BiCMOS (IHP 130nm SG13G2) **without** internal gain layer

2016

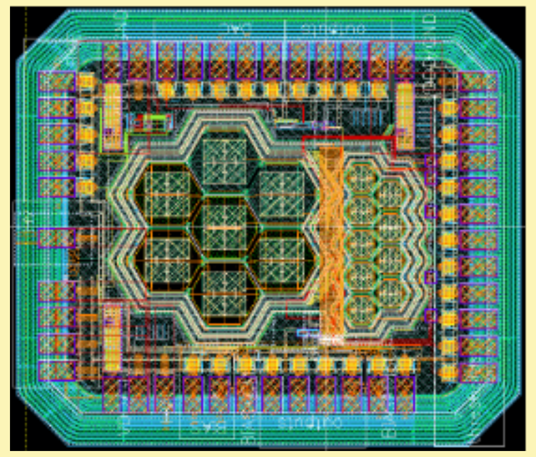


200ps
- 1 mm² pixel
- Discriminator

2017

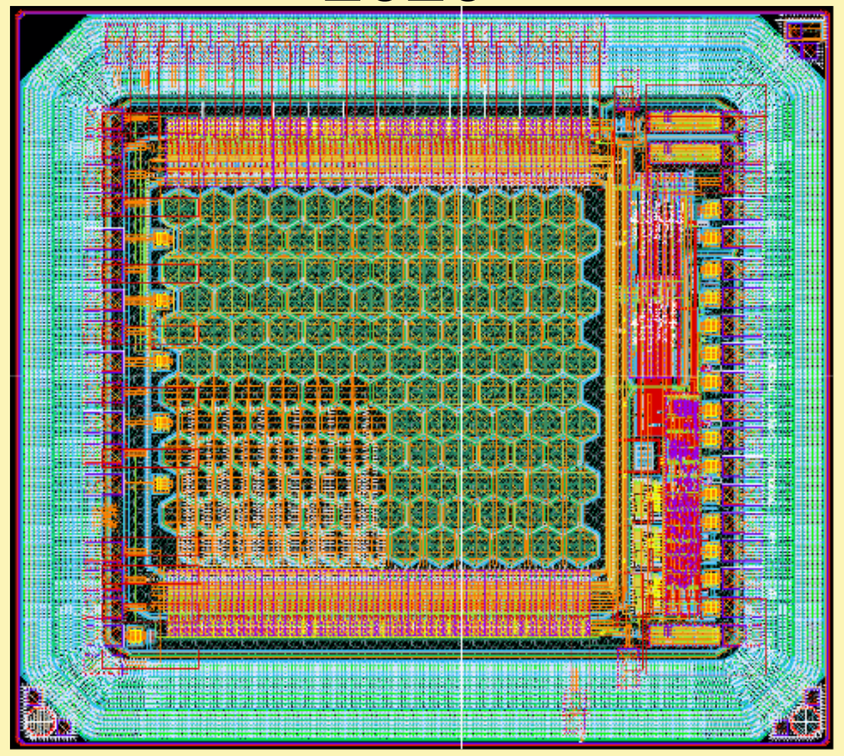
110ps
- 30 pixels 500x500μm²
- 100ps TDC +I/O logic

2018



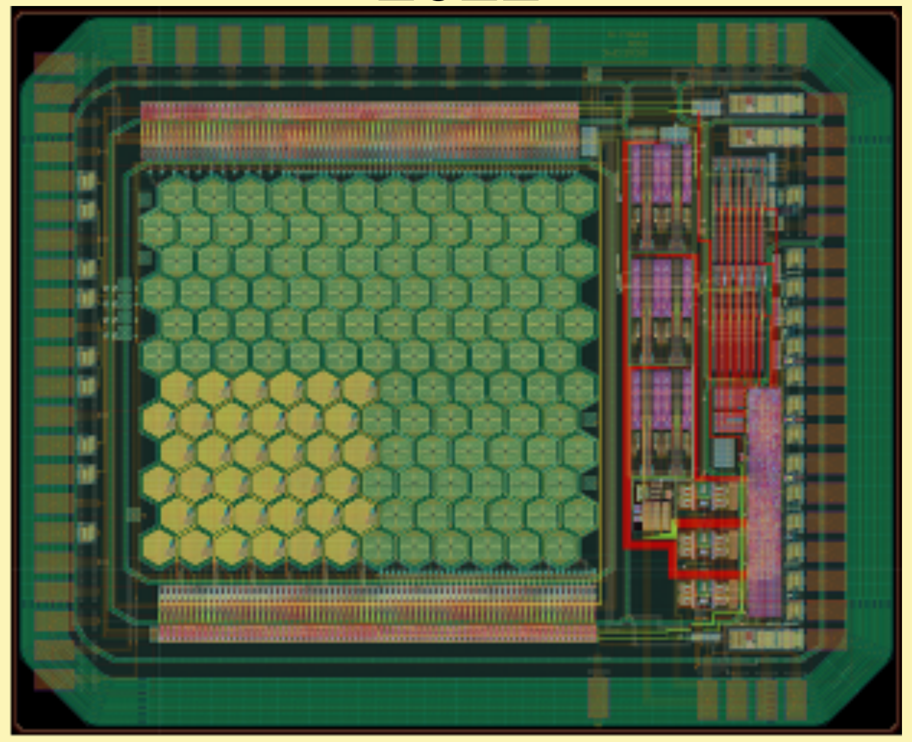
50ps
- Hexagonal pixels 100μm and 200μm pitch
- Discriminator output

MONOLITH prototype 1
2020



36 ps
- Hexagonal pixels 100μm pitch
- 30ps TDC +I/O logic
- Analog channels

MONOLITH prototype 2
2022



20 ps
- Hexagonal pixels 100μm pitch
- improved electronics
- 50μm epitaxial layer (350Ωcm)

In 2022 : **proof-of-concept**
monolithic prototype
with internal gain layer

(using 2020 masks)

PicoAD
special wafers
produced internally by IHP
(not optimised yet)

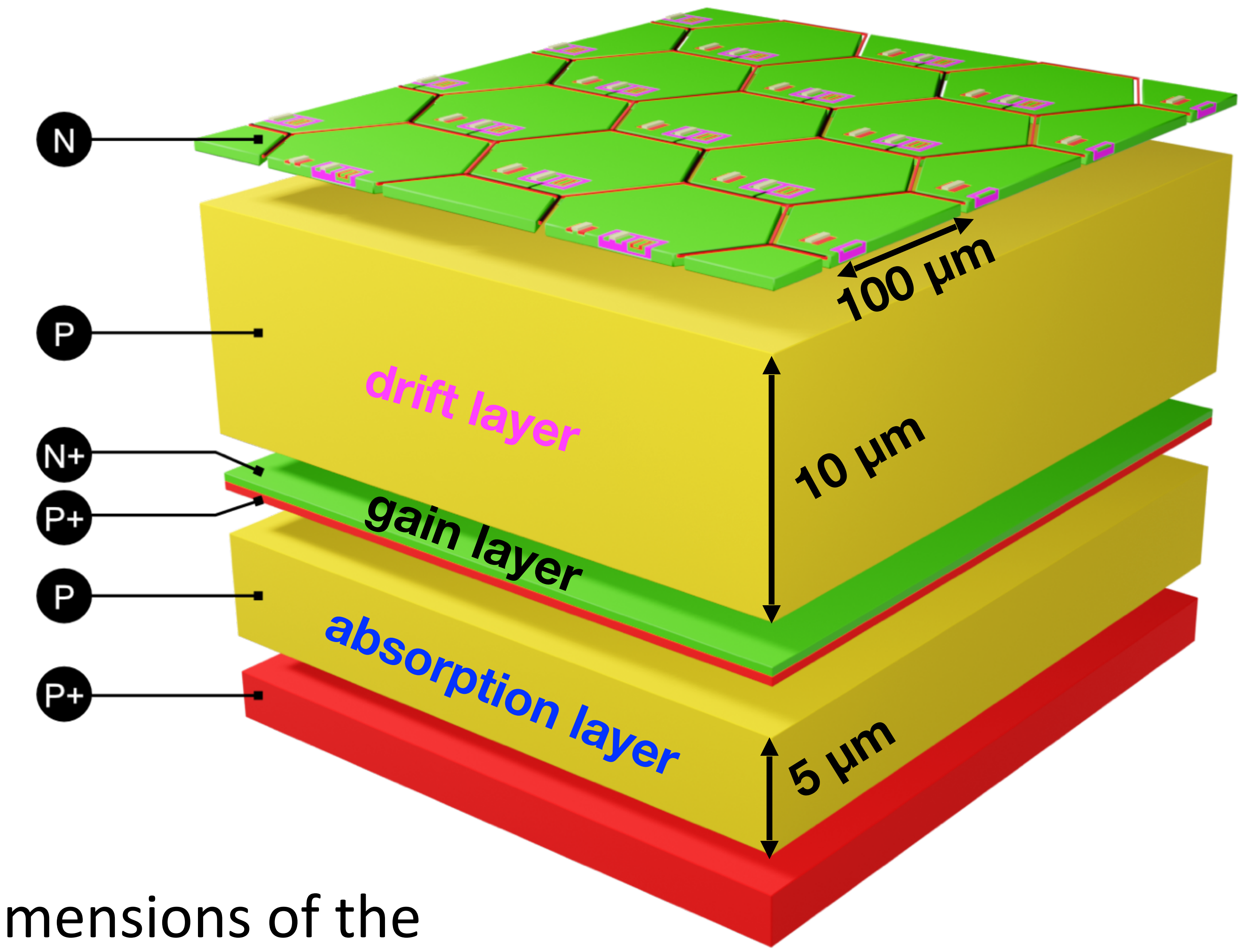
PicoAD Sensor Concept

© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector; European Patent EP3654376A1, US Patent US2021280734A1, Nov 2018

PicoAD:

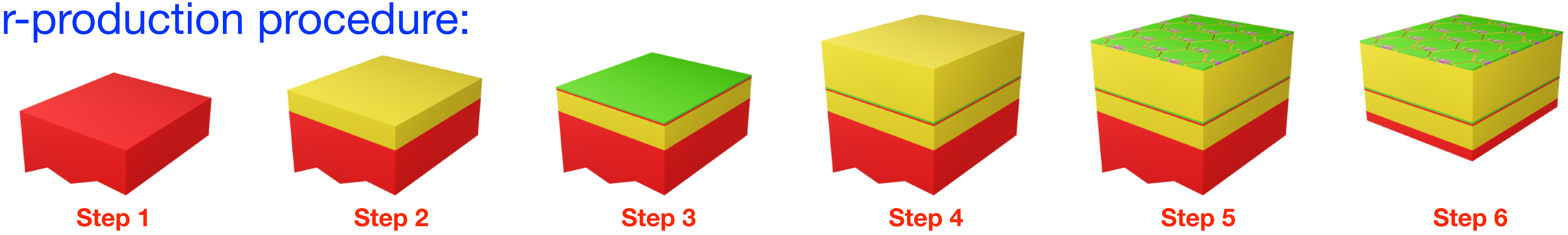
Multi-Junction Picosecond-Avalanche Detector© with continuous and deep gain layer:

- De-correlation from implant size/geometry
  ➞ **high pixel granularity and full fill factor**
  (high spatial resolution and efficiency)
- Only small fraction of charge gets amplified
  ➞ **reduced charge-collection (Landau) noise**
  (enhance timing resolution)



Dimensions of the proof-of-concept prototype (not optimised for timing)

Wafer-production procedure:



PicoAD p.o.c.: Gain with ^{55}Fe source

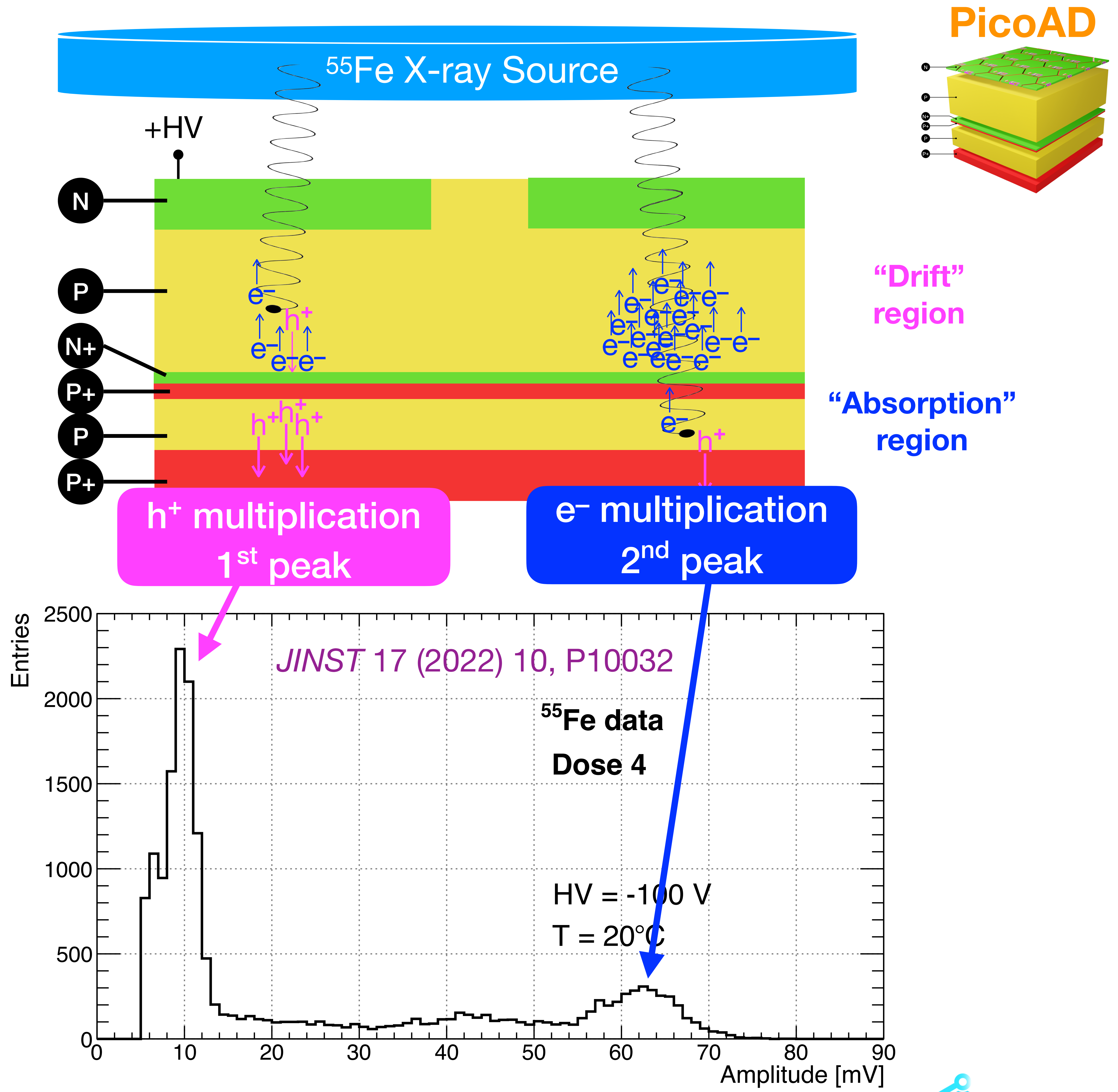
X-rays from ^{55}Fe radioactive source:

- mainly ~5.9 keV photons
- point-like charge deposition

We found a double-peak spectrum

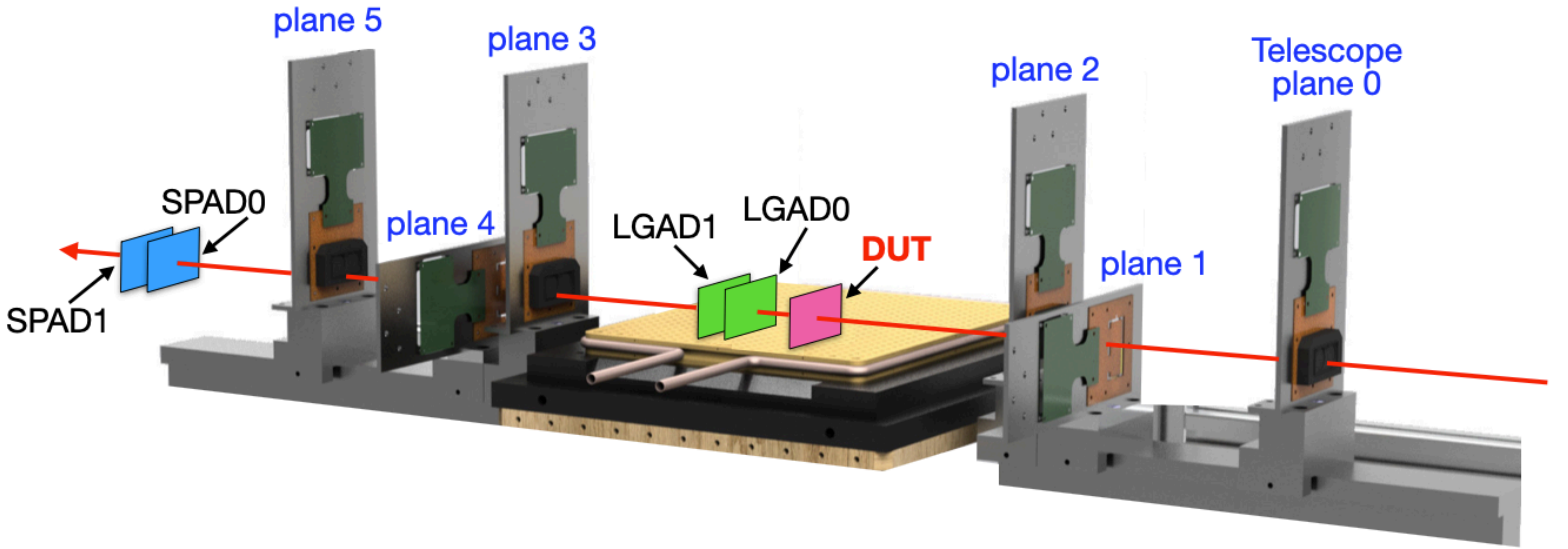
- photon absorbed in **drift region**
  - ➡ **holes** drift through gain layer & multiplied
  - ➡ **first peak** in the spectrum
- photon absorbed in **absorption region**
  - ➡ **electrons** through gain layer & multiplied
  - ➡ **second peak** in the spectrum

Gain measured: ~20 for ^{55}Fe
(corresponding to ~60 for a m.i.p.)



Test Beam: Experimental Setup

CERN SPS Testbeam with 180 GeV/c pions to measure **efficiency** and **time resolution**

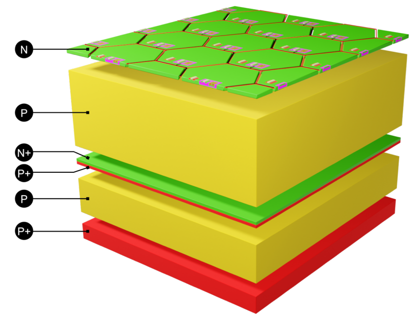


UNIGE FE-I4 telescope to provide spatial information ($\sigma_{x,y} \approx$10 μm)

Two LGADs ($\sigma_t \approx$35 ps) to provide the timing reference (and **two SPADs** with $\sigma_t \approx$20 ps)

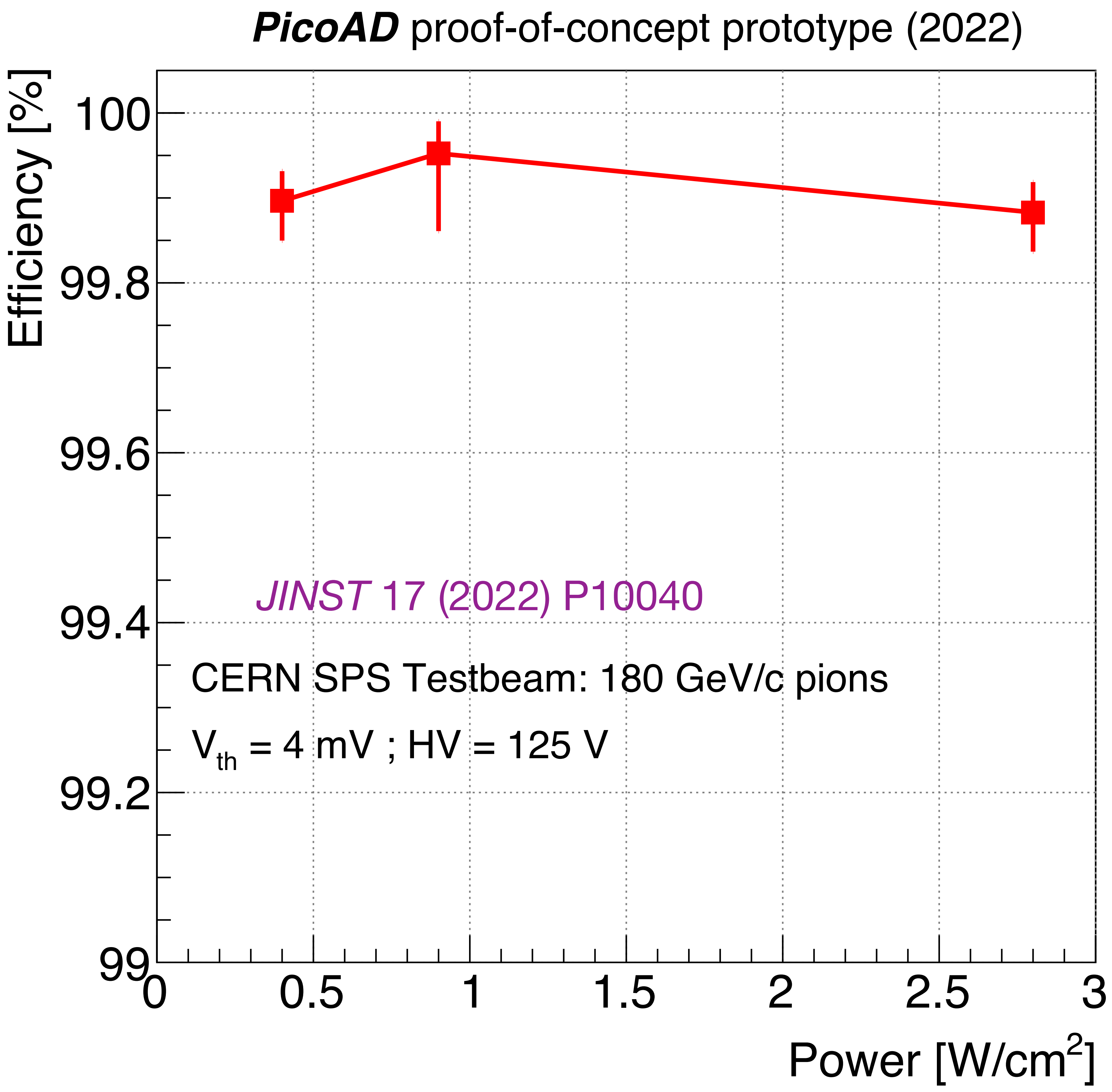
Testbeam PicoAD p.o.c.: Detection Efficiency

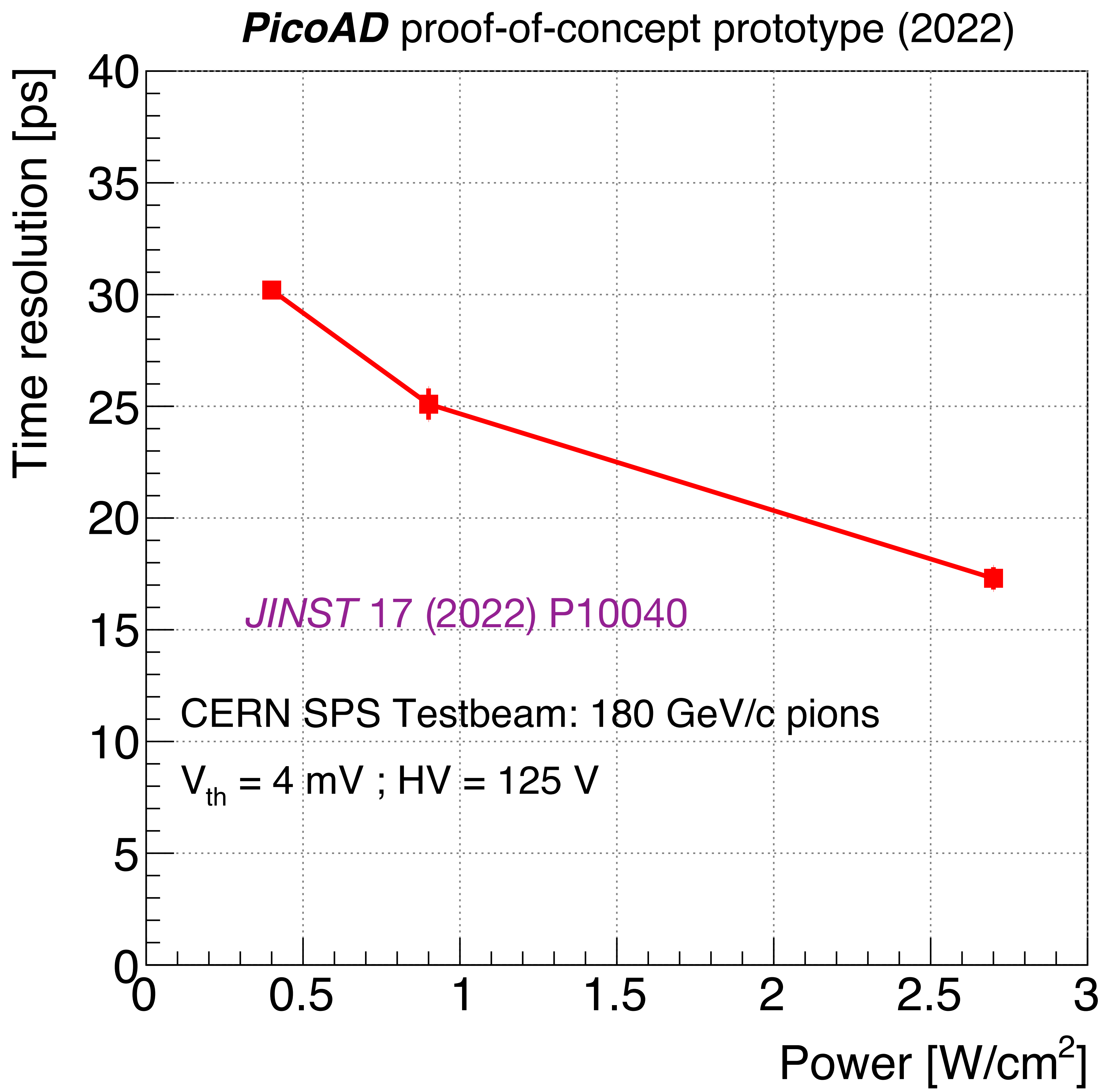
PicoAD



17 ps at **2.7 W/cm²**
30 ps at **0.4 W/cm²**

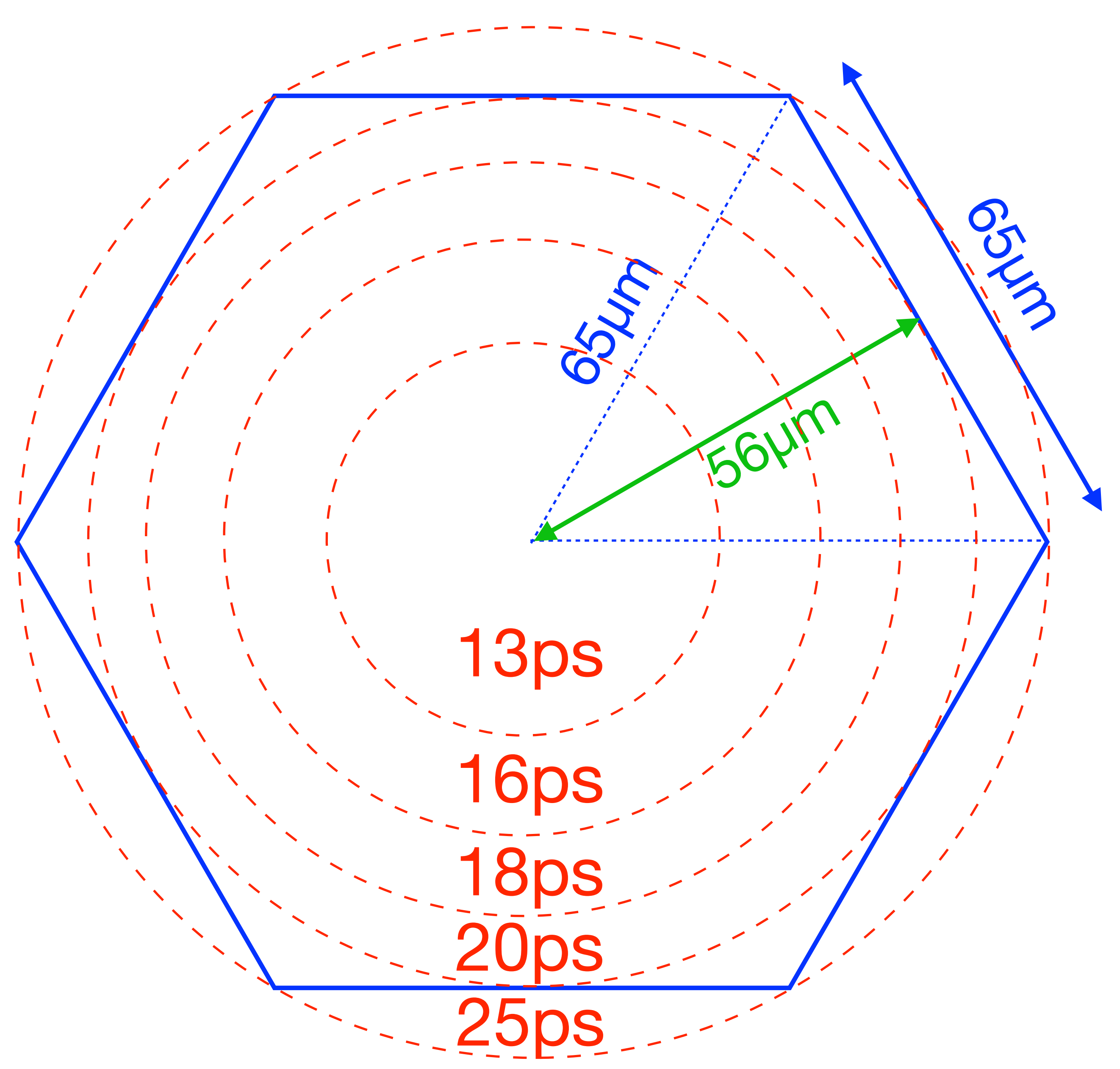
99.9% for all power consumptions





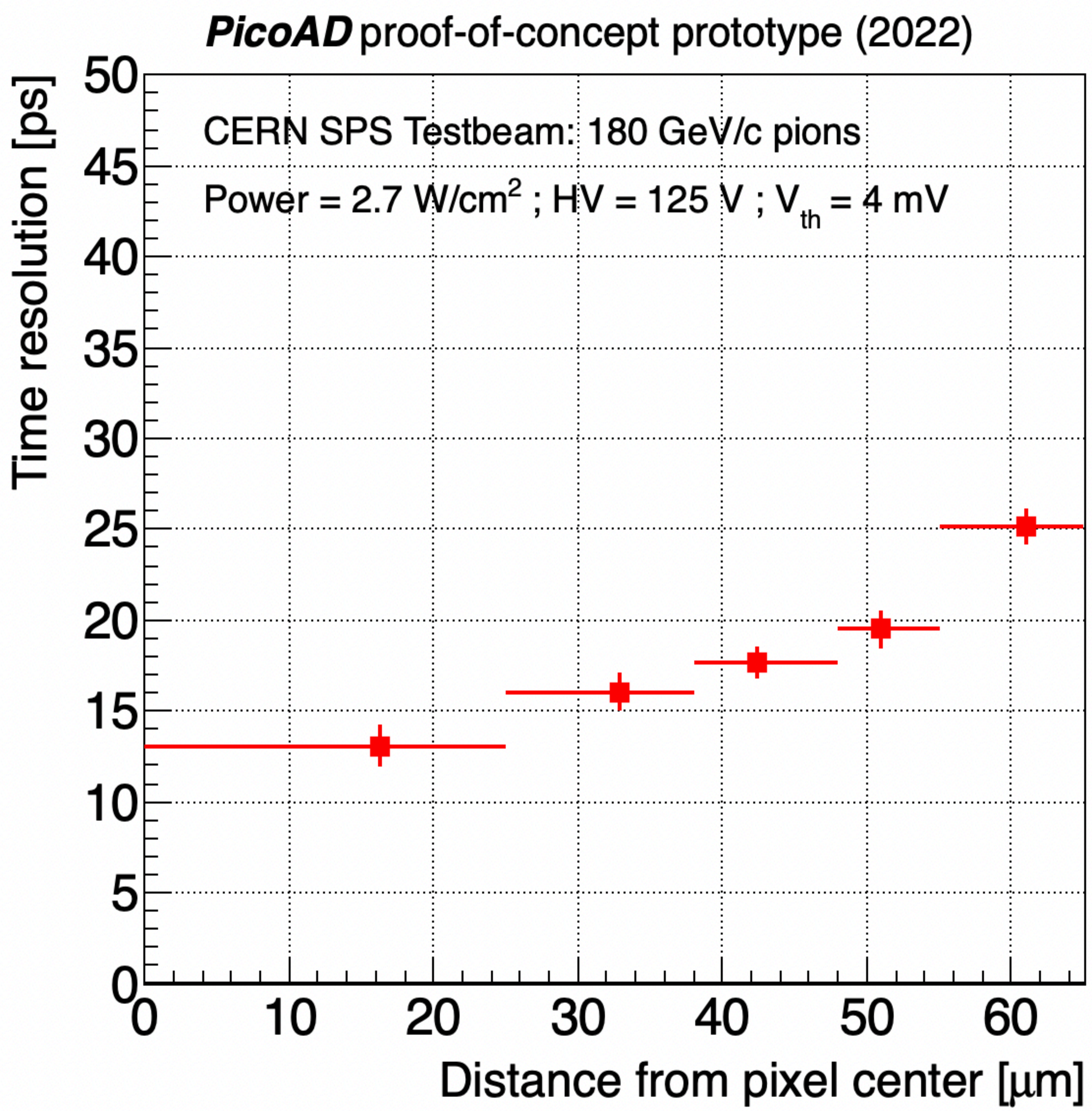
Testbeam PicoAD p.o.c.: Time Resolution

Pixel surface divided in 5 radial areas:



Time resolutions: **13 ps** at the pixel center
25 ps at the pixel edge

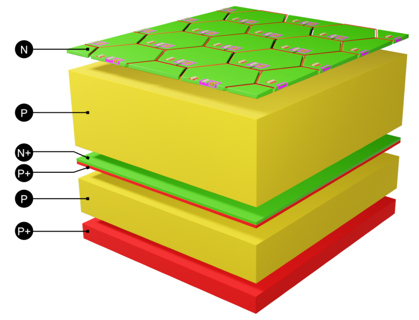
To be improved in future prototypes.



PicoAD

PicoAD p.o.c. — Summary & Outlook

PicoAD



The PicoAD© sensor works (*JINST* 17 (2022) 10 P10032 ; *JINST* 17 (2022) 17 P10040)

Testbeam of the monolithic proof-of-concept ASIC provided:

- **Efficiency = 99.9 %** including inter-pixel regions
- **Time resolution σ_t = (17.3 ± 0.4) ps**
  13 ps at center and **25 ps** at pixel edge
  (although sensor not yet optimized for timing)

New PicoAD prototypes optimised for timing back from foundry in **October 2023**

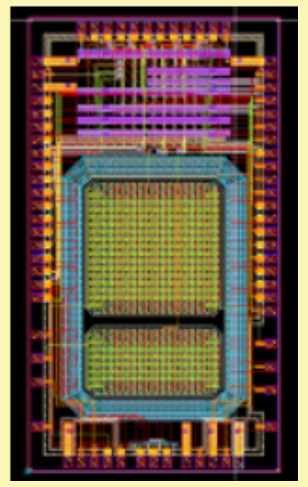
Deliverable of MONOLITH ERC project:

- Full-reticle monolithic ASIC in **Summer 2025** with 50μm pitch and 10ps timing

MONOLITH Project: outlook

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

2016

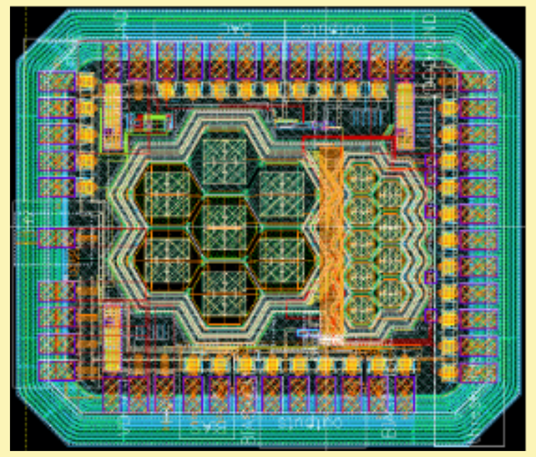


200ps
- 1 mm^2 pixel
- Discriminator

2017

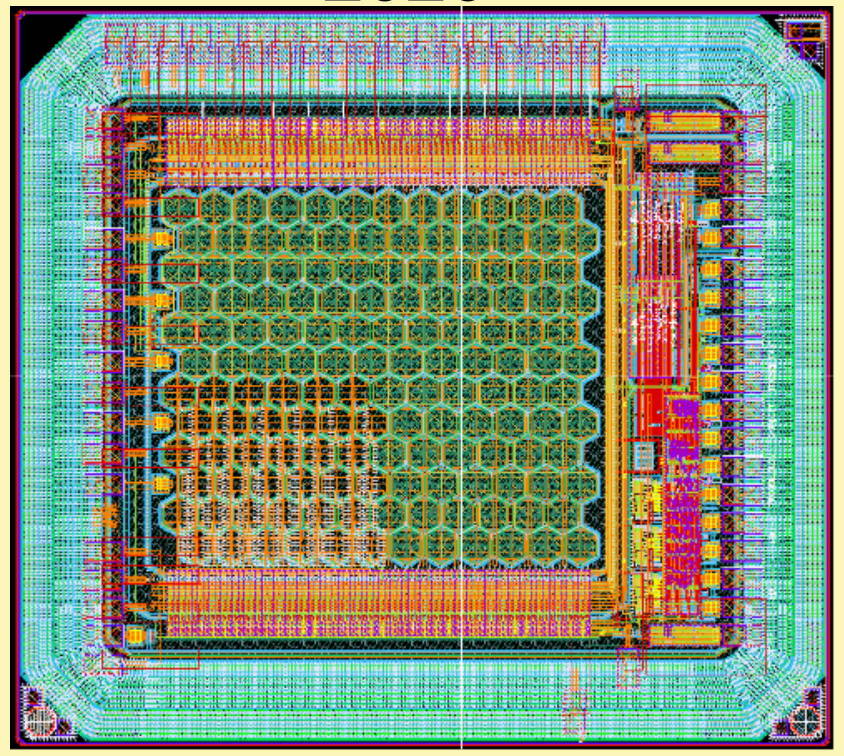
110ps
- 30 pixels 500x500µm^2
- 100ps TDC +I/O logic

2018



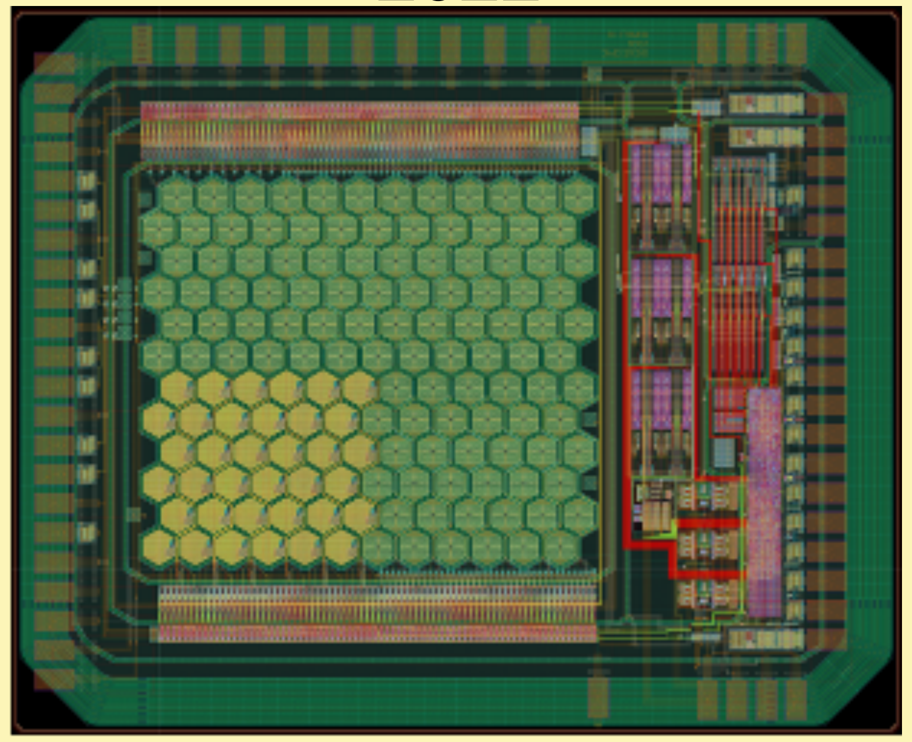
50ps
- Hexagonal pixels 100µm and 200µm pitch
- Discriminator output

MONOLITH prototype 1
2020



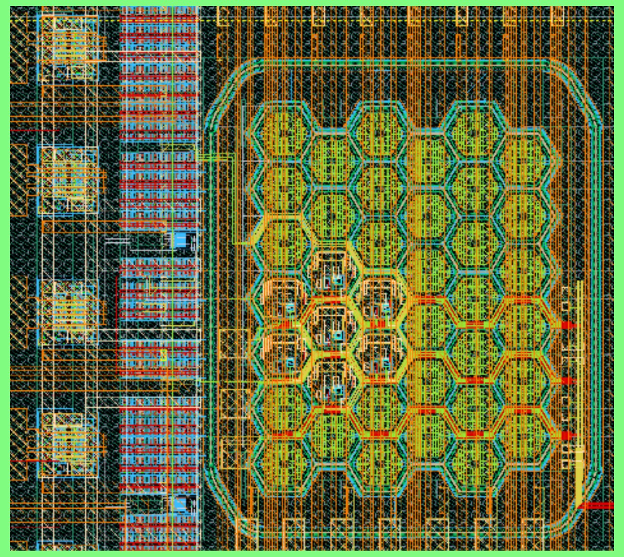
36 ps
- Hexagonal p…ls 100µm pitch
- 30ps TDC …ogic
- Analog cha…

MONOLITH prototype 2
2022



20 ps
- Hexagonal p…s 100µm pitch
- improved e…nics
- 50µm epita…yer (350Ωcm)

MONOLITH prototype 3
2023



- Hexagonal pixels **40µm pitch**
- improved electronics (4 times less power c…mption)

Monolithic prototypes
with internal gain layer:

PicoAD version (proof-of-concept) **17 ps**

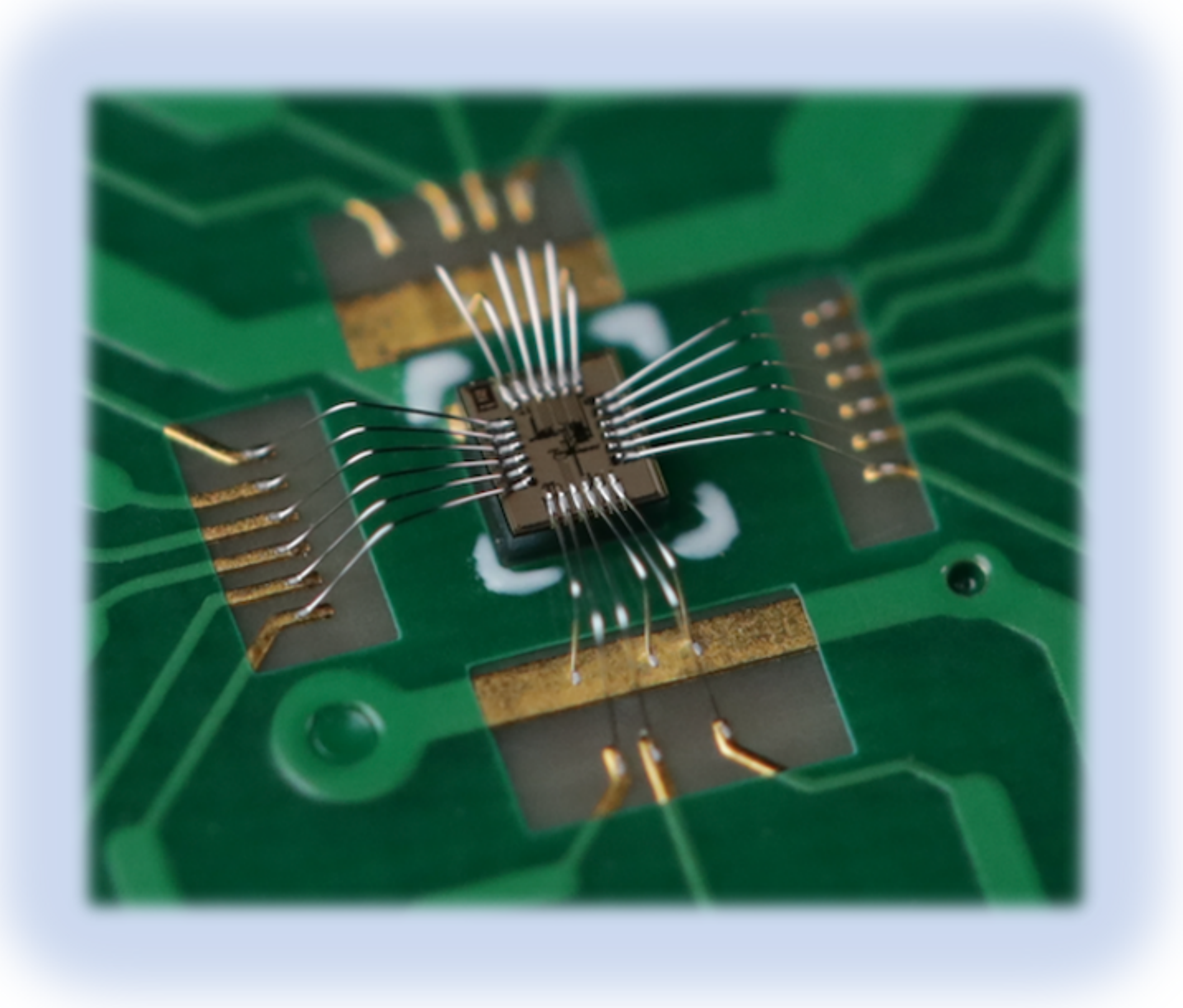
PicoAD version **in production** (back: **Oct. 2023**)

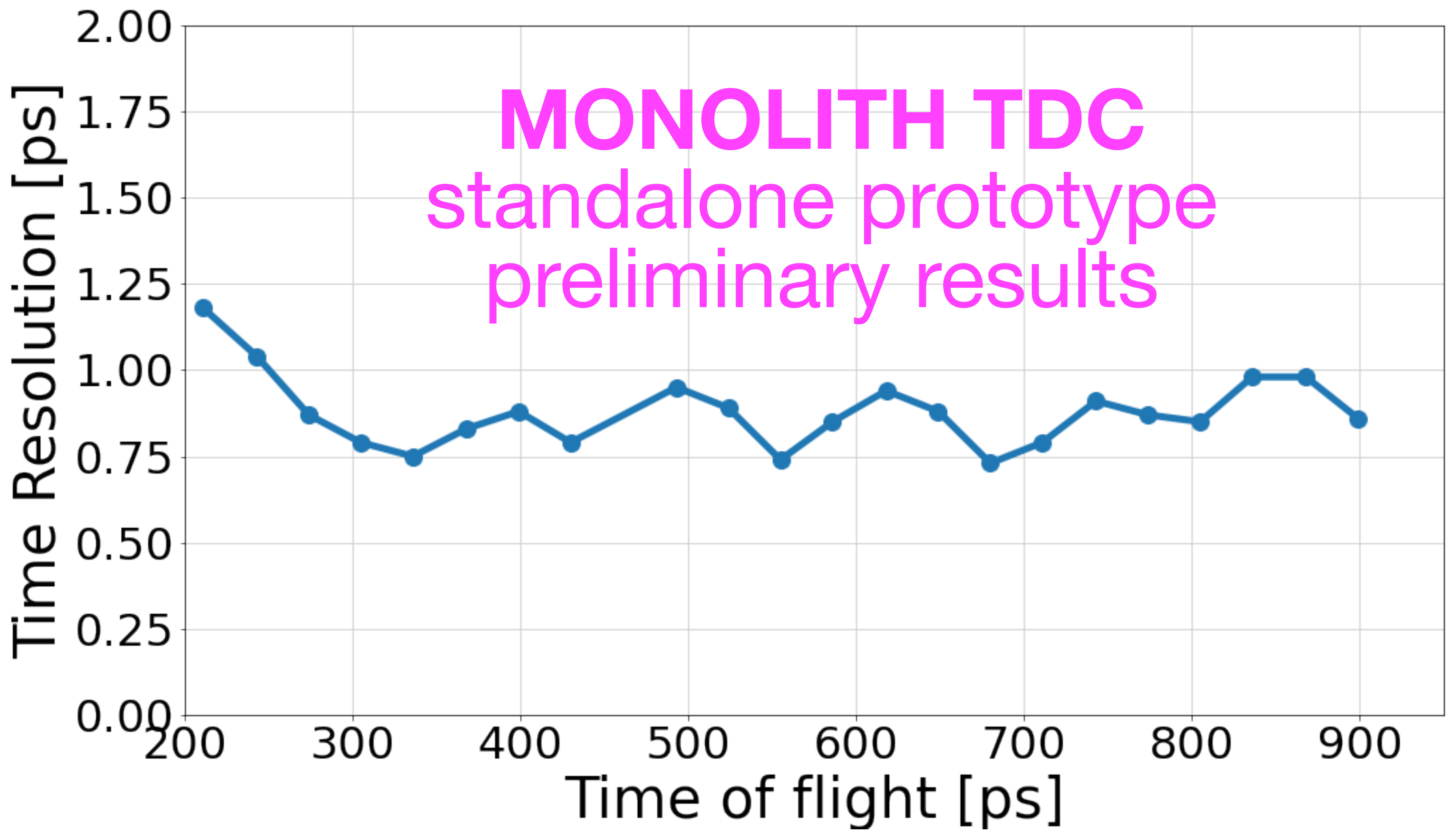
PicoAD version expected **Summer 2024**

MONOLITH sub-picosecond TDC

We are developing a sub-picosecond TDC based on a novel design (our patent© & more):

© R. Cardarelli, L. Paolozzi, P. Valerio and G. Iacobucci, European Patent Application / Filing - UGKP-P-001-EP, Europe Patent EP 18181123.3. 2 July 2018.





It was integrated in MONOLITH 2022 prototype2 ASIC