

The LHCb VELO Upgrade II: design and development of the readout electronics

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In order to fully exploit the High-Luminosity LHC potential in flavour physics, the LHCb collaboration proposes a Phase-II Upgrade of the detector, to be installed during the LHC Long Shutdown 4 (2032-2034). Operating in the HL-LHC environment poses significant challenges to the design of the upgraded detector, and in particular to its tracking system. The primary and secondary vertices reconstruction will become more difficult due to the increase, by a factor 8, of the average number of interactions per bunch crossing (pile-up). Similarly, the track reconstruction will become more challenging, as well as time-consuming, because of the large increase in the track multiplicity. Finally, the much harsher radiation environment will make the design of the sub systems quite challenging, with the radiation damage expected to be more severe for most detectors. In particular, the performance of the VERtex LOcator (VELO), which is the tracking detector surrounding the interaction region, is essential to the success of this Phase-II Upgrade. Data rates are especially critical for the LHCb full software trigger, and with the expected higher particle flux, the VELO Upgrade-II detector will have to tolerate a dramatically increased data rate: assuming the same hybrid pixel design and detector geometry, the front-end electronics (ASICs) of the VELO Upgrade-II will have to cope with rates as high as 8 Ghits/s, with the hottest pixels reaching up to 500 khits/s. With this input rate, the data output from the VELO will exceed 30 Tbit/s, with potentially a further increase if more information is added to the read-out. The VELO collaboration is currently exploring new sensor technologies, and the benefits that would derive from adding a time stamp to the track reconstruction, such that interactions in the same bunch crossing can be more effectively disentangled. Recently, the implementation of precise (~ 50 ps) time measurement in combination with excellent spatial resolution has become technologically possible. Moreover, the VELO case is extremely challenging, as the high granularity required for the spatial measurement severely limits the area in each pixel of the ASIC where the time-stamping circuitry can be implemented. Achieving a hit resolution of 50 ps per pixel is considered possible within the timescale of the Phase-II Upgrade. With such resolution, each VELO track would have multiple time measurements from the traversed pixels, which will lead to a precise estimation of the production time of charged particles. Moreover, at the hit level, a precise timing information will also help reducing the number of possible combinations to be considered for the track reconstruction, thus improving its quality. The most recent advances in this field, and the potential candidates that can meet the VELO Upgrade-II requirements, will be presented. In particular, the current state-of-the-art prototypes in the development of ASICs with TDC-per-pixel architecture, the PicoPix ASIC (which is an evolution of the Timepix4 design [3]) and the TIMESPOT ASIC [4], will be discussed. The most recent studies carried out on these two candidates will be presented, as well as the last results from simulations.

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