Stitched Passive CMOS Strip Sensors

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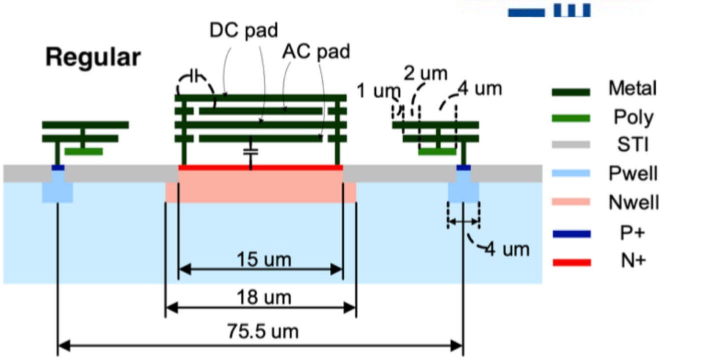
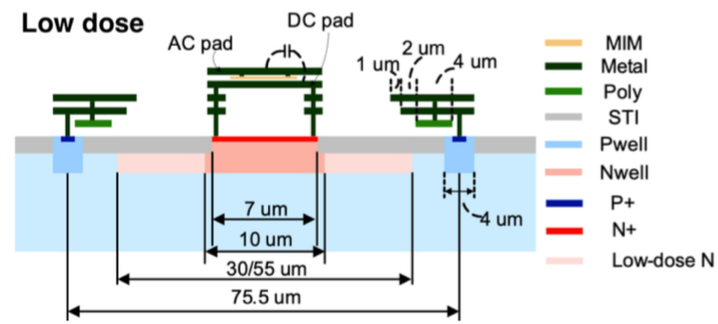
Introduction

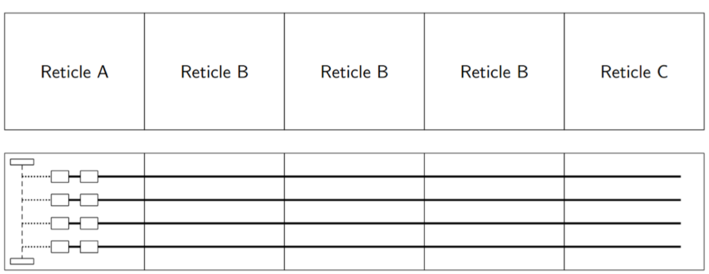
- Current experiments largely rely on silicon particle sensors from very small number of vendors
- CMOS widely seen as the new detector technology
  - Many vendors, monolithic sensors, small feature size, high resolution, cost savings….
- CMOS sensors are key R&D topic in RD50 and DRD3
- Vast majority of silicon area in LHC-Phase-II trackers covered by strip sensors
  - ATLAS ITk example: 13 m^2 pixels, 165 m^2 strips
- Strip sensors are 'large': typically one sensor per 6" wafer
  - Strip lengths around 2-5 cm, with sensors around 100cm^2
- This project aims to develop CMOS strip sensors, i.e. sensors able to cover the large areas
- Today: simulations, and results from lab tests and test beam campaigns

The Sensors

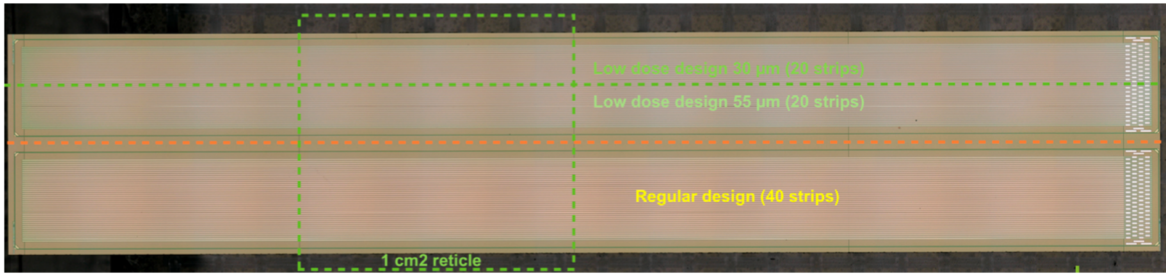
- Typical CMOS reticle size adapted to industrial chips (1-2cm^2), far too small for strip sensors
- Connect several reticles to obtain desired strip length: **stitching**
- LFoundry 150nm process, wafer thickness 150 µm, 75µm strip pitch. Passive sensors, backside treatment by IZM Berlin
- 3 different designs in each sensor: regular, low dose 33, low dose 55
- Strip lengths 2.1 cm and 4.2 cm (3 and 5 stitches)
- We simulate and characterise sensors, then turn sensors into test modules and evaluate their performance before and after irradiation
- Stitched regions in focus: look for stitching effects







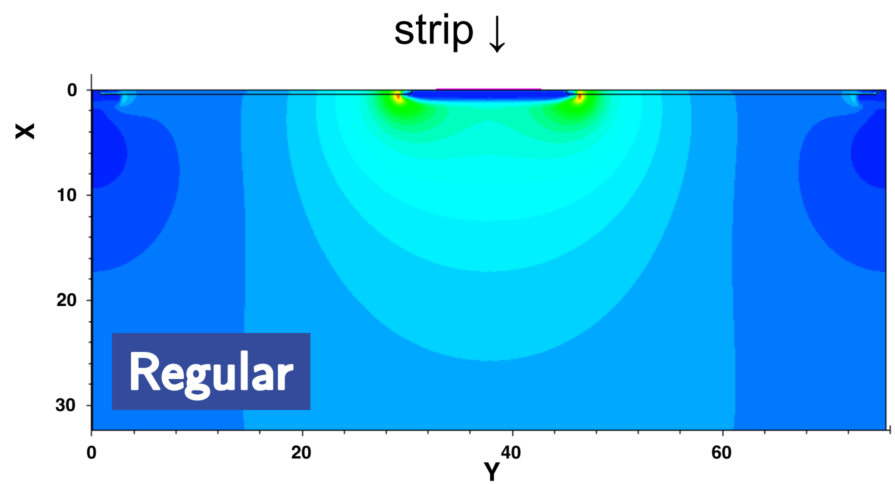
Sensor Schematic

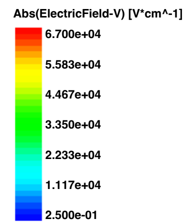


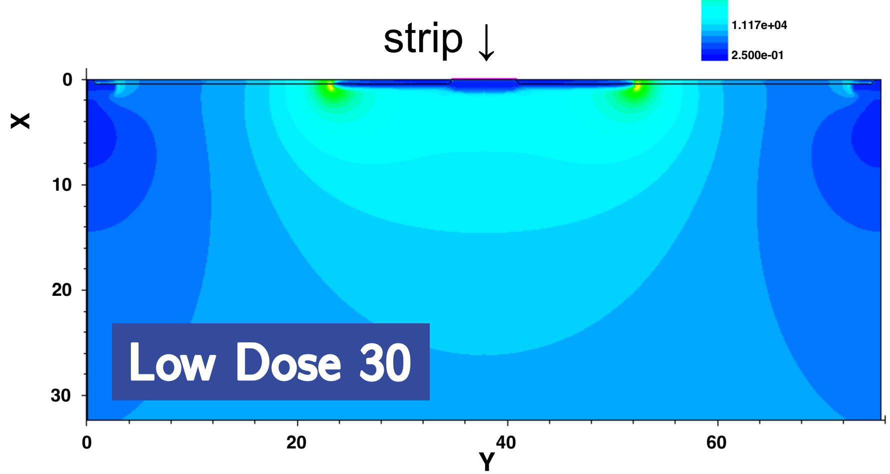
Sensor with 4.2 cm length in reality

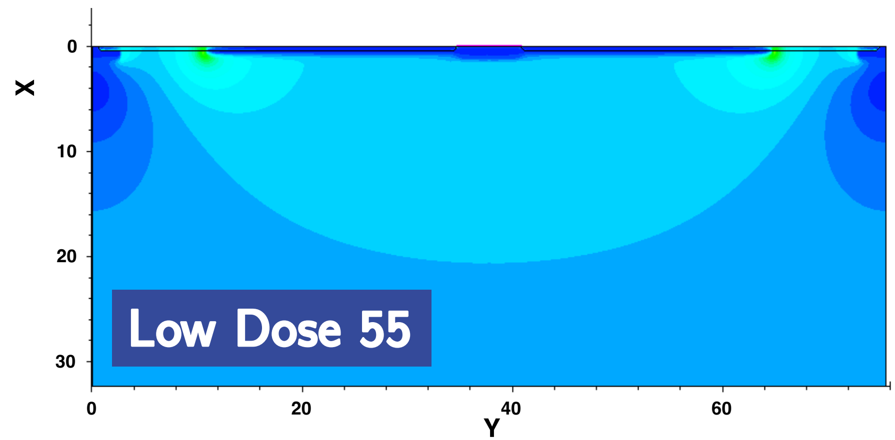
Electric Field Simulations

- All 3 designs simulated in detail
- Regular design vaguely based on ATLAS ITk strip sensor layouts
- Example: Electric field near surface in unit cell around one strip
- Design differences visible in E-field
- Simulations show no design flaws
- Stitches not simulated



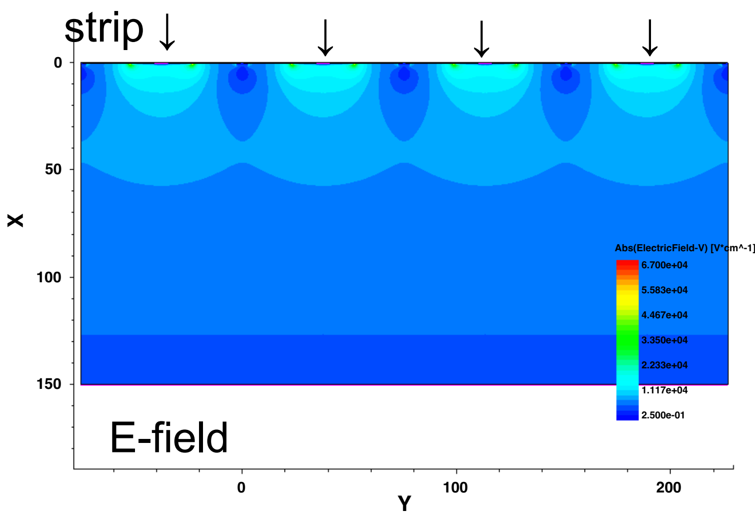


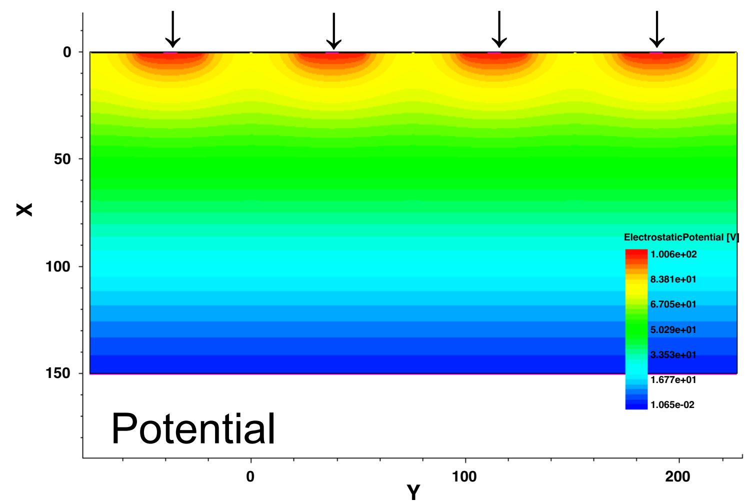




Four-Strip Simulations

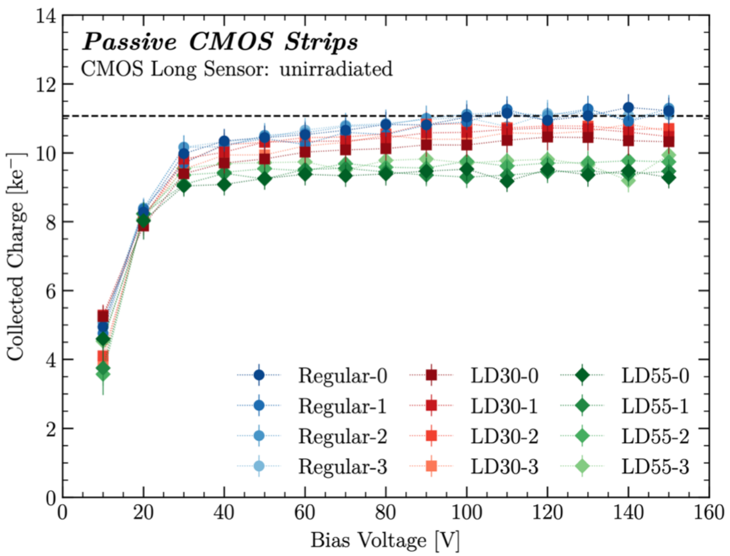
- CMOS sensors also simulated as four-strip structures
- Example: field and potential of low dose 30 at 100V
- Fields look reasonable
- We are also working on simulations of signal collection (using Allpix^2) but not finalised yet

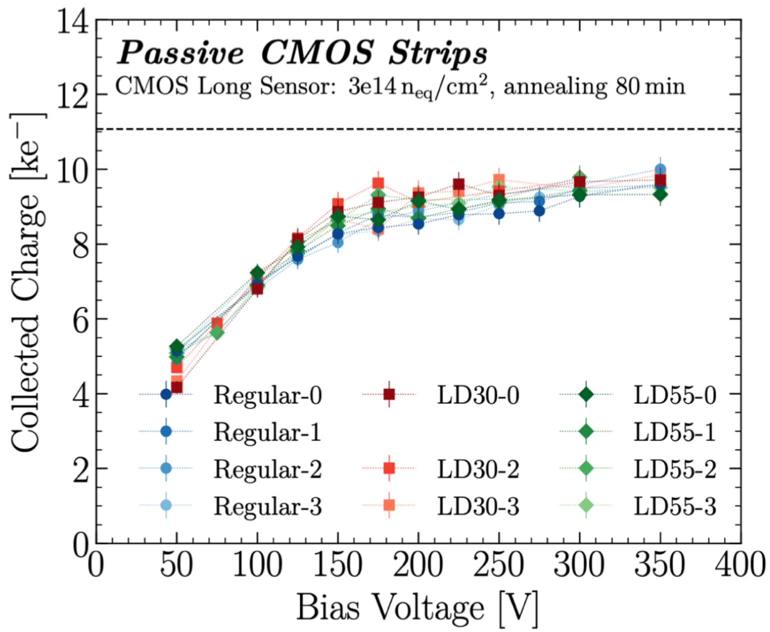


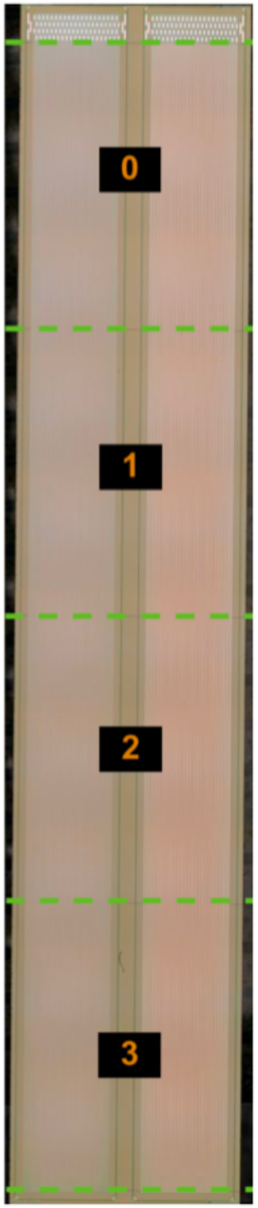


Lab Test Results with Particles

- Lab tests with Sr90-source based setup (ALiBaVa)
- Measuring collected charge as function of bias voltage for all designs and stitches
- Source is collimated to test only one reticle at a time
- **Results**:
- Designs perform slightly different
- No differences between the four stitches
- Neutron irradiation to $3x10^{14}n_{eq}$ reduces the charge for all designs, but for every design (and dose) stitches still behave the same







Results from 2D TCT Scans

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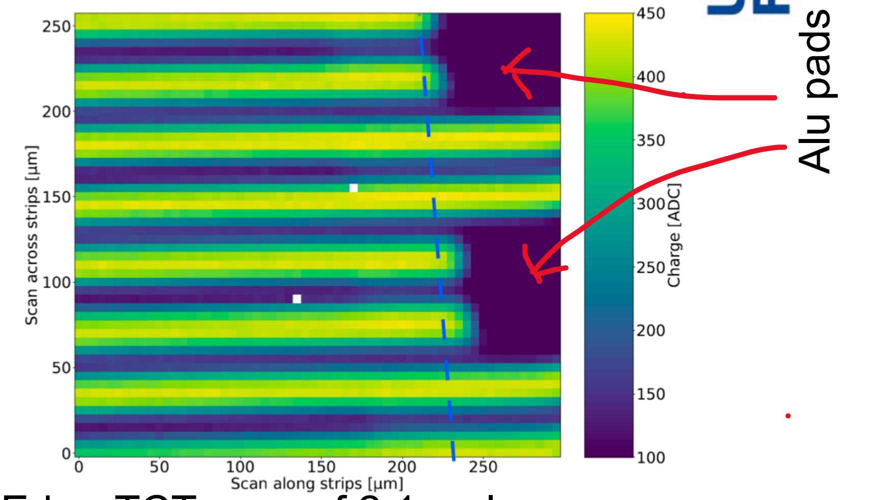
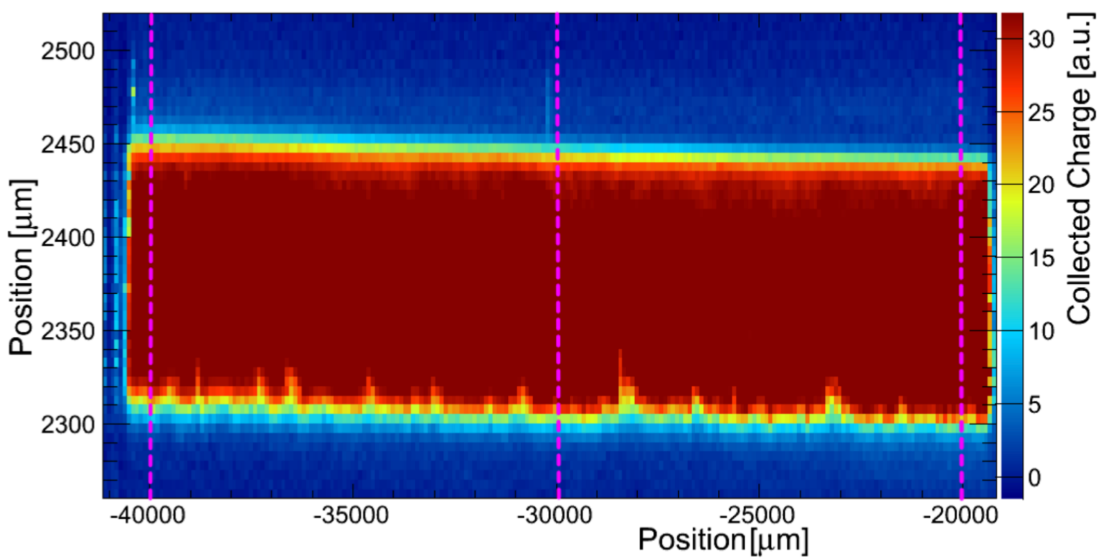
- Transient current technique (TCT) scans with focussed IR laser spot. Measure collected charge at X,Y
- Top-TCT scan of stitch region near strip bond pads
- Edge-TCT of one entire 2.1cm long sensor with 3 stitches
- Charge collection always homogenous in stitch regions

[stichtes indicated as dashed lines]

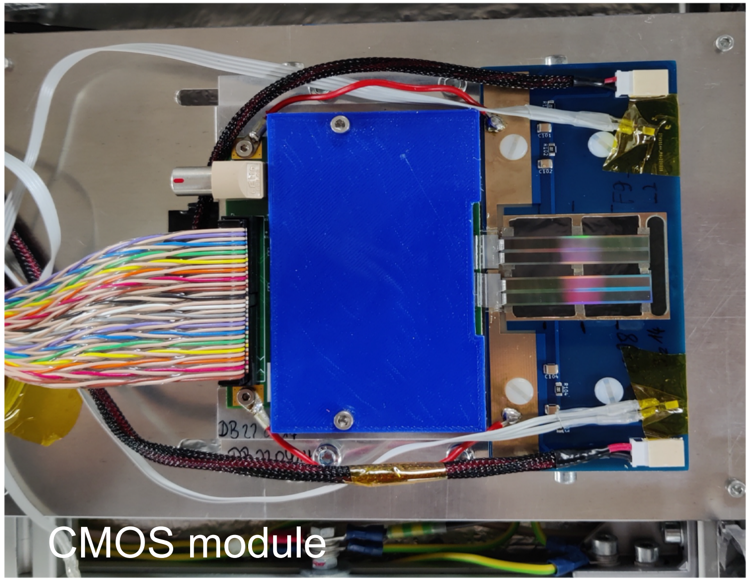
Top-TCT scan of stitch near bond pad



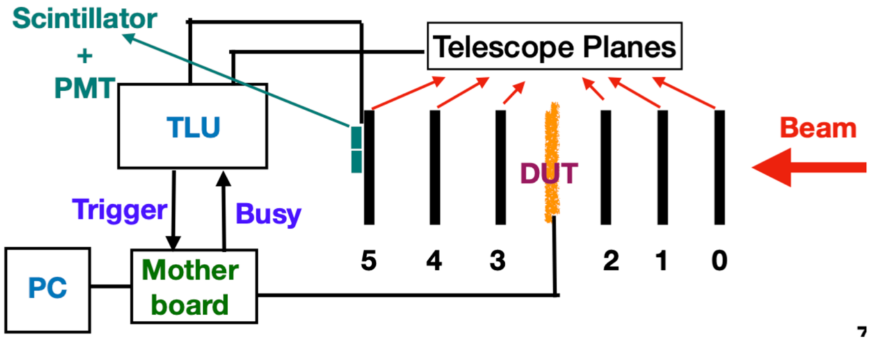
Edge-TCT scan of 2.1cm long sensor



And Now for Something Completely different: **Testbeam**



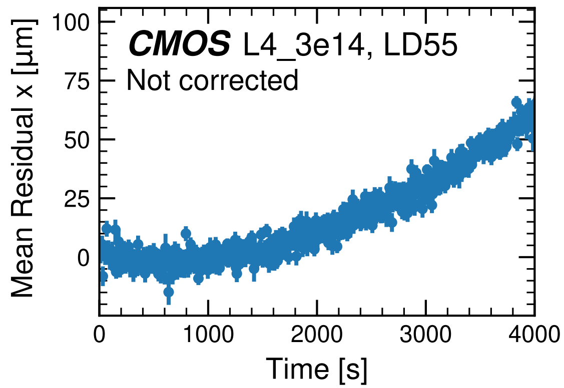
- CMOS strip modules also tested in two testbeam campaigns at DESY (3.4 and 4.2 GeV electrons)
- EUDET-Telescope with 6 ALPIDE-based planes
- Device Under Test (DUT) at centre of beam telescope
- Timing plane added in 2nd testbeam

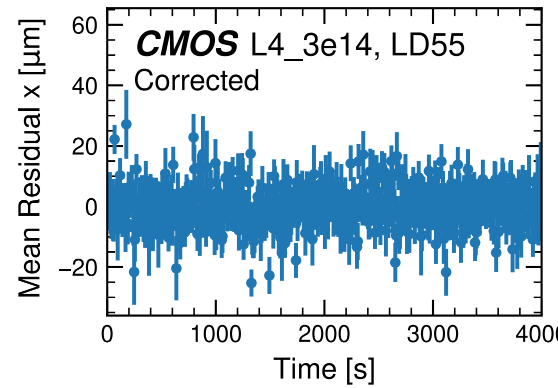


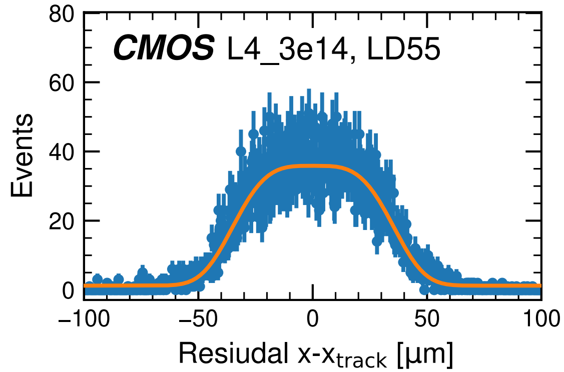
Results from Testbeam I

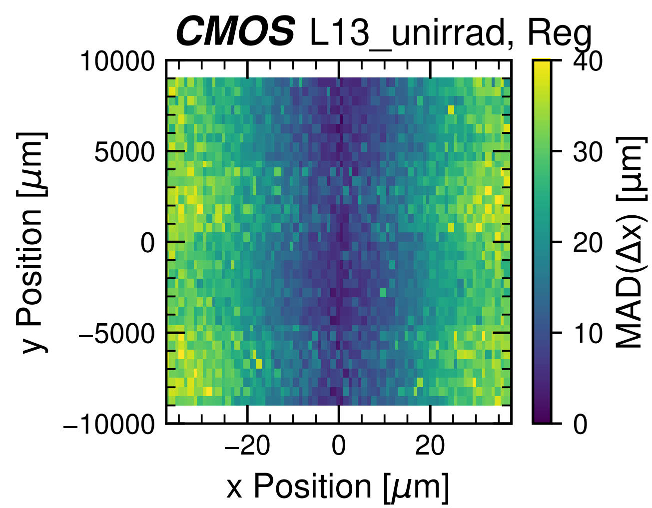
- DUT box cooled with dry ice which evaporates during run, reducing weight of box
- DUT moves by tens of µm as result
- Resolution needs time-dependent correction
- Once applied, CMOS sensors reach expected resolution

- 2D resolution map of unit cell (entire sensor folded onto one strip) allows looking at stitching effects -> None found









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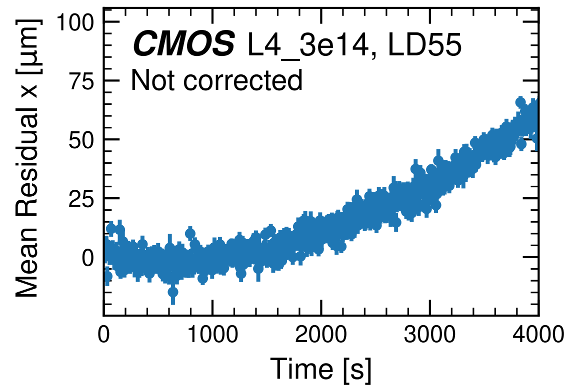
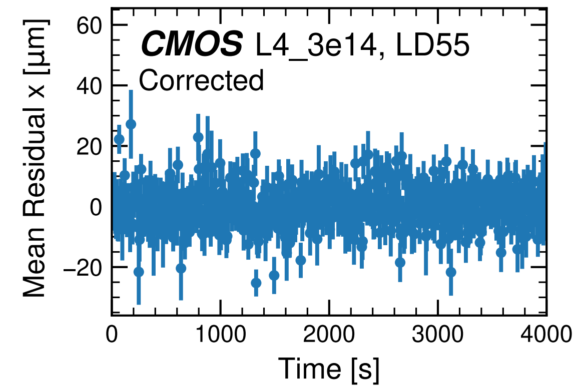
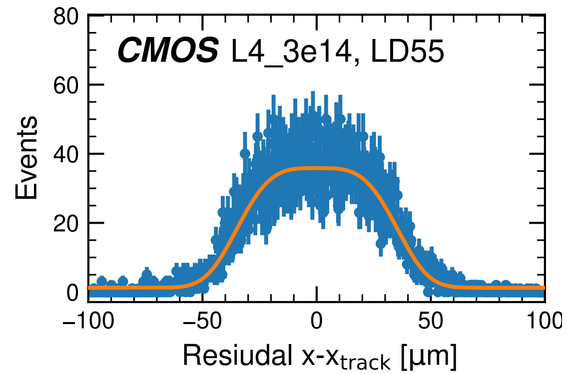
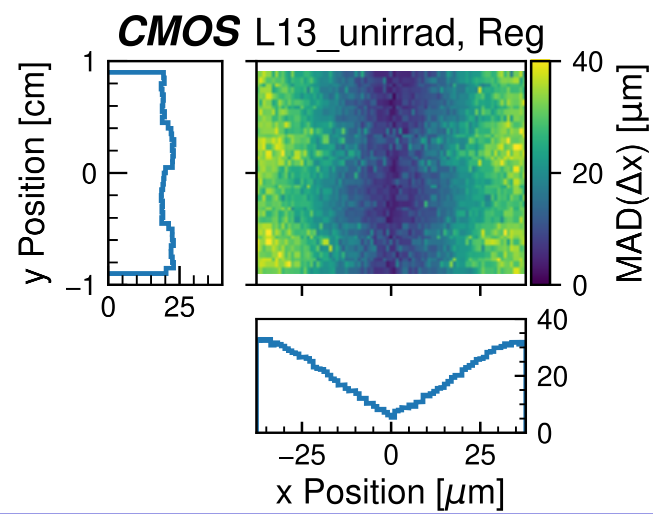


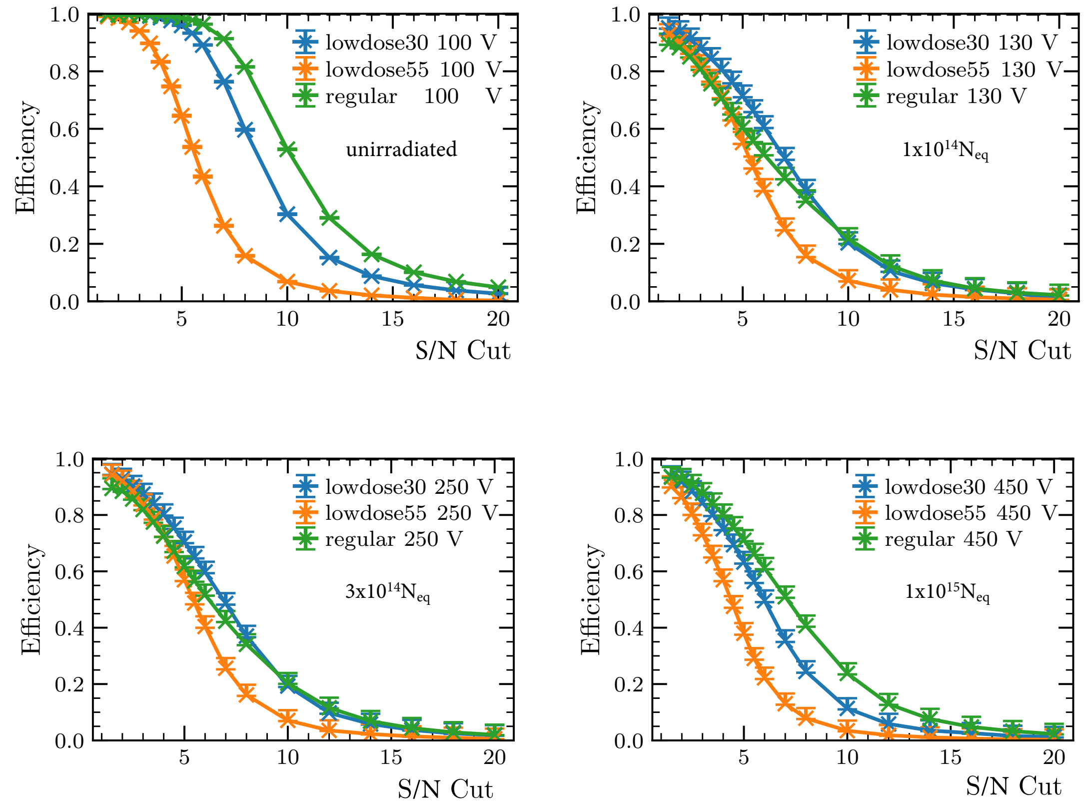






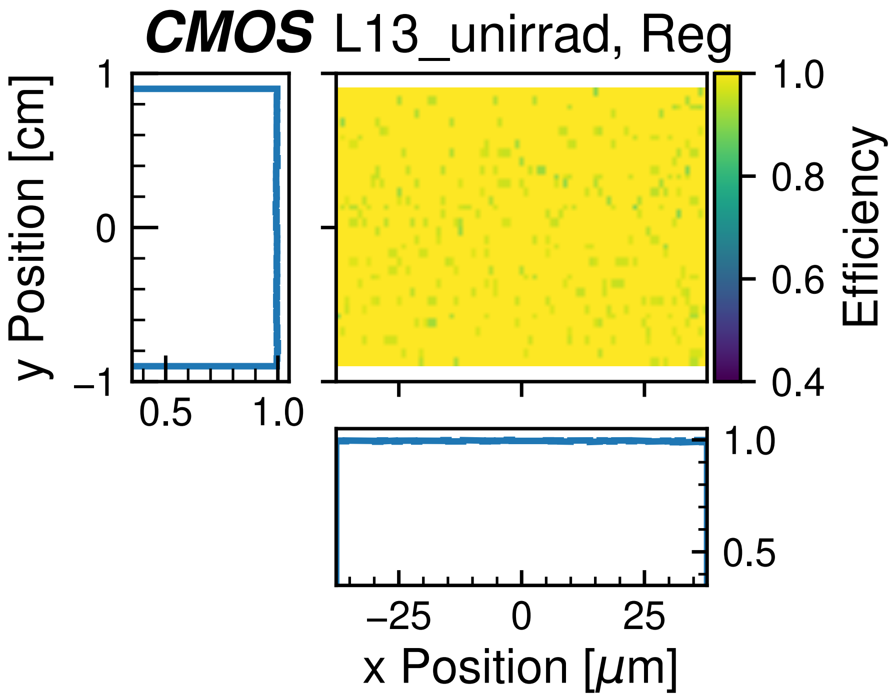
Results from Testbeam II

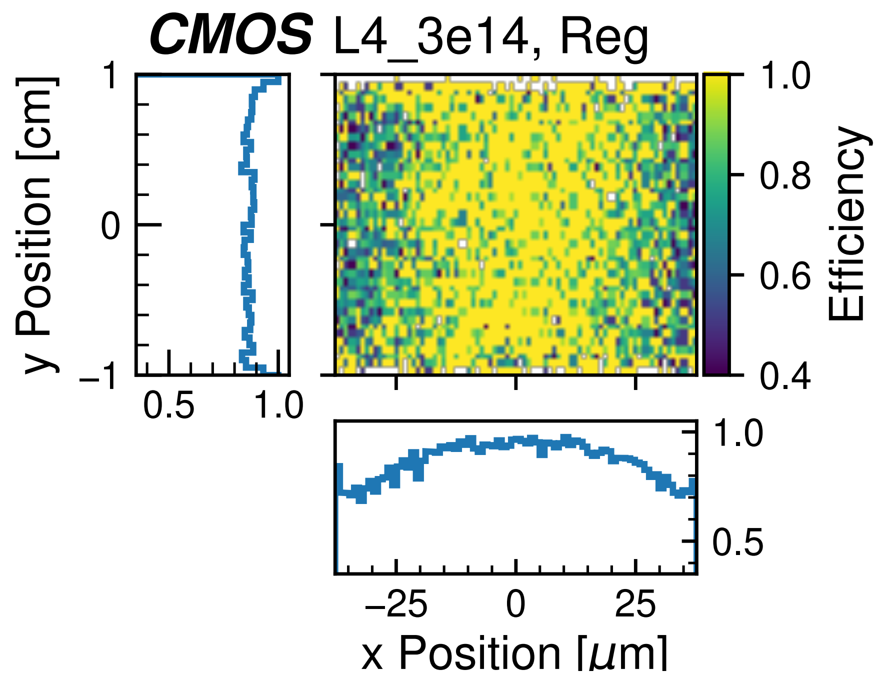
- Efficiency of unirradiated long sensor at 100V and S/N=5
  - Regular: 98.5% eff
  - LD 30: 96.0% eff
  - LD 55: 64.5% eff
  - Regular design performs best, LD55 is problematic
- Sensors irradiated to 3 fluences up to $10^{15}N_{eq}$
- Sensors still work after irradiation
- Radiation effects clearly visible
- Efficiency plateau disappears
- Likely caused by increased noise and reduced signal



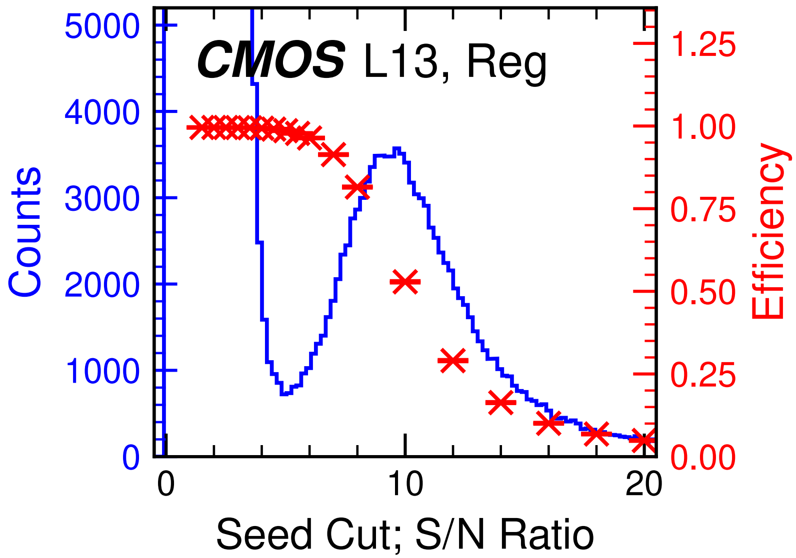
Results from Testbeam III

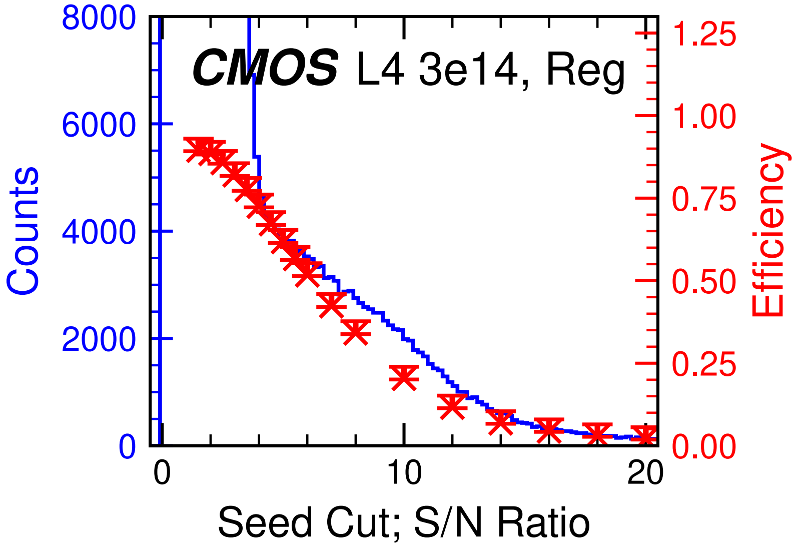
- **2D Efficiency Maps** (entire sensor folded onto one unit cell).
- Efficiency before irradiation is 99% and uniform. No change in efficiency along strip length.
- After $3x10^{14}N_{eq}$, overall efficiency drops. Inter-strip region less efficient than strip centre. Likely caused by charge sharing with one strip below threshold.
- No change along strip length ⇒ Stitching does not influence efficiency.





Results from Testbeam VI





- **Signal distribution and efficiency as function of S/N value of hit**
- **Efficiency loss** caused by reduced signal and increased noise after irradiation
- Typical working point to separate signal and noise: S/N =5. Easy to pick before irradiation, but less obvious when irradiated

Summary and Outlook

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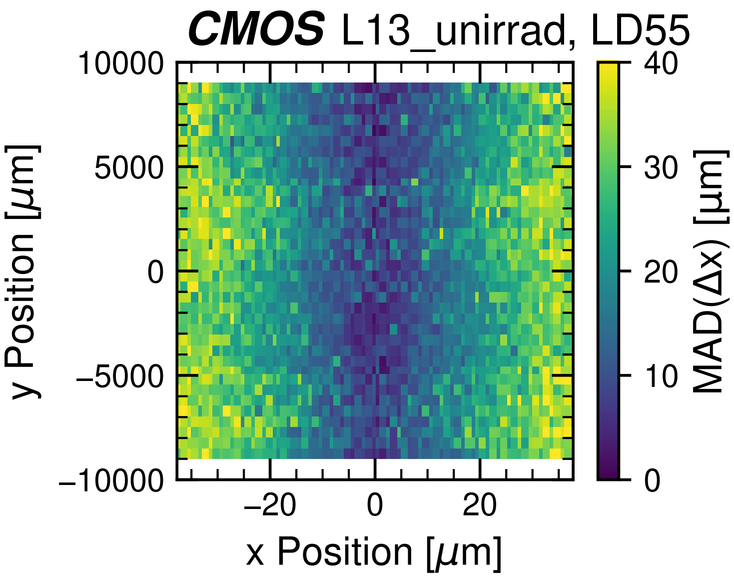
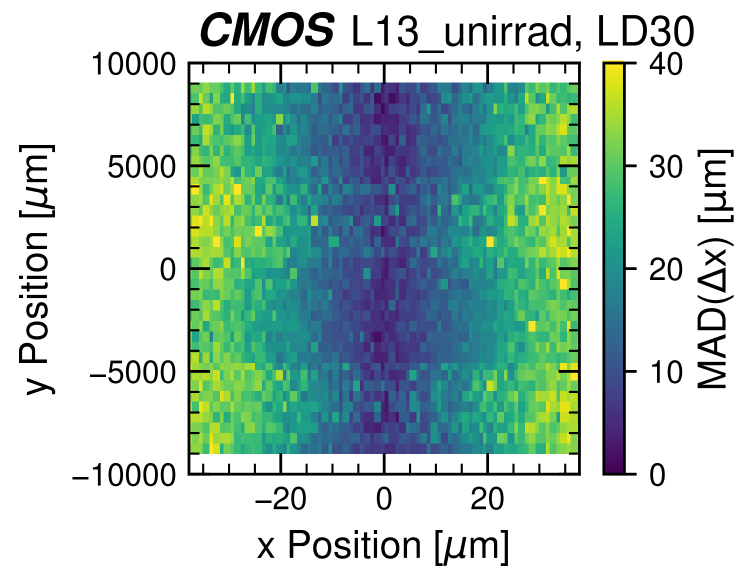
Passive stitched CMOS strip sensors made by LFoundry and studied in detail

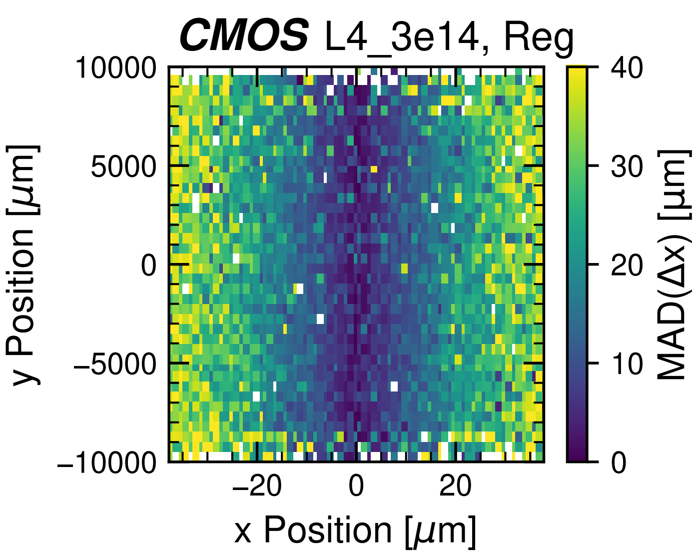
- Sensors perform well, resolution and efficiency as expected
- Stitching of multiple reticles fully successful, no drops of efficiency or resolution at stitches before or after irradiation
- Irradiation reduces the sensor performance (but does not kill them)
- 'Cost savings' arguments becoming less relevant (reducing feature size does not help to cover fixed area, rather than deliver ASIC)

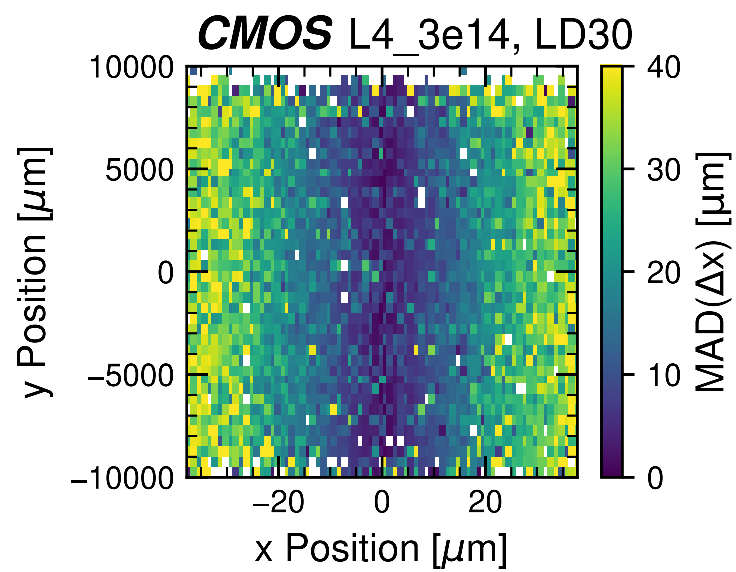
- **Next steps:**
- Irradiation up to $3x10^{16}N_{eq}$
- Again lab characterization, then testbeam at DESY
- **Longer Term goals:**
- Next CMOS strip submission with strip front end
- MPW run without stitching (cost)
- Thanks to the students who (as usual) perform the bulk of the work!

BACKUP: 2D Resolution









BACKUP: 2D Efficiency