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# Operational Experience and Performance with the ATLAS Pixel Detector at the Large Hadron Collider

PSD13: The 13th International Conference of Position Sensitive Detectors

Oxford, 08.09.2023

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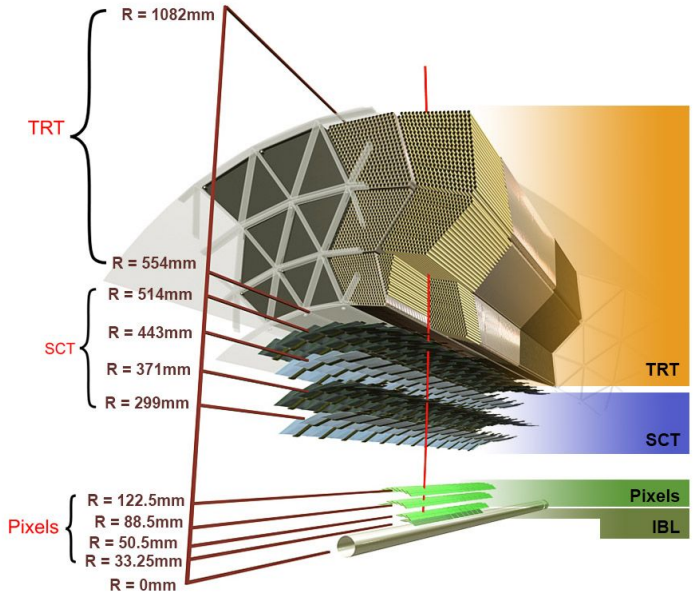
ATLAS Collaboration

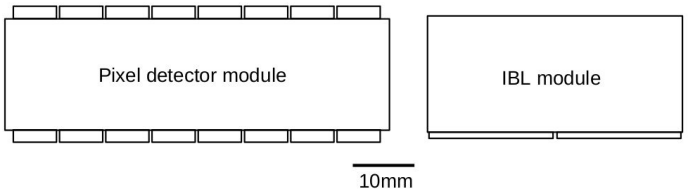
# The ATLAS Pixel Detector

- Four layers + three end caps (not shown) on either side
- Innermost layer: **IBL** only about 3 cm away from interaction point
  - 250 µm x 50 µm pixels, 200 µm thick sensor
  - FEI4 read-out chip
  - Installed during first long shut-down of LHC
- All other layers + disks: **Pixels** (closest is **B-Layer** at about 5 cm distance)
  - 400 µm x 50 µm pixels, 250 µm thick sensors
  - FEI3 read-out chip



# ATLAS pixel modules: FE3 and FEI4

- FEI3 Modules
  - 16 FEI3 per module, one module control chip (MCC)
  - DSM 0.25 µm CMOS technology
  - (up to) 2 x 80 Mbps output links
  - 8 bit ToT ADC (time-over-threshold digitisation)
  - 50 Mrad radiation hardness (EOL estimate for B-Layer 63 Mrad)
  - Designed for average pile-up (<µ>) of 23

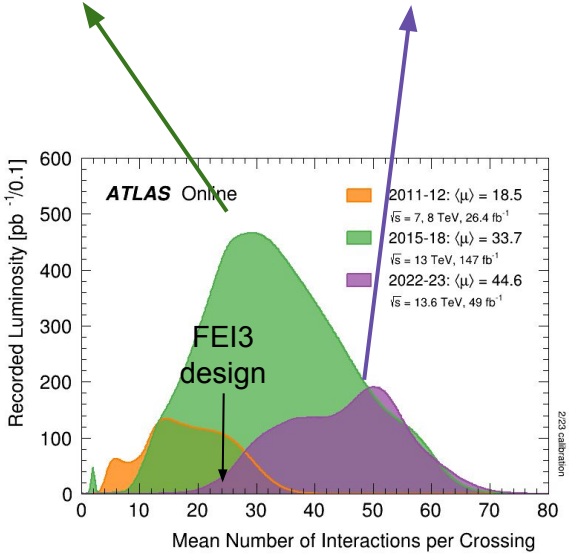


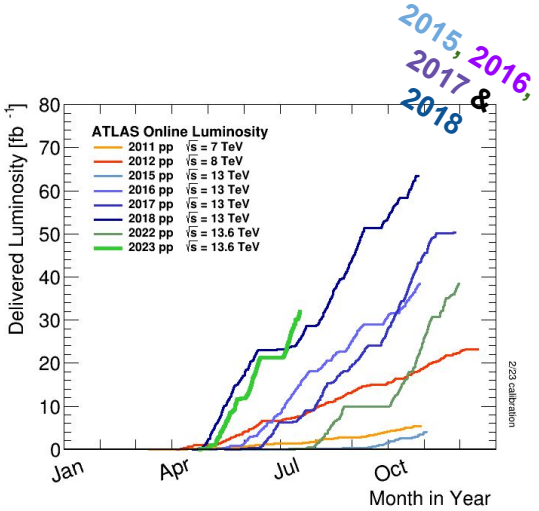

- FEI4 Modules
  - Two FEI4 per module (and no MCC)
  - IBM 130 nm CMOS technology
  - Single 160 Mbps output **per FE**
  - 4 bit ToT ADC
  - 250 Mrad radiation hardness (EOL estimate 130 Mrad)
  - IBL introduced to compensate (efficiency) loss of B-Layer
- Both
  - Individual threshold and ToT response tuning per pixel
  - Single-Event-Upset resilience

# LHC operations in Run 3

# LHC and ATLAS conditions in Run 2

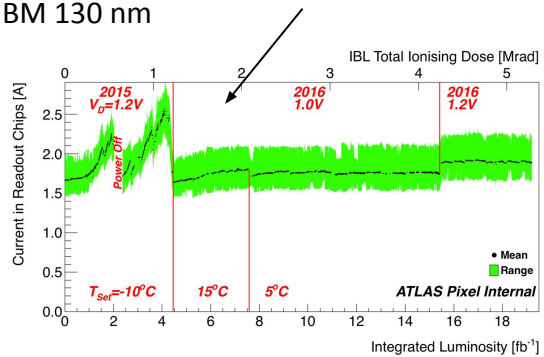

- Already in Run 2 the <μ> was exceeding the design value of 23 for the FEI3 modules
- After ramp-up phase in 2015, three successful years of collecting up to 65 $fb^{-1}$ in a year in 2018
- ATLAS trigger rates of up to slightly above 80 kHz



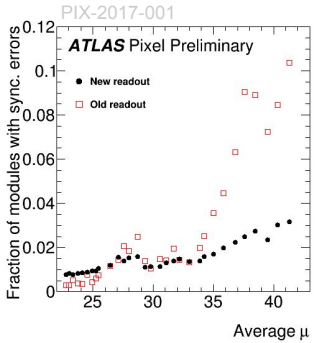
# Run 2 operations

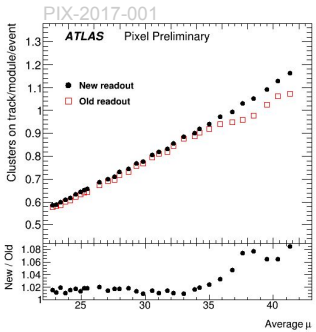
- IBL modules saw increase of LV currents after about 1 Mrad of irradiation
- Surface charges effect on transistor leakage current in IBM 130 nm process
- At high TID this effect is compensated
- Change of operational parameters to decrease leakage current and increase annealing




IBL TID effect → c.f. CERN Yellow Page Report: 10.23731/CYRM-2021-001

- The IBL off-detector read-out hardware was installed for the old Pixel system throughout Run 2
  - Benefits from new functionality developed for IBL
  - More homogeneous DAQ system
- For operators it is much easier to learn one set of tool
  - Also easier to maintain
  - → in many parts FEI3/FEI4 differences are hidden from the user




read-out system upgrade

# Hit on track efficiency: Run 2

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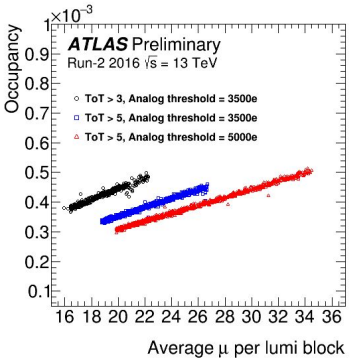
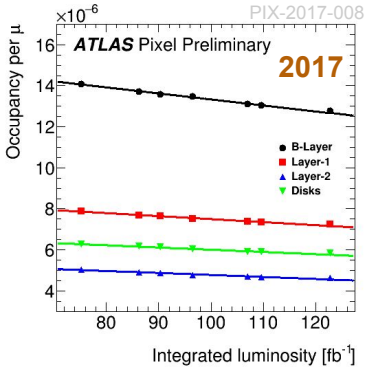
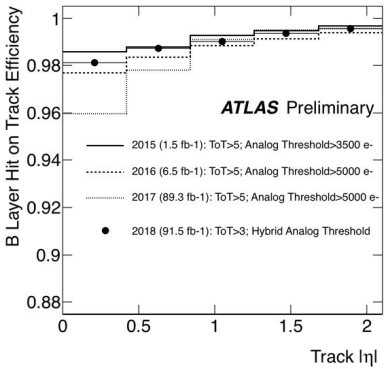
- Figure of merit for overall detector performance is tracking efficiency
  - For a given detector layer, look at hit-on-tracks or hit-on-track efficiency
- During Run 2: initially bandwidth limitations required to increase thresholds
- Later: radiation damage induced charge loss
- Operational parameters (tuning but also bias voltage set-points) should be known in advance since physics Monte Carlo are produced
- Ideally, good understanding on the impact of threshold on tracking performance and DAQ system performance




increase threshold to decrease bandwidth (2015→2016)




decrease threshold to compensate for charge loss (2017→2018)

# LHC and ATLAS operations in **Run 3**

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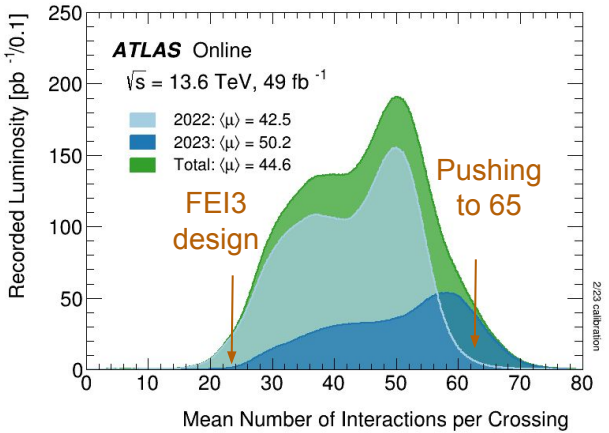
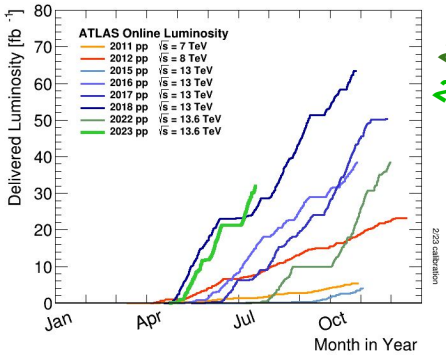
- Mean Number of Interactions per Crossing (avg. pile-up, <μ>) is pushing beyond 60 (target in 2023: 65) and the peak luminosity exceeds $2x10^{34}$ $cm^{-2}s^{-1}$
- Long periods of luminosity levelling
- Trigger rates of 90 kHz and above
- ⟶ overall challenging conditions with aim to maximise integrated luminosity
- ⟶ collect about 160 $fb^{-1}$ of more proton proton data in 2024 and 2025




2022 & 2023

# Hit on track efficiency: Run 3

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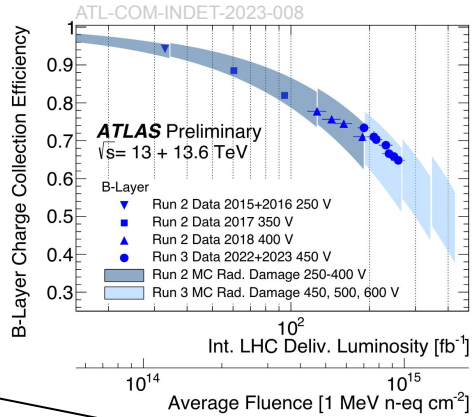
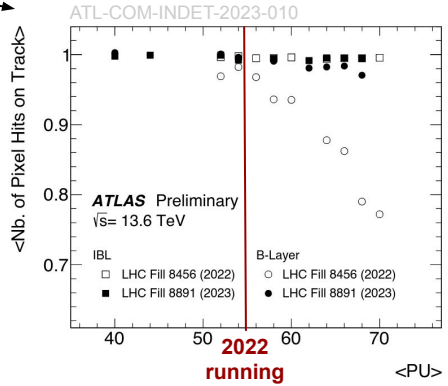
- Anticipating charge loss due to radiation damage → investigation of lower threshold tuning, with cosmic data validation
  - B-Layer threshold of 3500 e (hybrid)
- In 2022 LHC operating at <μ> of 55
- Special run to explore regime for future running
  - In this high-<μ> fill observed loss of B-Layer hits on track with increasing <μ>
  - Under these conditions IBL was performing well and sustained good tracking performance
  - This is exactly what IBL was designed for
- It is very difficult to predict operational behaviour considering DAQ system, radiation damage, FE behaviour, ATLAS/LHC performance, …
- After 10 years of operation still learning about the system!

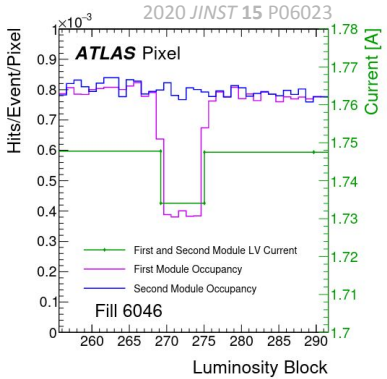


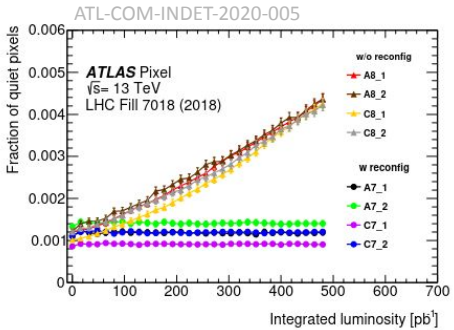



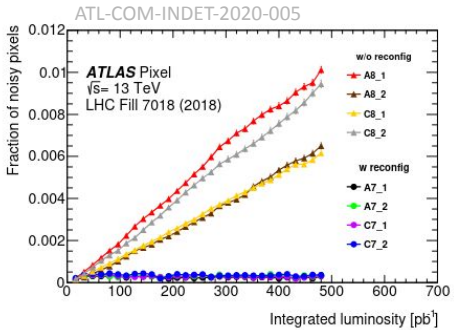

→ c.f. talk from Wednesday: **Including radiation damage effects in ATLAS Monte Carlo simulation: Status and perspectives**

# IBL SEU & SEU mitigation

- Already at end of Run 2, bit flips introduced by SEU in IBL caused modules or pixels to go upset
- Mechanism to reconfigure global registers in FE was introduced
  - No extra dead time by using the global ATLAS event counter reset dead-time
- Mechanism to reconfigure pixel level registers also implemented
  - Was unstable due to OS on read-out-driver (ROD)
- Migration to Linux kernel on ROD during LS2
- **In Run 3 we can do a full IBL reconfiguration (also with pixel registers) and FEI3 reconfiguration (global registers and MCC)**



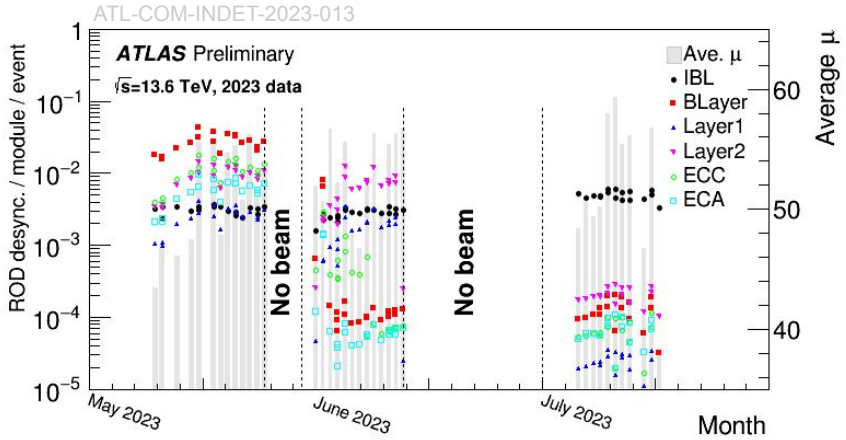



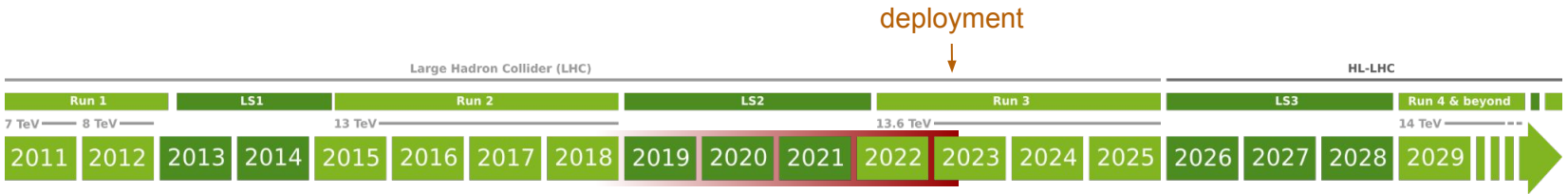

→ c.f. Balbi et al., 2020 *JINST* **15** P06023

# *"Smart"* L1 firmware

- The ROD propagates triggers to modules and receives data from modules for fragment building
- ROD knows if module has yet to send out data from previous triggers → can keep count of pending triggers
- The ROD can skip triggers if module is still processing (presumably large) events
  - ROD has to "smartly" resynchronise the data
- This has been deployed in the Pixel layers (not IBL) throughout 2023
- We operate with different FPGA firmwares on the fragment building FPGAs → hot-swapping of FW on-the-fly implemented at the end of LS2 in DAQ




Decrease of desynchronisation errors on the ROD due to usage of the new data taking firmware in 2023



# Hit on track efficiency: Run 3 (2023 updates)

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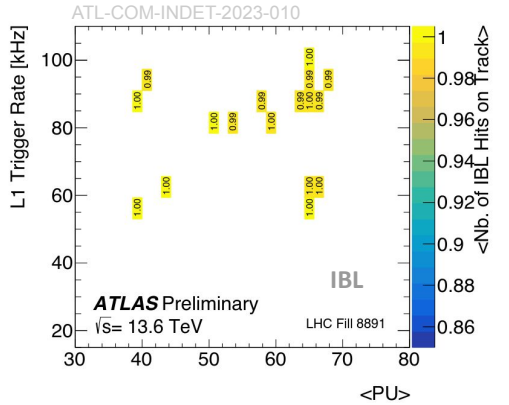
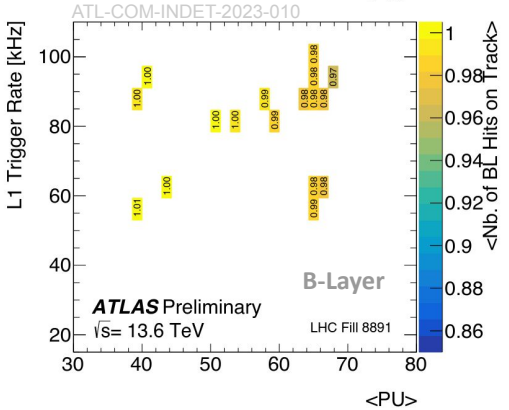
- Combination of FE reconfiguration to mitigate SEU, the novel data taking firmware and adjusting the tuning thresholds → recovery of B-Layer hit-on-track efficiency even at high <μ> and high trigger rate
- Excellent IBL performance
  - Global and pixel register reconfiguration
- B-Layer (and other Pixel layers) recovered for <μ> above 55
  - Global and MCC reconfiguration
  - Smart L1 firmware
  - Threshold adjustments
- <μ> of 65 and trigger rates of 90 kHz possible (ATLAS nominal target for future Run 3)
  - With even some safety margin

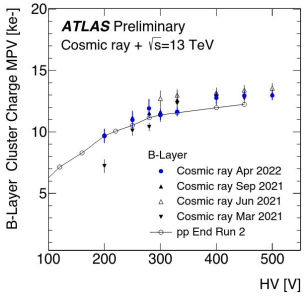



# Conclusions

- Under the challenging conditions of Run 3 the ATLAS Pixel Detector has resumed operation in 2022
- Large <μ> and high trigger rates are pushing the limits of the FEI3 modules
- After ramp-up in 2022, many features developed during LS2 allow to operate the detector at a <μ> of 65 and trigger rate of 90 kHz
- Ready for heavy ion data taking in the next weeks and more data in 2024 and 2025

Some of the topics left out …




HV and IV scans to monitor radiation damage

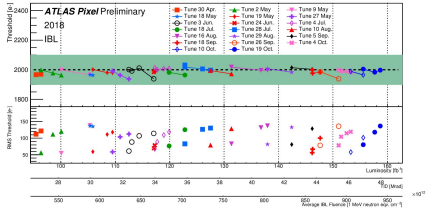
| Threshold | 2017 | 2018 |
|---|---|---|
| IBL | 2500e, ToT>0 | 2000e, ToT>0 |
| B-layer | 5000e, ToT>5 | 4300e(*), ToT>3 |
| Layer-1 | 3500e, ToT>5 | 3500e, ToT>5 |
| Layer-2 | 3500e, ToT>5 | 3500e, ToT>5 |
| Endcap | 4500e, ToT>5 | 3500e, ToT>5 |

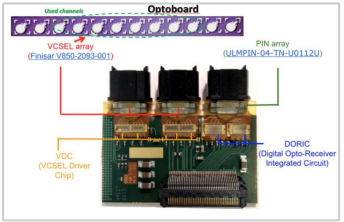
* central Eta: 4300e high Eta: 5000e

Run 2 Bias Voltage Evolution

| HV | 2015 | 2016 | 2017 | 2018 |
|---|---|---|---|---|
| IBL | 80V | 150V | 350V | 400V |
| B-layer | 250V | 350V | 350V | 400V |

detector monitoring and tuning and operational set points



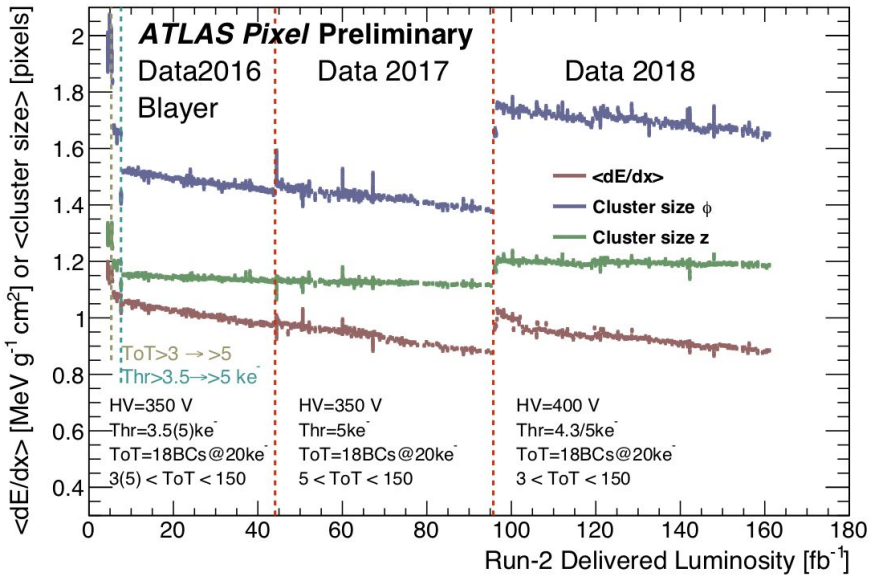

read out hardware maintenance … computers, opto-electrical components

… just some

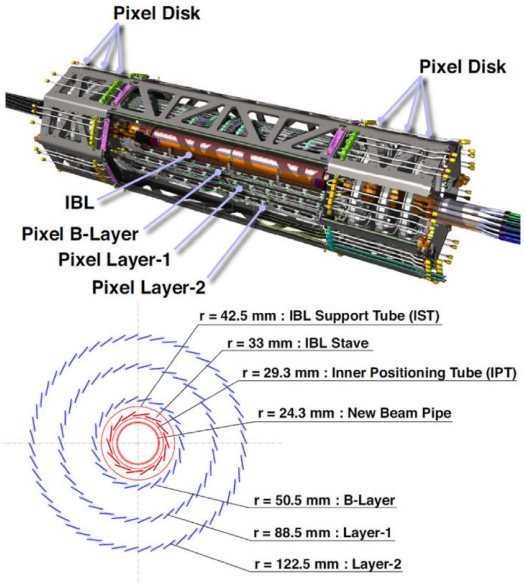
# Backup

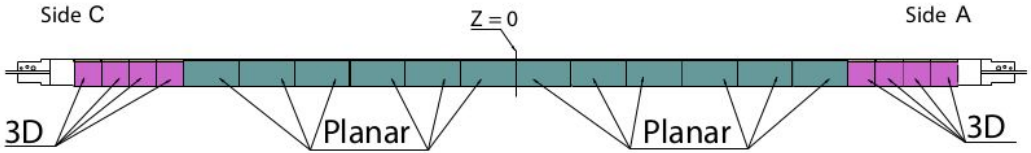
# <dE/dx> in Run 2

- B-Layer evolution of signal throughout Run 2
- Impacted by modification of thresholds
- Initial decrease (2015/16) of <dE/dx> attributed to increasing thresholds to cope with bandwidth
- Then loss of signal due to radiation damage → adjusted thresholds in 2018
- Impact also visible in cluster sizes

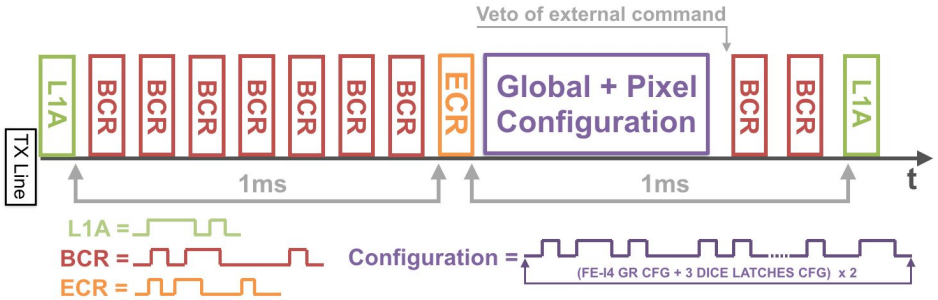


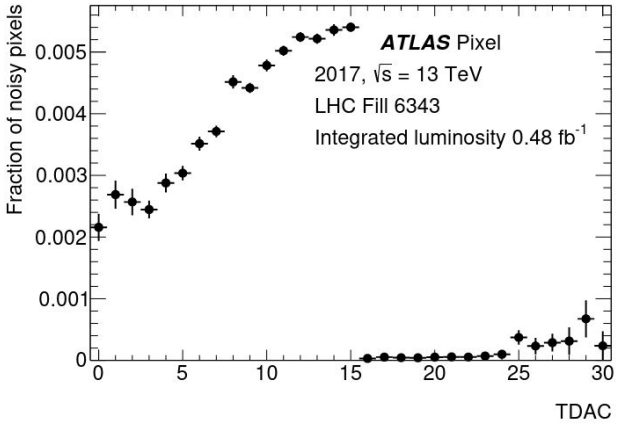

# Conclusions

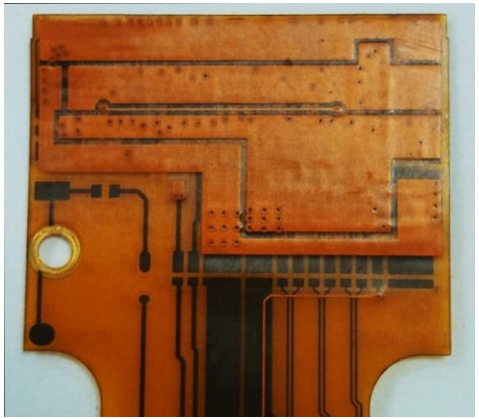


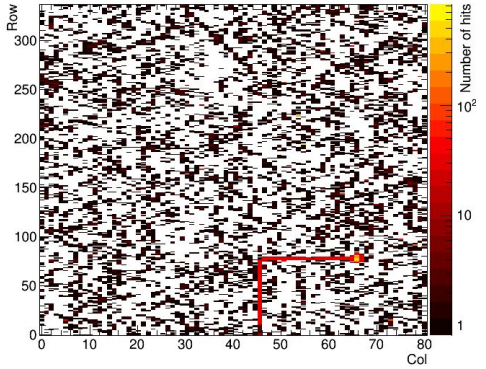



# IBL SEU


Veto of external command
L1A
BCR
BCR
BCR
BCR
BCR
BCR
BCR
ECR
Global + Pixel Configuration
BCR
BCR
L1A
TX Line
1ms
1ms
t
L1A =
BCR =
ECR =
Configuration =
(FE-I4 GR CFG + 3 DICE LATCHES CFG) x 2


Fraction of noisy pixels
0.005
0.004
0.003
0.002
0.001
0
ATLAS Pixel
2017, √s = 13 TeV
LHC Fill 6343
Integrated luminosity 0.48 fb-1
0
5
10
15
20
25
30
TDAC




Row
300
250
200
150
100
50
0
Number of hits
10²
10
1
0
10
20
30
40
50
60
70
80
Col