DynamiX

A charge cancelling ASIC for high dynamic range measurements of hard X-rays

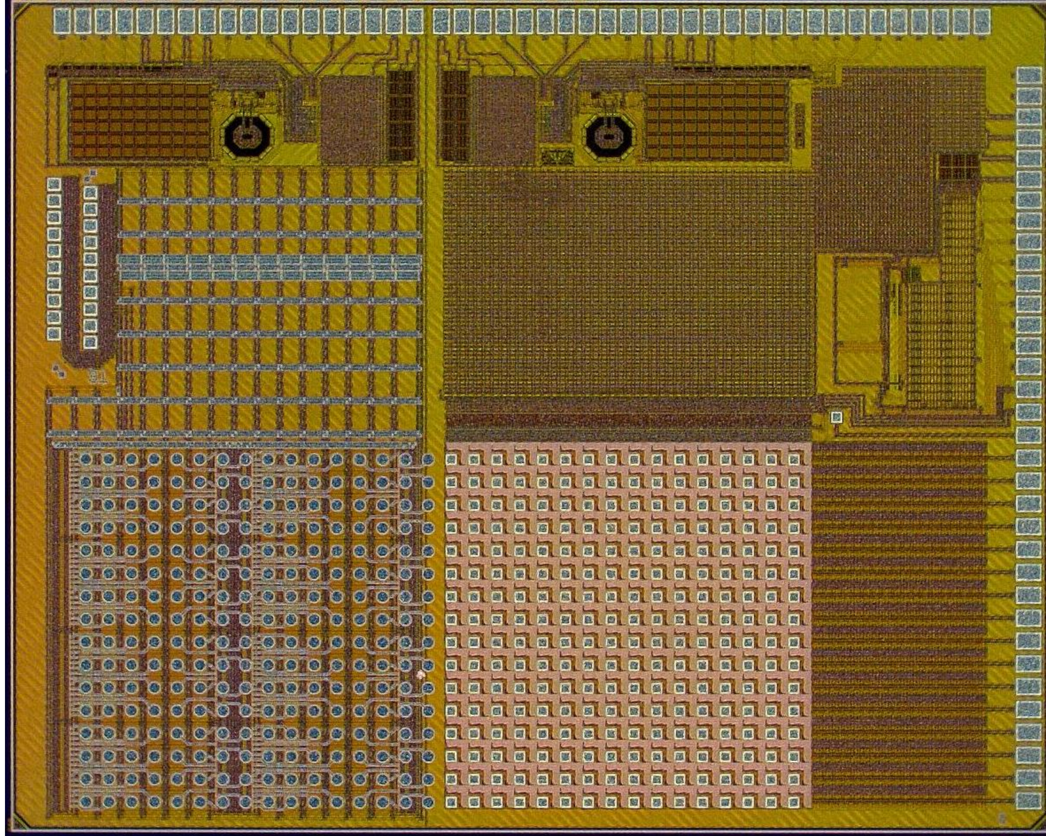
Matt.Wilson@stfc.ac.uk

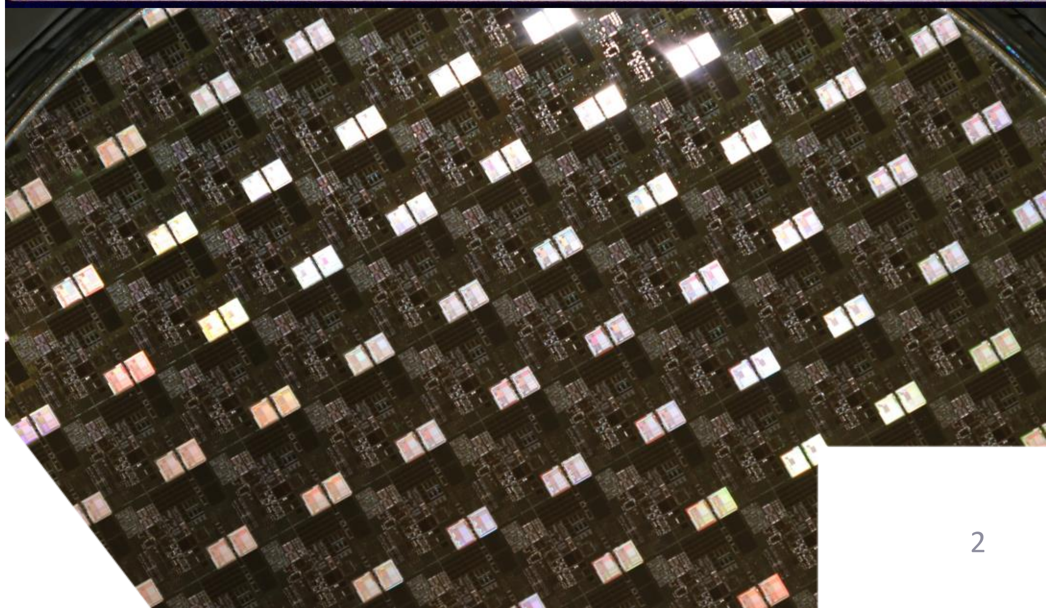
6^{th} of September 2023

Position Sensitive Detectors 13

Agenda

1. **Motivation**
    - STFC and Diamond II
2. **Design Decisions**
    - HF-CZT
    - Pixel Design
3. **Dynamix Design**
    - Pixel Design & High Speed Serialisers
    - MPW ASIC
    - DAQ System
4. **Next Steps**
    - Full ASIC scale-up
    - Collaboration
5. **Summary**





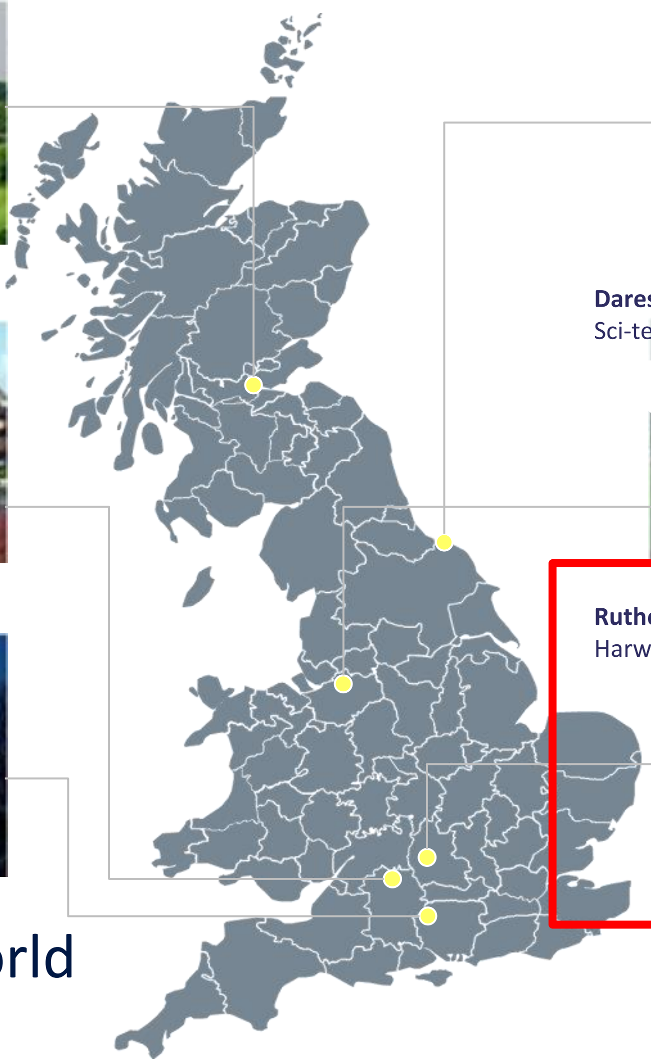
Science and Technology Facilities Council

STFC

UK Astronomy Technology Centre
Edinburgh, Scotland

Polaris House
Swindon, Wiltshire

Chilbolton Observatory
Stockbridge, Hampshire



Boulby Underground Laboratory
North Yorkshire

Daresbury Laboratory
Sci-tech Daresbury Campus, Liverpool City Region

Rutherford Appleton Laboratory
Harwell Didcot, Oxfordshire

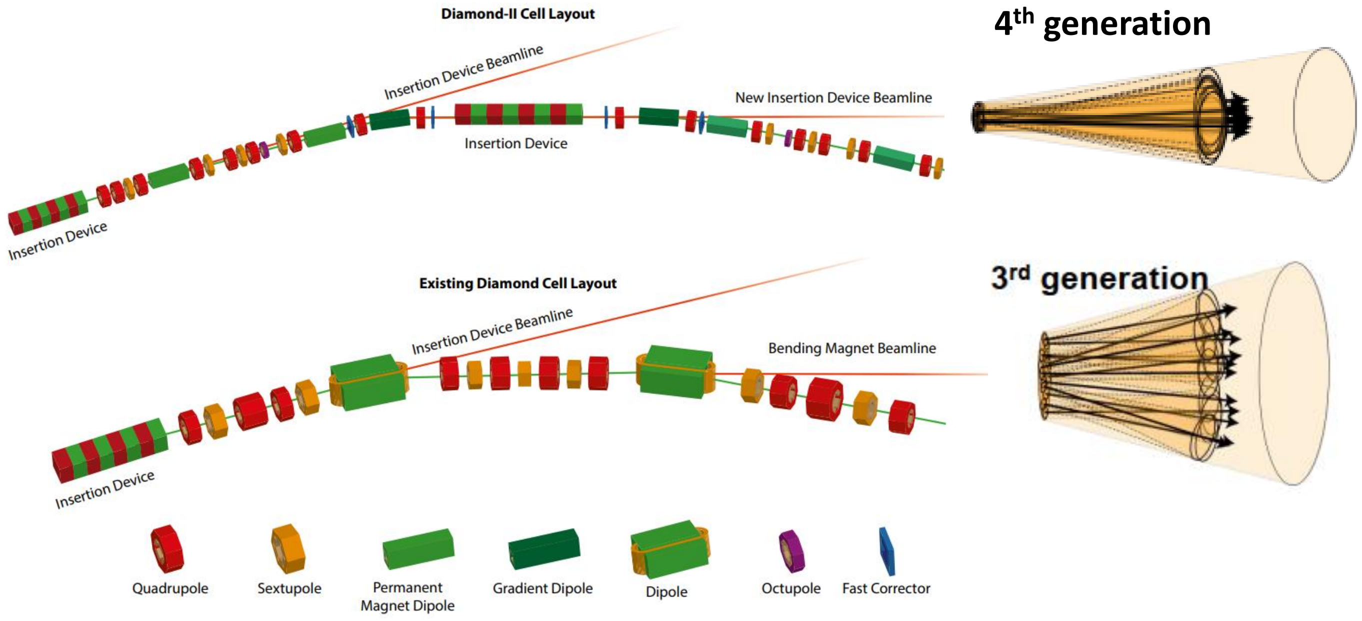
...and around the world

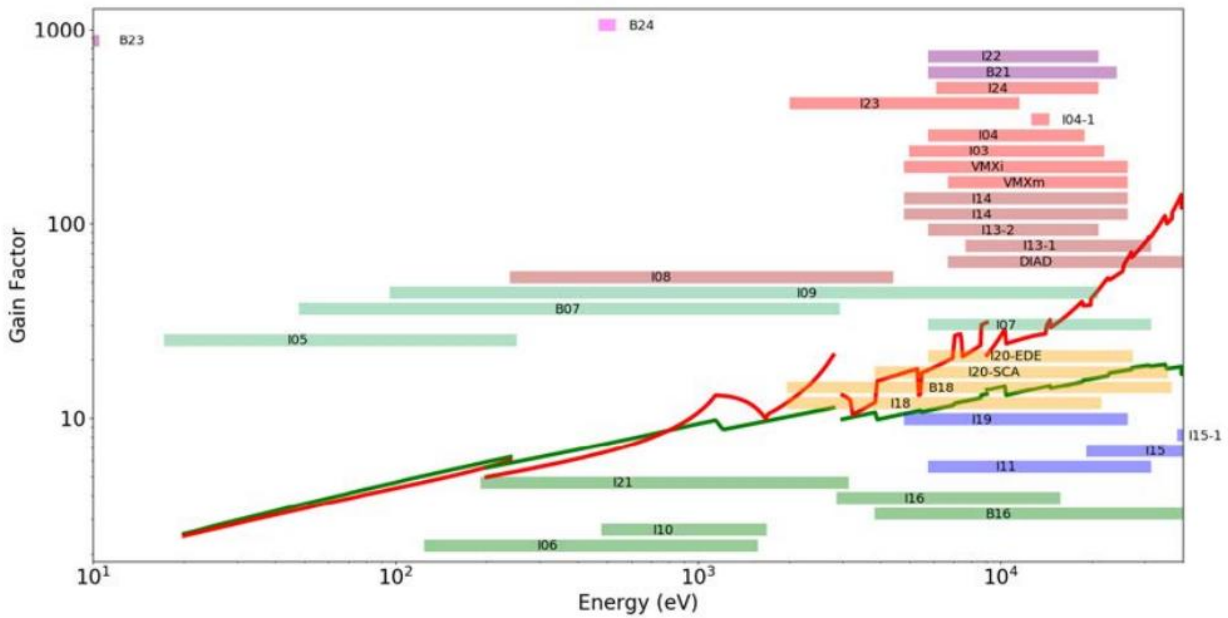
Science and Technology Facilities Council

Rutherford Appleton Laboratory

Motivation

- Diamond II upgrade to diffraction limit storage ring
- Many beamlines going to >20keV
- x100 increase in flux
- Up to 10^{12} ph/mm^2/s reaching the detector



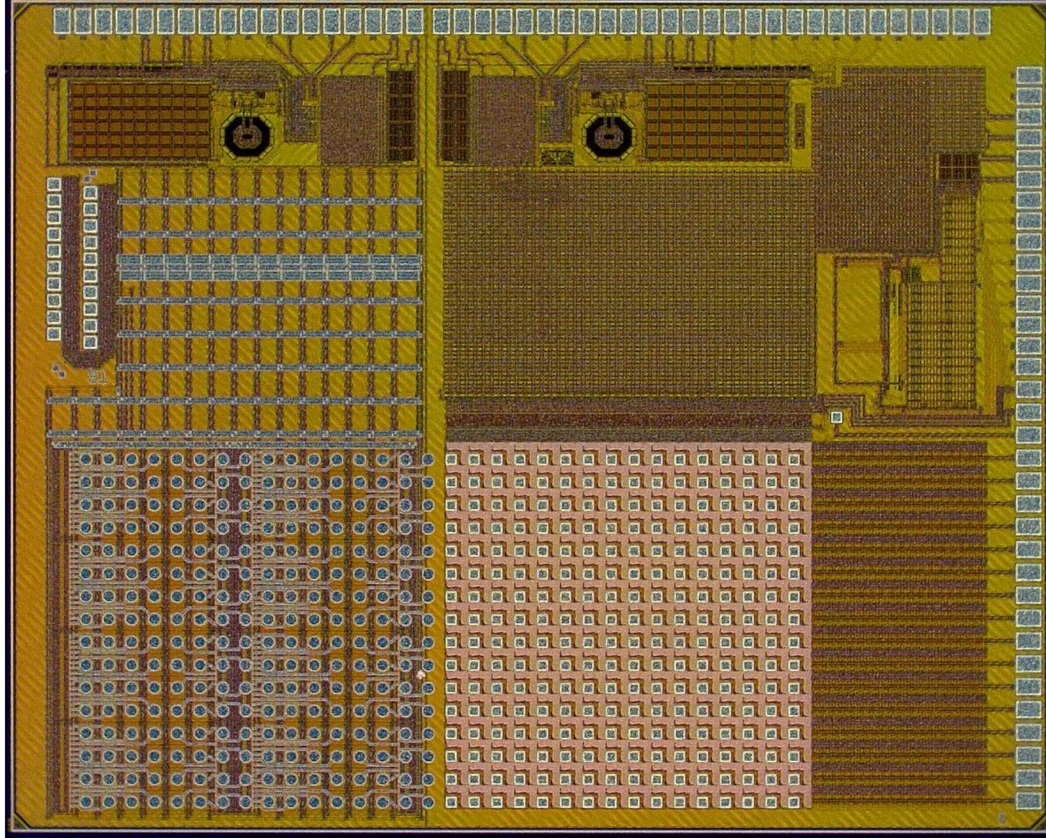


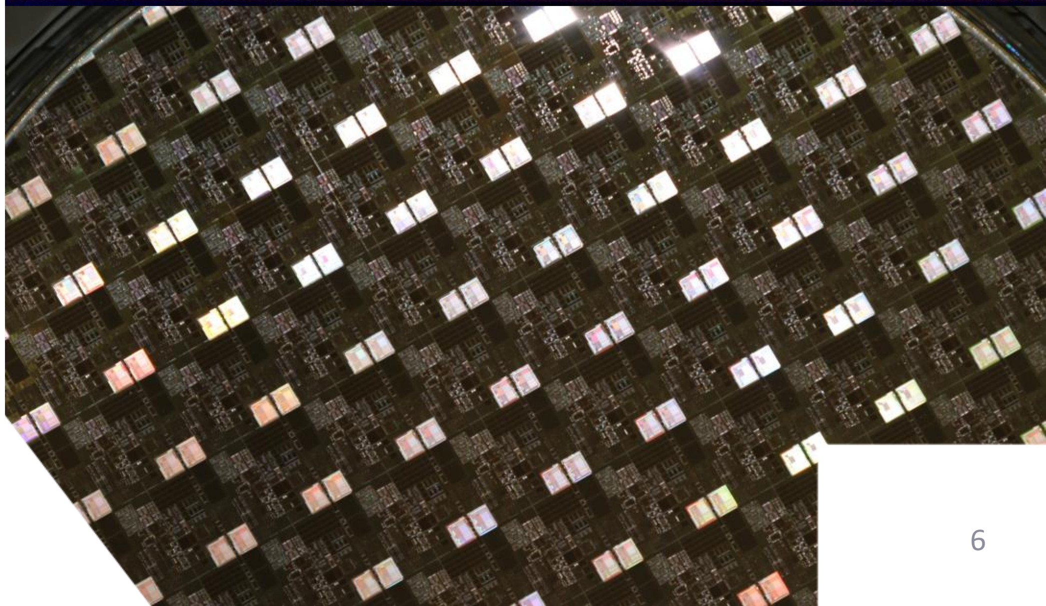
Science and Technology Facilities Council

Agenda

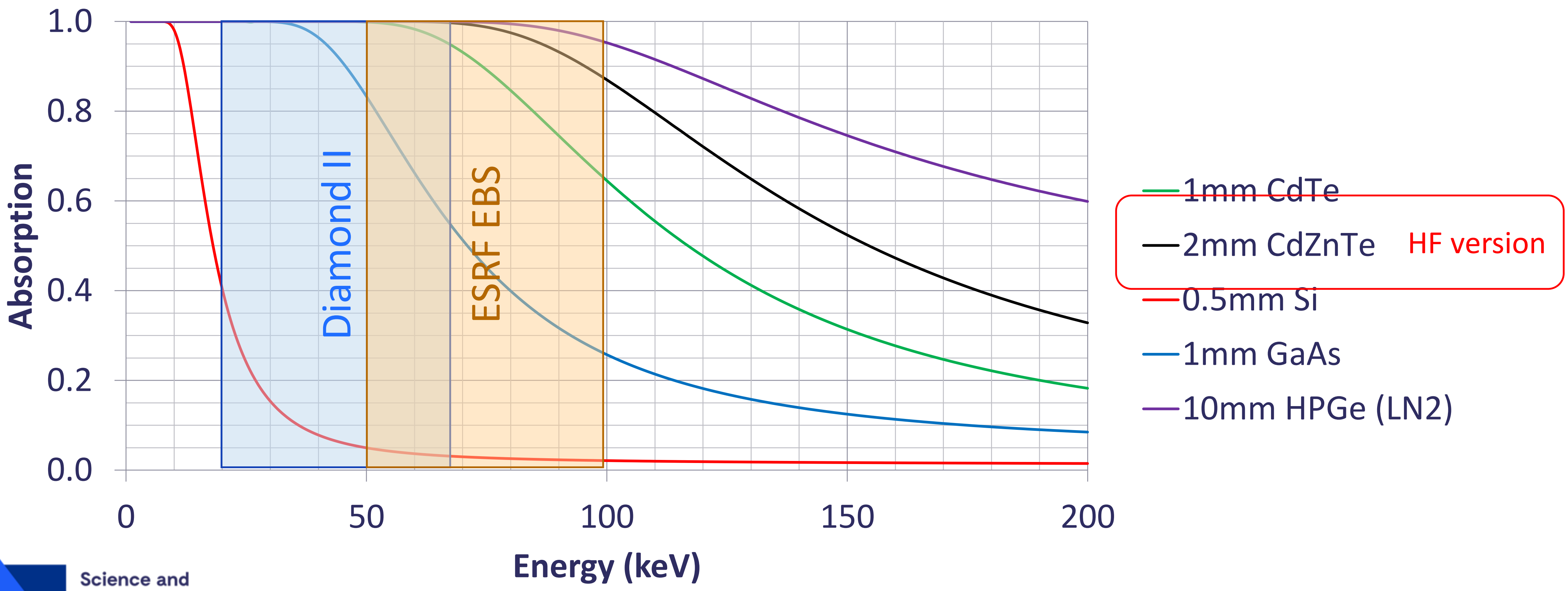
1. **Motivation**
   - STFC and Diamond II
2. **Design Decisions**
   - HF-CZT
   - Pixel Design
3. **Dynamix Design**
   - Pixel Design & High Speed Serialisers
   - MPW ASIC
   - DAQ System
   - MPW Test
4. **Next Steps**
   - Full ASIC scale-up
   - Collaboration
5. **Summary**

Science and Technology Facilities Council



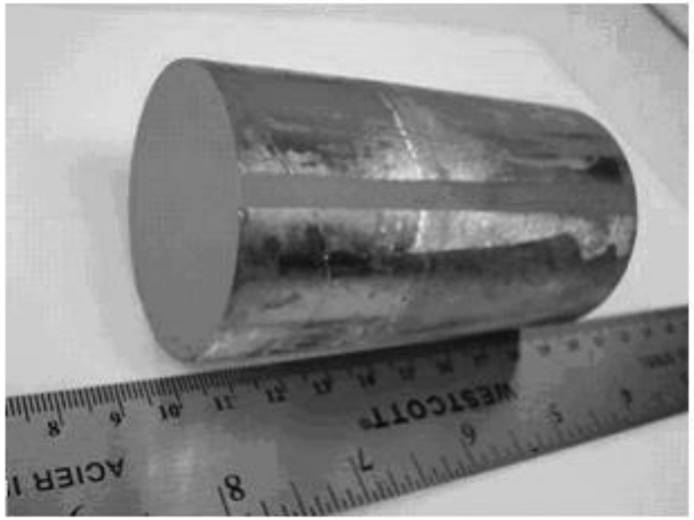


Detector Material



Science and Technology Facilities Council

HF-CZT



11TH International Conference on Position Sensitive Detectors
3–8 September 2017
The Open University, Walton Hall, Milton Keynes, U.K.

Characterisation of Redlen high-flux CdZnTe

B. Thomas,[a,b,1] M.C. Veale,[a] M.D. Wilson,[a] P. Seller,[a] A. Schneider[a] and K. Iniewski[c]

REDLEN TECHNOLOGIES

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 54, NO. 4, AUGUST 2007 811

Characterization of Traveling Heater Method (THM) Grown $Cd_{0.9}Zn_{0.1}Te$ Crystals

Henry Chen, *Member, IEEE*, Salah A. Awadalla, Jason Mackenzie, Robert Redden, Glenn Bindley, A. E. Bolotnikov, *Member, IEEE*, G. S. Camarda, G. Carini, *Member, IEEE*, and R. B. James, *Fellow, IEEE*

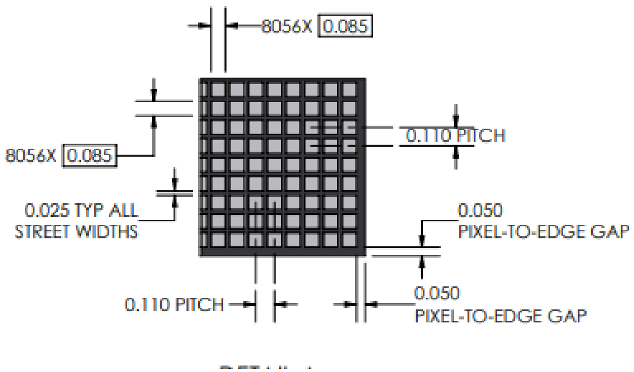
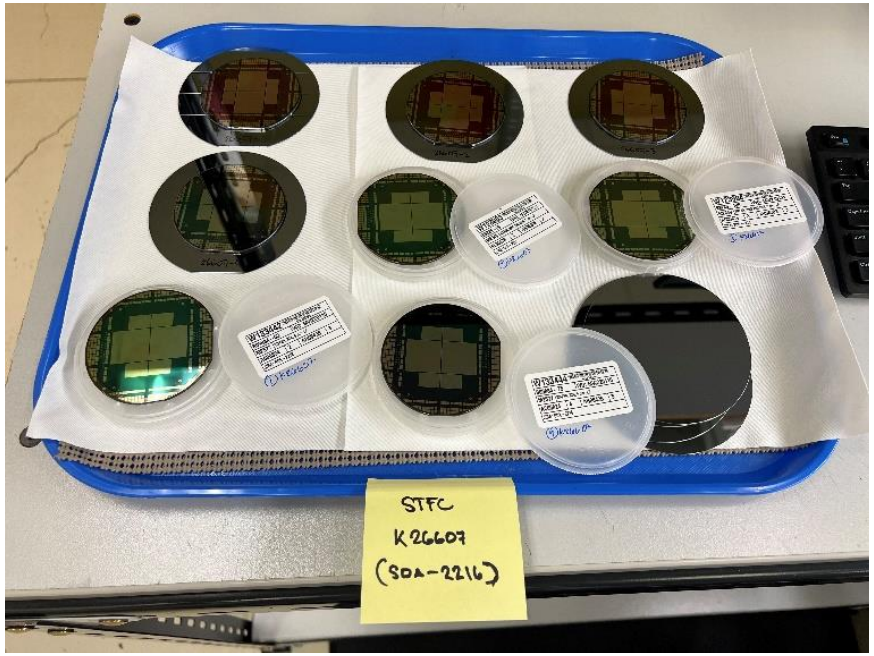


Table 1. A summary of the measured charge transport properties of three "high-flux" Redlen CdZnTe detectors [14, 16].

	$\mu_e\tau_e$ ($\times10^{-4}$ cm^{2}V^{-1})	μ_e (cm^{2}V^{-1}s^{-1})	τ_e ($\times10^{-6}$ s)	$\mu_h\tau_h$ ($\times10^{-4}$ cm^{2}V^{-1})	μ_h (cm^{2}V^{-1}s^{-1})	τ_h ($\times10^{-6}$ s)
High Flux CdZnTe	11 ± 6	940 ± 190	1.2 ± 0.8	2.9 ± 1.4	114 ± 22	2.5 ± 1.4
Standard CdZnTe	100	1100	11	0.2	88	0.2



- 2mm thick HF-CZT
    - 9x12mm to 28x28mm
- Redlen improved hole lifetimes to be delay polarization with flux
- 110µm pitch detectors in assembly with MPW ASIC
- Have more CZT in hand and interested in collaborating to test further

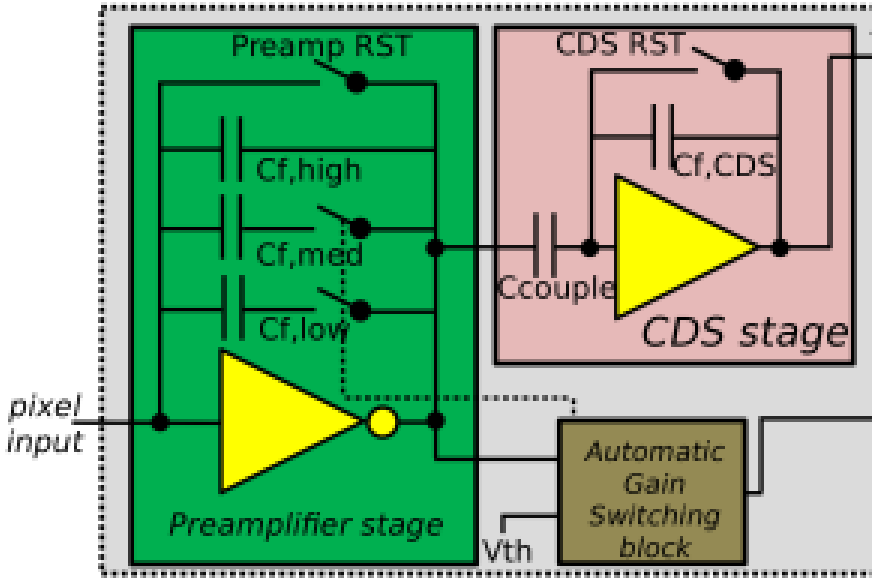
Science and Technology Facilities Council

High Flux >10^{11} ph/mm^2/s

JINST
PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB
RECEIVED: April 8, 2020
ACCEPTED: May 18, 2020
PUBLISHED: June 23, 2020

High dynamic range CdTe mixed-mode pixel array detector (MM-PAD) for kilohertz imaging of hard x-rays

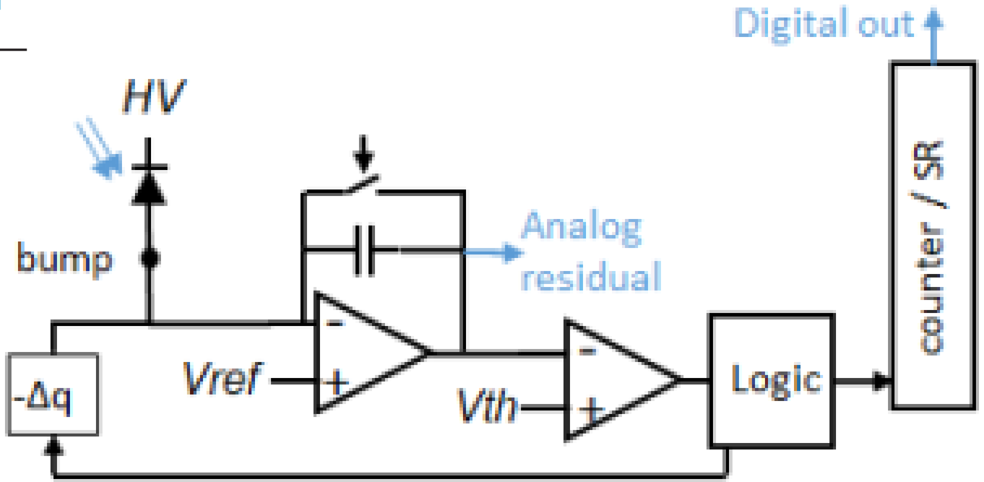
H.T. Philipp[a,1] M.W. Tate[a] K.S. Shanks[a] P. Purohit[a] and S.M. Gruner[a,b]
[a]Laboratory of Atomic and Solid State Physics,
Cornell University, Ithaca, NY 14853, U.S.A.



JINST
PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB
RECEIVED: December 13, 2013
ACCEPTED: March 28, 2014
PUBLISHED: May 9, 2014
15th INTERNATIONAL WORKSHOP ON RADIATION IMAGING DETECTORS
23–27 JUNE 2013,
PARIS, FRANCE

Prototype characterization of the JUNGFRAU pixel detector for SwissFEL

A. Mozzanica,[a,1] A. Bergamaschi,[a] S. Cartier,[a,b] R. Dinapoli,[a] D. Greiffenberg,[a] I. Johnson,[a] J. Jungmann,[a] D. Maliakal,[a] D. Mezza,[a] C. Ruder,[a] L. Schaedler,[a] B. Schmitt,[a] X. Shi[a] and G. Tinti[a,c]

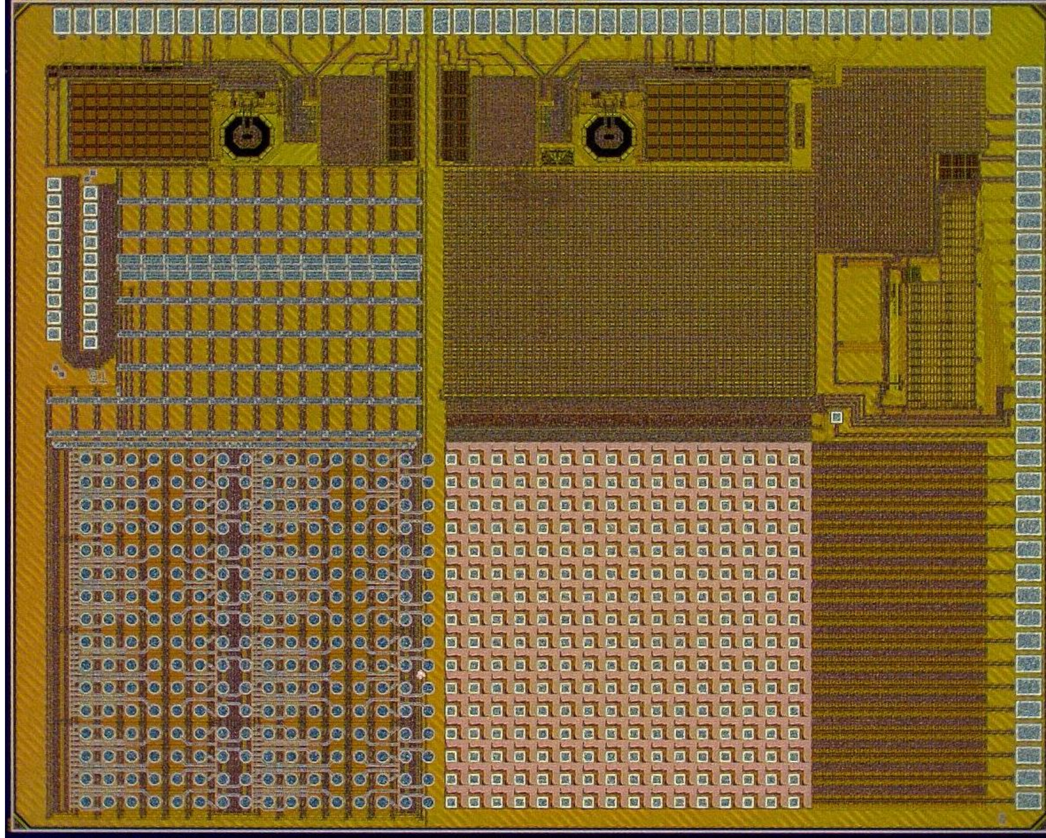


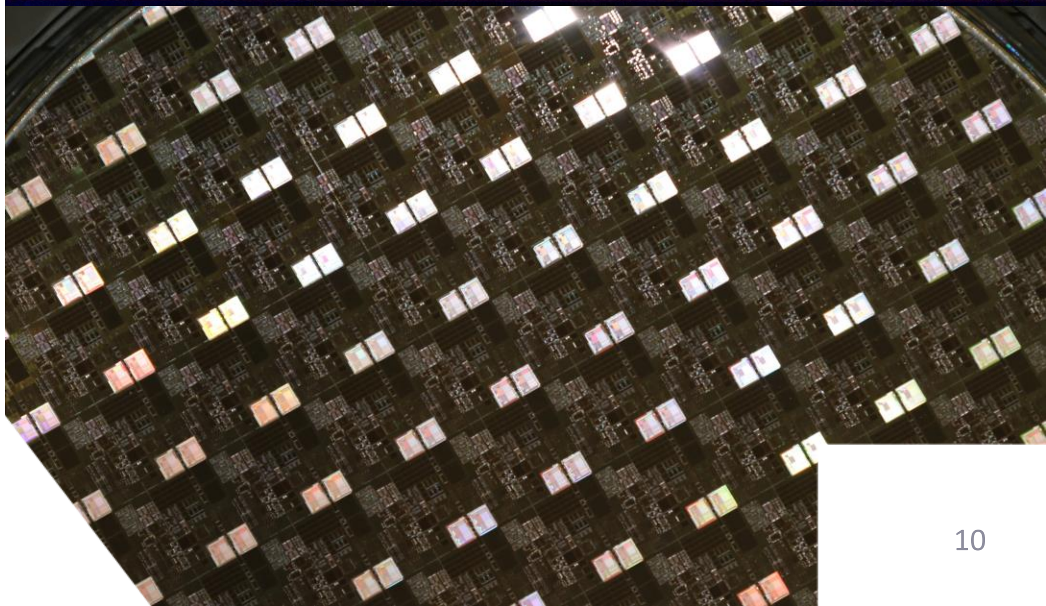
Adaptive Gain
Like AGIPD, CoRDIA, Jungfrau, ePix…

Charge cancellation and counting
Like MMPad…

Agenda

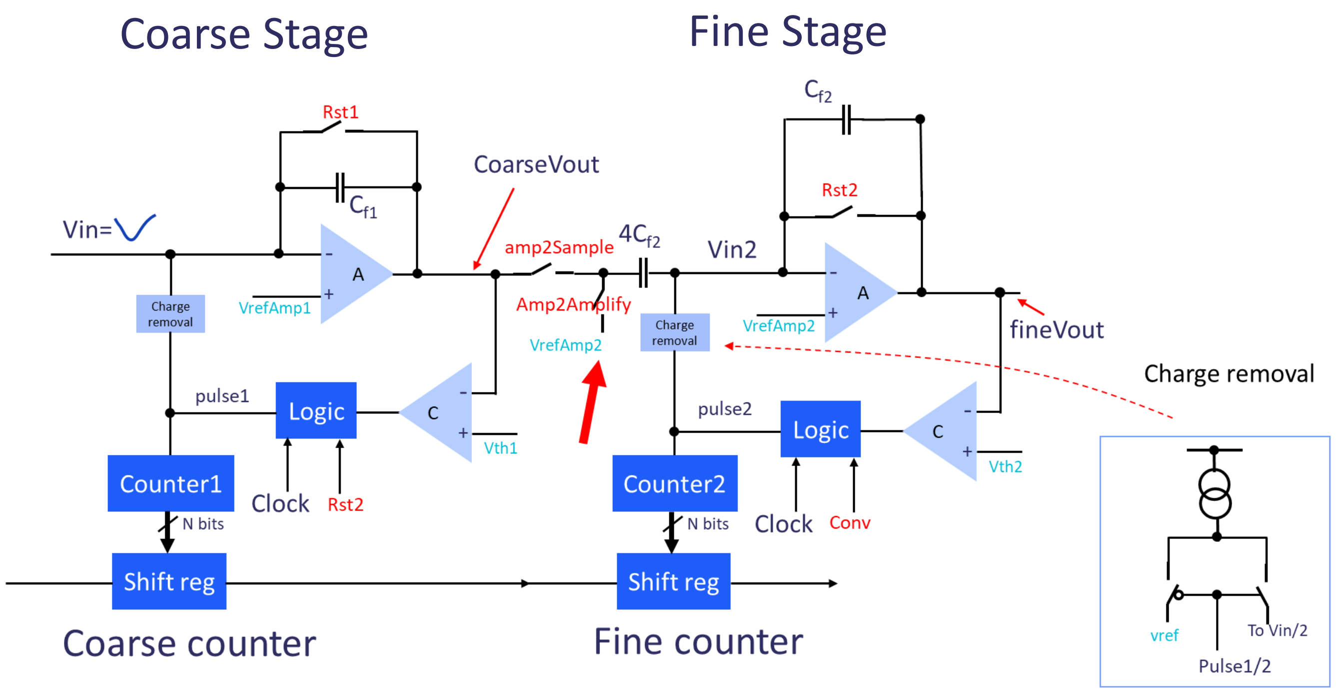
1. **Motivation**
   - STFC and Diamond II
2. **Design Decisions**
   - HF-CZT
   - Pixel Design
3. **Dynamix Design**
   - Pixel Design & High Speed Serialisers
   - MPW ASIC
   - DAQ System
   - MPW Test
4. **Next Steps**
   - Full ASIC scale-up
   - Collaboration
5. **Summary**





Science and Technology Facilities Council

DynamiX Design Choices



65nm process

Parameter	Spec	MPW Design
Pixel Size	110µm	Charge cancellation = compact design to fit in the pixel.
Count/Frame	0.25 to 6400 @25keV	Go as fast as possible to get the flux – 1 turn of Diamond (or other synchrotrons)
Frame Rate	533 kHz	
Dynamic Range	$>10^{11}$ ph/mm²/s	Test the HF-CZT and see raw data – how will it work?
Energy	25keV Typical	Electron collection for HF-CZT Adjust cancellation and threshold sizes for energy
Noise Level	Single photon	Sets fine-stage charge cancellation See charge sharing <0.25 ph

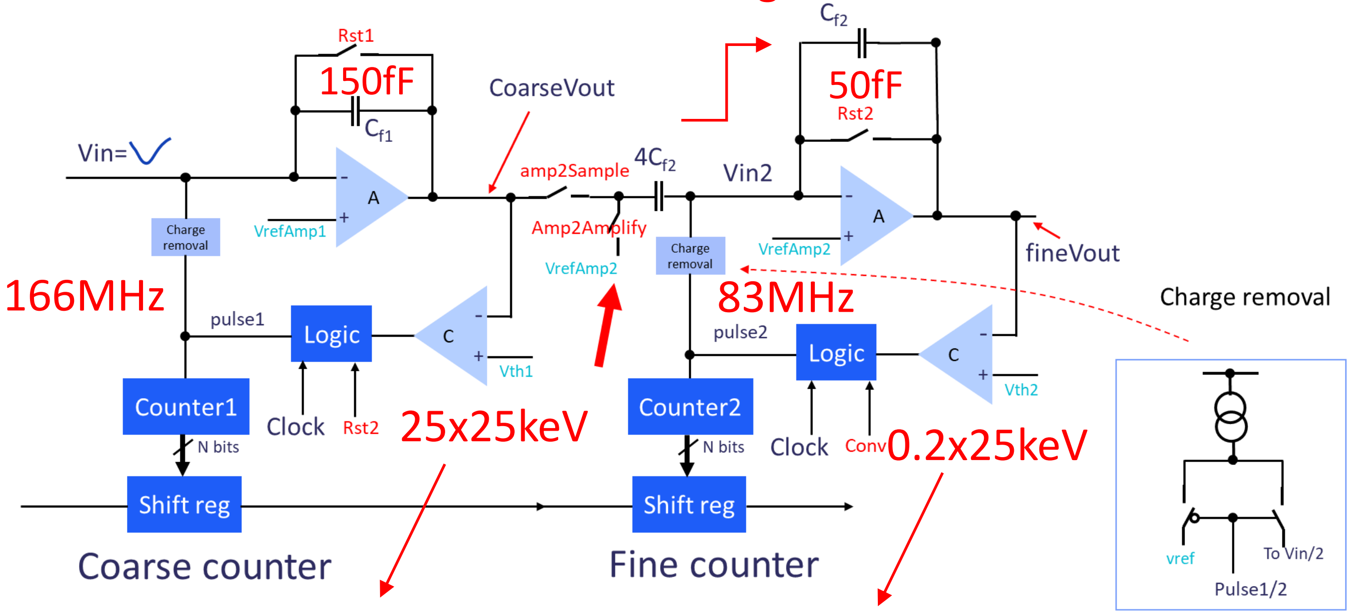
MPW = Multi project wafer → test ASIC

Science and Technology Facilities Council

DynamiX Pixel

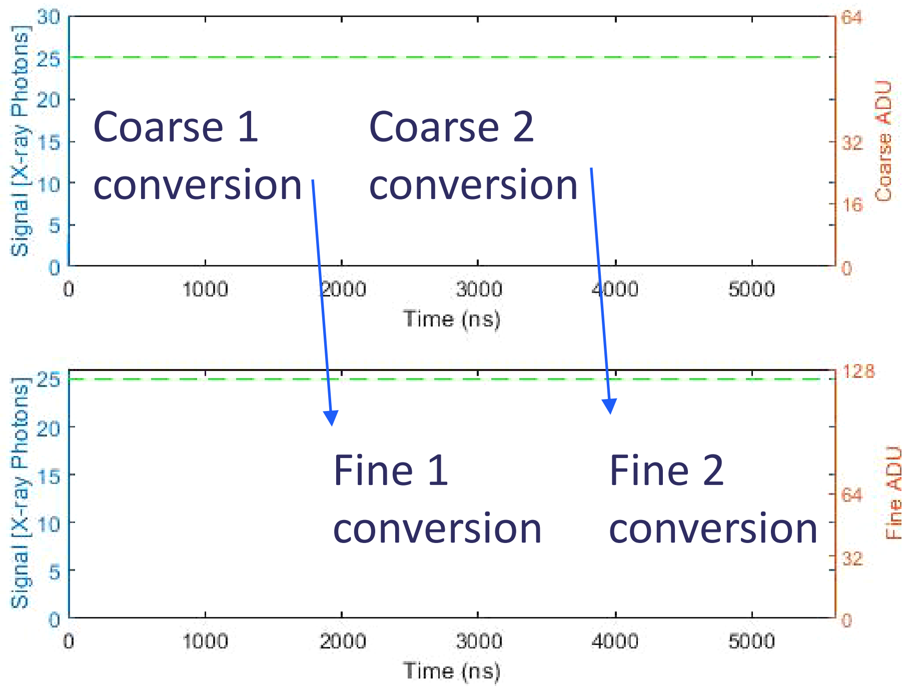
1 integration ~ 1.8µs = 1 turn of Diamond
(but programmable for any synchrotron)

Pipelined between coarse and fine stage



8bit counter = 25*256 =
6400 ph/frame
1 ADU = 25 photons

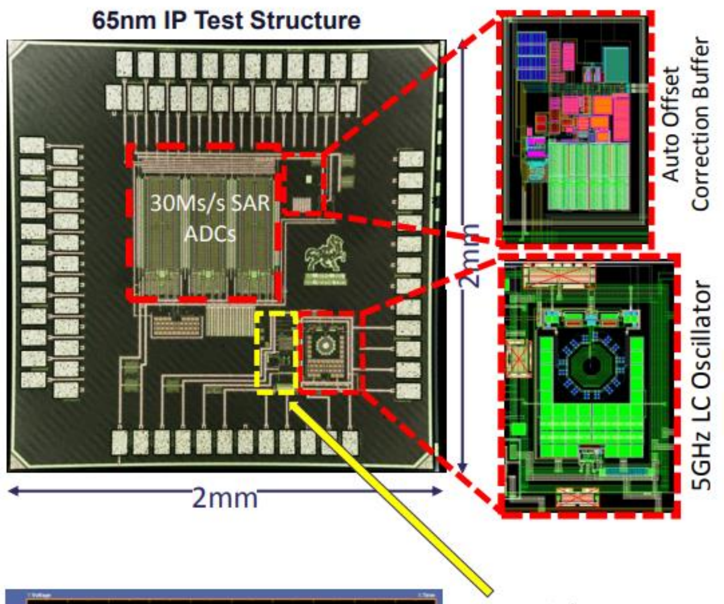
7bit counter = 0.2*128 =
25.6 ph/frame
1 ADU = 0.2 photon

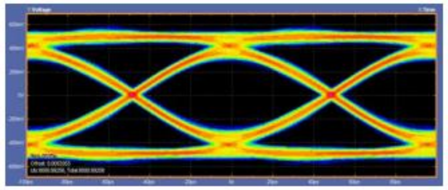


Science and Technology Facilities Council

Data Output

- CML serialiser with Aurora 64b66b
- Now in 65nm CMOS
  - v1 Test structure 10Gbps
  - Pushed to 14Gbps
- Work through the frame rate and 16bit per pixel
  - 8 columns by 192 rows per serialiser = 13.2Gbps
  - 192 x 192 pixels = 24 serialiser > 300Gbps/ASIC
  - For full frame readout at 533kHz **possible**





Serialiser Eye Diagram

An Ultra-Fast 10Gb/s 64b66b Data Serialiser Back-end in 65nm CMOS Technology

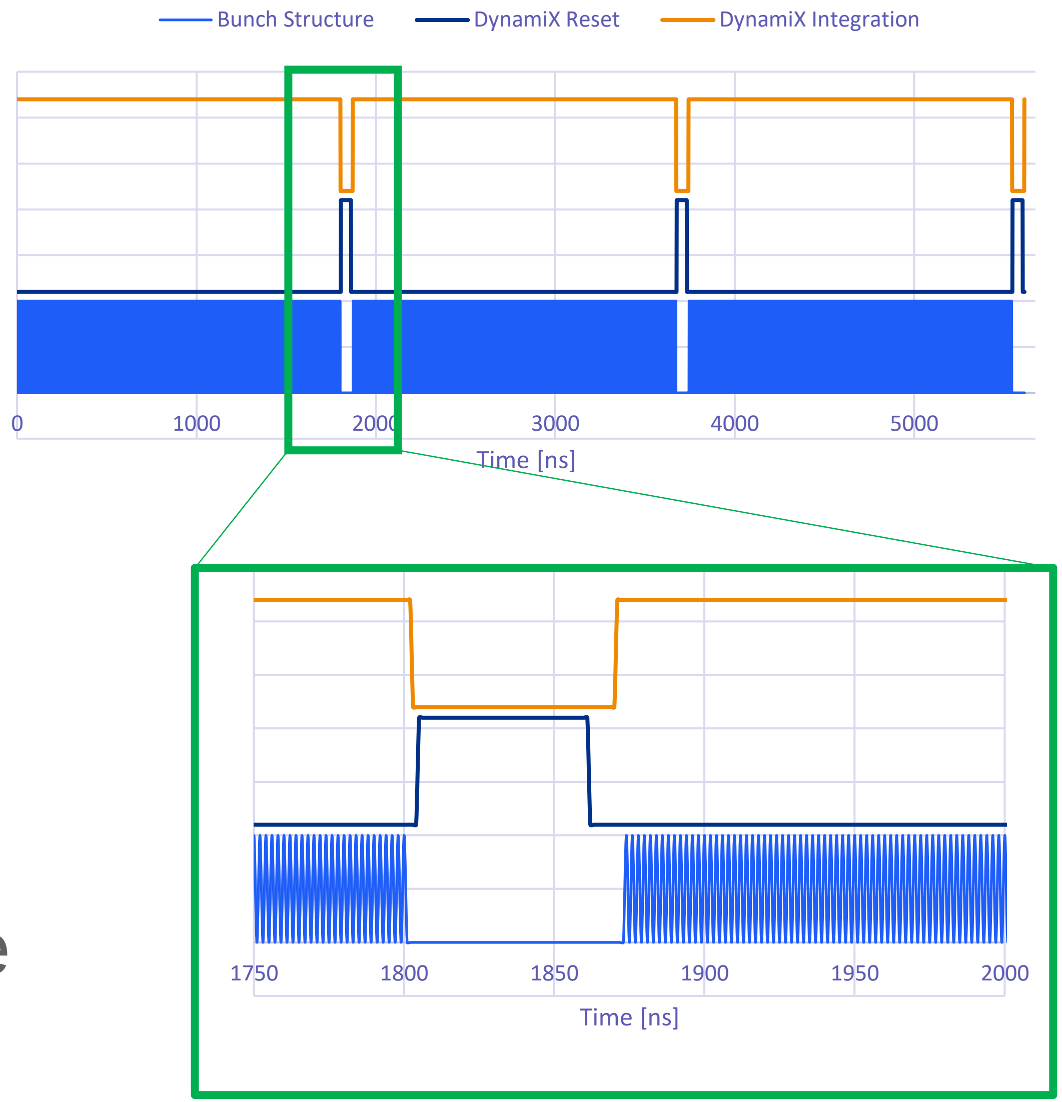
Thomas Gardiner[1]
Science and Technology Facilities Council
Rutherford Appleton Laboratory, Harwell Oxford, Didcot OX11 0QX, UK
E-mail: Thomas.Gardiner@stfc.ac.uk

Proc. TWEPP 2018

Science and Technology Facilities Council

Control

- SPI to set-up and control
- Driven by Synchrotron RF clock (499.68MHz)
- Integration and Reset registers = number of bunches
  - Default 936 for Diamond but programmable
- Match integration to X-ray delivery
- Ideally, need a bunch gap for charge transfer and reset

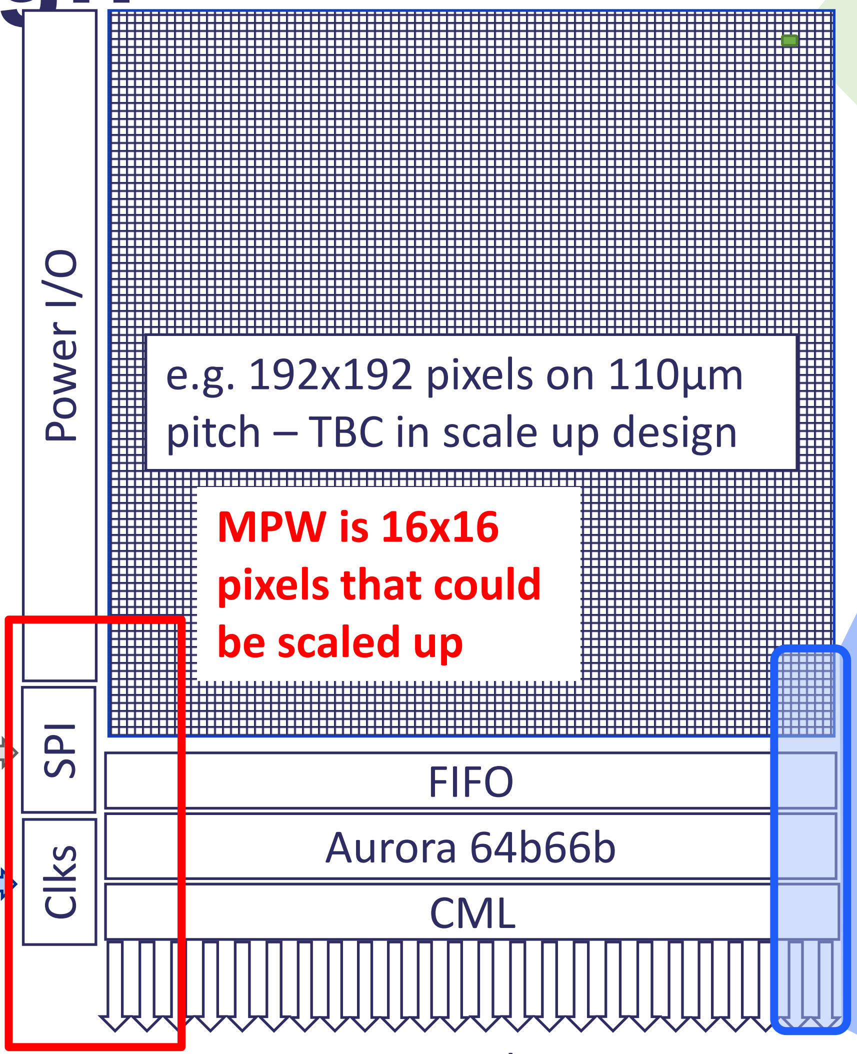


Science and Technology Facilities Council

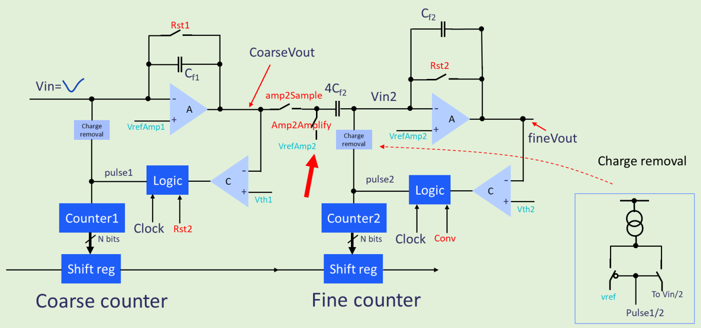
MPW Design

Control Readback for test modes

499.68MHz RF Drives clocks Sync to align to beam



2-stage cancellation per pixel



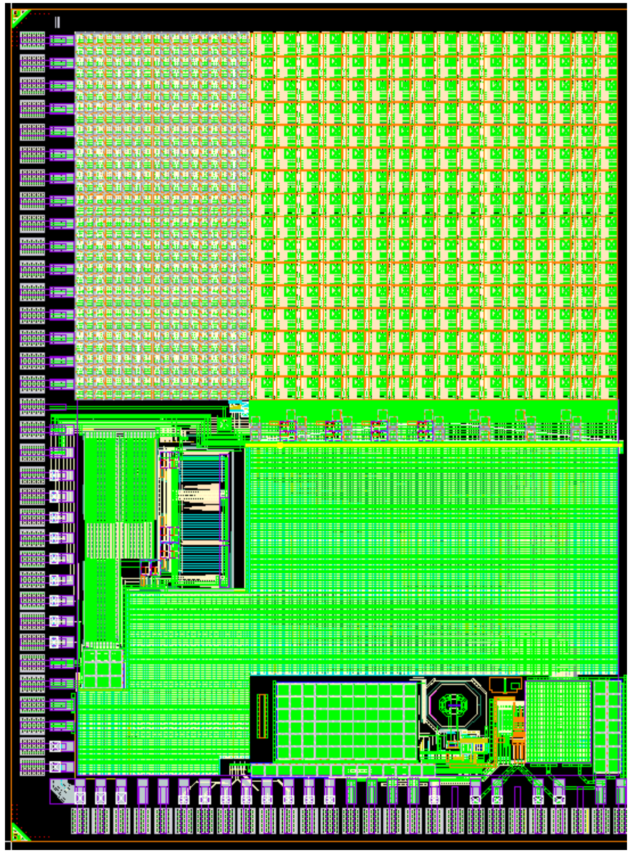
8bit Coarse 7bit Fine + Overflow

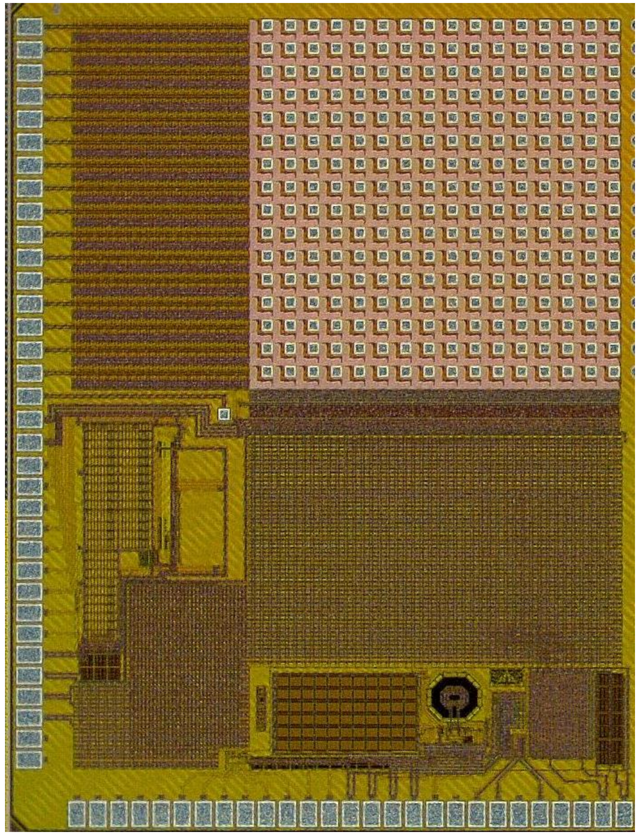
192 Rows
16bit per pixel

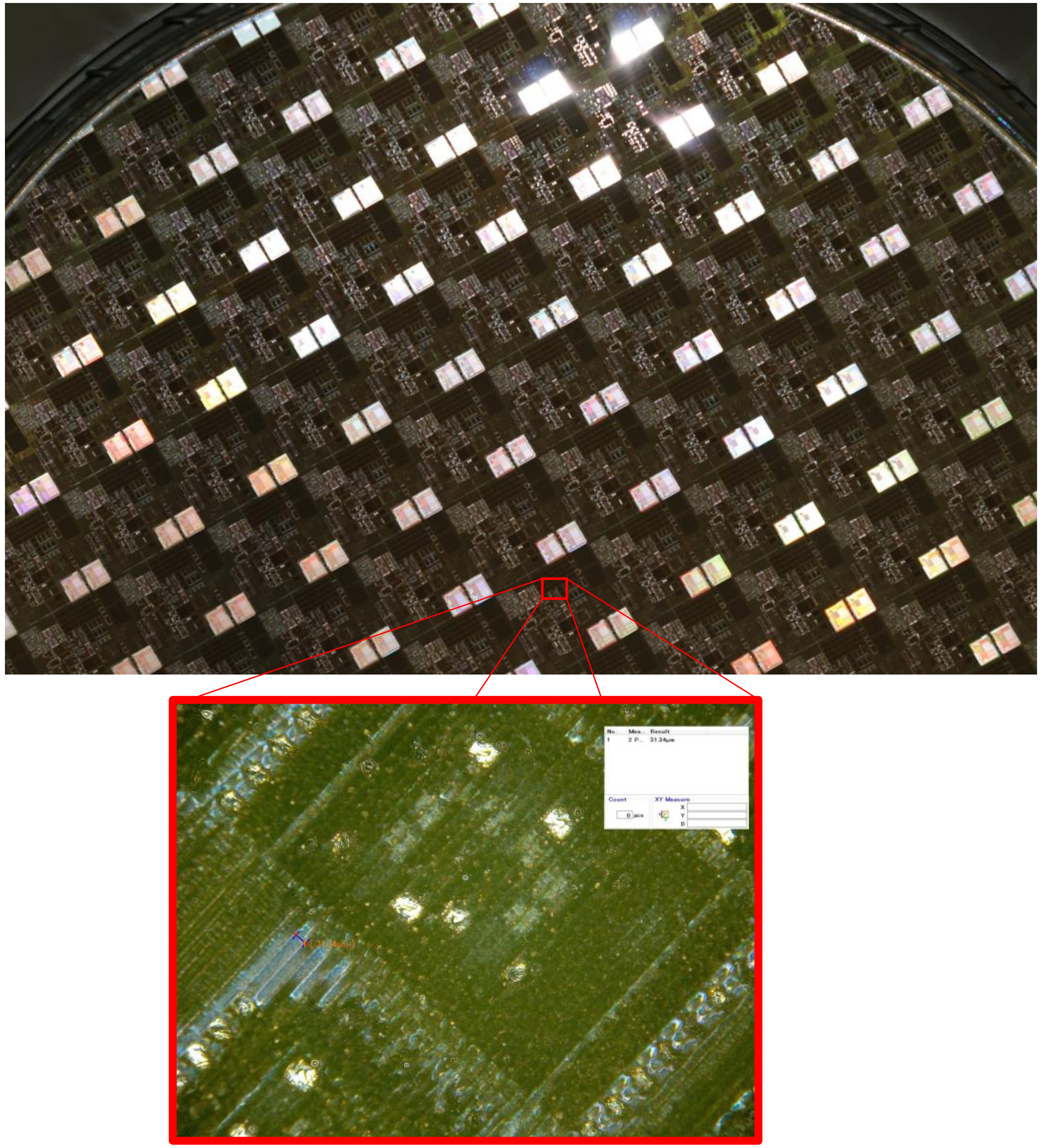
1536 pixels
= 24,576 b
@533.8kHz
(1 turn)
= 13.2Gbps

Room for encoding and clock compensations packets

MPW Design





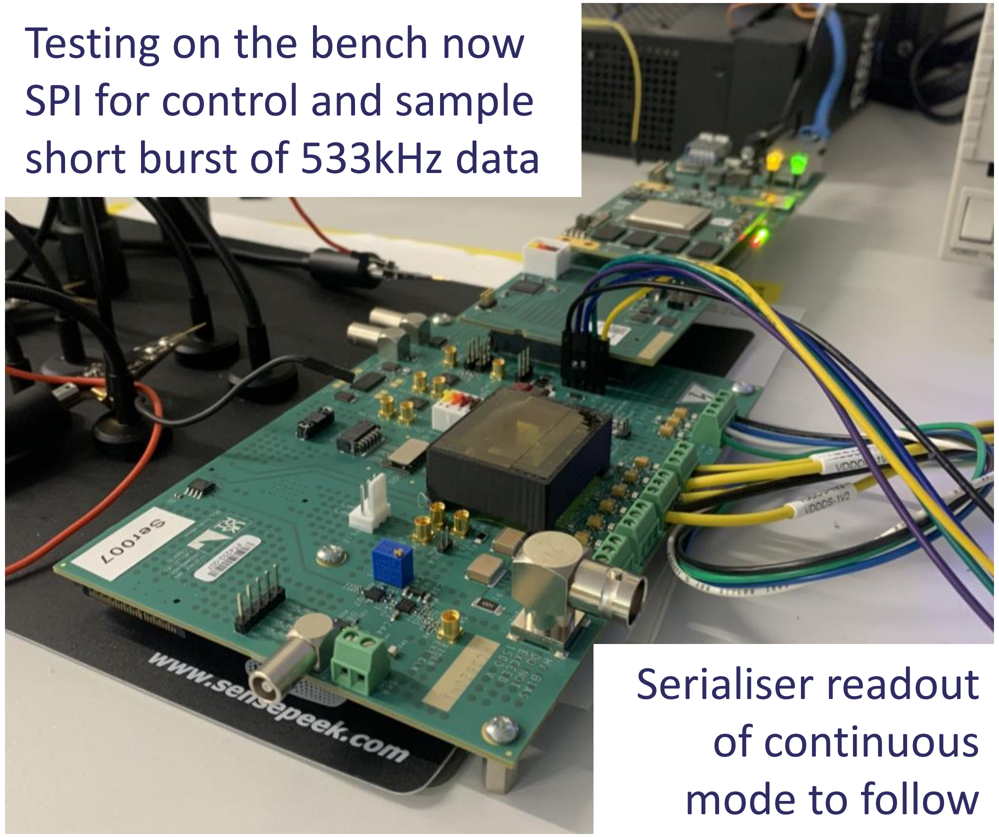


Science and Technology Facilities Council

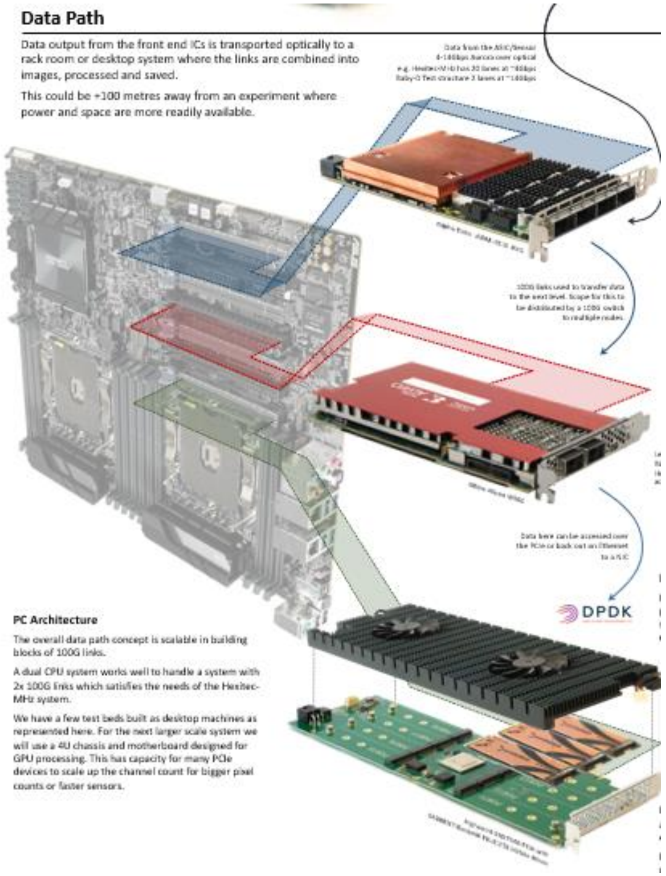
DAQ

Standardised System: Please see
Matthew Hart's poster tomorrow afternoon
Ben Cline's HEXITEC-MHz talk tomorrow

Testing on the bench now
SPI for control and sample
short burst of 533kHz data



Serialiser readout
of continuous
mode to follow



LOKI – standardised control board for ASIC and CMOS sensors

Aurora encoded CML data to optical via Samtec FireFly.

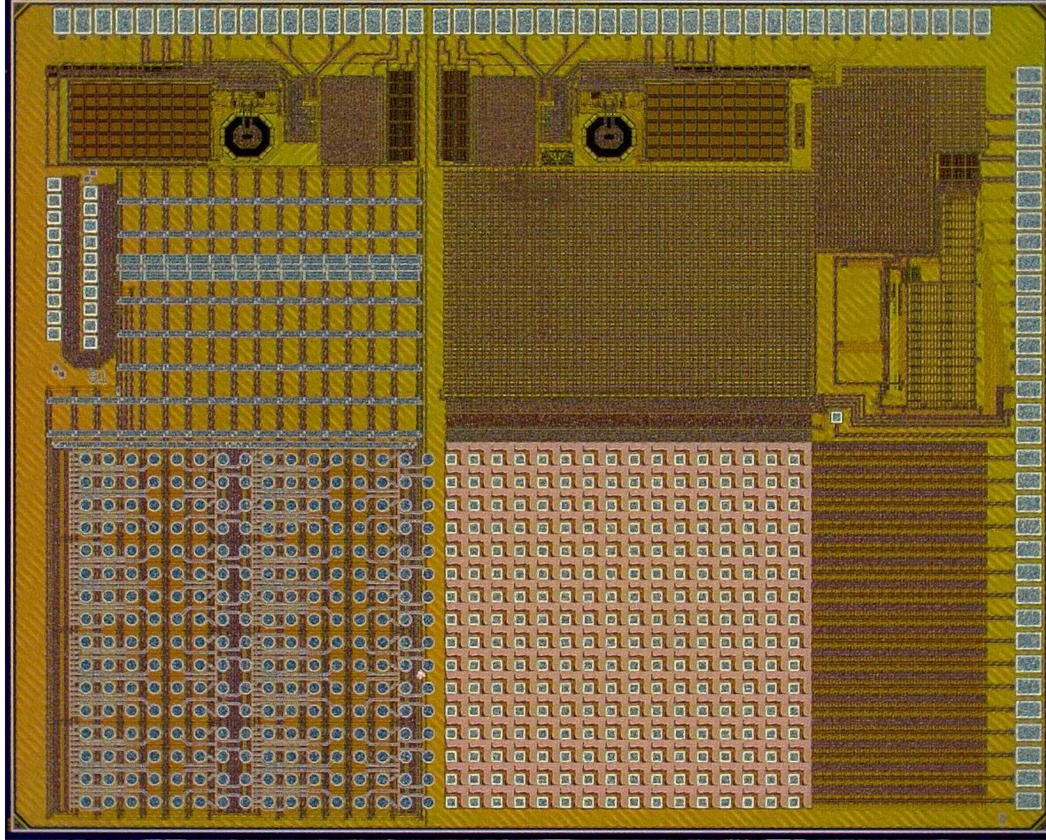
100G ethernet UDP for onward processing and DPDK data storage

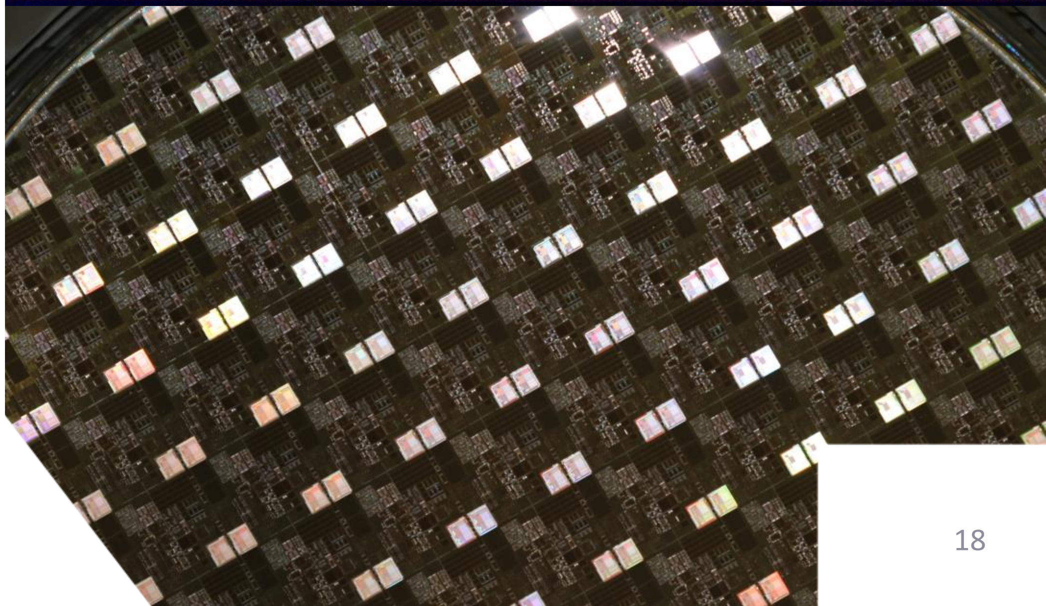
ODIN Data and Control Software framework

Science and Technology Facilities Council

Agenda

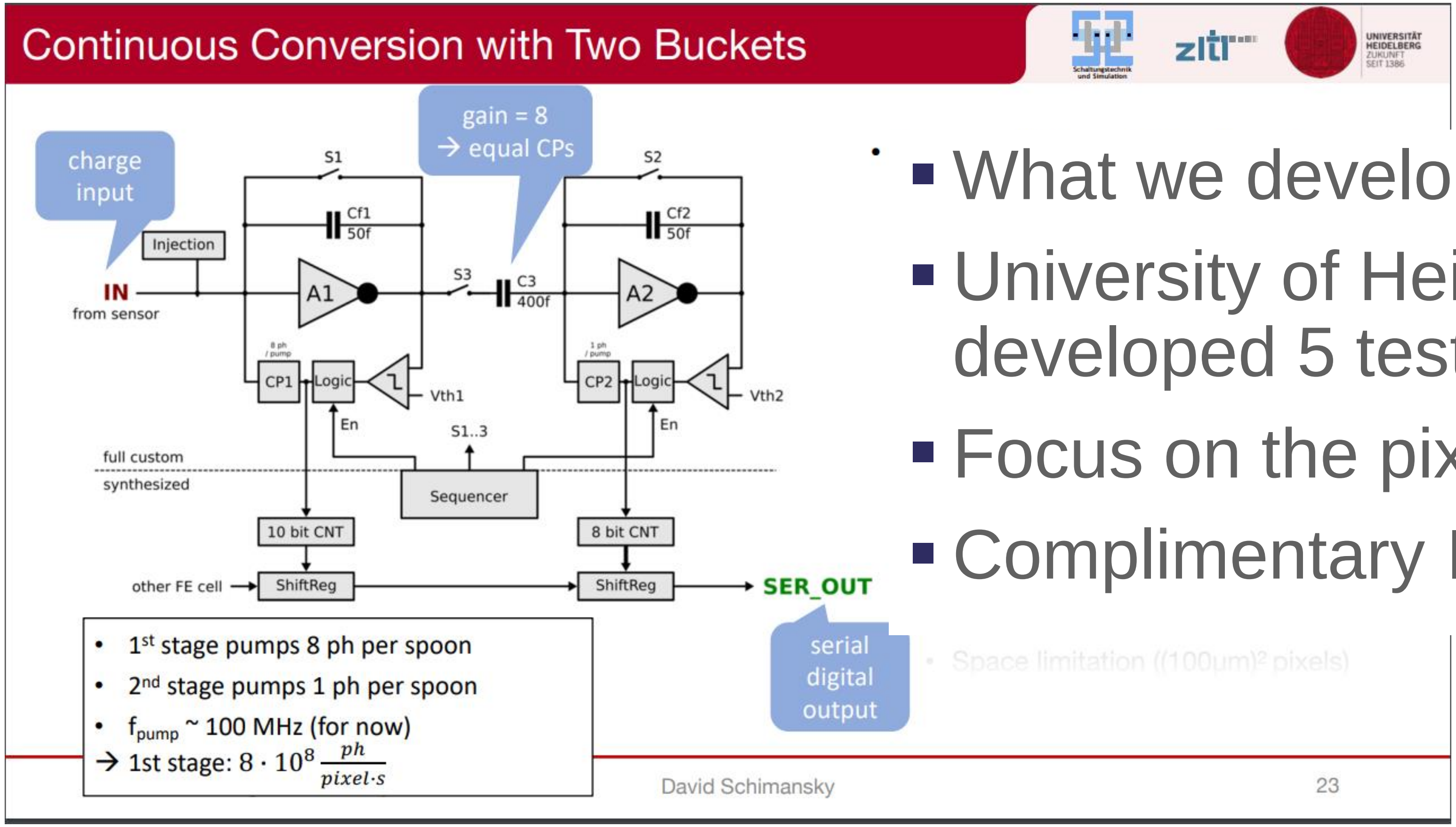
1. **Motivation**
   - STFC and Diamond II
2. **Design Decisions**
   - HF-CZT
   - Pixel Design
3. **Dynamix Design**
   - Pixel Design & High Speed Serialisers
   - MPW ASIC
   - DAQ System
   - MPW Test
4. **Next Steps**
   - Full ASIC scale-up
   - Collaboration
5. **Summary**





Science and Technology Facilities Council

Collaboration

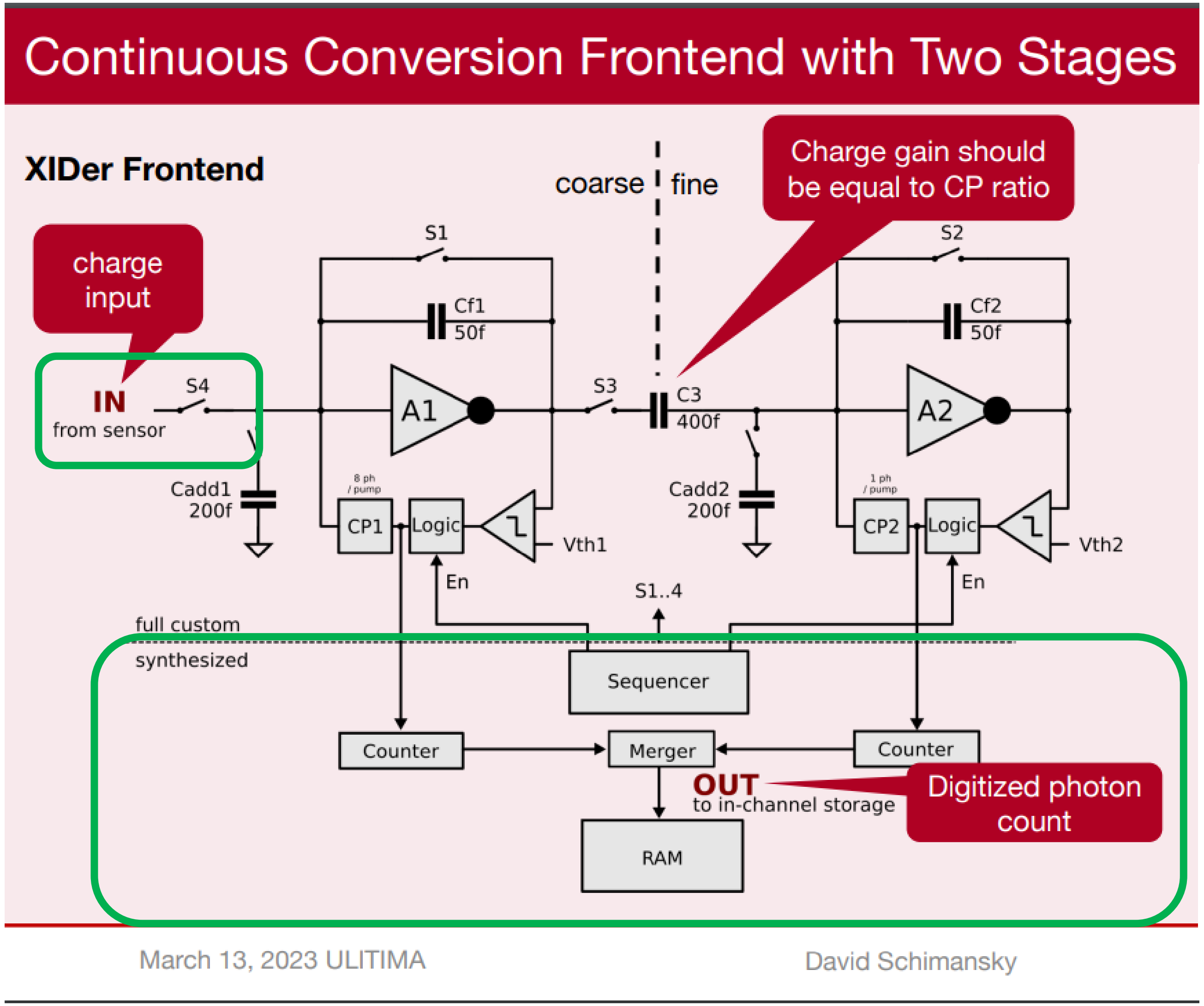


- What we developed is a lot like XIDER
- University of Heidelberg and ESRF developed 5 test devices
- Focus on the pixel optimisation
- Complimentary IP to STFC

Science and Technology Facilities Council

Collaboration

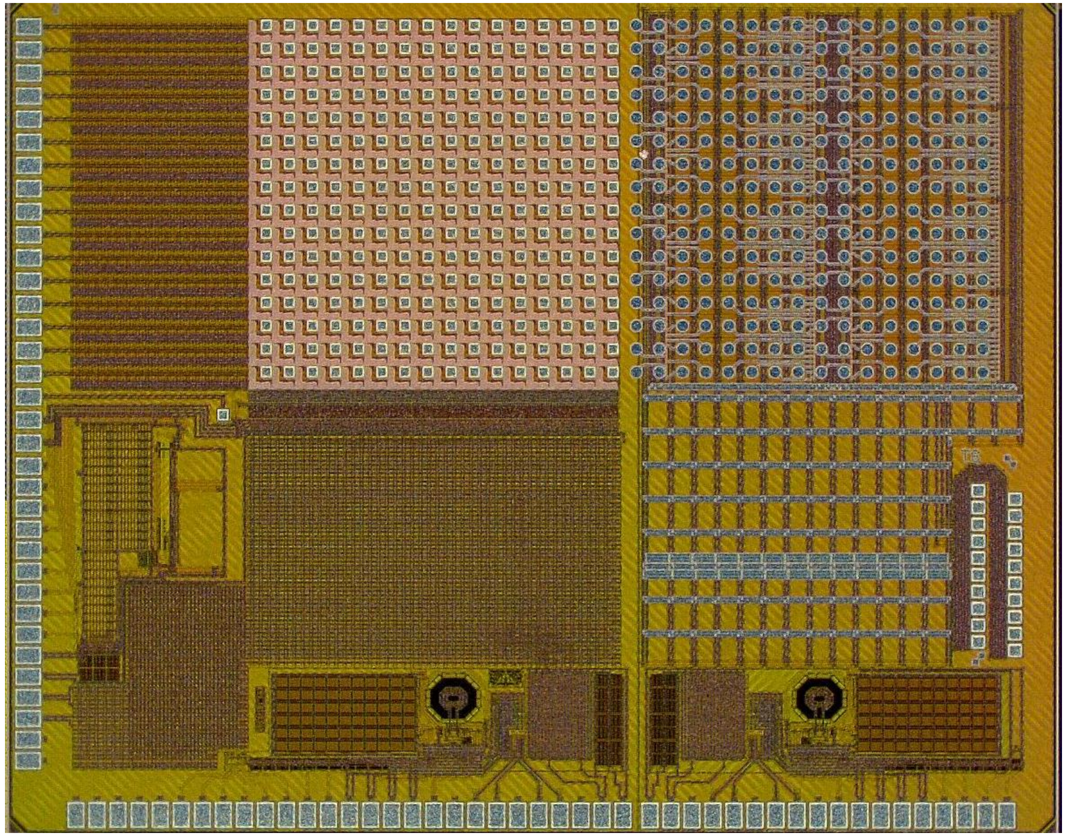
- ✓S4 to do reset in dark
- ✓In pixel logic to merge the pipeline digitisation
- ✓RAM
  - ✓Can store bursts of frames
  - ✓Can sum frames together
  - ✓Histogram
  - ✓Veto



Science and Technology Facilities Council

MPW Collaboration

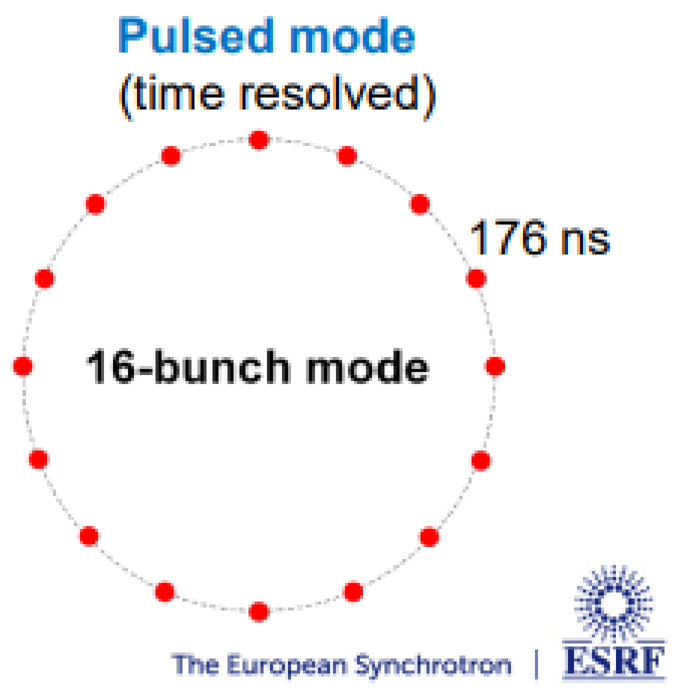
- MPW ASIC is actually
  - DynamiX 16x16 pixel
  - XIDer 16x16 + STFC serialiser
- Pitch is continuous
  - One piece of CZT over the MPW ASIC
  - With support for overhang of the CZT



Science and Technology Facilities Council

Full reticle scale-up

- “STFC Detector Hub” funding scale up to full reticle over next 18 months
- Add adjustable gains/cancellations to match ESRF (75keV) and Diamond (25keV)
- Performance optimisation and scale up
- Aim for adjustable number of serialisers
  - 8 for high rate → ~133kHz = 4 turns of Diamond
- Use RAM to sum frames or capture bursts with aim of 16 bunch mode of ESRF → 5.7MHz
- Interested in other collaborators, requirements… this version and future ones

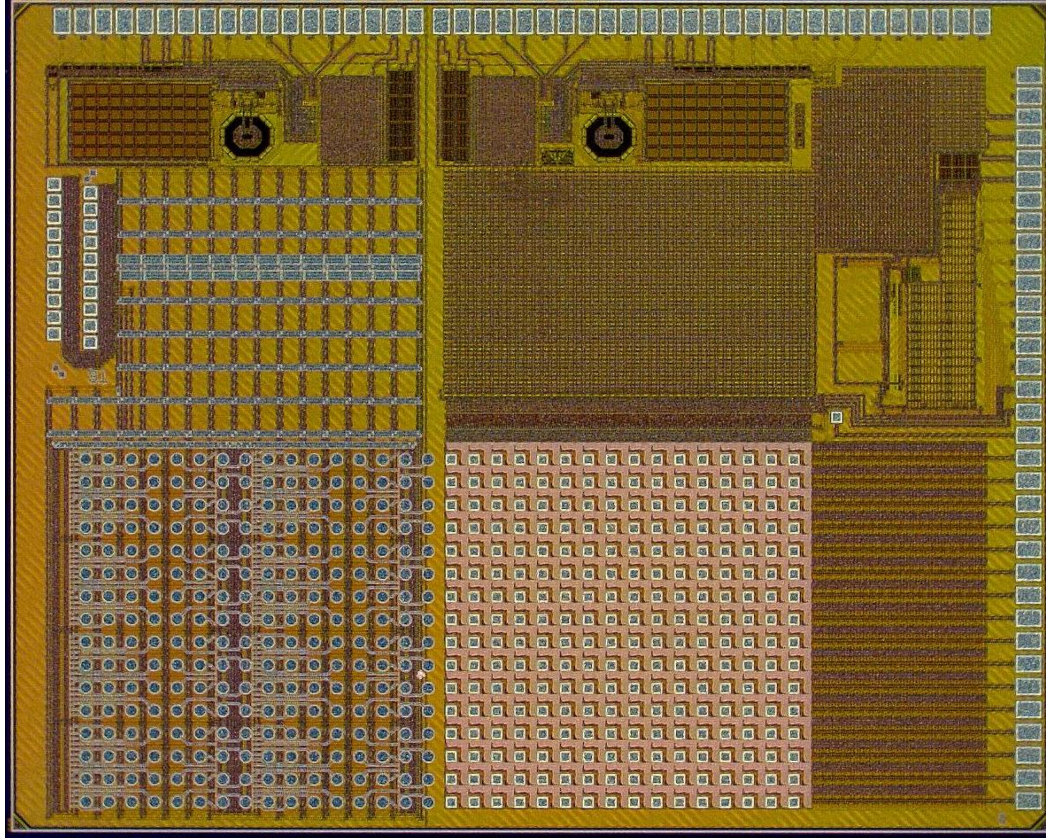


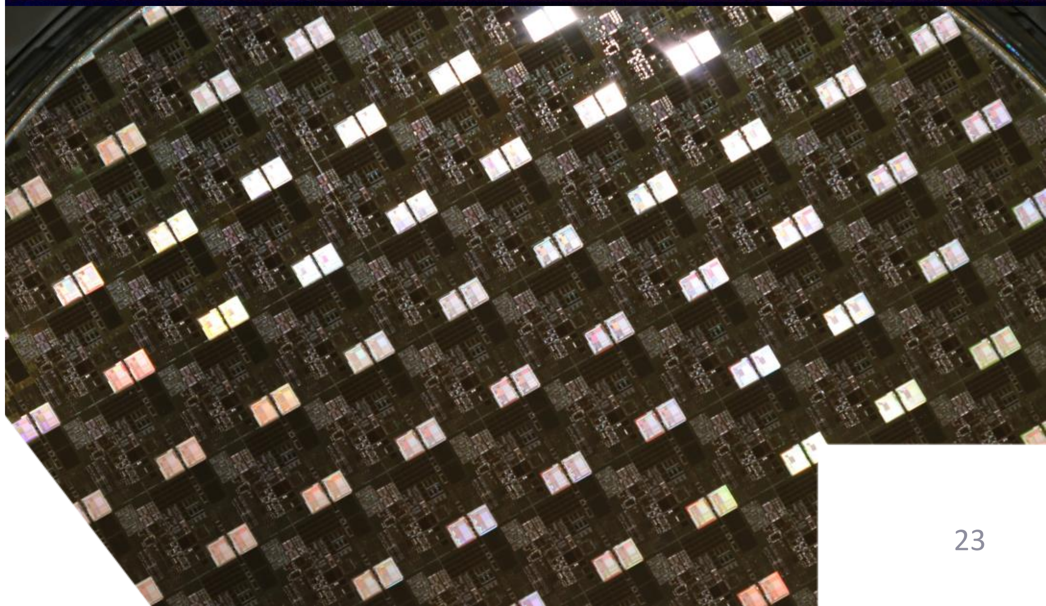
Science and Technology Facilities Council

Summary

- DynamiX is a charge cancellation ASIC focussed on the highest flux (10^{12} ph/mm^2/s @ 25keV) for Diamond II
- Use of HF-CdZnTe from Redlen for hard X-ray energies
- MPW test device manufactured with 16x16 DynamiX and 16x16 XIDER pixels and currently under test
- Plan to test HF-CZT out to 10^{12} ph/mm^2/s at 533kHz frame rate on Diamond
- Full scale ASIC design underway
  - Frame rate limited to ~133kHz to make DAQ and ASIC I/O more manageable
  - Merger of XIDER and DynamiX design with adjustable gains for different energies
- Full Scale ASIC back in 2025

Science and Technology Facilities Council





Acknowledgements

- This is work is from a broad team in STFC and Diamond
  - **ASIC Design Group**
    - Mark Prydderch, Thomas Gardiner, Stephen Bell, Lawrence Jones and Alex Steven
  - **Detector Software Systems**
    - Tim Nicholls, Joseph Nobes, Adam Davis, Dominic Banks
  - **Detector Development**
    - Matthew Hart, Ivan Church, Matthew Veale, Matt Larkin, Rhian Wheater
  - **Electronics Systems Design**
    - Rob Halsall, Matt Roberts, Sooraj Pradeep
  - **Diamond Detector Group**
    - Shane Scully, Eva Gimenez-Navarro, John Matheson
  - **ESRF and Heidelberg XIDER team**
    - Pablo Fajardo, Paolo Busca, Peter Fischer, David Schimansky and Michael Ritzer
- Acknowledge funding from the STFC Centre for Instrumentation and STFC Detector Hub

Science and Technology Facilities Council

ESRF

diamond

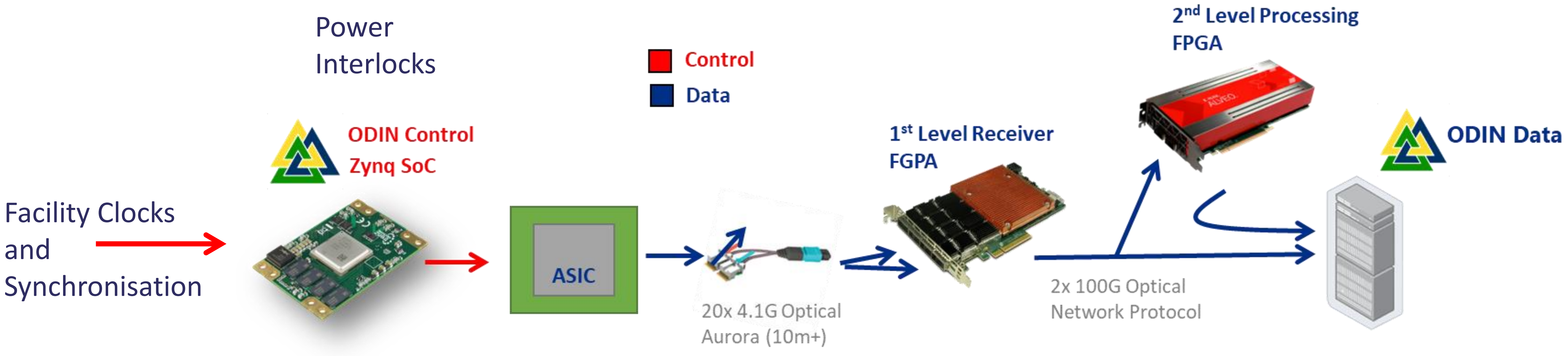
UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

Thank you for listening

Any Questions?

Matt.Wilson@stfc.ac.uk

Data Acquisition Framework



Data output path schematic

- Direct to optical at the detector head
- Optimise for N x 12 lane FireFly and number of AlphaData receivers
- Alveo board for processing on the fly

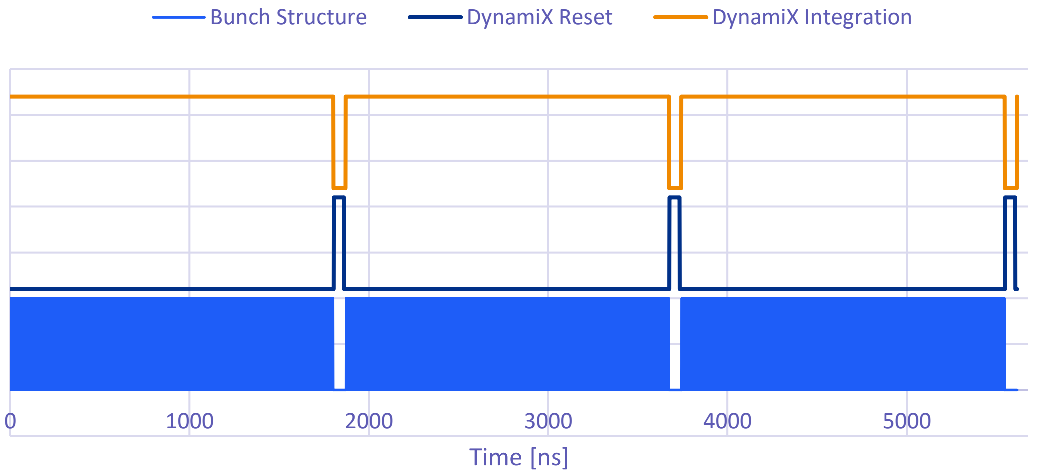
Science and Technology Facilities Council

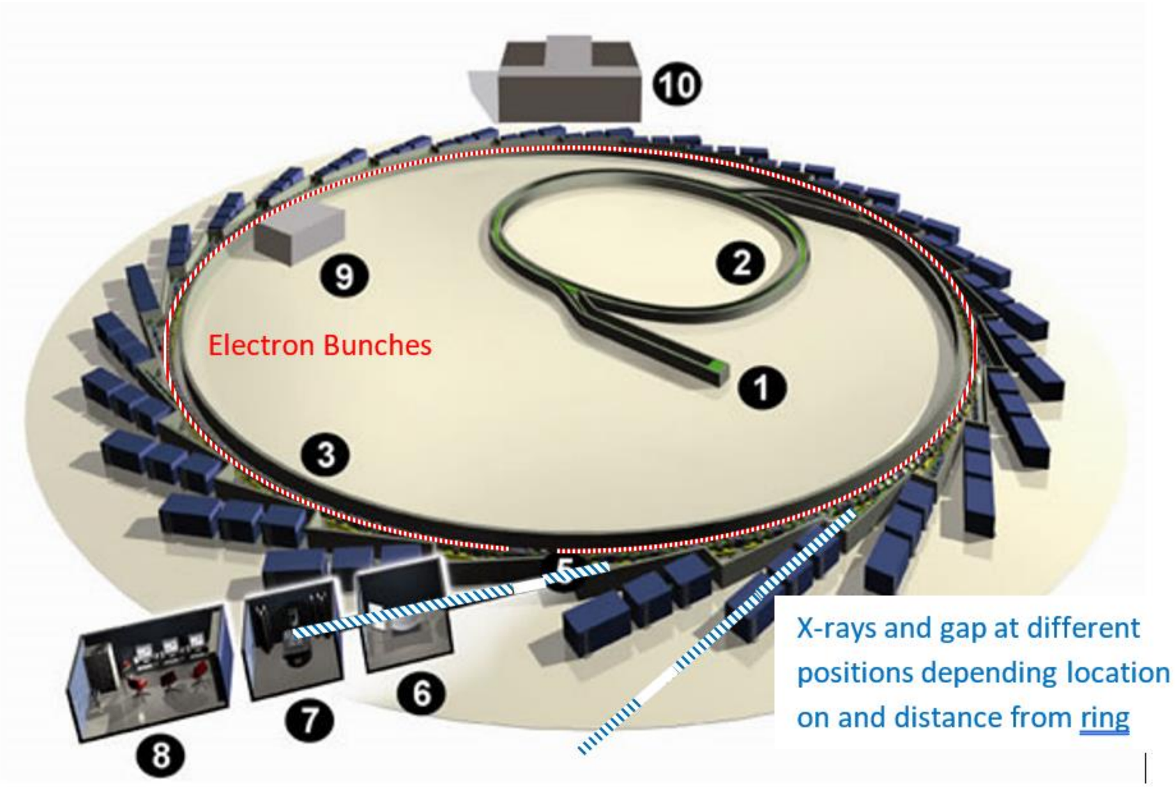
Synchrotrons

Diamond II Fill Pattern

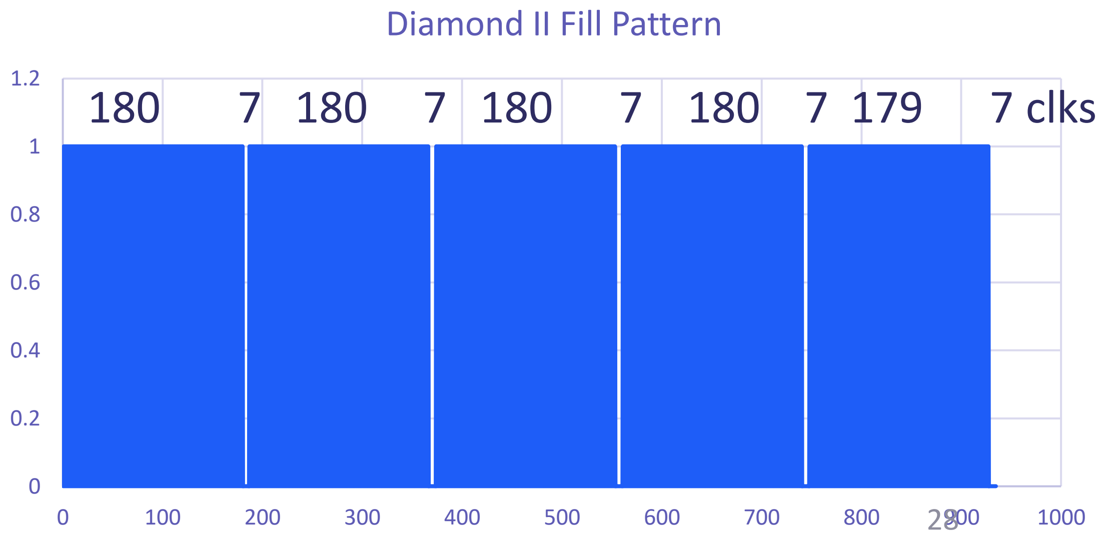
Table 2-18 : Bunch charge and current for different fill patterns. The values for a uniform fill are included for comparison.

Fill pattern	Bunch charge [nC]	Bunch current [mA]
Uniform fill (934 bunches)	0.60	0.32
Standard mode (900 bunches)	0.62	0.33
Hybrid mode (685 bunches)	3.0 (camshaft), 0.82 (train)	1.6 (camshaft), 0.44 (train)





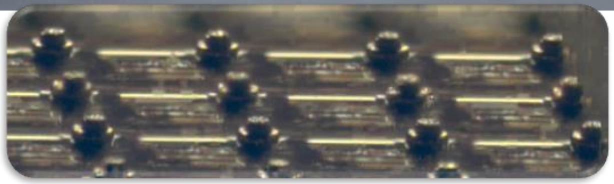
CHANGE OF DIAMOND II FILL PATTERN

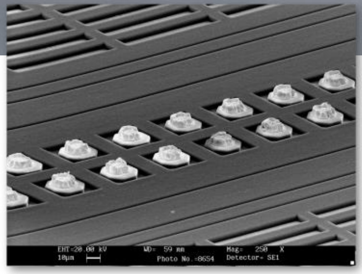


Want resets in the dark

Science and Technology Facilities Council

Detector Facilities – Bonding





Science and
Technology
Facilities Council