PSD13
The 13th International Conference on Position Sensitive Detectors
St. Catherine's College, Oxford, September 3-8, 2023

A 5.12-Gbps serializer circuit for front-end fast readout electronics of silicon pixelated detectors

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Introduction

- The advanced synchrotron radiation sources are major facilities to analyze the formation and evolution of material structure for multidisciplinary researches, in terms of its high luminosity, low emittance, wide energy bandwidth and so on.
- Several advanced synchrotron radiation sources are under construction in China, involving the HEPS (High Energy Photon Source) and SHINE (Shanghai high repetition rate X-ray Free Electron Laser and extreme light facility). They will be major multidisciplinary-researches platforms in China.
- To meet the requirements of pixel detectors in these facility, dedicated pixel readout chips are being developed, such as HEPS-BPIX and HYLITE.
- The full-scale (128×128) pixel readout chip of HYLITE requires a data rate of 4 Gbps. A dedicated high-speed serializer circuit developed in a commercial 130-nm CMOS technology is presented.

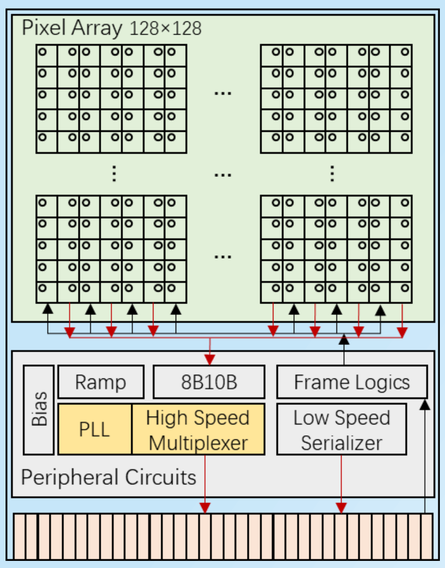

Fig.1. The block diagram of the full-scale HYLITE chip on an engineering run

Circuit design

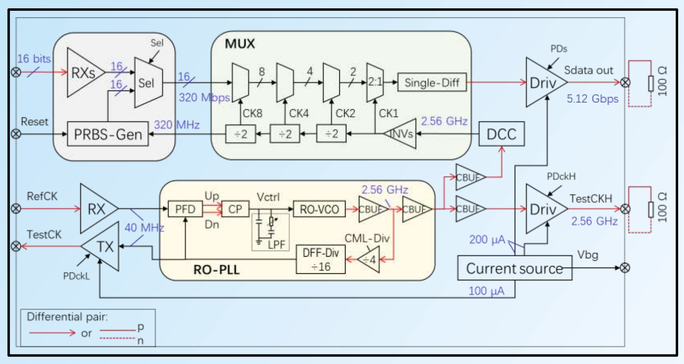

Fig.2. The block diagram of the serializer

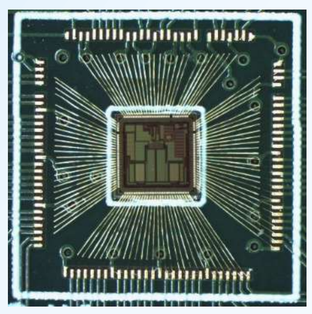

Fig.3. Photomicrographs of a wire-bonded prototype die (2.4 ×2.4 mm²)

The serializer consists of a ring-oscillating based phase locked loop (RO-PLL) , a 16-to-1 multiplexer (MUX), LVDS transceivers (RX/TX), two current mode logic (CML) drivers (Driv), a common current source and a 16-bit parallel PRBS7 generator for built-in self-tests. The TX and Drivs can be turned off (PDckL, PDs and PDckH) to measure the power consumption of the core circuits.

RO-PLL

- *The three pseudo-differential delay cells of the voltage-controlled oscillator (VCO) achieves a free running frequency range from 0.256 to 2.924 GHz at the typical corner.*
- *The phase noise at 1-MHz frequency offset of 2.56 GHz is about –92 dBc/Hz at the worst corner.*
- *The feedback chain consists of a 4-modulus CML divider and a 16-modulus D-flip-flop divider.*

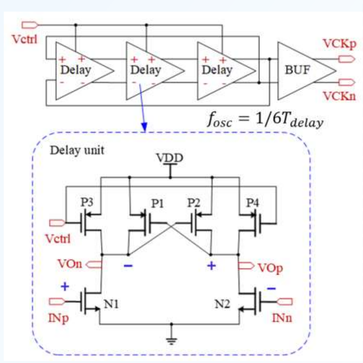

Fig.4a. Scheme of the RO-VCO

The CMOS-logic binary-tree 2:1 unit

- *Both the high and low voltage levels of the clock (CKm) are used to transfer data.*
- *Simulation results shows that the CMOS-logic structure can achieve a data rate up to 5.4 Gbps at the slowest corner, meeting the requirements of the HYLITE.*

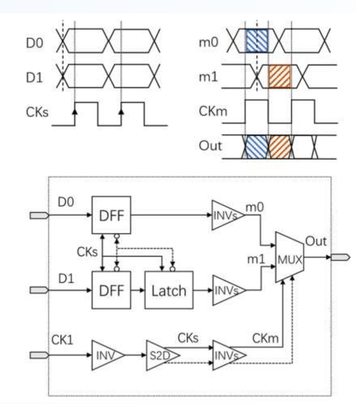

Fig.4b. Scheme of the 2:1 unit of the MUX

Fig.5. The overall timing of the MUX

Measurements and performance

The clock and serial data are tested by a 16-GHz wide-band oscilloscope (LeCroy SDA 816Zi-A) through SMA connectors and coaxial cables. The 1.2-V and 2.5-V power supplies of the die are provided by the TLV1117 chips on the PCB board.

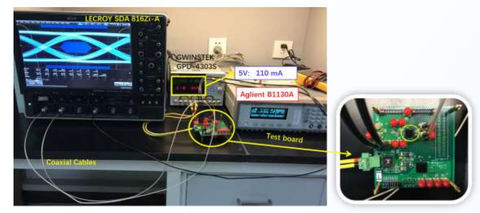

Fig.6. The test setup

Tests of the RO-PLL

- *The measured frequency locking range is from **0.26 GHz to 2.86 GHz**.*
- *The side-band phase noise can be calculated by the equation $PN_{SSB} = (P_{offset}-P_{ref})-10lg(RBW/1Hz)$.*
- *The measured random jitter (RMS) at 2.56 GHz and 0.42-kHz loop bandwidth is less than **1 ps**.*

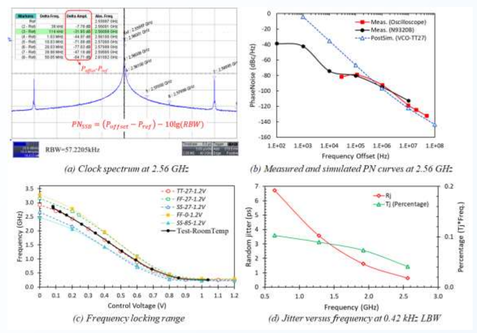

Fig.7. Performance of the RO-PLL

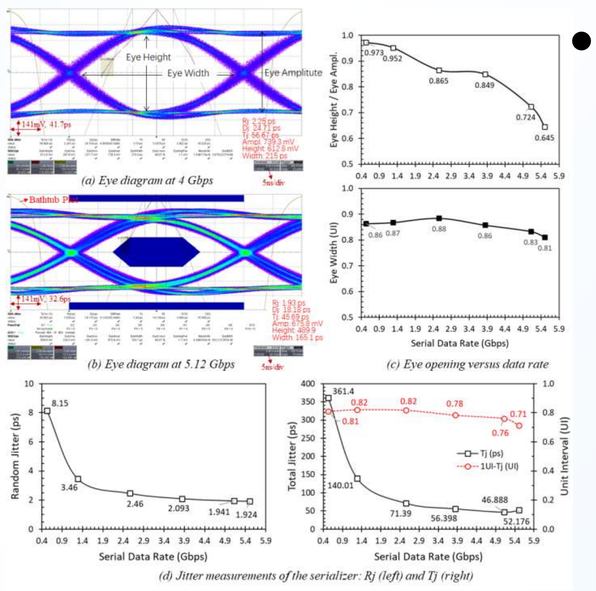

Fig.8. Performance of the serializer

Cable tests

- *As the serial data transmission in the HYLITE readout system uses twinax cables, an 18-inch twinax cable assembly (Samtec HQDP) is used for the performance evaluation.*
- *At 5.12 Gbps, the jitter and eye-diagram performance deteriorate severely.*
- *At **4 Gbps**, the eye-diagram is clear with the width and height of about **0.79 UI** and **392.7 mV** (66.7% of the eye amplitude), and larger jitter values.*

Tests of the serial outputs

- *Wide operating range of **0.52~5.5 Gbps***
- *The measured jitter values at 5.12 Gbps are about **2 ps** and 20 ps for the random and deterministic jitter, and **47 ps** for the total jitter, and the horizontal and vertical eye openings are about 0.84 UI and 72%.*
- *At the maximal 5.504 Gbps, the eye is still open and clear with the total jitter of about 52.2 ps.*

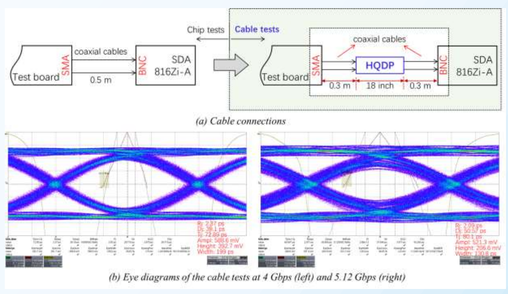

Fig.9. Cable tests

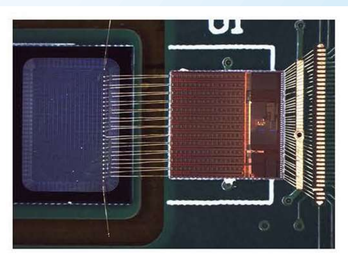

Fig.10. The HYLITE chip wire-boned with the sensor and the test board

Conclusion and outlook

A high-speed low-jitter serializer has been developed for silicon pixel detector readout electronics of high energy physics experiments. It has integrated an RO-PLL, a 16-to-1 multiplexer, standard LVDS and CML interfaces and some auxiliary circuits. The tests of the prototype design show a good performance and meet the current-stage requirements of the HYLITE chip. An HYLITE prototype chip integrated the serializer has been fabricated. The preliminary tests based on FPGA decoding verify the chip can work at a data rate up to 3.125 Gbps. More tests will be taken and the issue needs further research and resolution. Then a full-size chip of HYLITE will be produced.

Acknowledgements

This work was supported in part by the funding of the National Natural Science Foundation of China (No. 12005245, No. 11775244 and No. 12075100). It was also partially funded by the Scientific Instrument Developing Project of the Chinese Academy of Sciences (No. ZDKYYQ20200007), the Youth Innovation Promotion Association of the Chinese Academy of Sciences (No. Y201905), and the State Key Laboratory of Particle Detection and Electronics (No. SKLPDE-ZZ-201915 and No. SKLPDE-ZZ-202315).