An 8-channel Low Power ASIC for Helium-3 Tube Position Sensitive Neutron Detectors

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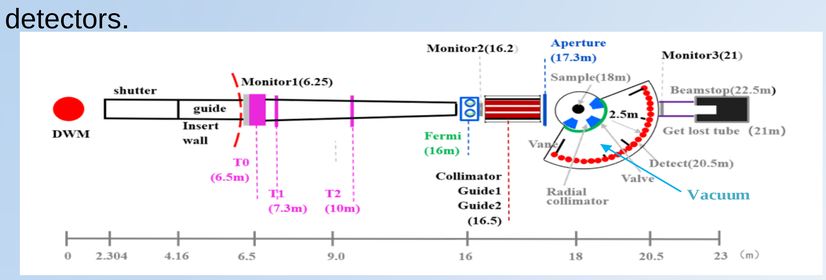
INTRODUCTION

Neutrons are ideal for exploring material dynamics, with neutron scattering pivotal in defense, industry, and research. High-performance neutron sources like CSNS drive demand for improved spectrometers, necessitating a vacuum to reduce neutron-air collisions for precise measurements. The traditional readout electronics, reliant on discrete components and commercial chips, fall short due to high power usage, large size, and limited event rates. These drawbacks impede next-gen neutron spectrometers' demands for performance and operational conditions.

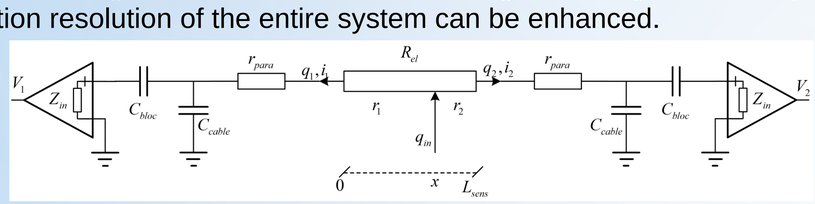
The HEROCV1 chip addresses these challenges. The ASIC optimizes front-end circuits for 3He detectors, aiming to substantially reduce power consumption. By tackling high power usage and heat dissipation issues linked to discrete-component electronics, this chip introduces a foundational research avenue for electronics suited to vacuum-operated ^{3}He neutron detectors.



the Illustration of Inelastic Scattering Spectrometer in CSNS

MODELING OF ^{3}He PSD

Position-sensitive ^{3}He detector utilize charge division methods to calculate the incident neutron position, making the precision of charge measurement directly impact the detector system's position resolution. Simultaneously, the charge equilibrium effect within the ^{3}He detector causes unequal charges at both ends to migrate towards the anode wire, equalizing the charge distribution and thus affecting the accuracy of charge measurement. Through software modeling of the ^{3}He detector's intrinsic characteristics and theoretical analysis of front-end circuit parameters, a circuit-level solution for the aforementioned issues is presented. This solution involves considering factors such as the input impedance and open-loop gain of core operational amplifiers, as well as shaping circuit-level aspects like signal width and structure during the design phase. By doing so, the overall position resolution of the entire system can be enhanced.

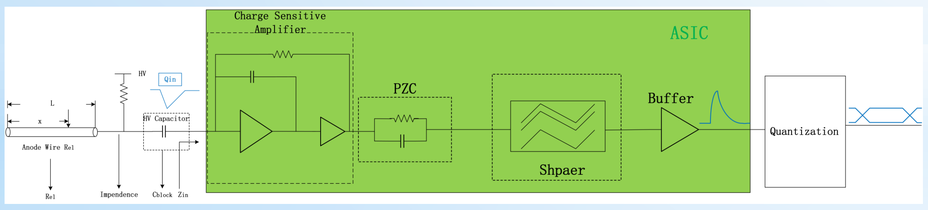


the Equivalent Circuit Model for ^{3}He Tube Detector with Second-Order Effects

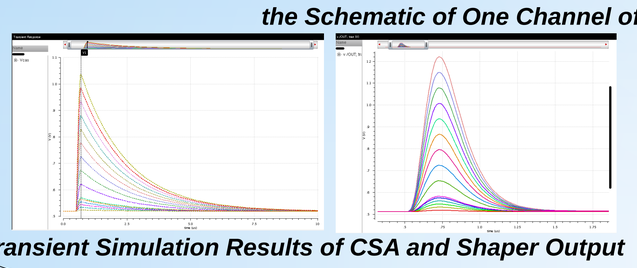
HEROC ASIC

The 8-channel HEROCV1 chip is designed using the Global Foundry 0.18 μm IC process. To minimize front-end circuit power consumption, the input stage employs a telescopic cascode circuit with as few transistors and stages as possible, ultimately providing sufficient open-loop gain and unity gain bandwidth. Simultaneously, a current branch is introduced in the input stage operational amplifier to supply greater current to the input transistor, elevating the transconductance and achieving higher gain.

For the charge-sensitive preamplifier, a "self-bias" NMOS feedback resistor operating in the linear region is utilized as the discharge resistor. This resistor can be externally adjusted to meet different event rate requirements. The shaping circuit incorporates a quasi-Gaussian waveform with conjugate imaginary roots. This structure ensures a narrower signal width compared to other shaping circuit configurations while maintaining consistent rise time, thereby safeguarding the circuit's counting rate capability.



the Schematic of One Channel of HEROCV1



Transient Simulation Results of CSA and Shaper Output

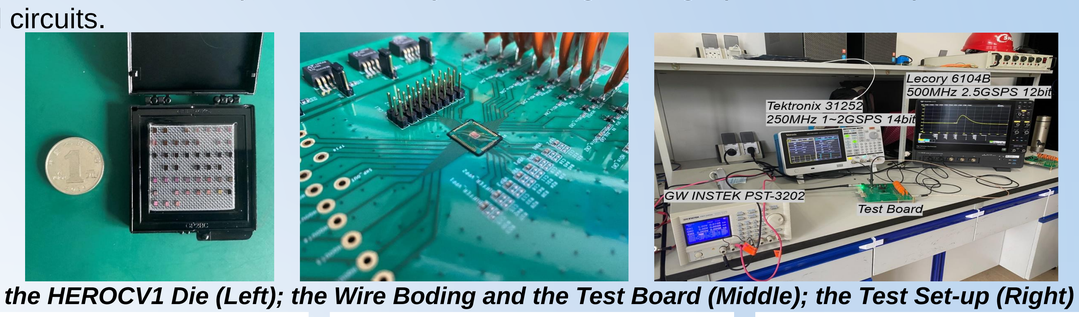
The Layout of HEROCV1. The ASIC integrates 8 channels and the size is 1.4 × 2 mm²

PERFORMANCE

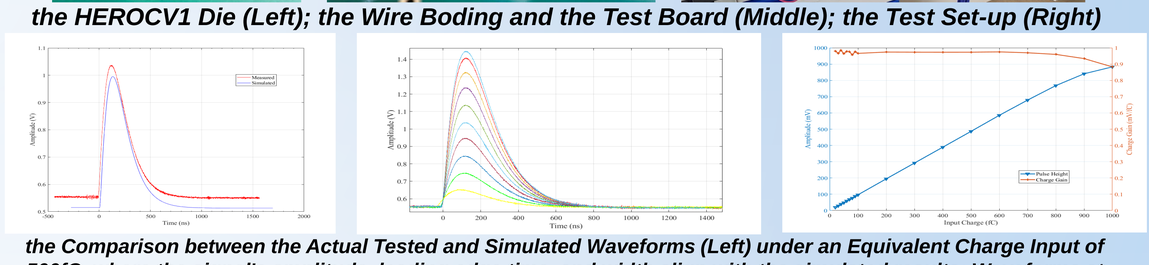
Key Parameters	Measurement Results
Input Dynamic Range	10 fC – 1 pC
Trigger Rate	100 kHz
Equivalent Noise Charge (ENC)	1297 e- @ 15 pF
Integral Nonlinearity (INL)	±3‰
Power	<9.9 mW/Channel

MEASUREMENT RESULTS

After chip assembly, the wire bonding was directly performed to connect the chip to a test circuit board. Comprehensive testing was conducted at the CSNS electronics laboratory using a dedicated ASIC testing platform. In the CSNS source library, a ^{3}He tube detector with a connection length of 30 cm and a pressure of 20 atm was used for detector intercalibration testing with an Am-Be neutron source. The HEROCV1 successfully read and amplified the neutron signals detected by the ^{3}He tube. Compared to the current electronics that based on discrete components and commercial chips, the HEROCV1 ASIC significantly improves key performance indicators (like the trigger rate and the ENC), while substantially reducing power consumption (single-channel power consumption reduced from over 100 mW to below 10 mW, a reduction of over 90%), fundamentally addressing the high power consumption issue in front-end circuits.



the HEROCV1 Die (Left); the Wire Boding and the Test Board (Middle); the Test Set-up (Right)

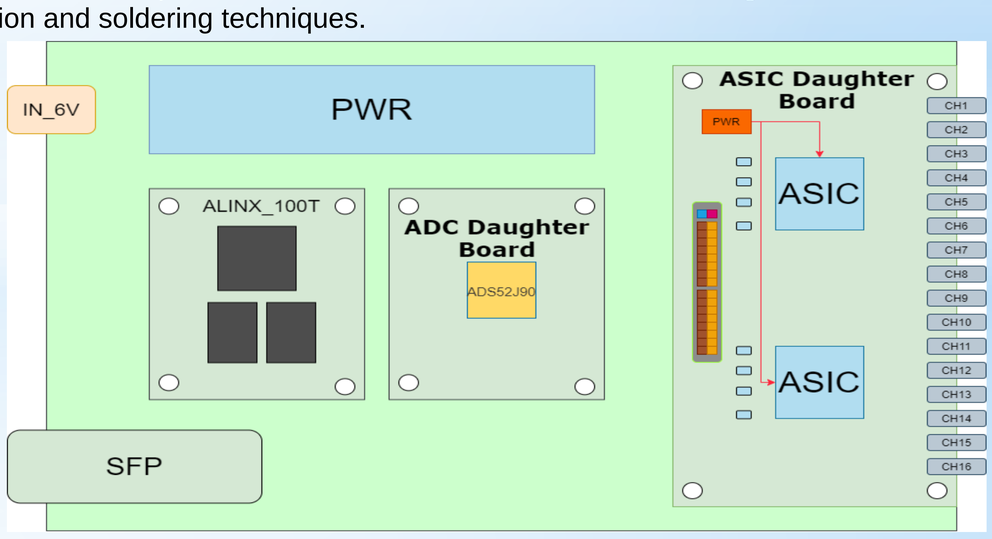


the Comparison between the Actual Tested and Simulated Waveforms (Left) under an Equivalent Charge Input of 500fC, where the signal's amplitude, leading edge time, and width align with the simulated results; Waveforms at different input charge levels from 100fC to 1pC (Middle); the Function Graph of Charge Gain, Output Amplitude, and Input Charge (Right), exhibiting a noticeable gain reduction at 900fC and above. The linear dynamic range meets the charge requirements of 3He tube detectors, and for future spectrometer upgrades and chip versatility, performance improvement in this aspect will be addressed in the next version chip.

HEROCV1 Chip Connected to the Detector - Real-world Image (Left); Neutron Source Test Set-up(Middle); Neutron Signal Output Waveform through ASIC Shown on Oscilloscope (Right)

SYSTEM VALIDATION

Building upon the successful design and testing of the HEROCV1 chip, ongoing efforts focus on validating an integrated system based on the ASIC chip. With the front-end circuit's high power consumption issue resolved, low-power considerations extend to the backend data quantization module and FPGA processing. The complete electronic system will feature 16-channel inputs, supporting 8 connected 3He tubes. Powered by a single 6V source, the system's overall power consumption will be under 2.6 W, making it suitable for vacuum environments. Addressing cable complexities, a minimal number of cables will transmit multi-channel digital signals to the backend for processing. Furthermore, attention is given to effective heat dissipation from the vacuum environment through considerations of PCB fabrication and soldering techniques.



the Block Diagram of the Integrated Electronics System Based on the HEROCV1 Chip

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