PSD13

St. Catherine's College
September 3-8, 2023

UNIVERSITY OF OXFORD

The monolithic ASIC for the high precision Preshower detector of the FASER experiment at the LHC

FASER

D. Ferrere, University of Geneva
On behalf of the FASER collaboration

UNIVERSITÉ DE GENÈVE
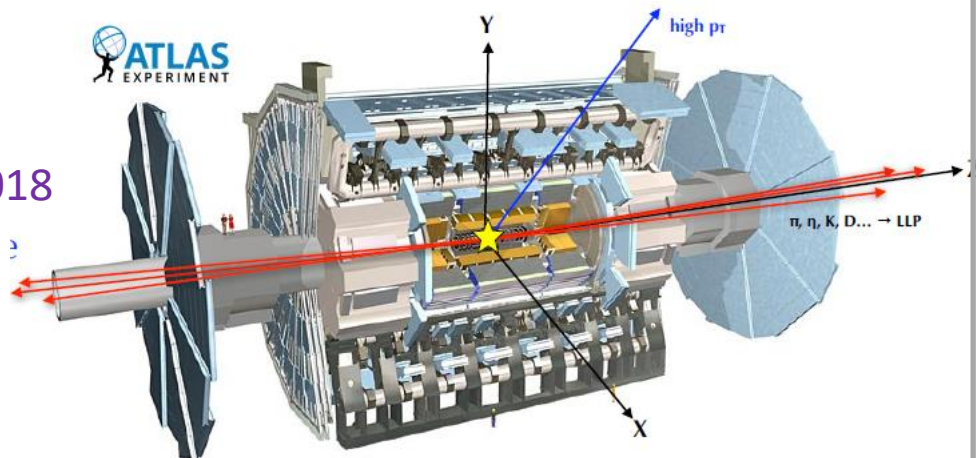FACULTÉ DES SCIENCES

FASER - The ForwArd Search ExpeRiment

It is a new LHC experimented located 480 m downstream from the ATLAS IP

Aim to search for light and very weakly-interacting new particles (LLP) produced in the LHC collisions in ATLAS IP:
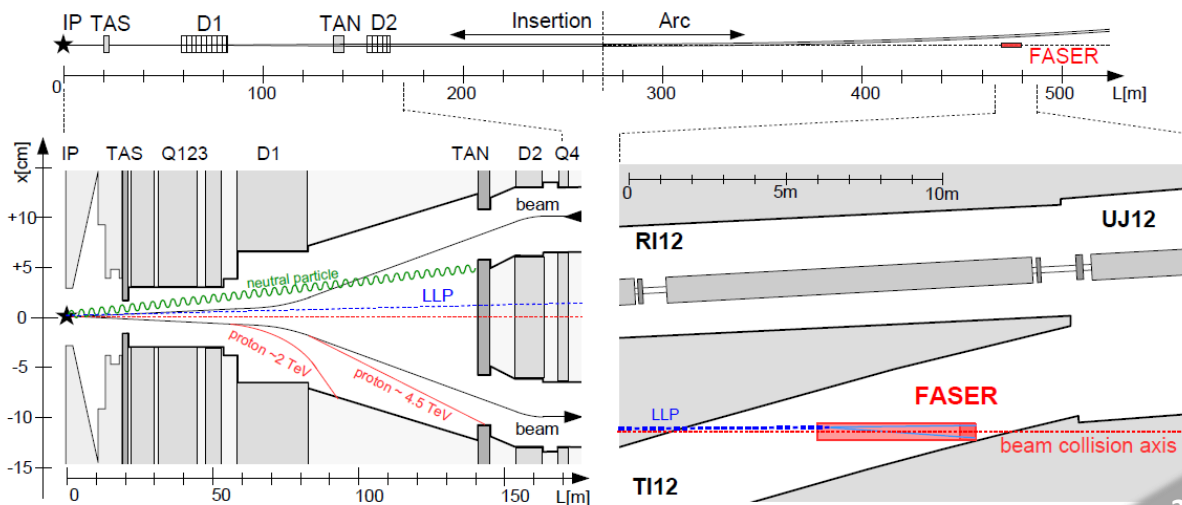→ light and highly boosted particles (TeV scale) are extremely collimated, in the very forward direction (θ ~< 1mrad)

- Technical Proposal was approved in Dec 2018
- Refurbishment of TI12 completed in 2020
- Detector installation and commissioning completed early in 2022
- Started to take data at Run 3 (last year)

→ Preliminary results published this year: collider neutrino observations and dark photon search

FASERnu in addition allow studying the huge neutrinos flux (e, μ and τ) with up to TeV scale
→ 1st time in a collider experiment

FASER Detector

arXiv:2207.11427

320mm
320mm
82 mm

SCT module plane

Veto station for neutrino physics

Tracker stations in spectrometer

To ATLAS IP

1.5m long decay volume

Pre-shower and backsplash stopper

Tracker "backbone"

Emulsion detector

Veto station

Interface tracker station

Trigger / timing station

Calorimeter

Trigger / pre-shower station

Magnets 0.57 T dipoles

y

x

z
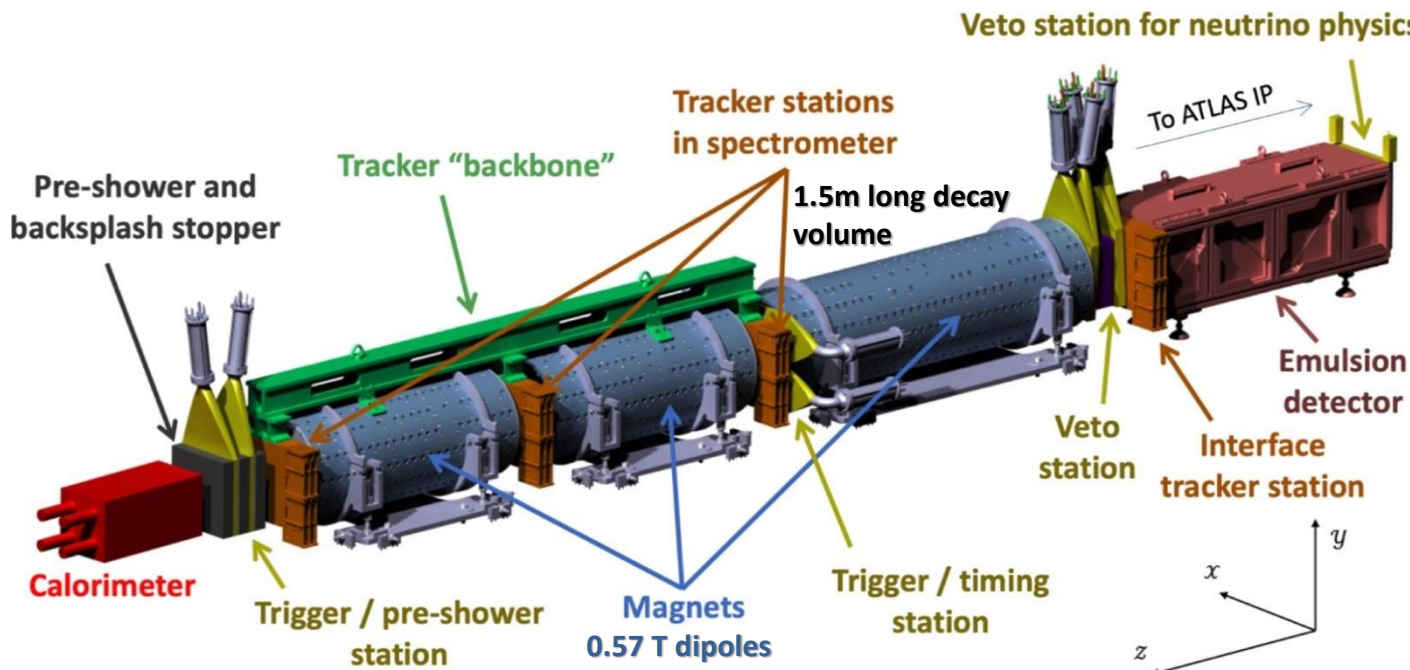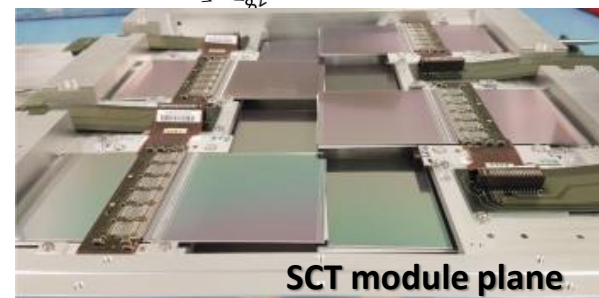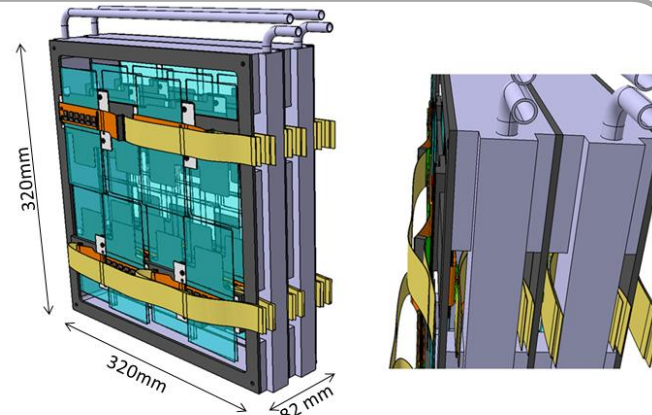
**Physics potential mainly driven by Axion-like particles (ALP):**

→ Identification with a decay in the final state of two photons very closely spaced (0.2 to 1 mm) not detectable with the current detector configuration

A new preshower detector with high granularity should allow:

- **Tagging di-photons events** and providing significant extension of FASER's sensitivity reach in the ALP phase-space
- Enhance detection capability and maximizing the sensitivity to new physics, for instance:
  - LLPs that can decay into final states with photons involving neutral pions ($V \rightarrow \gamma\pi^0 \rightarrow 3\gamma$)
  - Scalar particle that only couples to up quark with final decay either $\pi^0\pi^0 \rightarrow 4\gamma$ or $\pi^+\pi^-$

Technical proposal (CERN-LHCC-2022-006)

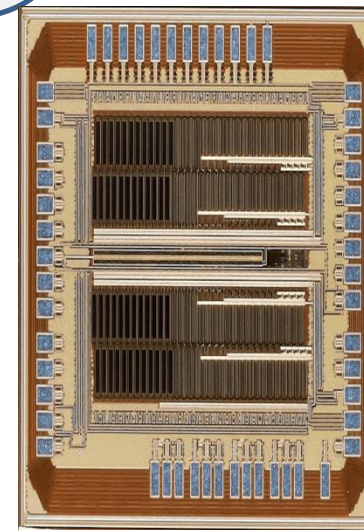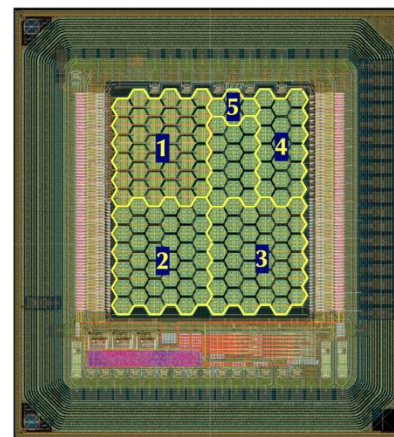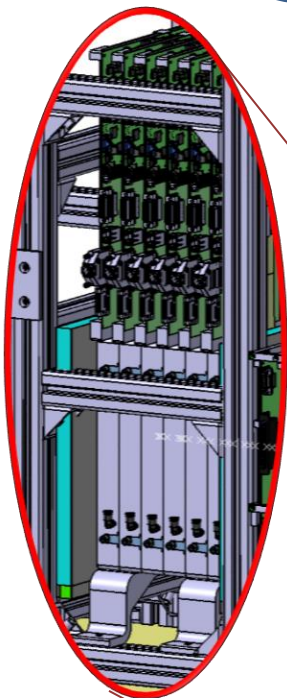**Very collimated photons which would be highly energetic (O(100GeV – 5TeV))**
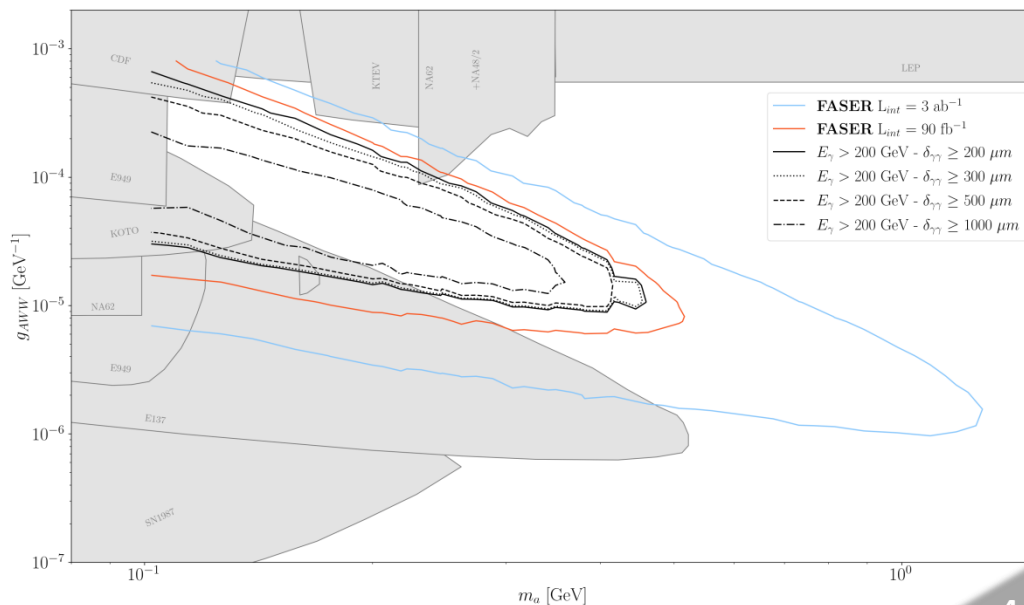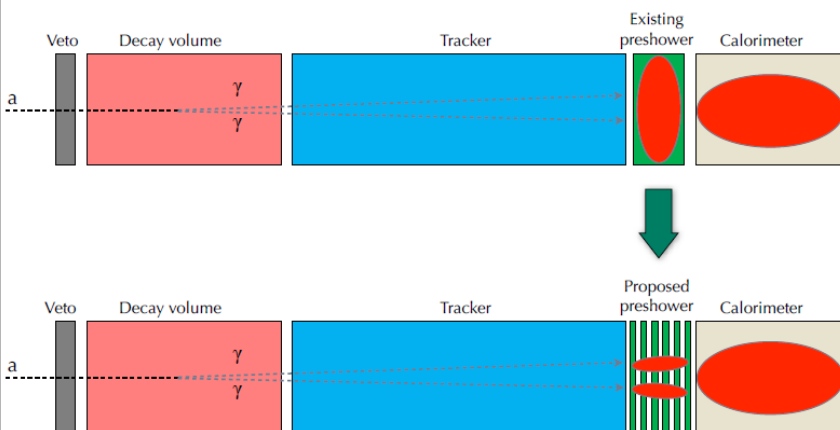
The Birth of the new Preshower Detector

FASER
Enhance detection performances with high granularity detection
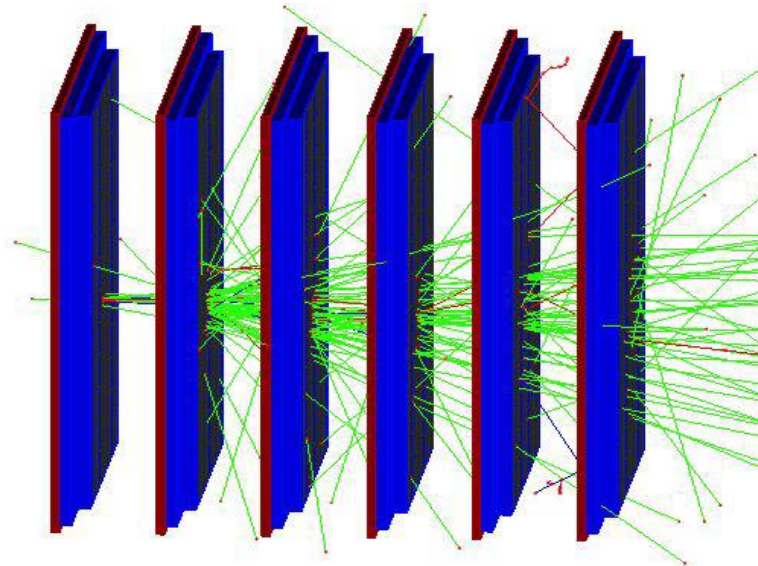
UniGe
R&D on MAPS with SiGe technology

About 8 years of research and development work with SiGe at UniGe and many publications mainly for pixel timing detector

2019 *JINST* **14** P02009
2019 *JINST* **14** P07013
2019 *JINST* **14** P11008
2020 *JINST* **15** P11025
2021 JINST **16** P12038
2022 JINST **17** P02019
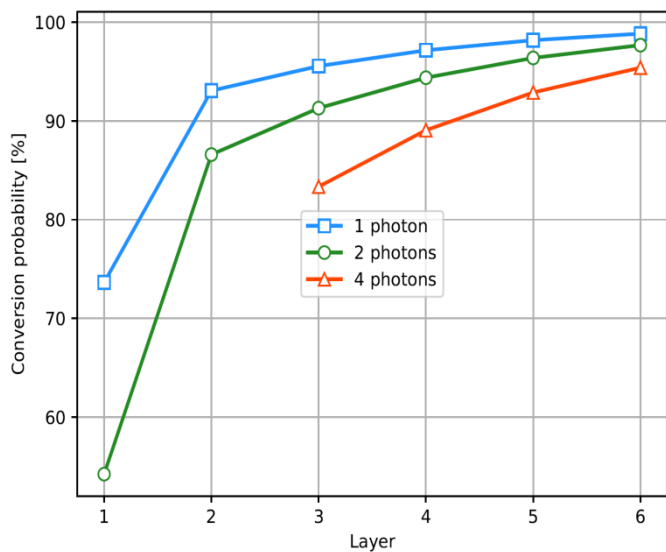2023 *JINST* **18** P03047

*G. Iacobucci talk on Thursday...*

Simulation implemented in ALLPIX2

- ➢ **Up to 6 instrumented layers** with up to 6 X0 of Tungsten
- ➢ **Realistic hexagonal pixel** matrix with ~100 μm pitch
- ➢ MC simulations → 60% of Tungsten absorber distributed in the 1st 2 layers.
- ➢ **Charge measurement simulation**

Two photons signatures of E=1 TeV, 500 μm separation

Conversion probability

Plane 3

Plane 6
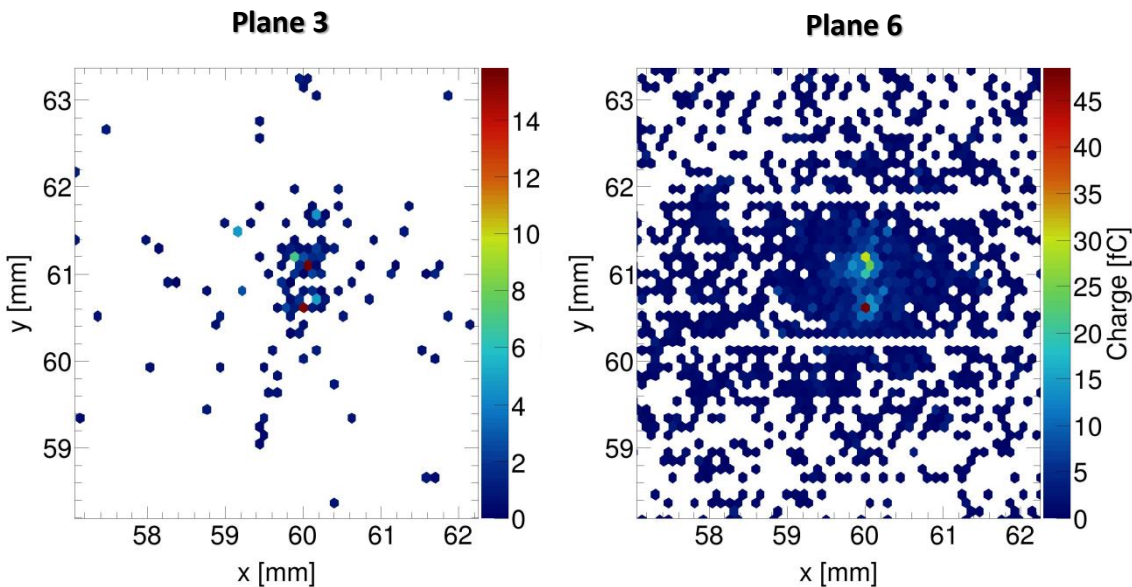
FASER Monolithic Pixel Asic

SiGe HBT technology 130 nm BiCMOS produced at IHP

7. Digital electronics be placed in a separate deep-nwell to improve noise robustness (non-sensitive region).

6. Analog electronics in pixel.

5. Pixel and electronic deep n-wells are kept at positive low voltage.

$\rho = 220 \ \Omega cm$

1. Wafer thinned down to 150 μm

150 μm

2. High resistivity substrate as detection volume. Depletion: 50 μm

3. Electronics inside the guard-ring, isolated from substrate using deep n-well.

4. Negative High Voltage applied to the substrate.
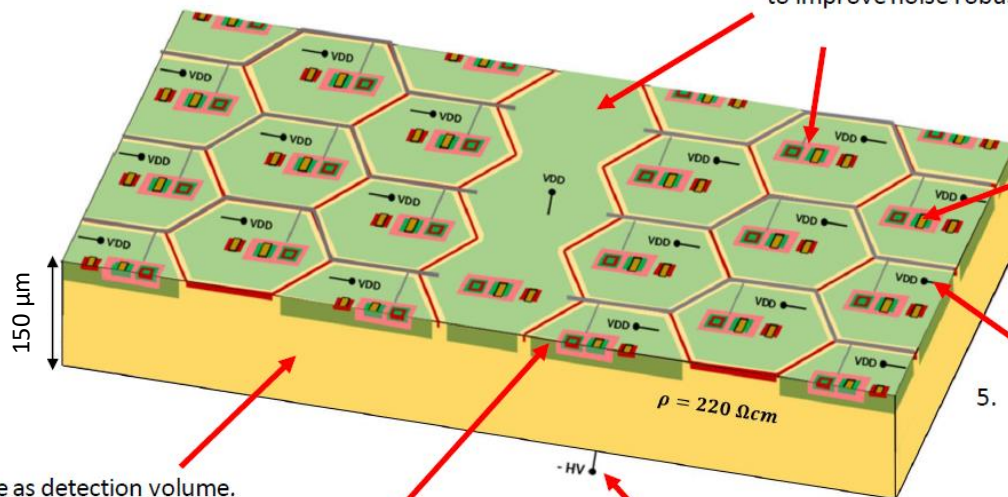
Digital column   40 μm
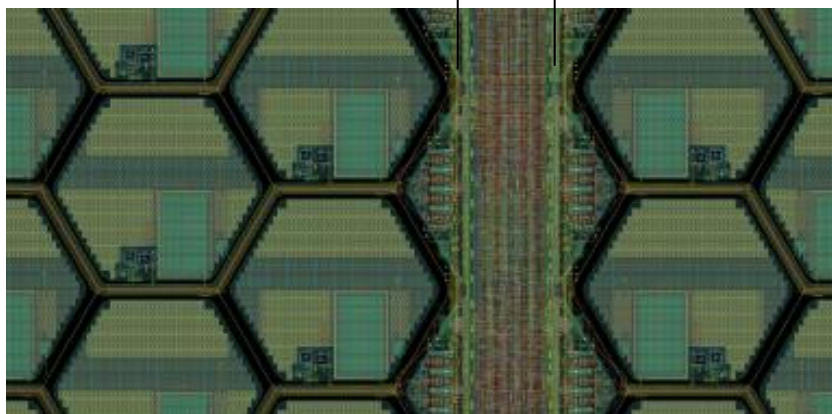
| Main chip features	
Pixel (hexagonal) pitch	~ 100 μm
Pixel dynamic range	0.5 – 65 fC
Cluster size	~1000 pixels
Readout time	200 μs
Power consumption	<~150 mW/cm^2
Time resolution	~200 ps

Sensor-Asic Features

FASER final chip features:

- Chip size of 2.2 x 1.5 cm2, with matrix size of 208 x 128 pixels (26'624 total pixels)
- 13 super-columns which consist of:
    - i. An active region
    - ii. A digital column in the middle (40 µm width) which is inactive
    - iii. A super-column (SC) is composed of 8 super-pixels (SP) of 16x16 pixels
- The dead area in the periphery consists of:
    - 720 µm on the readout side for the digital processing and I/Os
    - 270 µm on the guard ring sides
- Chip is backside metalized for the uniformity of the electric field

SC0 SC1 SC2 SC12

SP of 16x16 pixels

40 µm

Super-pixel

Pixel

65 µm

Pre-production and Final Asic
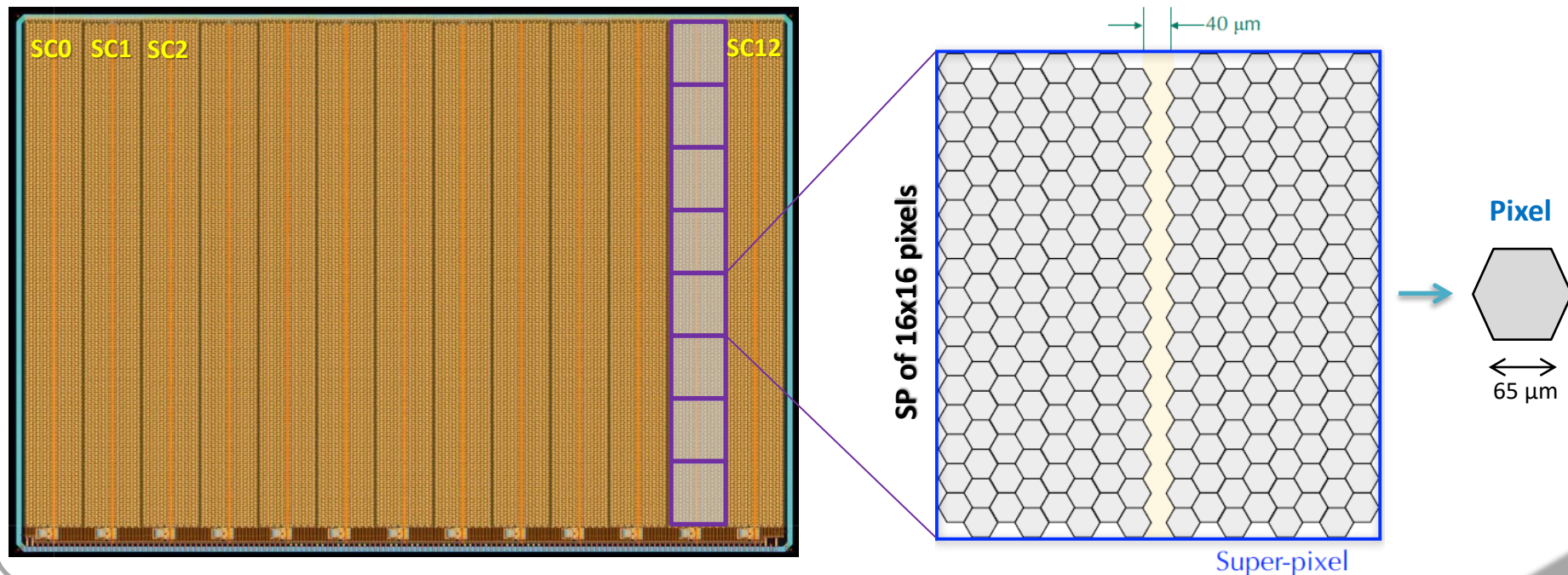
> **Pre-production → Delivered in June 2022**

- 6 wafers:
    - 3 Epi-layer + low resistivity
    - 3 standard wafer (50 Ω.cm)
    - Thickness: 300 μm

- Reticle size: 2.4 x 1.5 cm^2
- Extensively tested in the lab and TB
    - Allowed improving features for final chip design
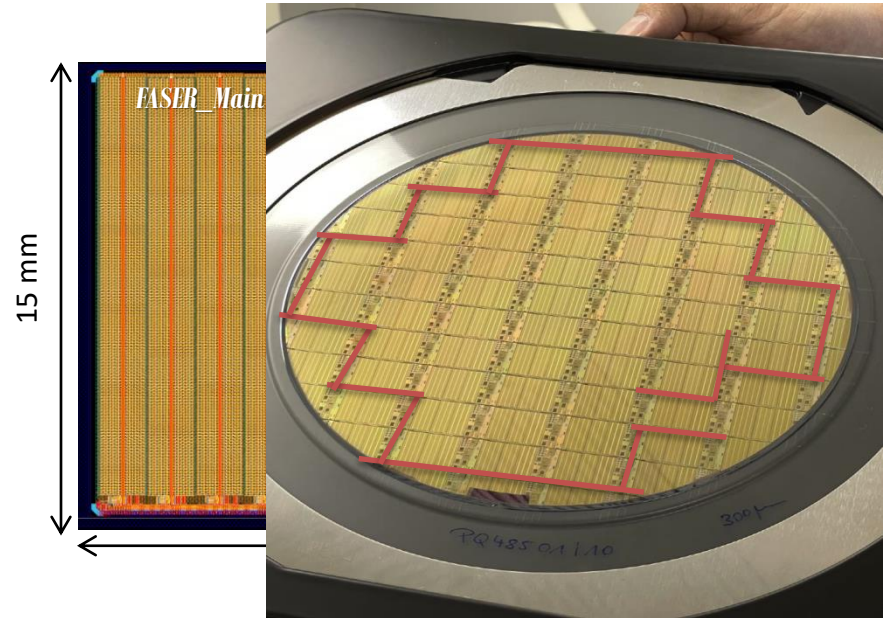
> **Final asic → Submission was on May 23rd**

- Standard wafer (200 Ω.cm)
- 20 wafers ordered
- Bad features corrected: Leakage in analog memory drift, Retriggering during memory reset and low thresholds …
- Improvement was made: Charge to TOT distribution, power distribution, …
- Consolidation and improvement of the digital architecture
- Complete verification was made before submission

Delivery expected in Jan 24


FASER_Main

15 mm

53 reticles / wafer

TOT [ns]

9
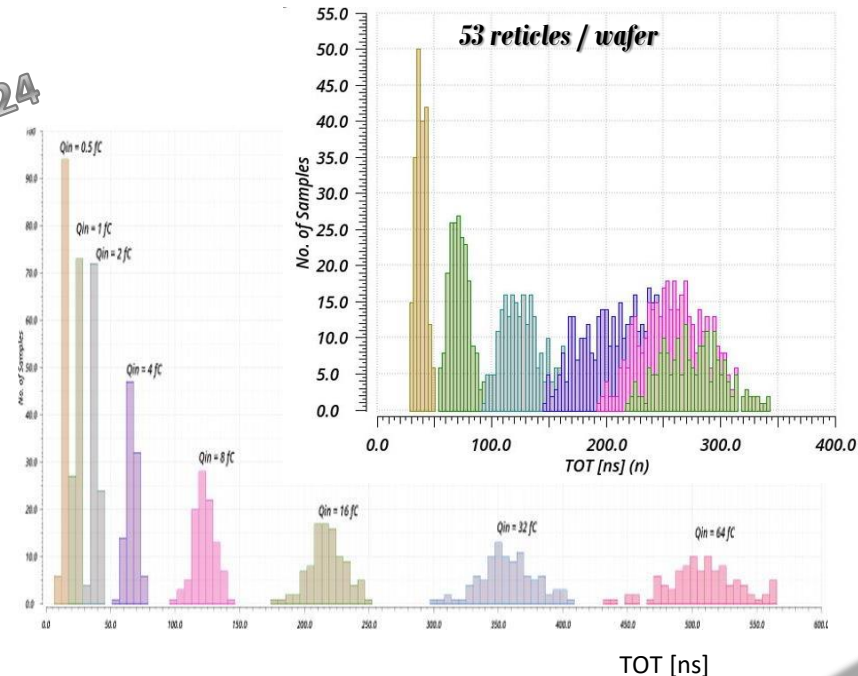
Tests performed so far:

- **IV working perfectly ok** for all types
- V1 analog circuit is not working → Powering line issue
- **V2 and V3 are working ok** in the lab and provide data stream and FAST_OR signals
- **Chip configuration** (via SPI) works **ok**
- **Data decoding works ok**
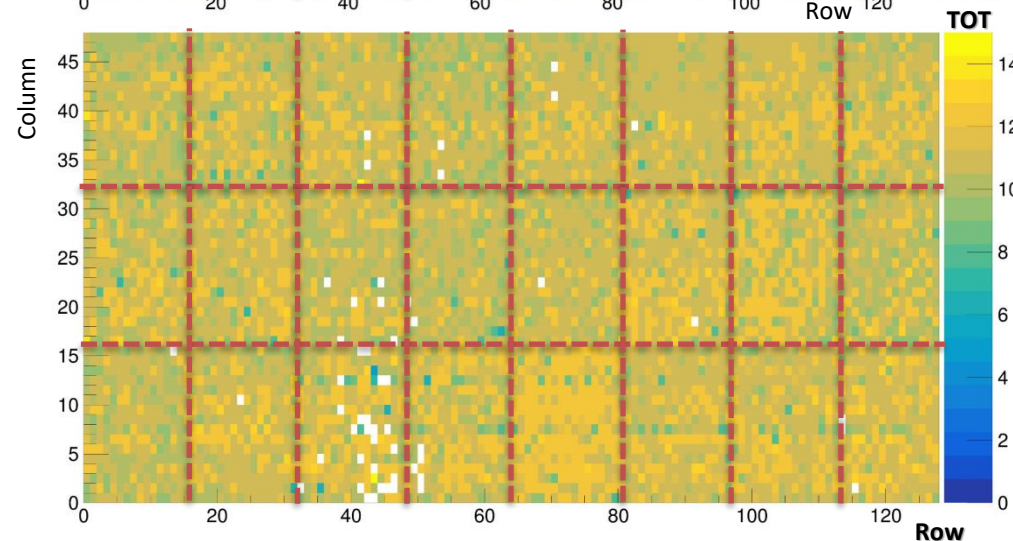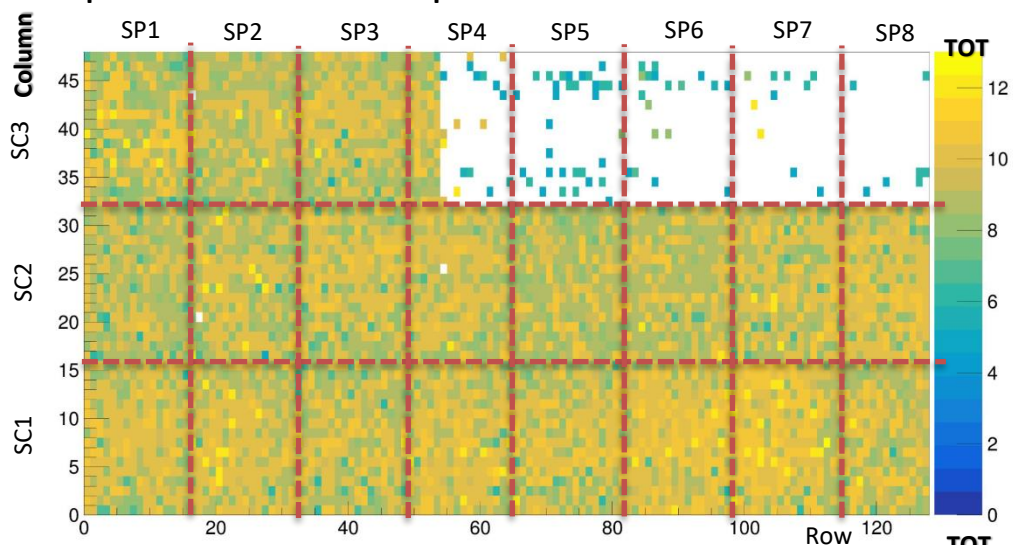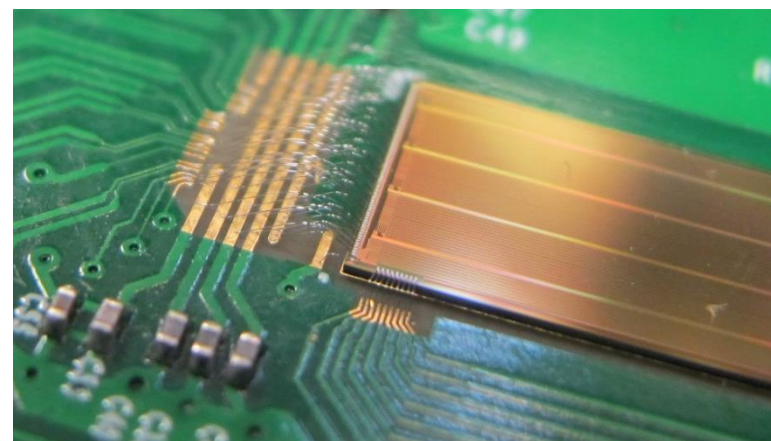- Investigating features in the lab → Production chip design is in progress with few small fixes
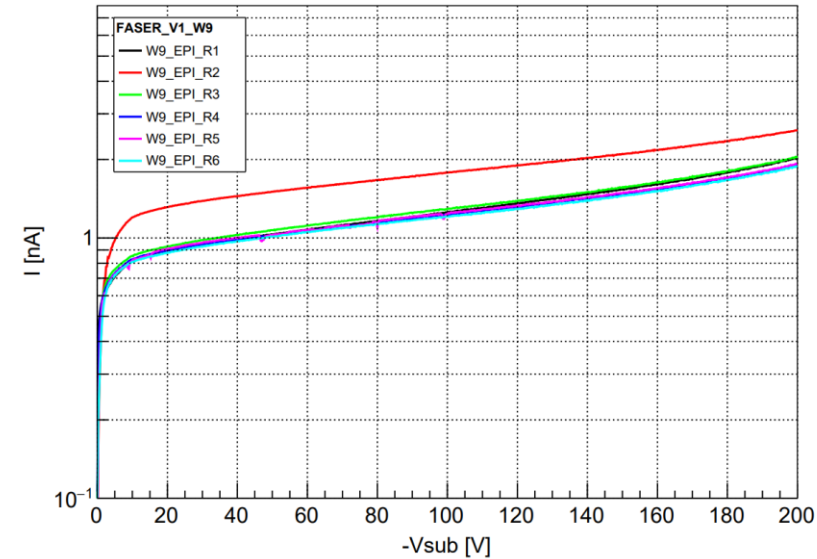
Innermost guard-ring set to ground to **achieve > 200V breakdown voltage** (170 V otherwise)
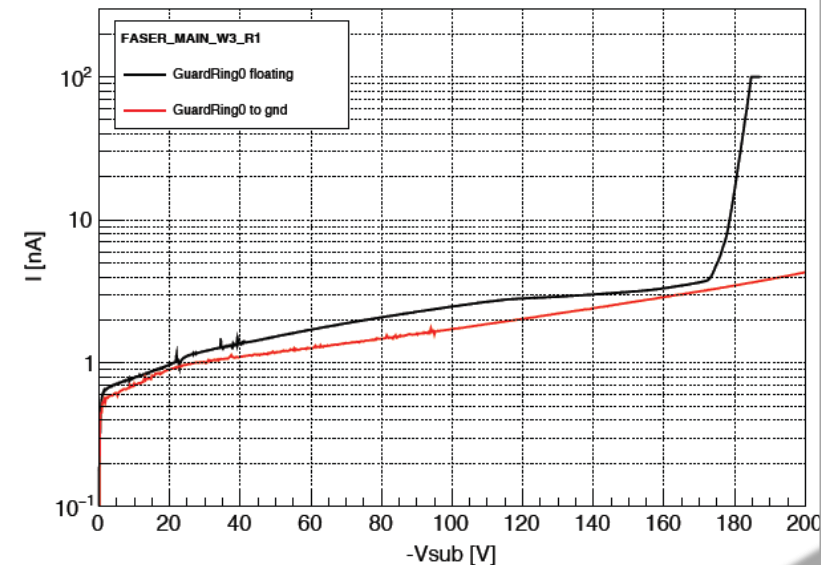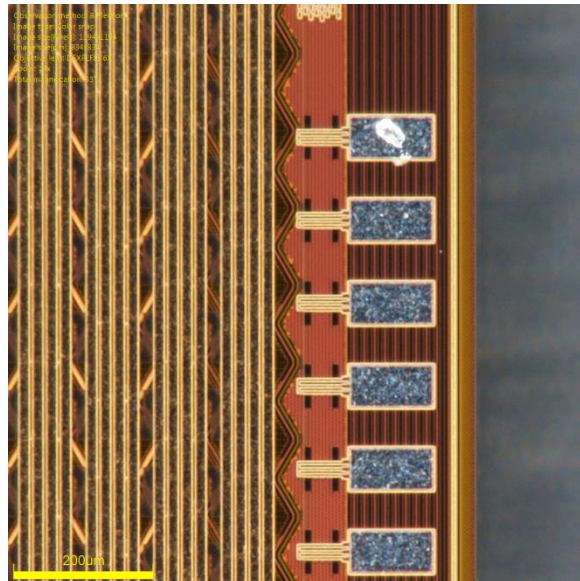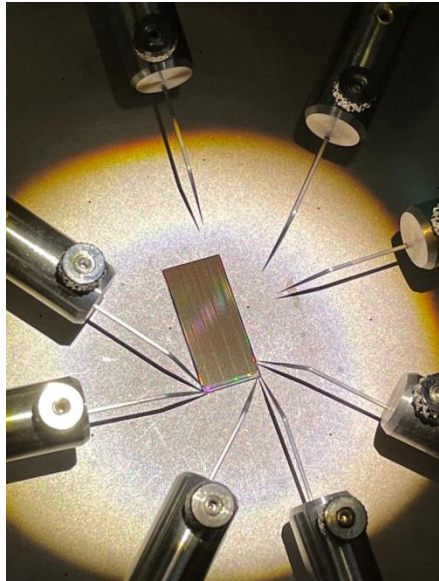
- Chips (all types) are assembled and wire bonded to a test board (SCC) → full characterization
- Checking pixel response by injection of test pulse in the 6144 pixels


Summary in a nutshell:

- V1 version analog circuit is not operating normally (Analog powering issue)
- V2 and V3 chips are working as expected
- V2 built on epitaxial layer are showing features:
    - Large region of pixels with defects
    - Yield issue
- V2 on standard wafer is showing the most uniform and highest quality

Tests with Laser system:

- The chip is powered and configured: 1 pixel unmasked
- An IR laser (1060 nm) is shot at the chip back side
- The TOT information can be readout via the Fast_Or signal (monitored with a scope)
- Laser pulse intensity can be varied with attenuator
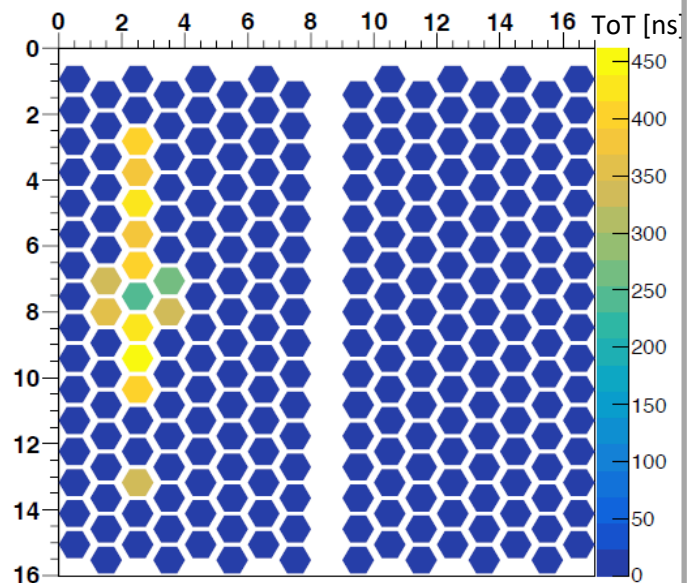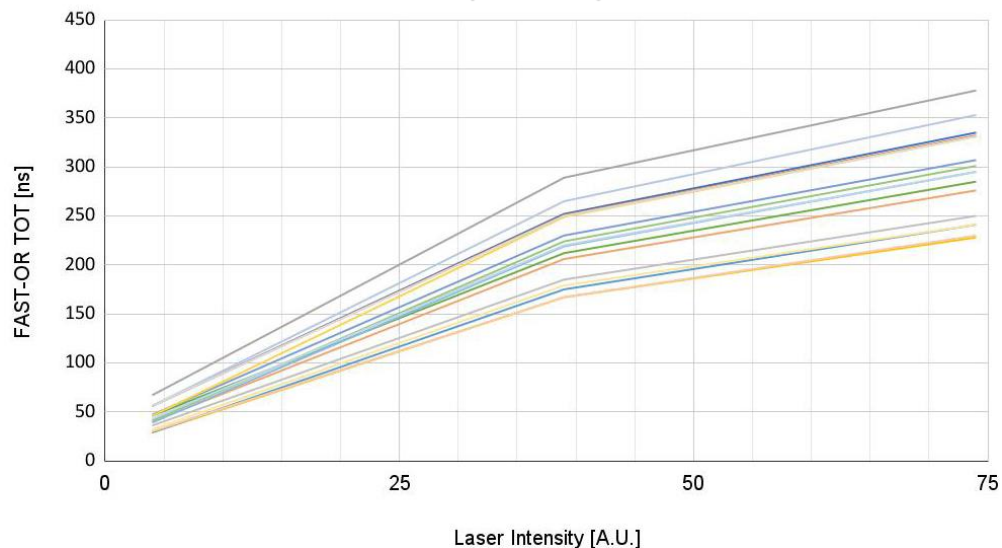- Laser intensity to charge calibration thanks to a Cd^{109} source

12
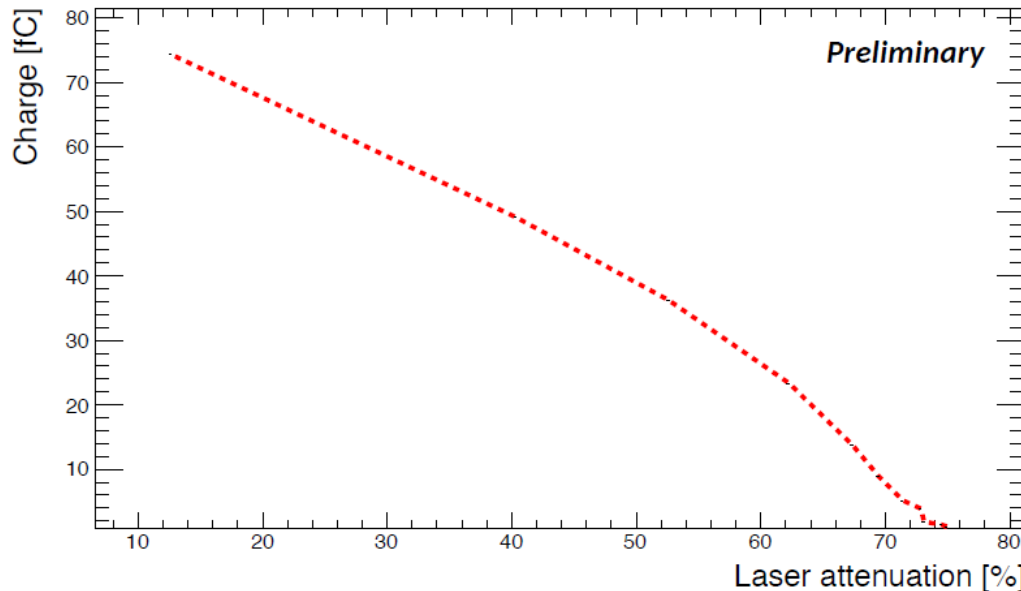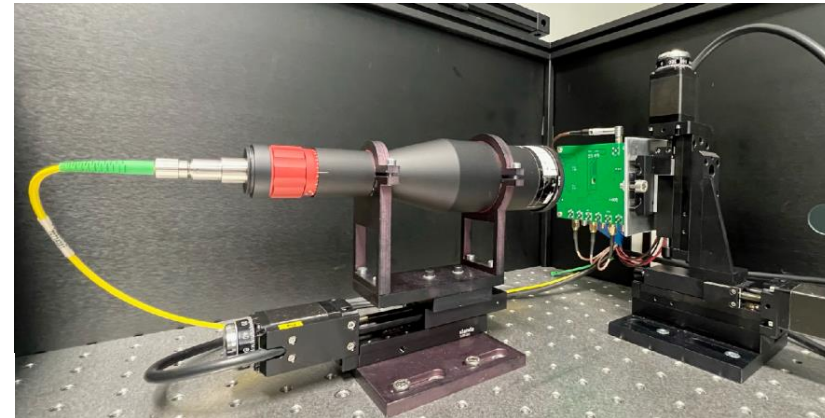
Few sets of results with LASER – Scan across pixels

Preamp @ 3 µA

Preamp @ 0.7 µA

Preamp @ 0.7 µA

Excellent Jitter performance down to ~30 ps with Pream   2 µA

Super-pixel response – Data stream 4 bit TOT

ADC map - SC2 - SP0, testpulse 50
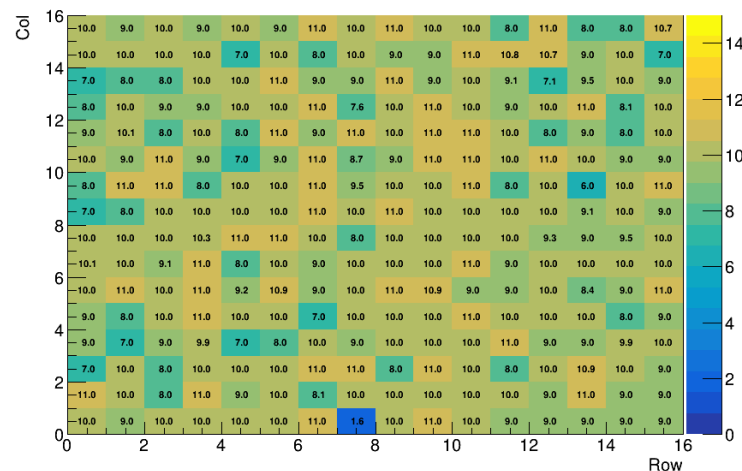
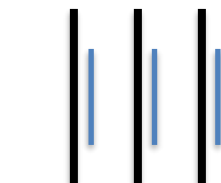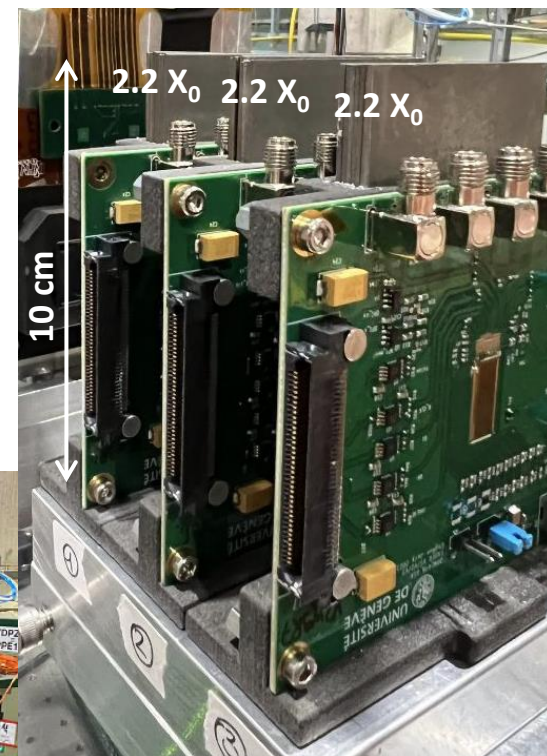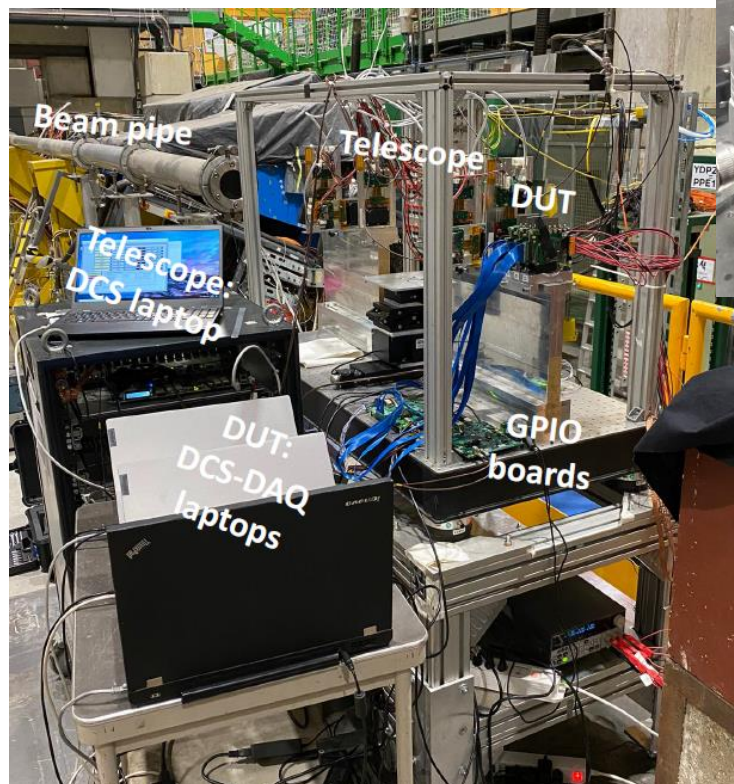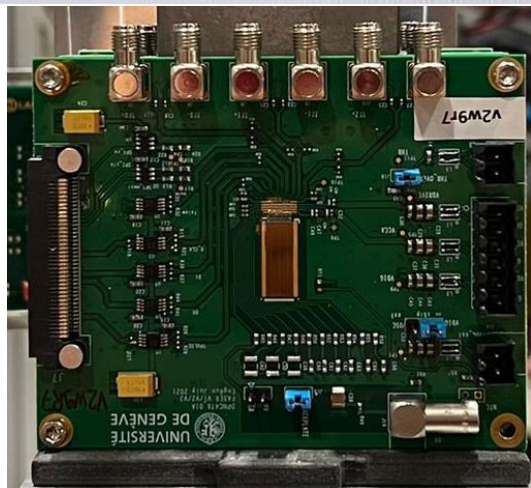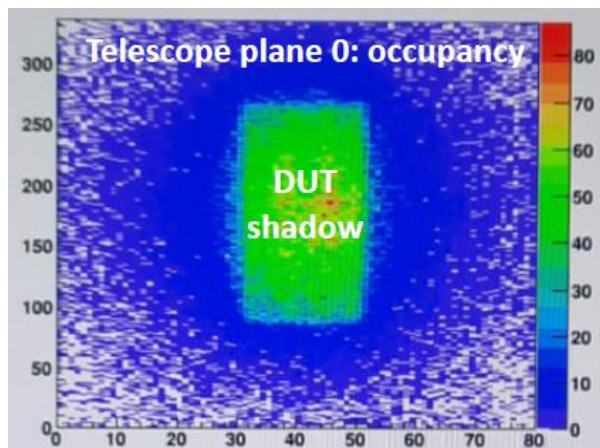TB at CERN SPS H2 beam line – electron beam up to 150 GeV/c
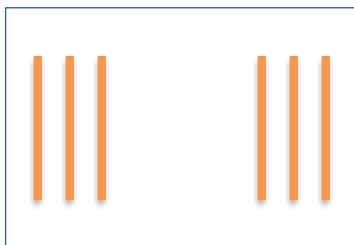
FEI4 telescope

DUT Preshower with absorber planes

Calorimeter Module

2.2 X_0 2.2 X_0 2.2 X_0

10 cm

Telescope plane 0: occupancy

DUT shadow

Beam pipe
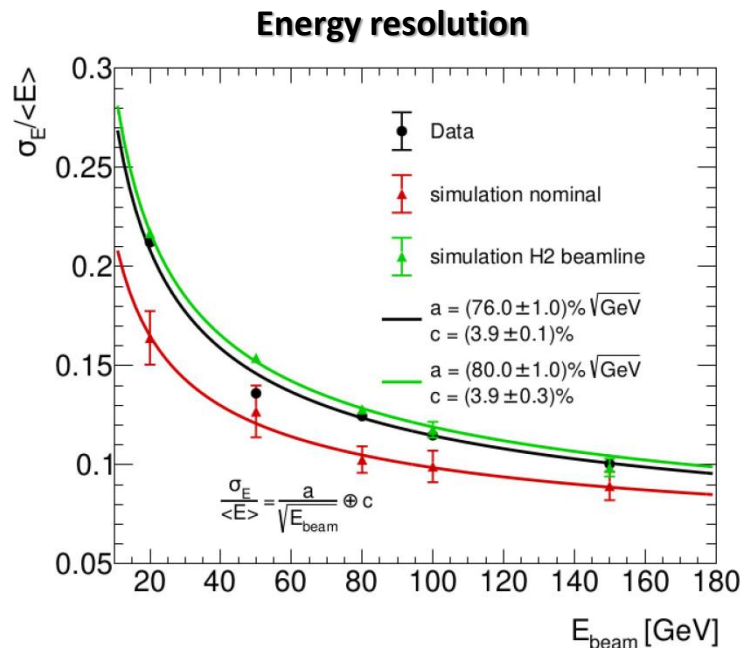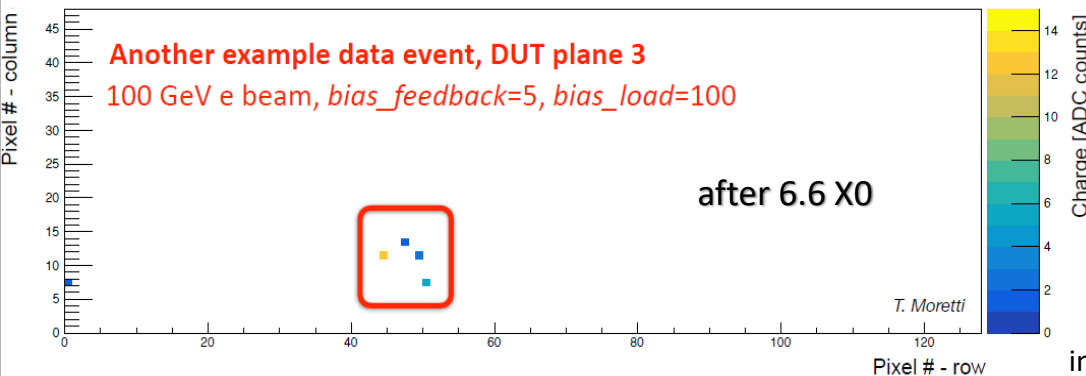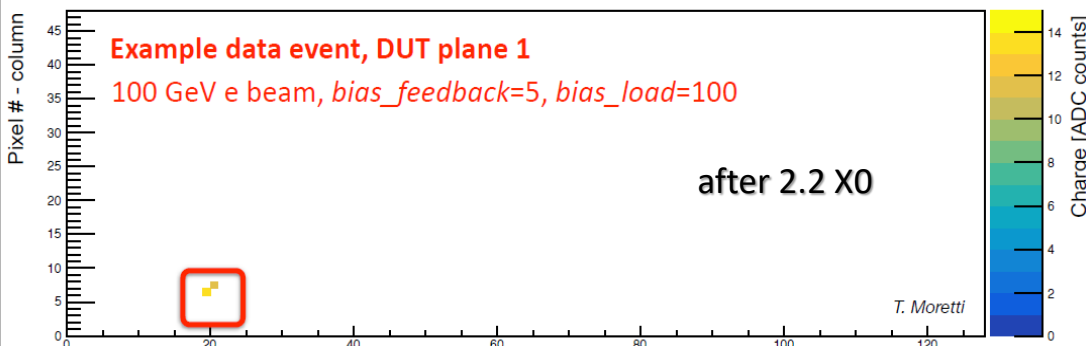
Telescope

DUT

Telescope: DCS laptop

DUT: DCS-DAQ laptops

GPIO boards

- E- beam energy selected between 20 to 150 GeV
- Preshower planes 1 &3 → triggered the FEI4 telescope and the calorimeter
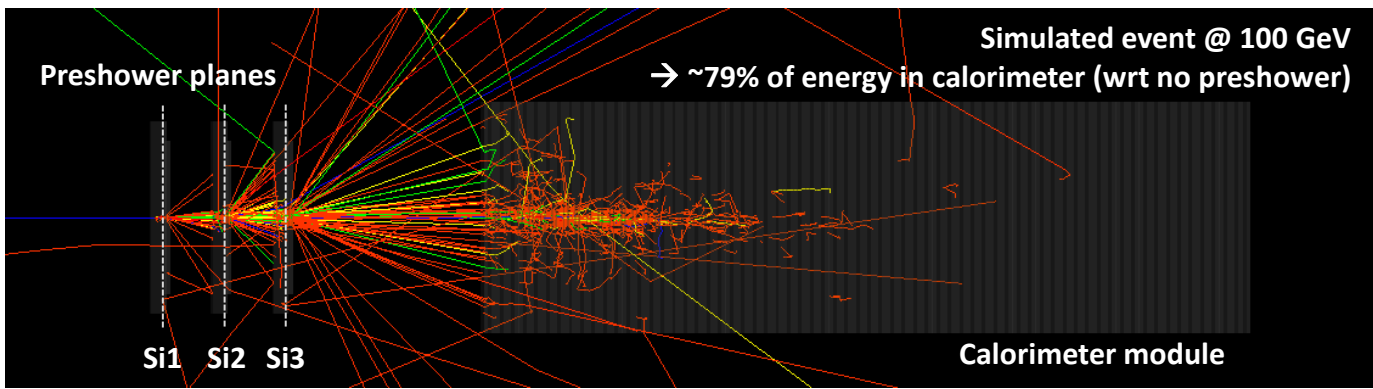- Up to 6.6 X0 in front of the calorimeter

Example data event, DUT plane 1
100 GeV e beam, *bias_feedback*=5, *bias_load*=100

after 2.2 X0

T. Moretti

Another example data event, DUT plane 3
100 GeV e beam, *bias_feedback*=5, *bias_load*=100

after 6.6 X0

T. Moretti

Pixel # - row

Energy resolution

- Data
- simulation nominal
- simulation H2 beamline
- $a = (76.0 \pm 1.0)\% \sqrt{GeV}$
  $c = (3.9 \pm 0.1)\%$
- $a = (80.0 \pm 1.0)\% \sqrt{GeV}$
  $c = (3.9 \pm 0.3)\%$

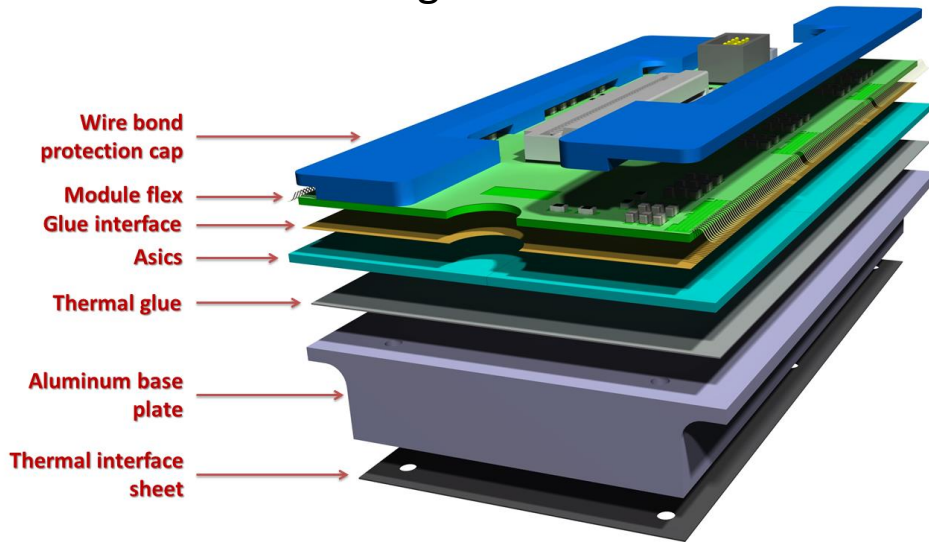$$\frac{\sigma_E}{\langle E \rangle} = \frac{a}{\sqrt{E_{beam}}} \oplus c$$

E_{beam} [GeV]

Upstream material description (NA61, HGCAL)
in the H2 beamline improves Data vs Simulation agreement

After investigation with a Cd109 source the estimated threshold set during the TB was ~ 4 fC
NB: Charge is only a 4 bit ADC with dynamic range of 65 fC

Preshower planes

Simulated event @ 100 GeV
→ **~79% of energy in calorimeter (wrt no preshower)**

Si1 Si2 Si3

Calorimeter module

Module Design and Prototype

- Module consists of integrating 6 asics . Prototype: using v1 and v2 single dies on a base plate with the module flex glued on top and wire bonded to v1 for the electrical interface.
- Wire bond protection caps are added allowing services to run on top
- The base plate is made of aluminum with hard anodization treatment to allow an electrical insulation layer preventing an electrical breakdown of the sensor backplane
- Module prototype with flex PCB already made with two pigtails (power/data) → very close to final design

First prototype module made

Wire bond protection cap
Module flex
Glue interface
Asics
Thermal glue
Aluminum base plate
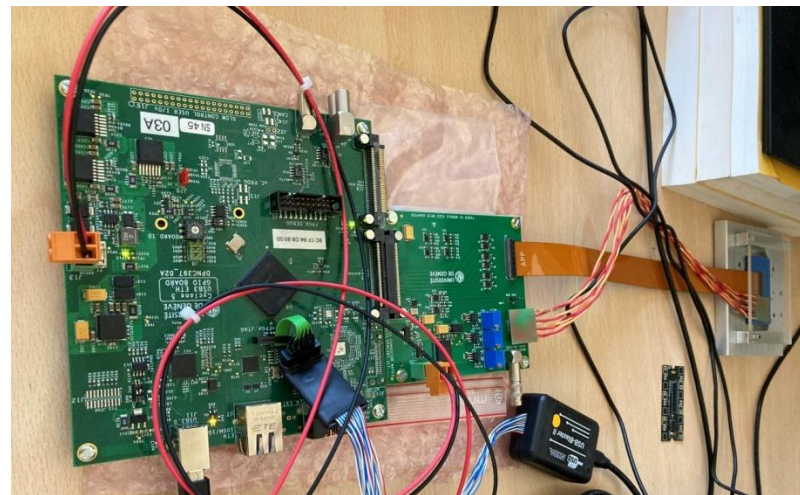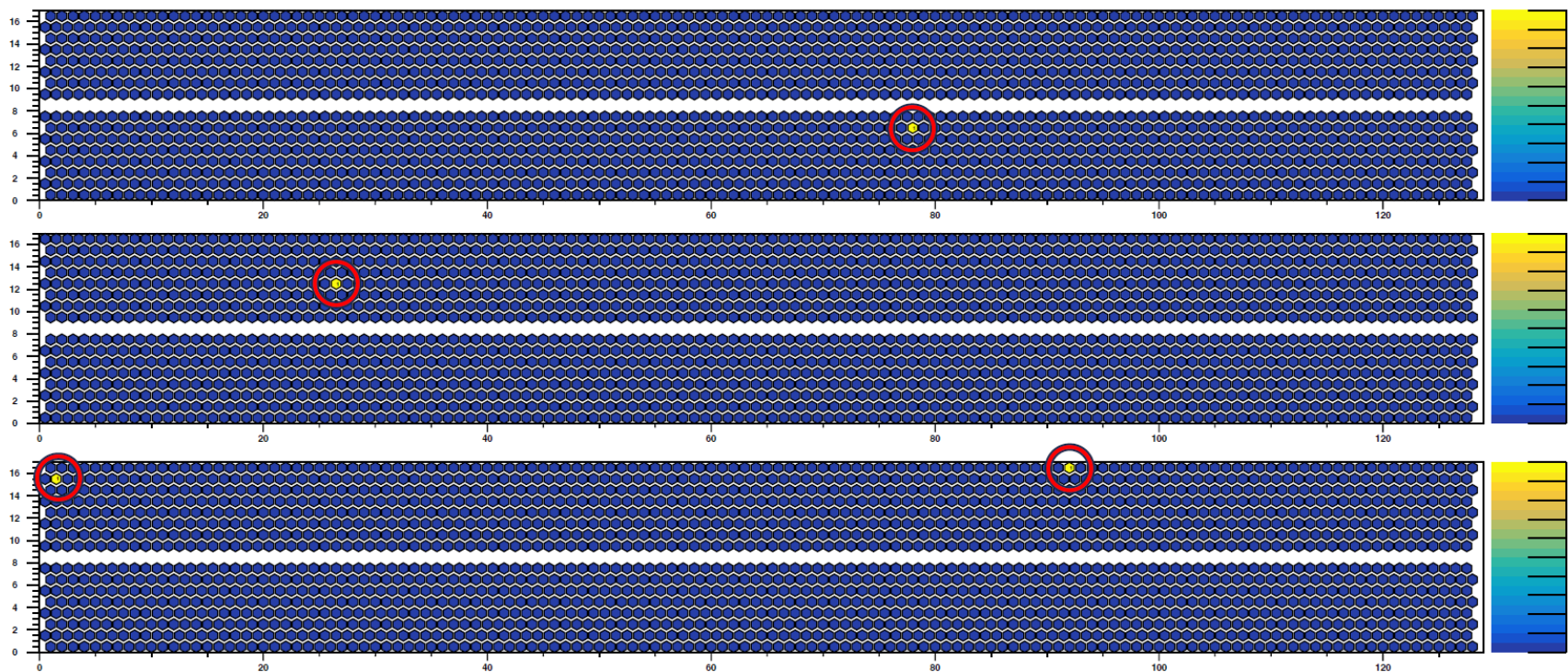Thermal interface sheet
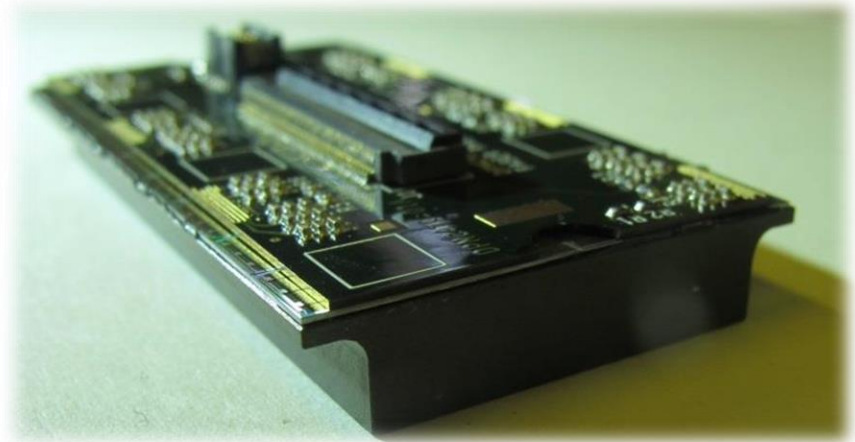
Wire bonding
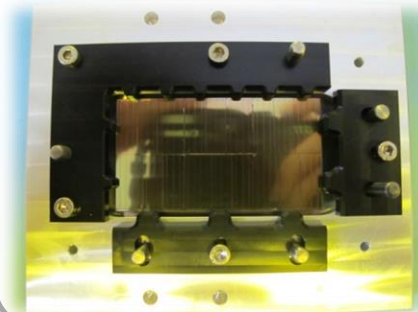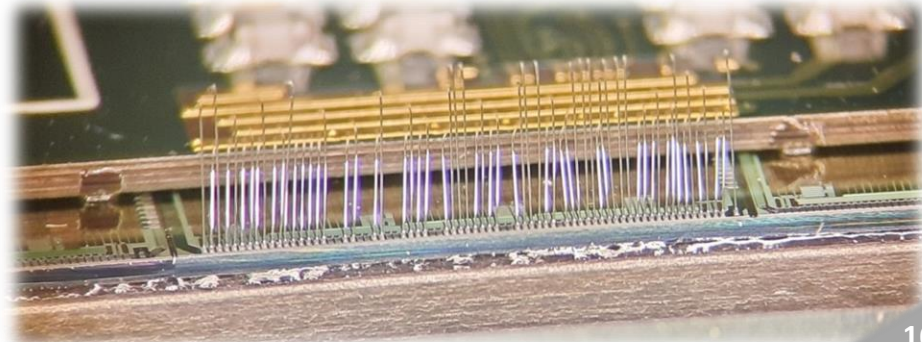
Module Prototype

- Module program is essential:
  - For validation of the full chain with module flex with multi-chip readout
  - Optimization of the FPGA and software codes
  - Development of the calibration routing
- 6 prototypes made with v1 and v2 chips

**1st step is to identify problematic channels for masking**

A plane is instrumented with 2 rows of 6 modules:

- Cooling plate made in DMLS (Direct Metal Laser Sintering) made in AlSiMg with high isotropic thermal conductivity when annealed (180 W/mK)
- The module will be interfaced with pigtails connecting to the active patch panel (APP) boards
- Integration and commissioning of the full preshower upgrade will be done in surface before its installation in Dec 24 in TI12.
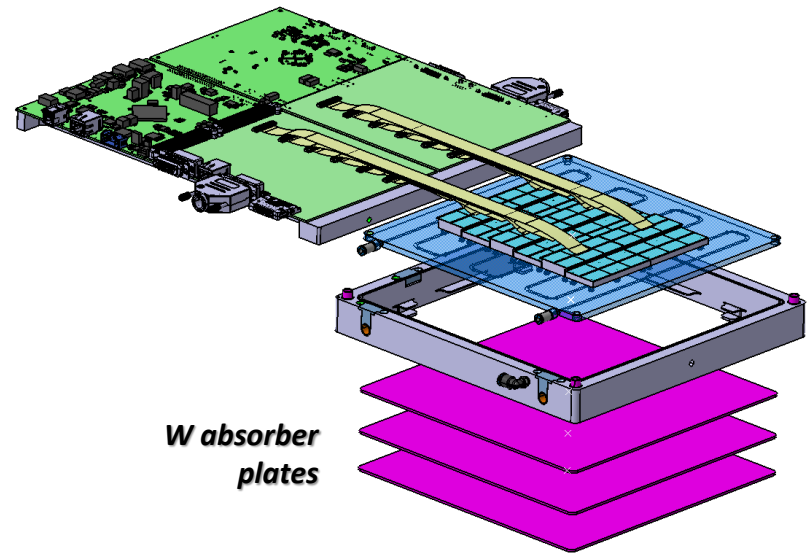
W absorber plates
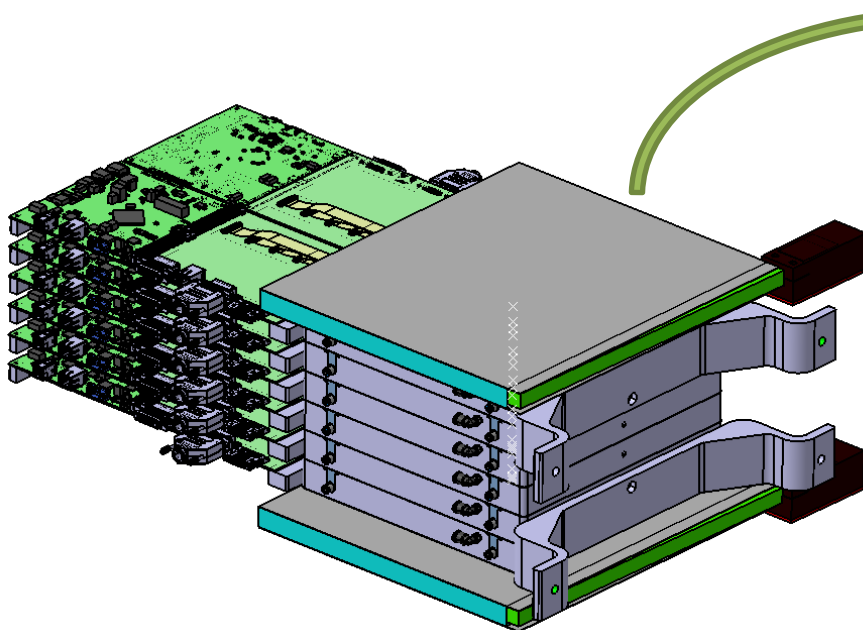
Full preshower upgrade with 2 plastic scintilaltors

Calorimeter
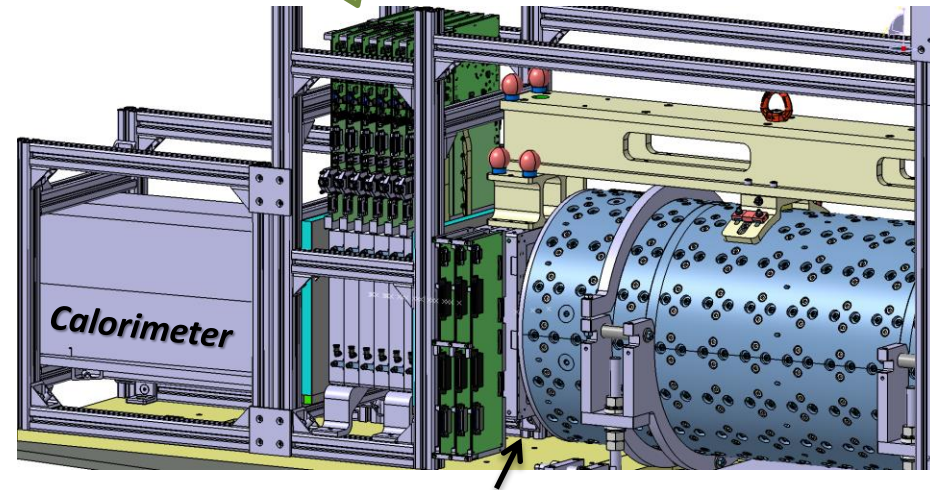
Last tracker plane

Summary & Outlook

- FASER preshower upgrade will be instrumented with the SiGe MAPS designed and developed at UniGe

- In the last year of Run-3 data taking FASER should have capability needed for two closely spaced photons detection and extend the sensitivity reach in the ALP phase-space

- The pre-production chips delivered in June are working fine but with undesired features that were corrected in the final chips:
  - Extensive lab characterization made
  - Tested in H2 bealine at CERN SPS with the calorimeter

- Final chip submission made end of May and delivery expected in Jan 24

- Prototypes modules are being made allowing:
  - Testing assembly and fine tuning the jigs
  - Multi-chip readout and design of the module flex and pigtails
  - Getting experience with the back-end readout for module calibration

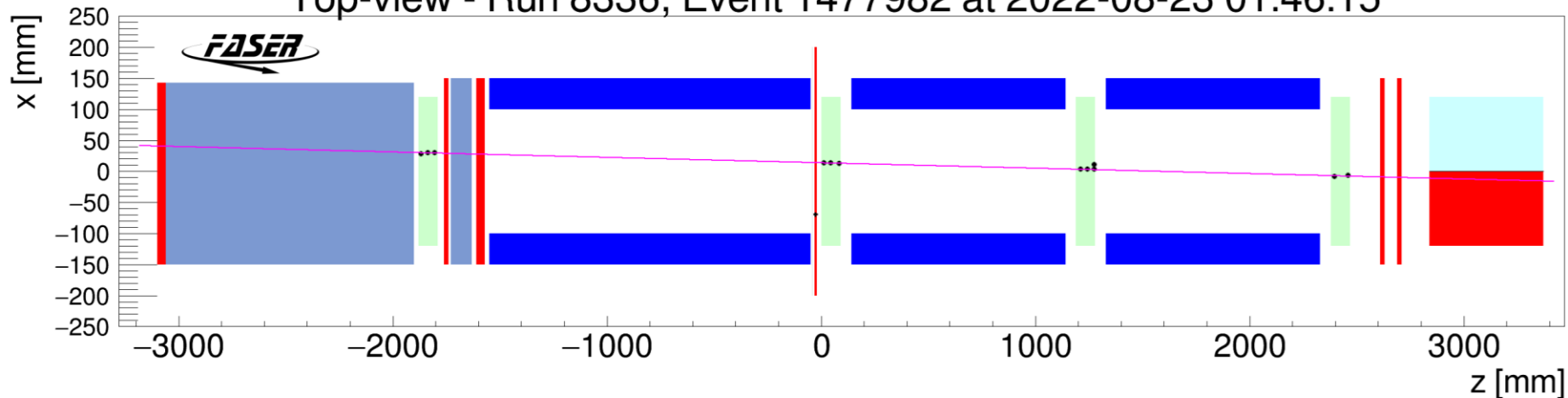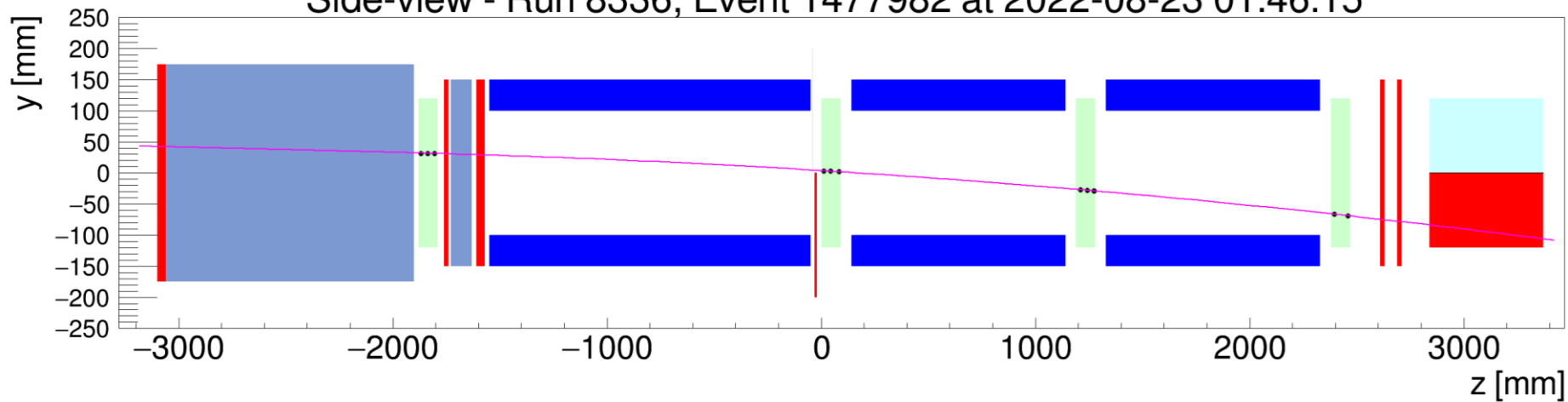- Production and integration are expected in 2024 for an installation in December

Event Display of a Muon event in FASER

Top-view - Run 8336, Event 1477982 at 2022-08-23 01:46:15
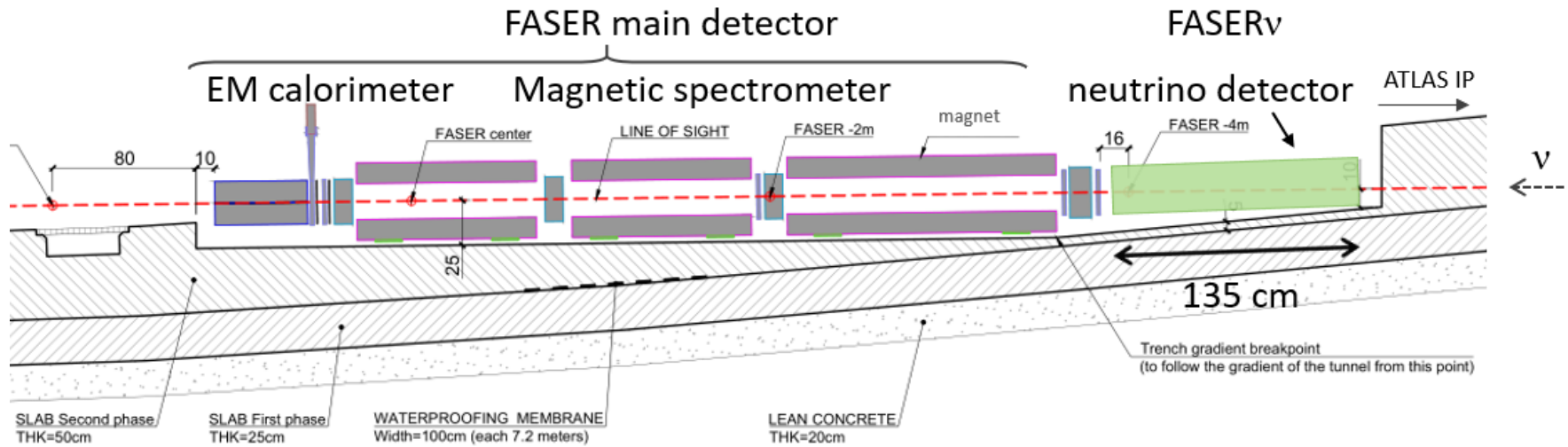
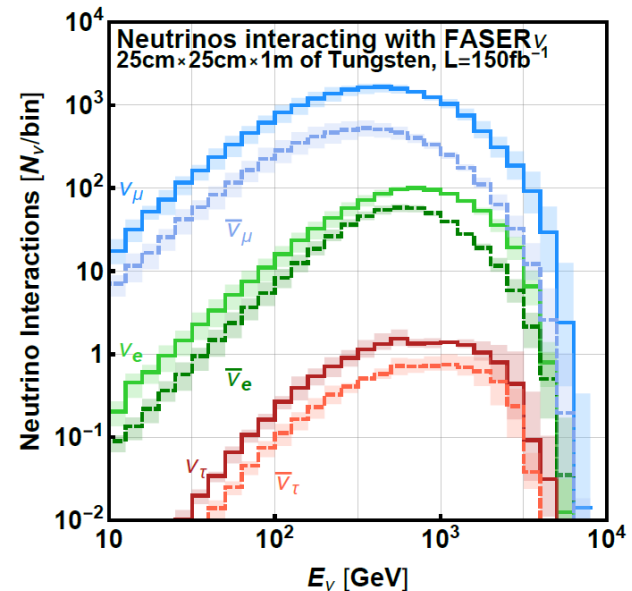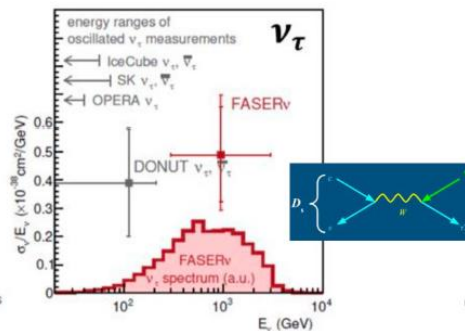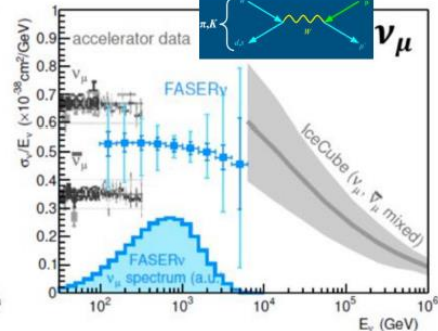Side-view - Run 8336, Event 1477982 at 2022-08-23 01:46:15

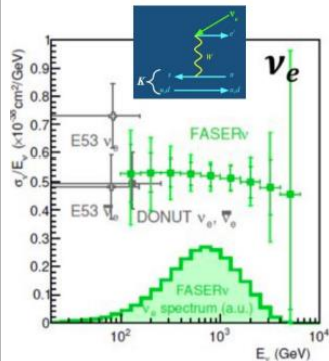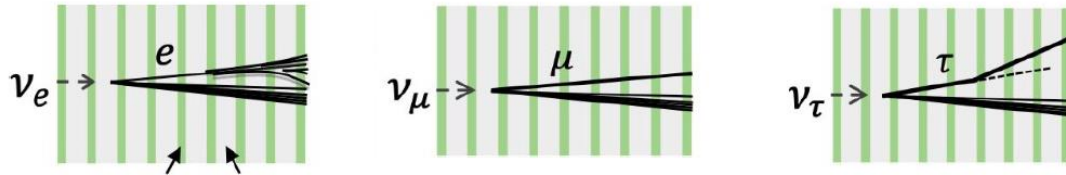FASER main detector — EM calorimeter, Magnetic spectrometer, FASERν neutrino detector, ATLAS IP

- Sensitive to new physics by measuring scattering cross sections and studying each flavor

Why MAPS and SiGe?

- MAPS when a mature design and technology is reached → allows gaining significant cost and efforts for a detector construction
- UniGe is developing SiGe HBT technology since many years and the observed performances are indicating that the technology is mature and accessible.
- The backend readout is also an important ingredient for the deployment of the new readout chip → UniGe developed the readout and trigger logic boards for FASER TDAQ ([2021_JINST_16_P12028](#)) and also for many other projects.
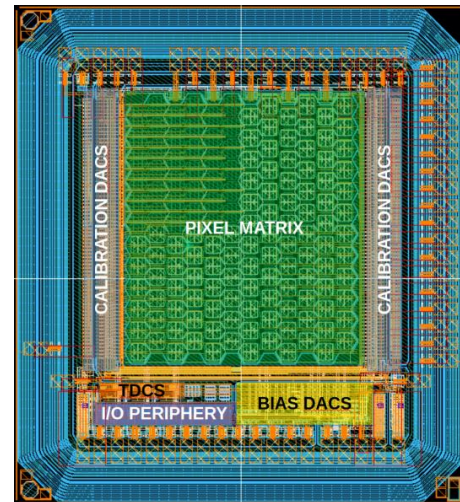
*G. Iacobucci et al 2022 JINST **17** P02019*

Performances obtained in TB with recent chip development → Low preamp current ok for FASER
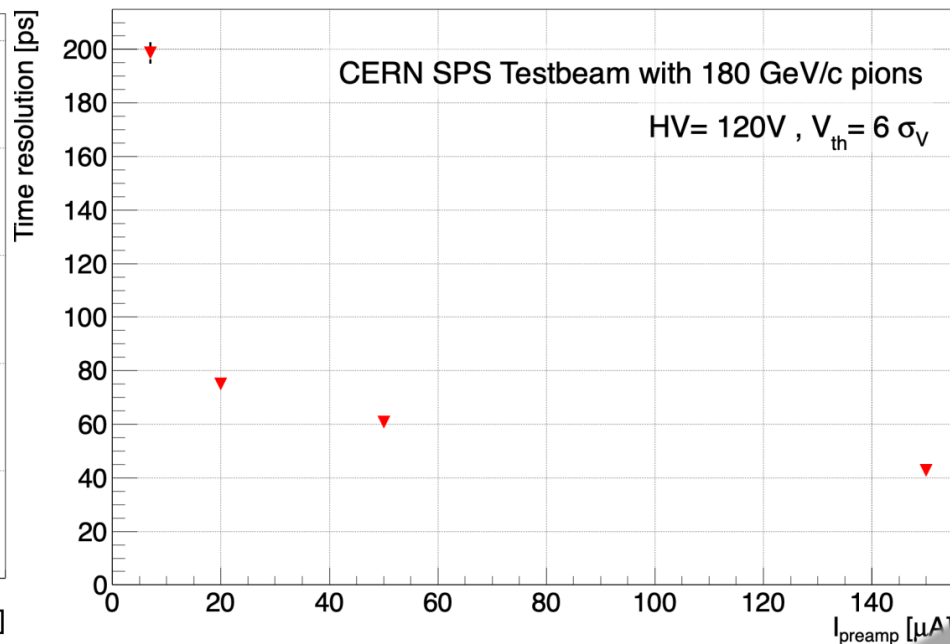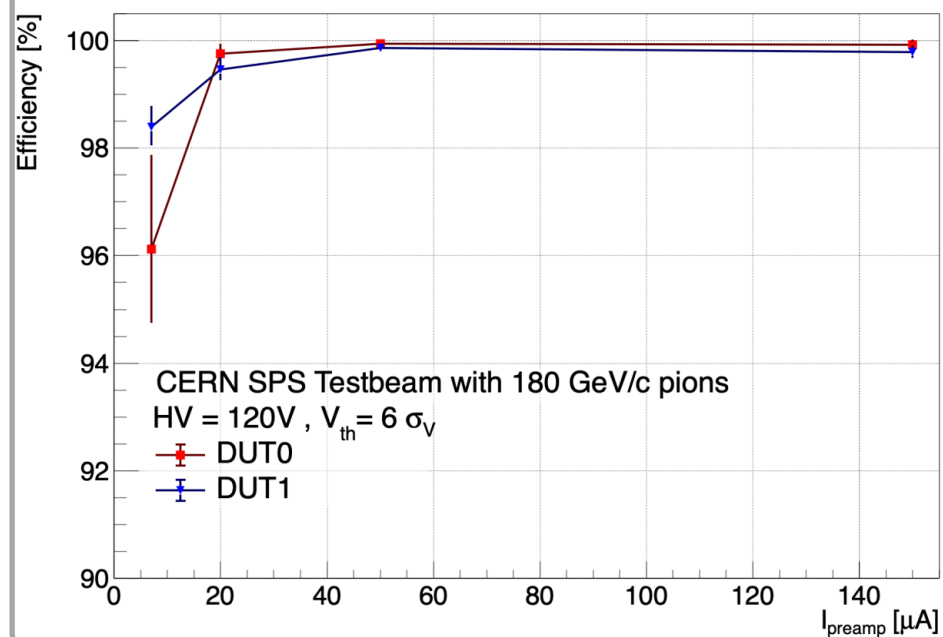
Super-pixel structure:

- 16 pixel rows (of 2x8 pixels each)
- Pixels are digitized at the same time using a 256-to-1 analog multiplexer and a 4-bit flash ADC
- 3 fast-OR lines per super-pixel to generate a readout trigger signal (arbitration logic)
- Local bias circuits
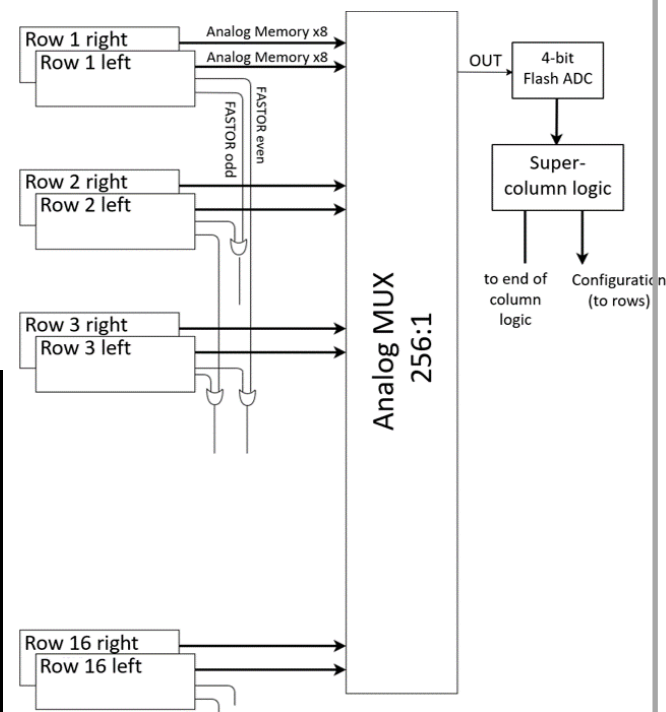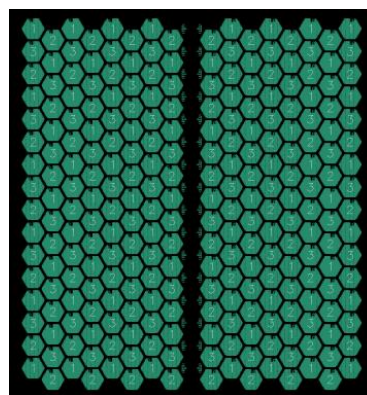
Digital periphery:

- **Times of arrival** (TOA) of fast-OR signals **digitized at the base of the super-column** with a 24-channel TDC
- **The digital periphery will start the readout** of the chip (super-column after super-column) **after a programmable delay** (up to 2.55 µs)
- During readout, the **charge stored in the analogue memories are digitized at SP** level
- **Slow control via SPI commands** (pixel masking, 8-bit bias DACs)
- **Baseline readout** mode: single data rate based upon a 200 MHz clock

Pre-production asic periphery with 3 SCs
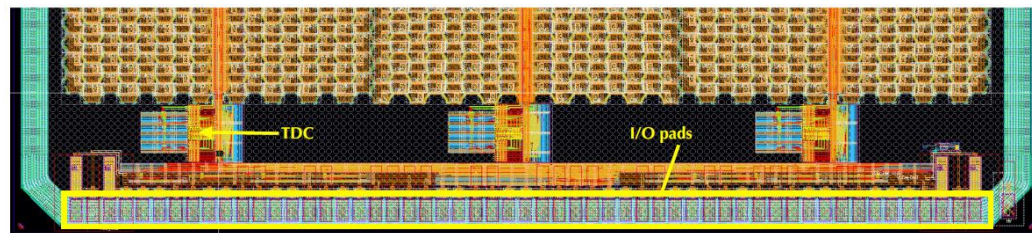
*Delivered in June 2022*

Pre-production submission:

- 6 wafers:
  - 3 Epi-layer + low resistivity
  - 3 standard wafer (50 Ω.cm)
  - Thickness: 300 µm

- Reticle size: 2.4 x 1.5 cm^2
- Faser_Main (V1): 4 SPs (128x64 pixels)
  - ✓ In-pixel pre-amp and driver
  - ✓ Discriminator outside
- FASER_V2 (V2): 3 SPs (128x48 pixels)
  - ✓ In-pixel pre-amp, driver, and discriminator
- FASER_Alt (V3): 3 SPs (128x48 pixels)
  - ✓ Same as FASER_Main
  - ✓ No analogue memories
  - ✓ Counter for charge information
- Test structures
  - ✓ TDC, sensor, …

- All chips are diced individually except 1 wafer with V1, V2 & V3 diced together for module prototype

FASER_Main   FASER_V2   FASER_Alt

15 mm

24 mm

FASER_Main

53 reticles / wafer

26
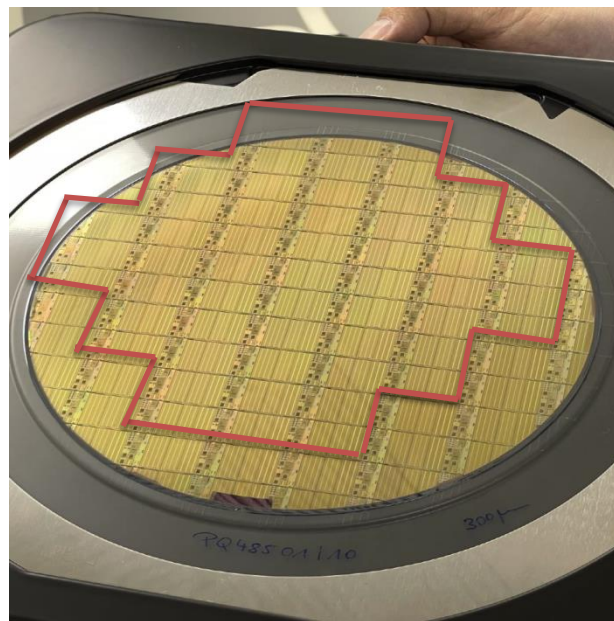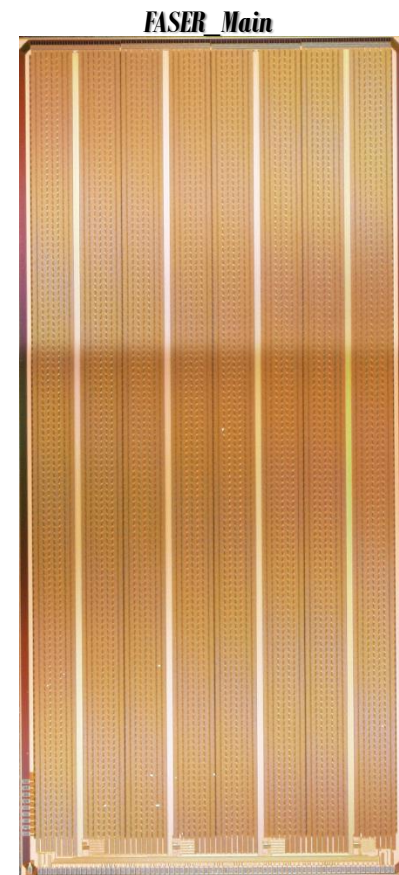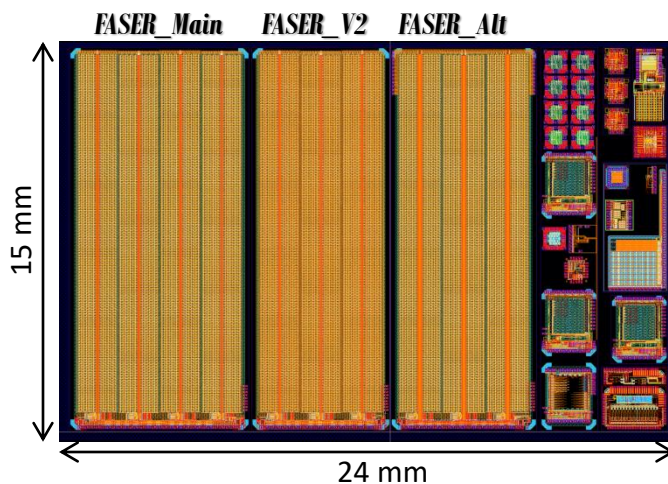
Prototype for v2
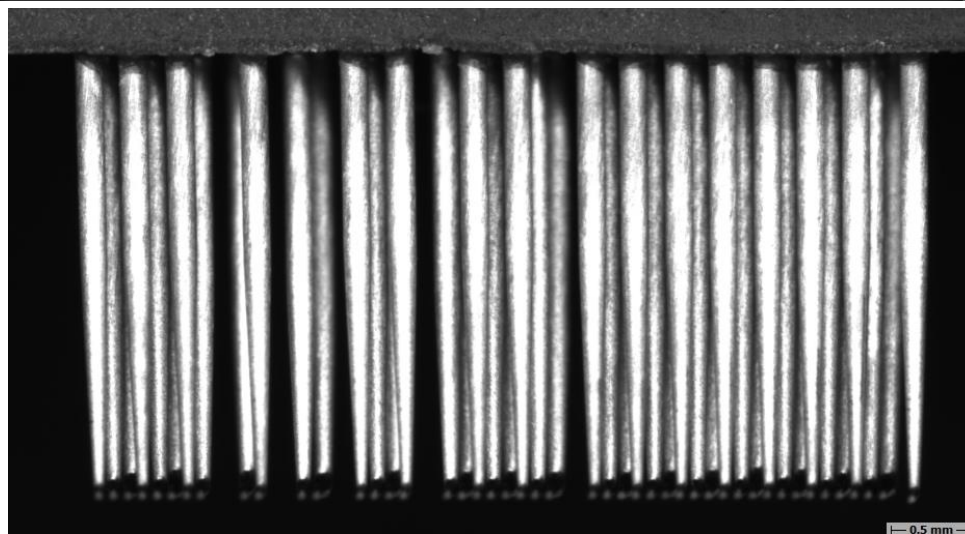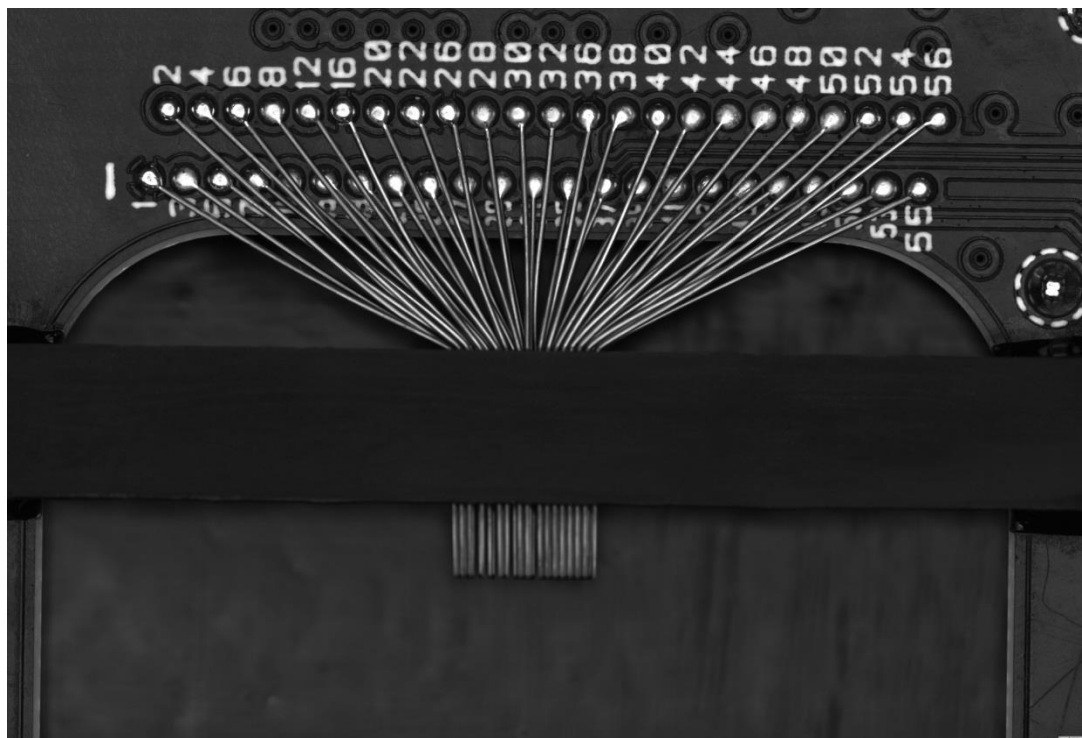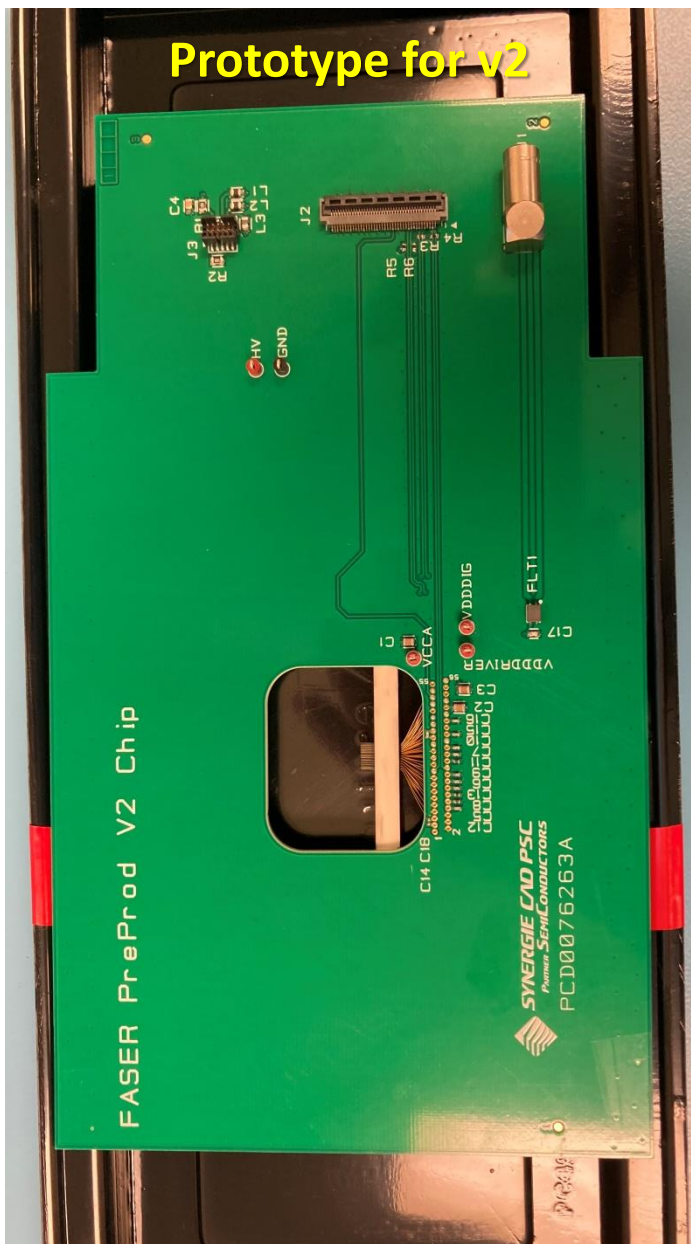
- Four scintillator stations are commissioned and installed
  - \> 99.9% efficiency, enough to trigger LLP decay inside the FASER detector
  - Confirmed by in situ measurements in 2018.

(a) First veto station. (b) Second veto station. (c) Timing station. (d) Preshower station

- Calorimeter based on LHCb ECAL module is also installed. One module has:
  - 12 cm x 12 cm (25 $X0$)
  - 66 layers of (2mm lead and 4mm scintillator)
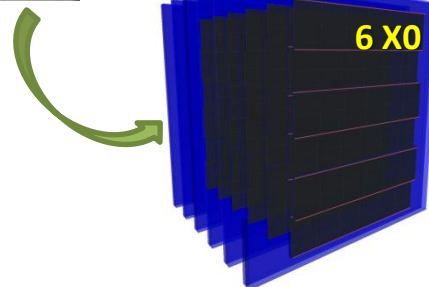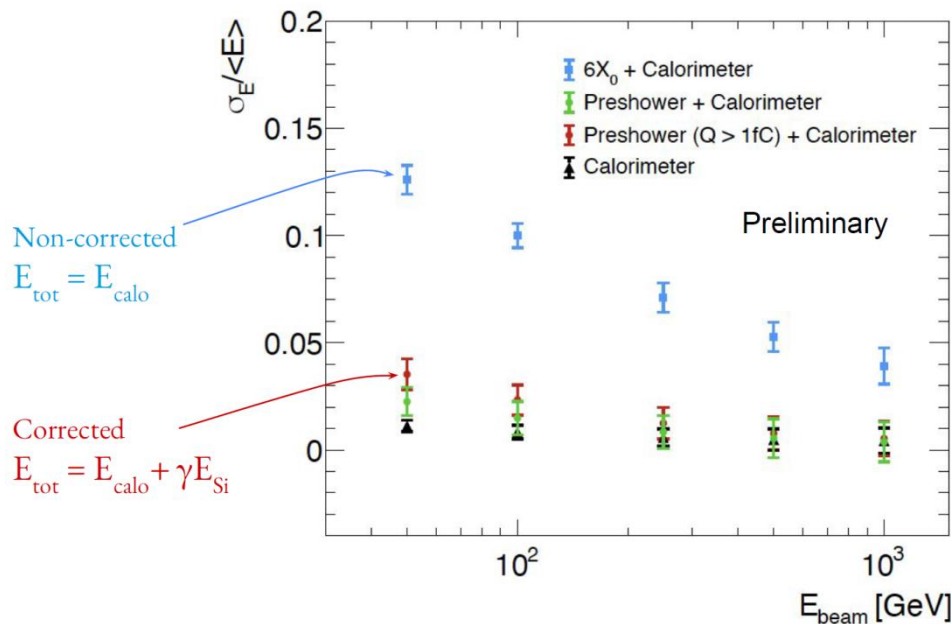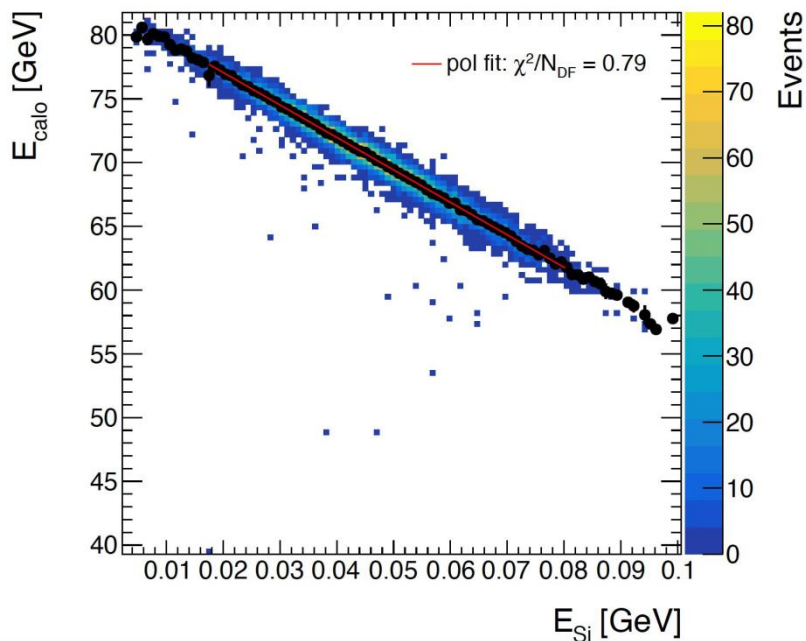 - Resolution ~1% for 1 TeV electron energy deposits
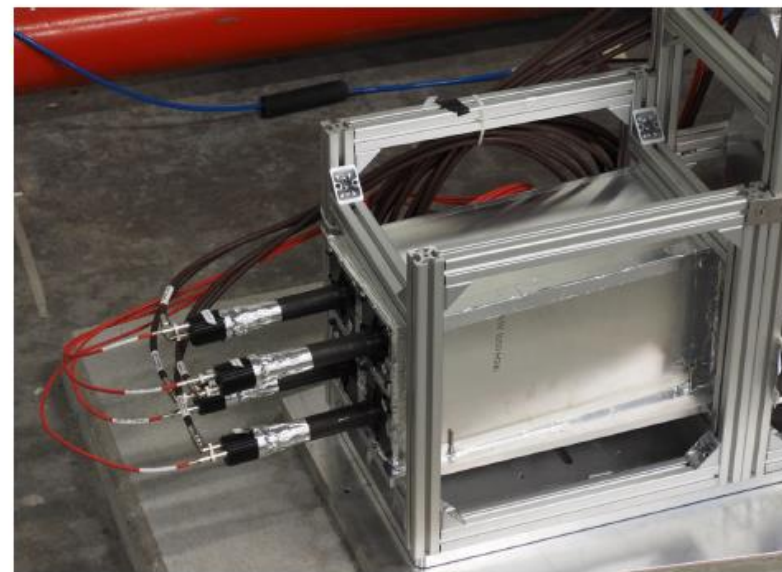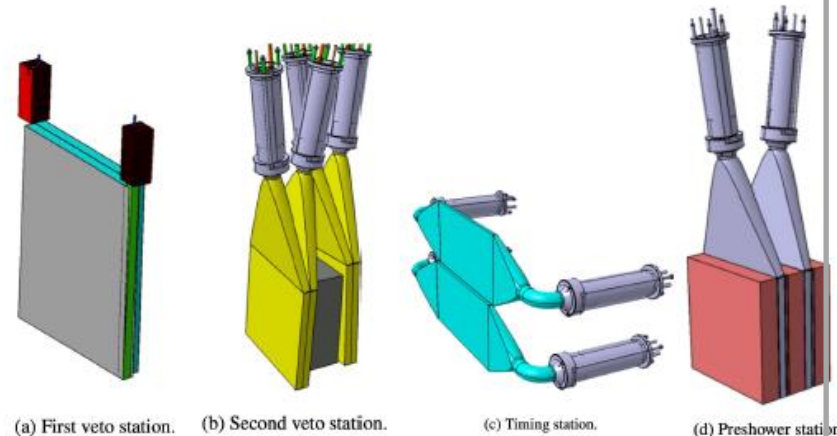
- Energy loss in calorimeter will be compensated with what is reconstructed in the Preshower
- Preliminary Geant4 simulations give good indication with and without information added from the preshower

2 X0

+

1 of the 4 calorimeter modules

6 X0

→ **Similar performances above 250 GeV**

pol fit: $\chi^2/N_{DF} = 0.79$

E_{calo} [GeV]

E_{Si} [GeV]

Events

$\sigma_E/\langle E \rangle$

- 6X_0 + Calorimeter
- Preshower + Calorimeter
- Preshower (Q > 1fC) + Calorimeter
- Calorimeter

Preliminary

Non-corrected
$E_{tot} = E_{calo}$

Corrected
$E_{tot} = E_{calo} + \gamma E_{Si}$

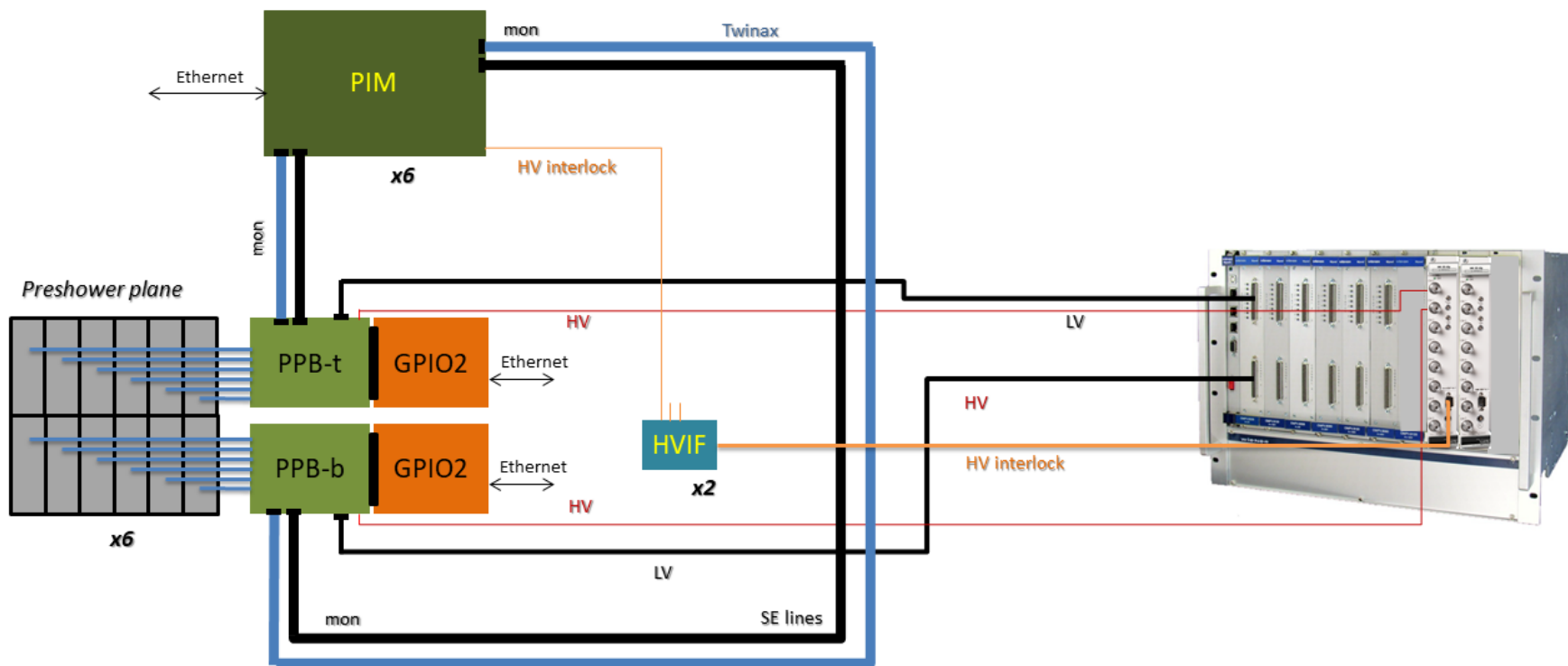E_{beam} [GeV]

Detector interfaces:

- Active Patch Panel (APP): PPB + FPGA readout board
- Preshower Interlock and Monitoring (PIM) will monitor power and environmental DCS (through the APP) and steer the detector safety
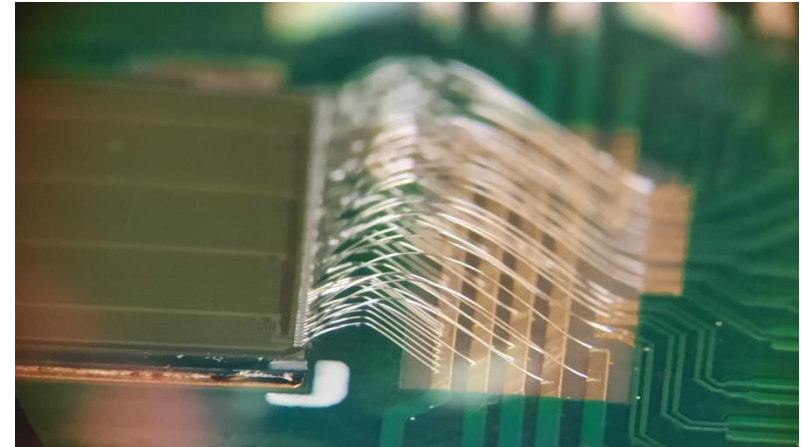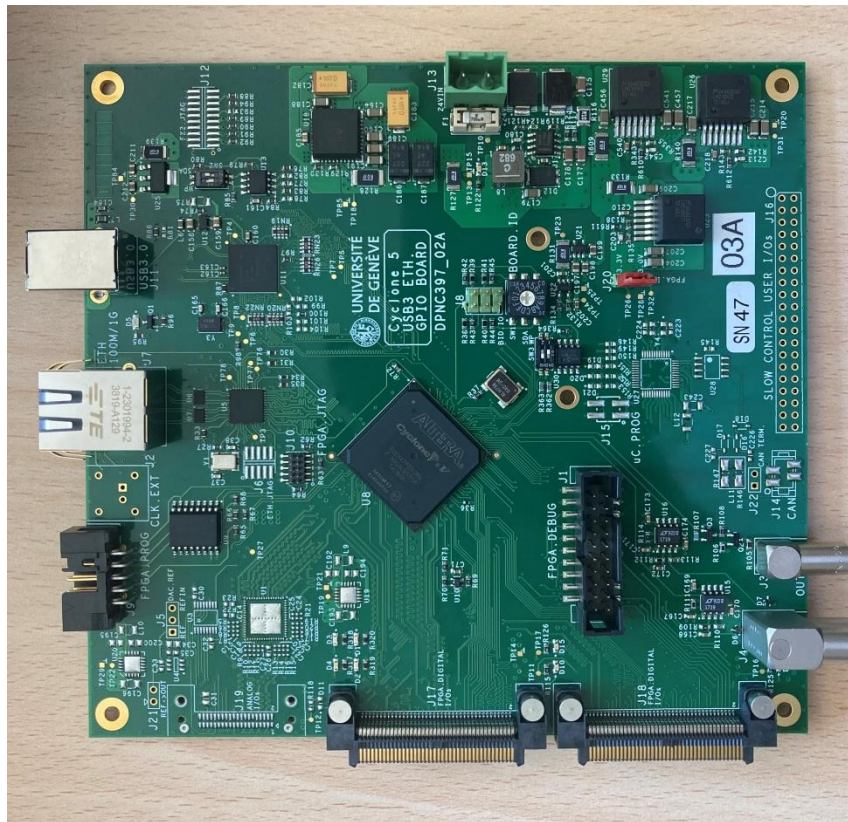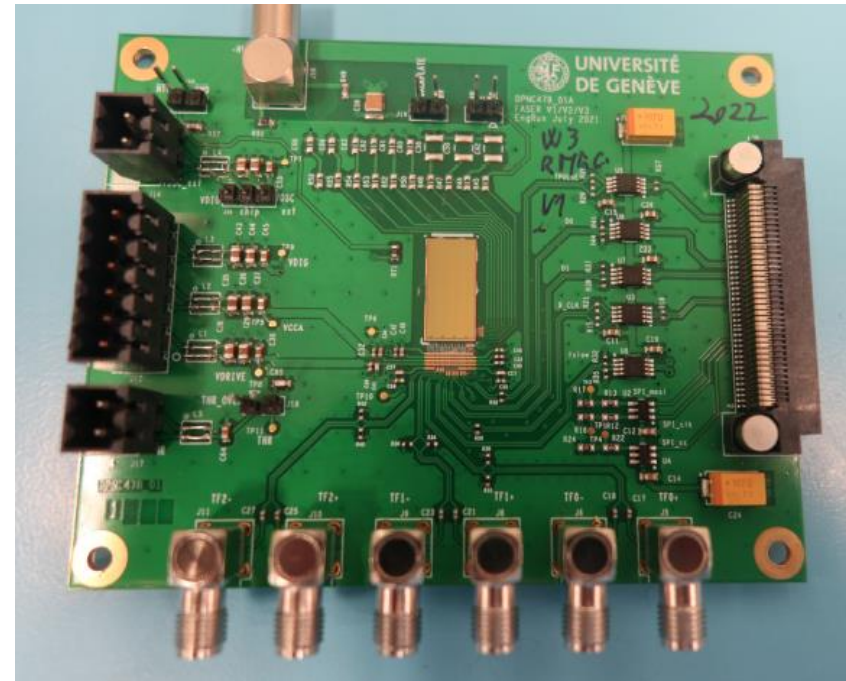- MPOD crate will contain all the LV and HV power supply

Single Chip Card (SCC):
- Compatible with the three chip layouts
- Several independent power supply domains
- Readout of output fast-OR signals (SMA)
- Interface to UniGe GPIO for SPI communication and 200 MHz readout

GPIO - FPGA readout board

SCC assembly with bonding

Total charge stored ∝ ToT
- Preamplifier designed to produce a signal proportional to the log of input charge
- Capacitor charged with a constant current during the ToT
- When signal goes below threshold again, the memory is disconnected and left floating until read by flash ADC:
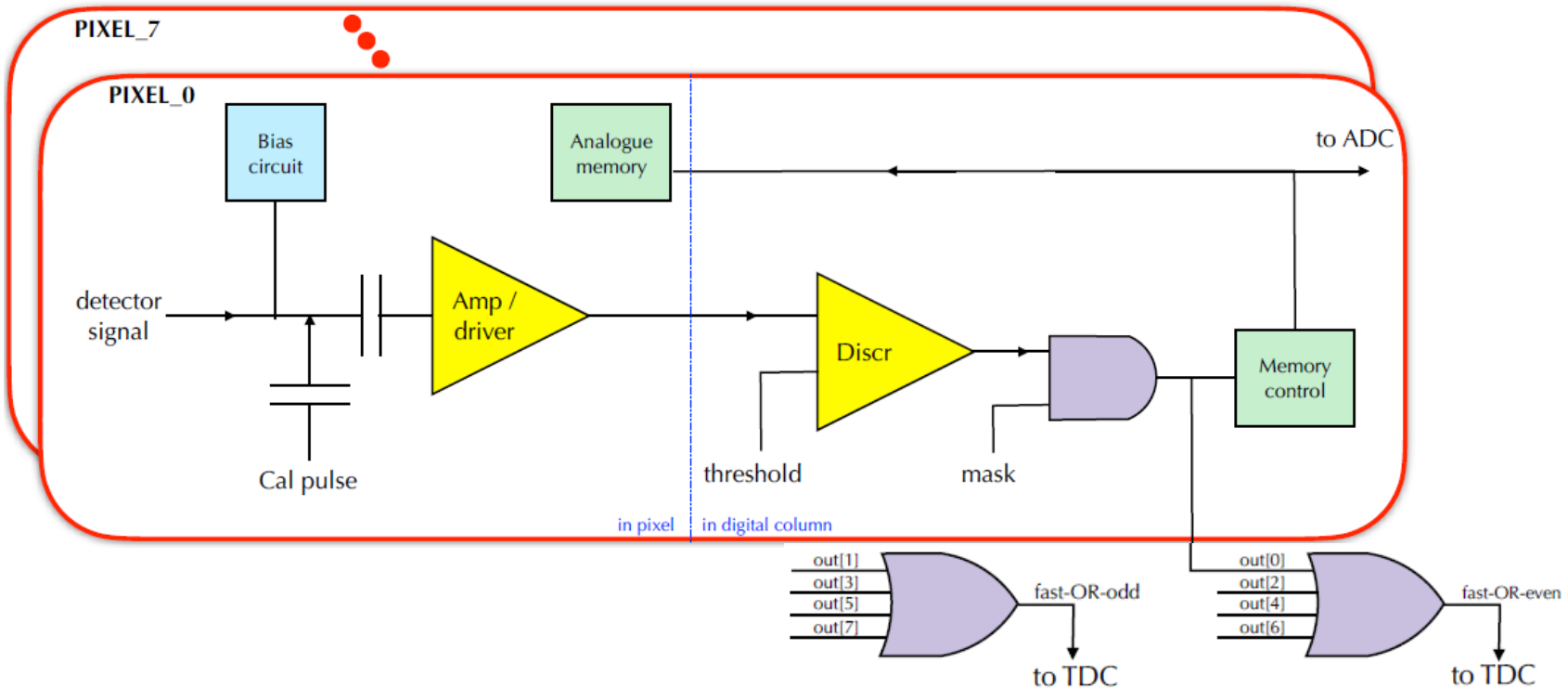 - Low current leakage: error < 1 LSB (ADC) for readout time <= 200 µs
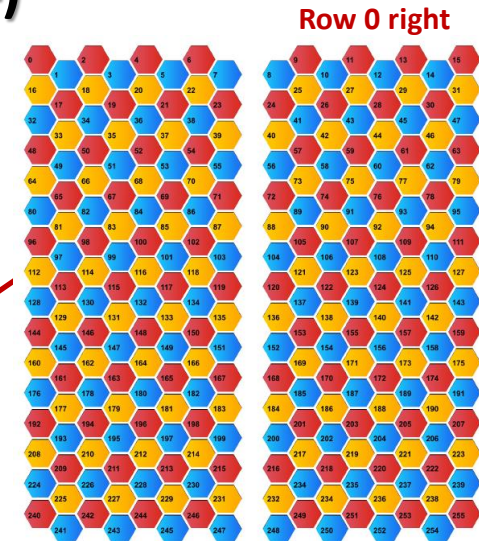
Simulation data
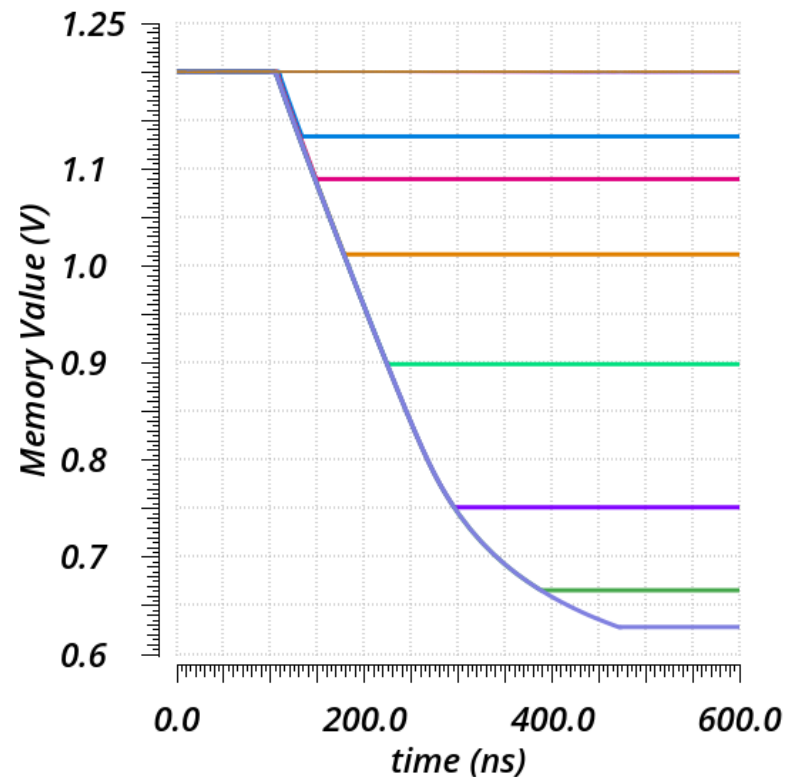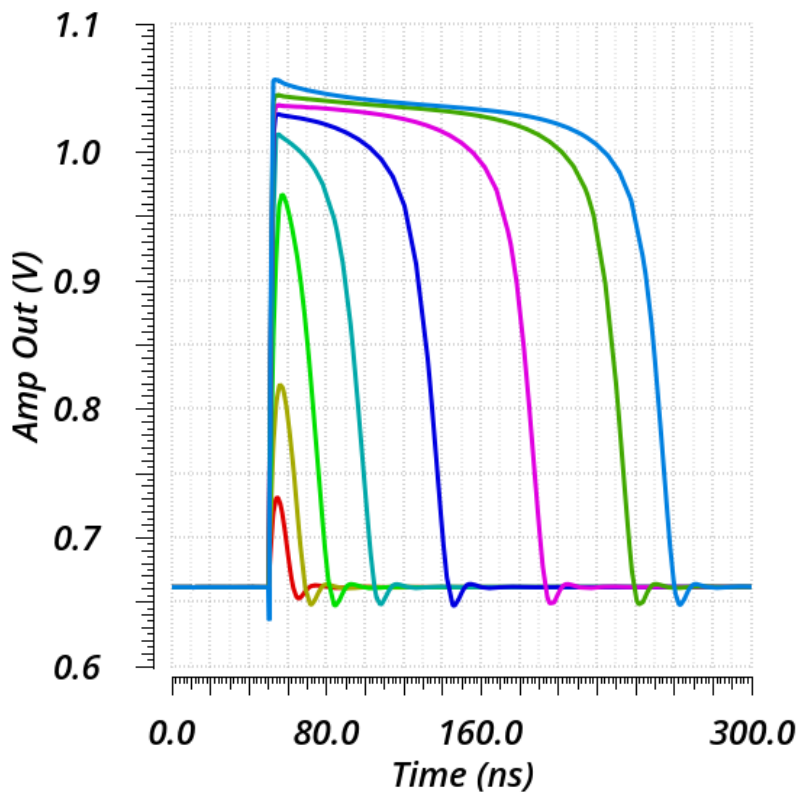
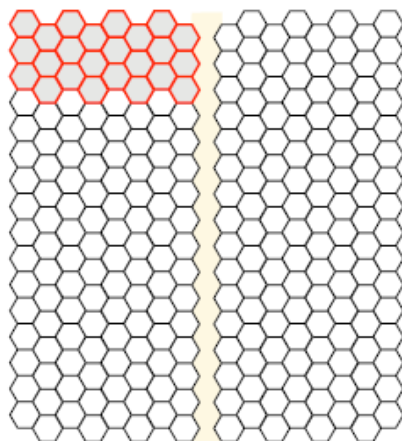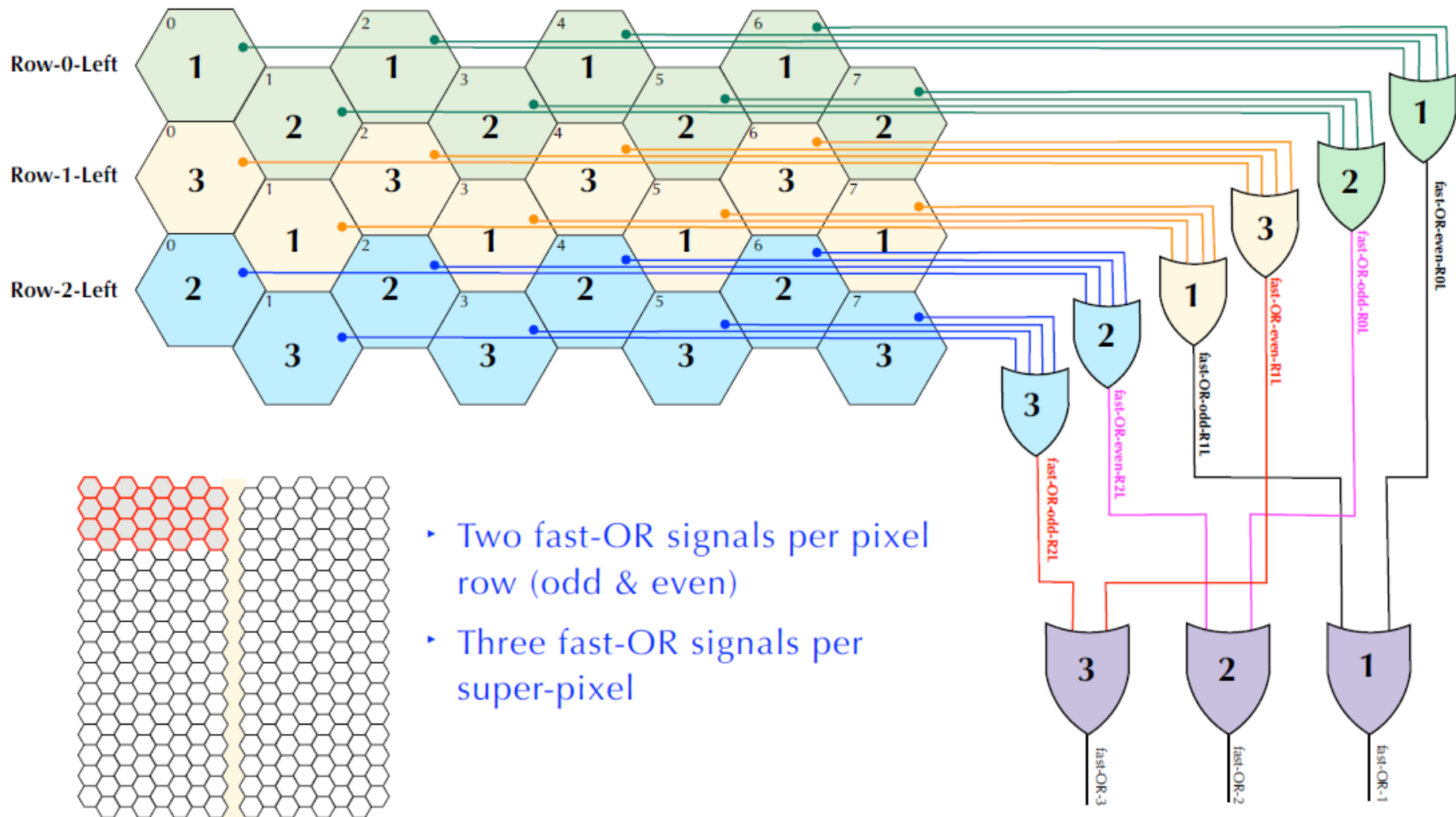**Pixel structure and row:**

- 8 pixels at either side of the digital column
- Left and right rows are processed identically
- Charge (from signal or test pulse) per pixel
- If above threshold & unmasked:
    - Stored in an analog memory
    - Immediately sent to periphery via fast-OR

‣ Two fast-OR signals per pixel row (odd & even)

‣ Three fast-OR signals per super-pixel

Four types of scan for chip/module characterization:

1. Minimum threshold search and check for noise response by scanning threshold → To be done once Threshold scan

2. Threshold scan for a targeted injection pulse – Typically 100 pulses/threshold /pixel group → Typically 1 min/chip while several chip can be done in parallel

3. Noise scan at the targeted threshold typically readout over 1 min → can mask up to 1 ‰ of noisy pixel

4. Charge calibration by injecting 16 charge levels and checking response → Typically 1 min/chip while several chip can be done in parallel

The pixels are pulsed in groups of 16, 4 pixels per row → a rolling mask will be used

Mask shift
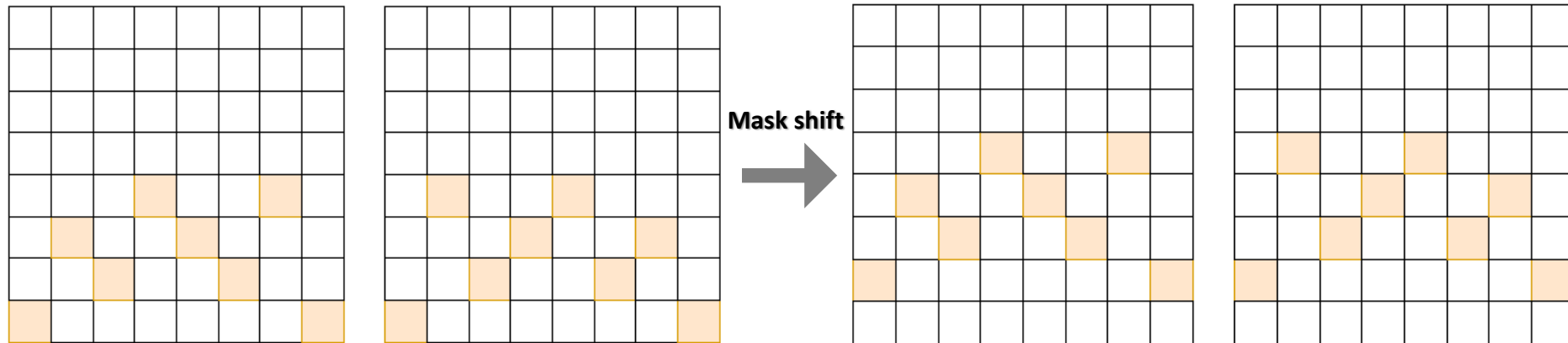
Readout and Interfaces

Readout integration to FASER:

- Trigger signal steered by TLB
- The 200 MHz clock sent to the chips are based upon the LHC clock
- Each chip has a data line and a reset
- Chip configuration thanks to SPI lines
- FPGA readout board:
  - Steer trigger and digital signal from/to TLB
  - Multiplex up to 18 chip data streams → 1 Gbps ethernet link
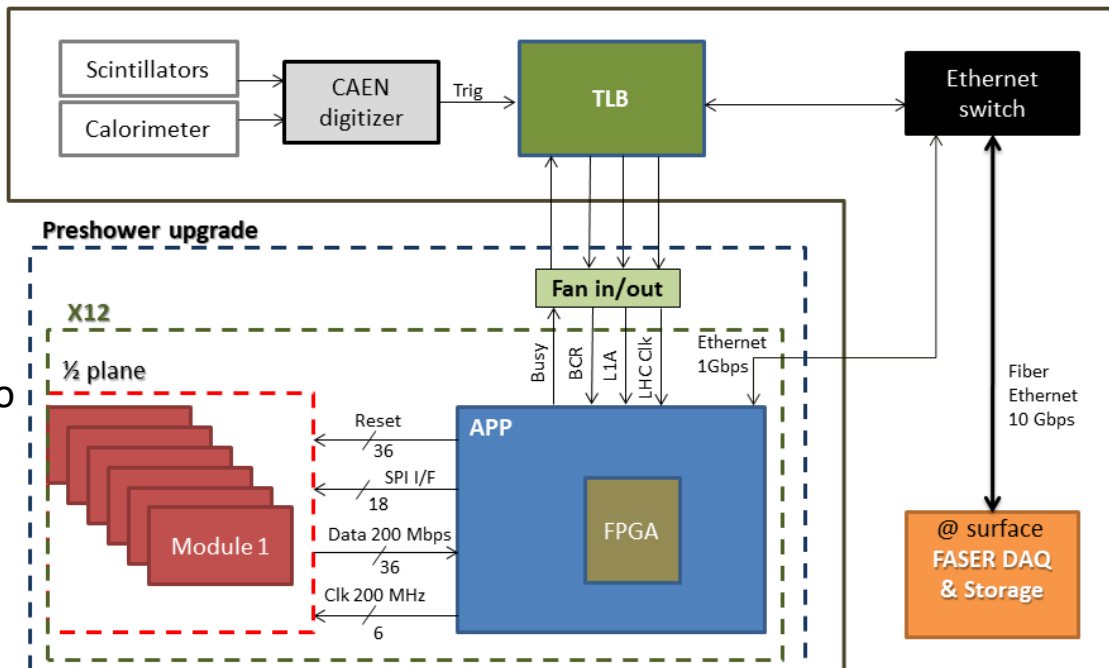 - In total, 12 FPGA boards are needed

FASER infrastructure

Preshower upgrade

- **FPGA board**:
 - Cyclone V FPGA from Intel
  - Gigabit Ethernet link

- **Adapter board** features**:
  - Two types (bottom and top)
  - Adapt on the left-hand side 6 modules
  - Adapt on the right-hand side the FPGA board
 - Adapt with many connector on top to PS and to monitoring board

Layout and design of the readout boards already started

Adapter board

FPGA board

Cyclone V FPGA

Power and IO module connectors
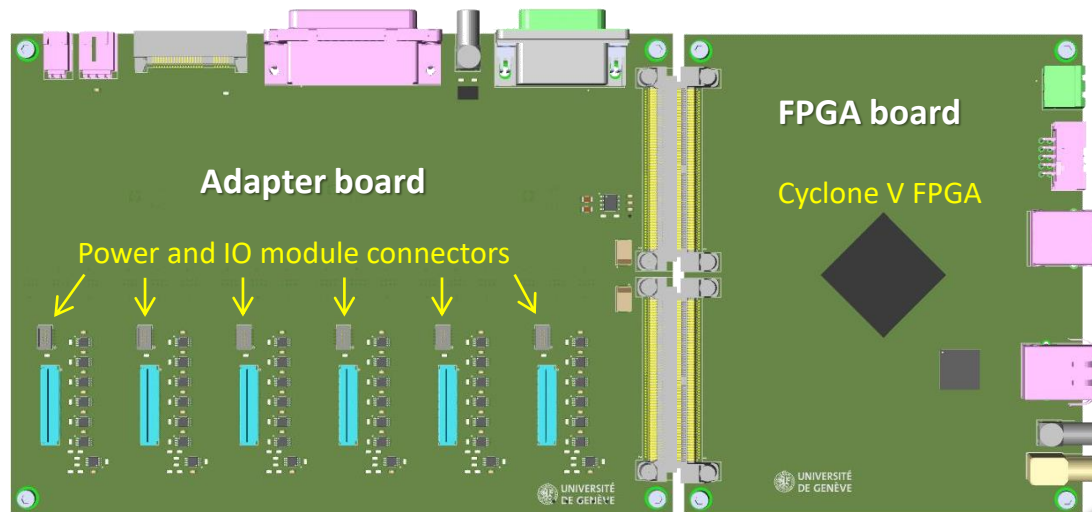
Thermal Mock-up

- Equipped a cooling plate made of AlSiMg in DMLS
- Mounted module baseplate with dummy heater (flexible kapton)
- Plane fully equipped - 6 module on each side
- Testing condition:
  - ➢ Up to 4 W per module (including some contingency)
  - ➢ Cooling flow up to 2 l/min
- A maximum ΔT of 3K is observed even in worst condition
- Heat transfer coefficient calculated: ~ 15500 W/m^{2}K
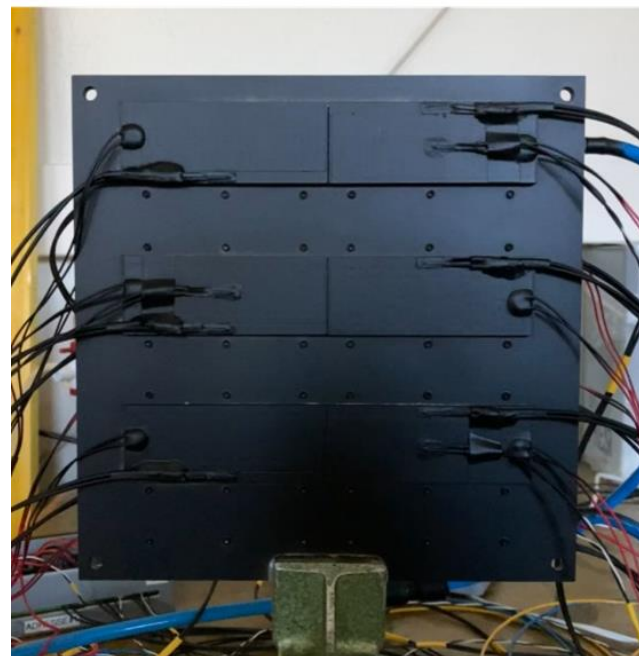
→ System very safe and stable even with very low cooling flow
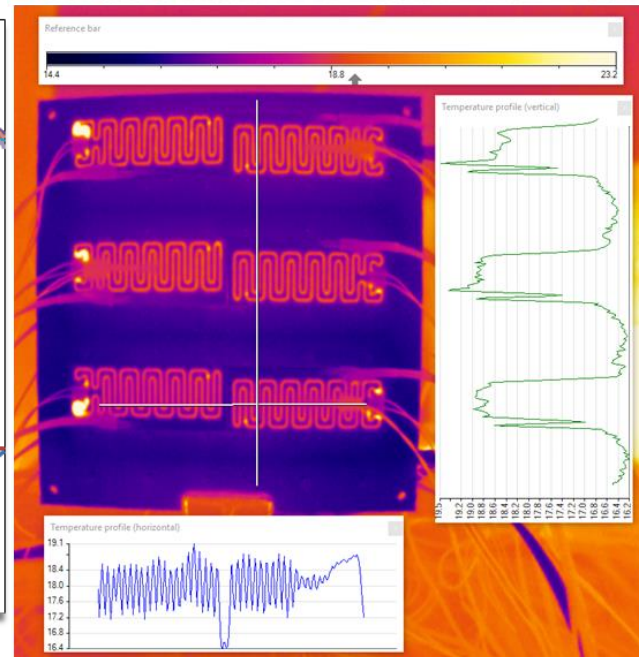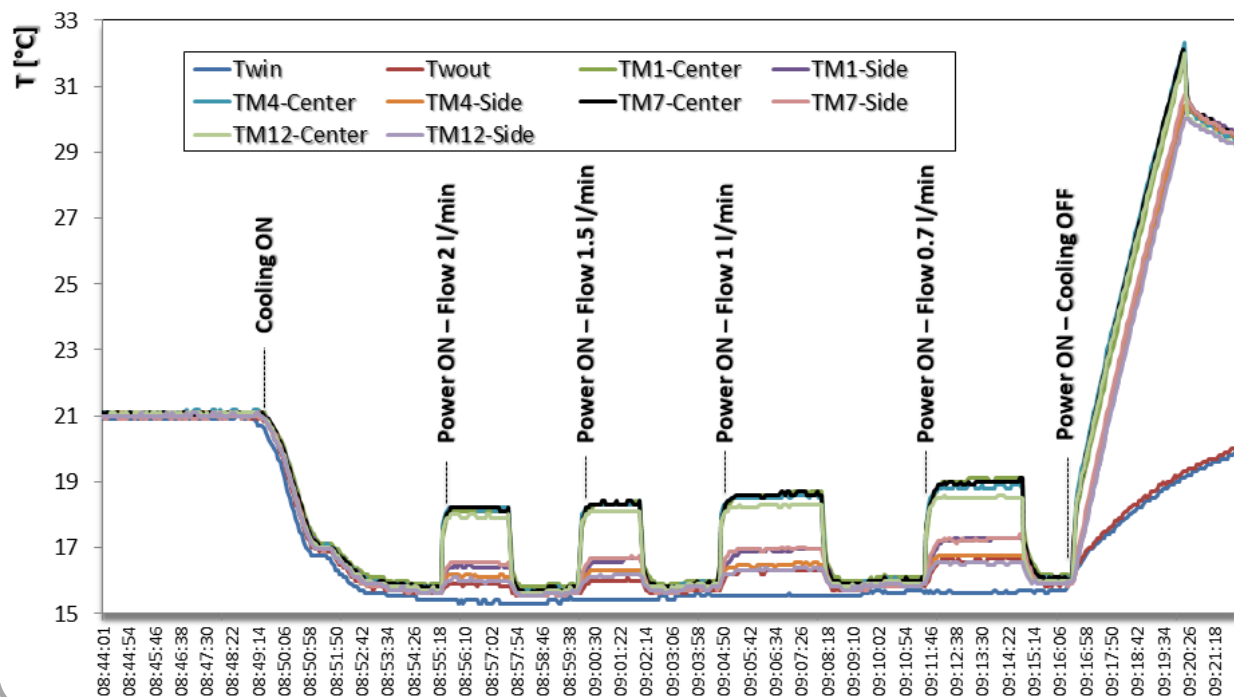
Thermal IR images

Complementary tool for diagnosis in case of local defect search

Prototype module 2